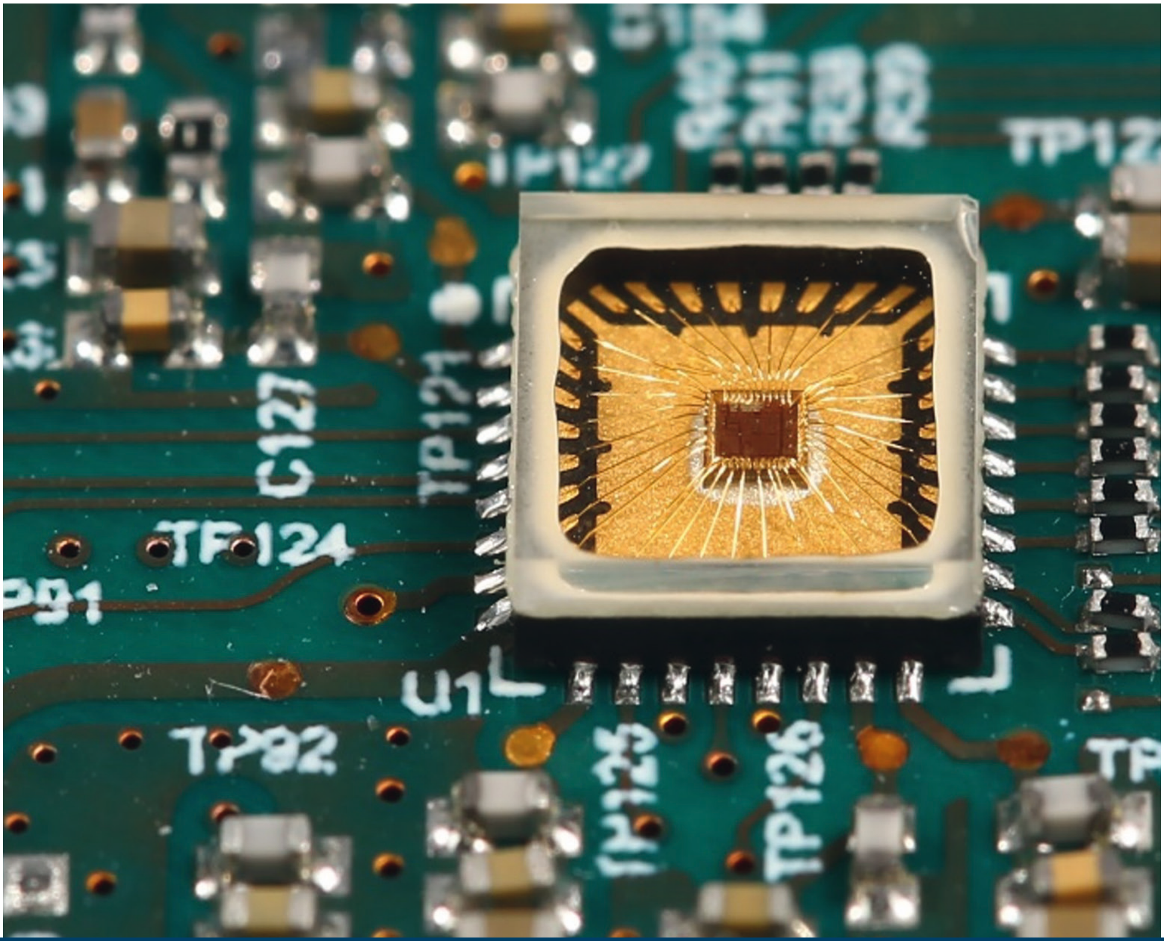

Software-Configurable Analog-To-Digital Converters for Configurable Pulse Detection

Lukas Krystofiak

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Abstract

With ever increasing digital processing capabilities, the analog-to-digital converter moves more and more in the focus of analog integrated circuit design becoming one of the most important building blocks. The progression to modern process technology nodes offers great potential, but comes in general along with an exponential growth in time effort for design, layout and verification. The overall cost for projects exceeds the capacities in research traditionally coping with smaller budgets than industry. Future developments therefore have to be accomplished in joint efforts, distributing different circuit blocks among research groups. But this also implicates that future electronics become more generic covering multiple areas of application.

In this thesis, the concept of a software-configurable analog-to-digital converter is proposed. Its matrix-like structure consisting of many sub analog-to-digital converters is able to adjust the resolution and sample rate, but ultimately the power consumption, to fit a wide range of applications in research. A first version of a software-configurable analog-to-digital converter can be switched from a high-precision mode with 11 bit resolution to a low-power mode with 8 bit. It is the focus of this work and is manufactured in a silicon 28 nm bulk CMOS process technology node. Its high integration factor allows the implementation of powerful digital signal processing on-chip, while analog performance and conventional design methodologies largely stay valid as it is still a planar bulk silicon process.

In a first step, a chip was designed and manufactured featuring a 6 bit successive approximation register analog-to-digital converter. It served as a pilot project marking the transition from a previously used 65 nm technology process to a more modern 28 nm node at the institute. The main focus here was to identify the potential and also the drawbacks of the technology as well as to gather experience in the design of successive approximation register analog-to-digital converters. The results of literature research, design decisions, consequences and finally the measurement results are presented in detail.

Subsequently, a second chip has a first version of a software-configurable analog-to-digital converter at its core. For the two sub analog-to-digital converters it is mainly based on, the experience from the first chip helped to accelerate the design and enabled significant improvements. Apart from that, further improvements were integrated on an architectural level to increase power efficiency and increase the competitiveness of a generic solution. Simulation and measurement results are presented in detail. Finally, an error analysis is given investigating the non optimal behavior of the high-precision mode.

Zusammenfassung

Der stetige Anstieg der Leistungsfähigkeit digitaler Signalverarbeitung rückt Analog-Digital-Wandler mehr und mehr in den Fokus der Entwicklung integrierter Schaltungskreise. Der Fortschritt beim Wechsel zu modernen Prozesstechnologien zeigt einerseits starkes Potenzial, allerdings erhöht sich auch der Design-, Layout- und Verifikationsaufwand exponentiell. Die Gesamtkosten von Projekten übersteigen so die Möglichkeiten in der Forschung, welche traditionell mit kleineren Budgets auskommen muss als die Industrie. Entwicklungen müssen daher in Zukunft gemeinsam erarbeitet werden und einzelne Schaltblöcke auf unterschiedliche Forschungsgruppen aufgeteilt werden. Dies hat allerdings auch zur Folge, dass Schaltungen allgemeiner gebaut werden müssen, um verschiedene Anwendungsgebiete abzudecken.

In dieser Arbeit wird das Konzept eines softwareseitig einstellbaren Analog-Digital-Wandlers vorgestellt. Dieser ist aus mehreren kleineren und simplen Analog-Digital-Wandlern aufgebaut, die in einer Art Matrixstruktur zusammengefasst werden. Durch Abschalten einzelner Bereiche ist es möglich unterschiedliche Auflösungen und Abtastraten zu realisieren, wodurch letztendlich die Leistungsaufnahme skaliert werden kann. Zur genaueren Untersuchung wurde eine erste Version eines softwareseitig einstellbaren Analog-Digital-Wandlers entwickelt. Dieser hat einen Modus mit hoher Auflösung von 11 bit sowie einen Modus mit verringerter Leistungsaufnahme und 8 bit Auflösung. Als Prozessknoten wird eine 28 nm bulk CMOS Technologie eingesetzt. Mit einer hohen Integrationsdichte können komplexe Signalverarbeitungsblöcke realisiert werden, gleichzeitig erlaubt die Ähnlichkeit zu früheren Knoten den Einsatz von bekannten Designmethoden.

In einem ersten Schritt wurde ein Chip mit einem 6 Bit Analog-Digital-Wandler entwickelt und gefertigt, der nach dem Prinzip der sukzessiven Approximation arbeitet. Dieses Pilotprojekt markiert dabei den Wechsel von einer 65 nm-Technologie zu einer 28 nm-Technologie am Institut. Hauptziel war die Untersuchung von Vor- und Nachteilen der neuen Prozesstechnologie und allgemeiner Erfahrungsgewinn beim Entwickeln von Analog-Digital-Wandlern, die nach dem Prinzip der sukzessiven Approximation arbeiten. Die Resultate der Literaturrecherche, der Simulationen und der Verifikationsmessungen im Labor werden detailliert wiedergegeben.

Ein zweiter Chip mit einer ersten Version eines softwareseitig einstellbaren Analog-Digital-Wandlers wurde darauf basierend entwickelt. Für die kleineren und simplen Analog-Digital-Wandler konnte dabei stark auf die Erfahrungen des ersten Chips zurückgegriffen werden. Darüber hinaus wurden weitere Verbesserungen auf Architekturebene eingefügt, um die Nachteile einer generischen Lösung zu verringern. Simulationen und Messungen werden wieder detailliert beschrieben. Weiterhin wird auch eine Analyse vorgestellt, die das nicht optimale Verhalten im Hochpräzisionsmodus untersucht.

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Acronyms

AC	Alternating Current
ADC	Analog-to-digital Converter
BJT	Bipolar Junction Transistor
CDAC	Capacitive Digital-to-analog Converter
CMOS	Complementary Metal-oxide Semiconductor
CPU	Central Processing Unit
DAC	Digital-to-analog Converter
dBc	Decibel Relative To The Carrier
dBFS	Decibel Relative To Full Scale
DC	Direct Current
DFF	D Flip-flop
DNL	Diferential Nonlinearity
DR	Dynamic Range
ENOB	Effective Number Of Bits
FoM	Figure Of Merit
FoM$_\text{S}$	Schreier Figure Of Merit
FoM$_\text{W}$	Walden Figure Of Merit
IC	Integrated Circuit
INL	Integral Nonlinearity
JTAG	Joint Test Action Group
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signaling
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
MSB	Most Significant Bit
NMOS	N-type Metal-oxide Semiconductor
PCB	Printed Circuit Board
PMOS	P-type Metal-oxide Semiconductor
PSD	Power Spectral Density
PVT	Process, Voltage And Temperature
QFN	Quad-flat No-leads
RMS	Root-mean-square
SAR	Successive Approximation Register
SFDR	Spurious-free Dynamic Range
SNDR	Signal-to-noise-and-distortion Ratio
SNR	Signal-to-noise Ratio
SRAM	Static Random-access Memory
THD	Total Harmonic Distortion

Chapter 1

Introduction

1.1 Motivation

Since the invention of the first transistor in the Bell Labs in 1947, integrated circuits (ICs) rapidly evolved fitting nowadays triple-digit million transistors on a square millimeter of silicon. The latest complementary metal-oxide semiconductor (CMOS) process node generation at the writing of this thesis is 3 nm, albeit node notations have become only a marketing term and there are no physical structures on the chip, that actually have these dimensions. The steadily growing integration and the performance per power and area, paved the way for microchip's ubiquity, advancing the functionality of applications and enabling the feasibility of complex implementations. But with it also the fabrication methods became highly sophisticated; so much, that manufacturing companies offering the latest process node generation thinned due to the unbearable cost of modern fabrication facilities, leaving only a few. There is not much publicly available information about the current user share of the different technology nodes in the industry and research as manufacturing foundries are very restrictive about their data and most is confidential, but a rough insight can be derived from the user report of EUROPRACTICE [1]. The platform EUROPRACTICE acts as an interface between customer and technology providers for IC design software and manufacturing alleviating the cost by collecting designs from different clients on multi-project wafer runs or use multi level masks. It is mainly used by research facilities in Europe, but also to a lesser degree by startups and businesses with small volume production. Figure. 1.1a illustrates the current state of the process technology distribution. The vast majority is still using 65 nm, introduced in 2005, and larger nodes. This is attributed to the exponential increase of cost as indicated by Fig. 1.1b. It should be noted, that it only shows the manufacturing cost. As complexity increases, the time effort for design, layout and verification also grows exponentially contributing an even higher amount to the overall cost. For more advanced nodes design methods change drastically, which forces new architectures making old intellectual property obsolete. It would mean a start from scratch, which discourages transfer.

Particle detector experiments have a high requirement for spatial resolution necessitating many sensors in a confined space. Additionally, these experiments are exposed to harsh environments hostile to electronics. Off-the-shelf components do not meet these requirements, which is why custom ICs are often developed by the particle detector community. The developments in this thesis are not limited to particle detectors, but as its first target application, derive legitimization from it. This research area reflects the current node distribution shown in Fig. 1.1a well, albeit 65 nm bulk CMOS being the state-of-the-art, while older process nodes are

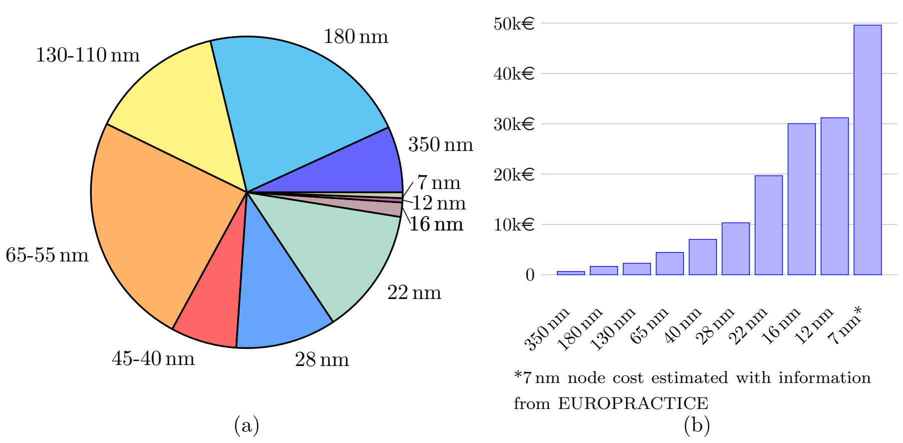


Figure 1.1: (a) Share of the individual process node on the overall manufactured chips.
(b) Manufacturing cost for process nodes in a multi-project wafer run [1].

still heavily used [2]. It was also concluded, that while a transfer for future detector experiments to more advanced nodes is inevitable to achieve new discoveries, the complexity and therewith the cost exceed the capacities of individual research groups. Future developments therefore have to be accomplished in joint efforts, distributing different circuit blocks among research groups. But this also implicates, that future electronics become more generic covering multiple detector experiment requirements [3]. This trend will likely also be seen in other research areas relying on IC design as the overwhelming complexity is a universal problem.

The analog-to-digital converter (ADC) is the bridge between the analog and digital domain. It is therefore needed whenever a signal from the real world is to be investigated and processed computationally. This spans from simple applications like weight displaying on a scale to complex wireless communication modulation enabling high bandwidths. As digital processing capabilities increase, so is the role of ADCs becoming one of the most important building blocks. Coincidentally, it is also among the most complex blocks consisting of many sub circuits both of analog and of digital nature. Its development is a lengthy process that accounts for a major part of the resources and poses a high risk to the success of a whole project. A ready and fully-verified generic ADC especially will therefore reduce the overall time and effort for custom chip design significantly. Prototyping and verification of new concepts can also be facilitated. Furthermore proving, that generic approaches can be implemented successfully and bring overall benefits, if used in combination with modern process nodes, is an important milestone for the assessment of future chip design in research.

1.2 Outline of the Thesis

The structure of this thesis is a follows. In chapter two the fundamentals for ADCs as well as fundamental architectures and the state of the art for ADCs are summarized. Chapter three presents the concept for a software-configurable ADC intended to be used in more generic chips, that cover a broad range of applications. Furthermore, the choice of the process technology node for the implementation is explained. Following, chapter four gives detailed insight in the design of the first chip. It is a pre-development done to get familiar with the new process technology and its characteristics. The chip's main feature is a simple, low-resolution ADC, that serves as the basis for the continued development towards more sophisticated ADCs. Chapter five reports the measurement results of the performance of the ADC and puts them into context in a discussion. Chapter six then covers all aspects of the creation of a first software-configurable ADC which has two resolution modes, a low-power mode and a high-precision mode, and is implemented two times in parallel for read out of two channels. Chapter seven presents the measurement results and discusses the achieved performance. Finally, chapter eight gives a conclusion and outlook for future works.

Chapter 2

Fundamentals of the Analog-To-Digital Converter

2.1 Principle Theory of Operation

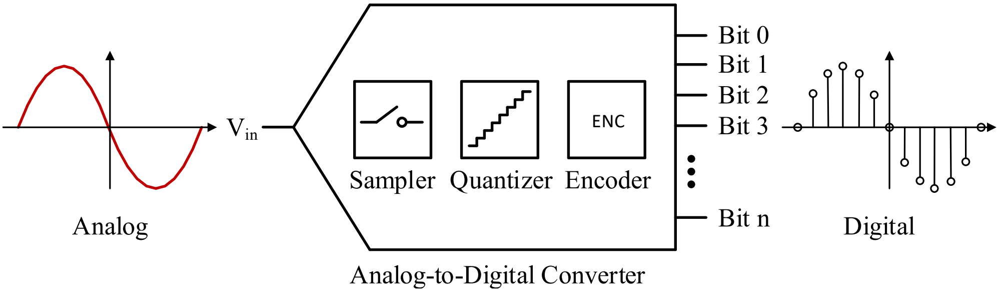


Figure 2.1: Fundamental elements of an ADC

An ADC translates an analog signal in the form of a voltage or current to a digital representation. It comprises of three core functionalities, it has to accomplish, as illustrated in Fig. 2.1. At first, a sampling block forms the signal to discrete-time by allowing it to only pass on in periodic intervals. Subsequently, a quantizer compares the signal to fixed thresholds transforming it to a discrete value. Finally, an encoder provides a binary bit representation of the analog sample. The physical resolution of an ADC is given in bit. It is a measure for the ideal amount of signal levels that can be differentiated and doubles with every additional bit implemented in the ADC. Mathematically, this relation is expressed as

$$\text{Detectable signal levels} = 2^N. \tag{2.1}$$

Here, N is the resolution in bit. A 12 bit ADC for example therefore has ideally $2^{12} = 4096$ steps it can resolve.

2.2 Fundamental Limits

2.2.1 Quantization Noise

The quantization interval, measuring the minimum detectable change in a signal magnitude, can be described mathematically as

$$\Delta = \frac{V_{FS}}{2^N}. \tag{2.2}$$

Here, V_{FS} represents the maximum peak-to-peak voltage an ADC can handle and N is the resolution in bit. An exemplary, ideal output characteristic of an ADC is shown in Fig. 2.2a to illustrate the form and distribution of quantization intervals. In this case the 3 bit ADC has eight quantization intervals with a V_{FS} of 1 V, depicted also in steps of eighths to make the transitions more clear. Notice, that the maximum digital value "111" represents the analog value 7/8 V full scale. The maximum digital scale is inherently always one least significant bit (LSB) below the analog full scale. Usually, the value representing a digital output is chosen as the mid-point of the quantization interval as illustrated with a linear, red line going through all mid-points in the figure. With this definition a quantization error occurs between the real analog value and its digital representation ranging from $-1/2$ LSB to $+1/2$ LSB as shown in Fig. 2.2b.

To get a general understanding of the effect quantization has on alternating current (AC) signals, a mean error is approximated called quantization noise. It can be derived from the sawtooth waveform in Fig. 2.2b having a peak-to-peak amplitude of q. With this the quantization error can be described as

$$e(t) = s\,t, \; \frac{-q}{2s} < t < \frac{q}{2s}. \tag{2.3}$$

t represents the time and s the slope of the sawtooth waveform here. Forming the root-mean-square (RMS) will result in

$$\text{RMS quantization noise} = \sqrt{\overline{e^2(t)}} = \sqrt{\frac{s}{q}\int_{\frac{-q}{2s}}^{\frac{q}{2s}} (s\,t)^2 dt} = \frac{q}{\sqrt{12}}. \tag{2.4}$$

The analysis of quantization noise and its spectrum was investigated in detail by [4]. It shows, that the derivation of the quantization noise from a simple sawtooth shape for the error presented here holds for most signal forms. It is approximately Gaussian and has a uniform spread over the the Nyquist bandwidth. One general assumption is that the quantization noise is uncorrelated with the input signal. If this is not the case, it appears centered around the harmonics deteriorating the signal quality. Strictly, whenever the ratio between the sampling frequency and the input signal frequency is a rational number which is always the case the quantization error is correlated with the input signal, because there is bound to be a periodicity after a certain amount of cycles. In reality, other noise sources alleviate this problem acting as a dither to randomize the quantization noise spectrum. Nonetheless, picking the right sampling frequency to weaken the impact of quantization noise correlation is a crucial step in every application.

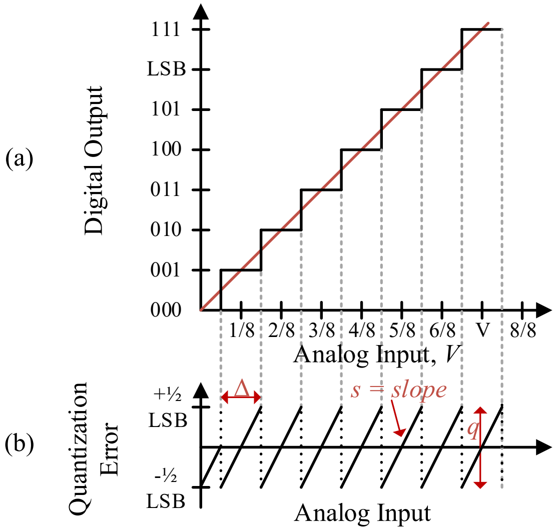


Figure 2.2: (a) Ideal output characteristic for a 3 bit ADC and its eight quantization intervals. (b) Resulting quantization error for the individual quantization intervals.

2.2.2 kTC Noise

Thermal noise, discovered by John B. Johnson in 1926 and explained by Harry Nyquist in a paper in 1928 [5], has a RMS voltage for a given bandwidth of

$$v_n = \sqrt{\overline{v_n^2}}\sqrt{\Delta f} = \sqrt{4\, k_B\, T\, R\, \Delta f}. \tag{2.5}$$

k_B is the Boltzmann constant, T is the temperature in Kelvin, and R is the resistance. In combination with a capacitor which forms the equivalent circuit of a classical sampler of an ADC, the noise coming from the resistor shows a different behavior. Assume the following configuration as shown in Fig. 2.3. R_S is the equivalent resistance of the sampling switch, C_S is the sampling capacitance and v_n is the equivalent noise source for the resistance. The absolute voltage over the sampling capacitor C_S is calculated as

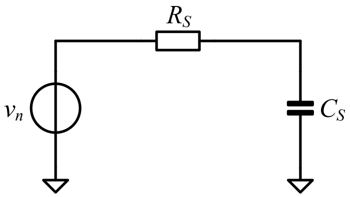


Figure 2.3: Equivalent noise circuit of a classical sampler in an ADC.

$$|v_{n,C}| = v_n \frac{1}{\sqrt{1 + (\omega\, R C)^2}}. \tag{2.6}$$

This corresponds to the spectral noise voltage at one frequency. Equation 2.5 on the other hand is defined for a bandwidth Δf. To be able to insert it in the equation, an infinitesimal range is used

$$dv_n = \sqrt{4\,k_B\,T\,R\,df}. \tag{2.7}$$

Now, the equations combines to

$$|dv_{n,C}| = \sqrt{\frac{4\,k_B\,T\,R\,df}{1 + (\omega\,R\,C)^2}}. \tag{2.8}$$

It is squared as it eases the subsequent integration over the frequency. The final equation

$$\overline{v_{n,C}^2} = \int_0^\infty \frac{4\,k_B\,T\,R}{1 + (\omega\,R\,C)^2} df = \frac{k_B\,T}{C} \tag{2.9}$$

reduces to a simple form which is only dependent on the temperature and the capacitance in the circuit. The resistance has no impact on the overall noise anymore. This is due to the fact that an increase in the thermal noise voltage is negated by the reduced cutoff frequency of the lowpass formed by the resistance and the capacitance. As the kTC noise goes to zero only if the capacitance becomes infinitely large or the temperature goes to zero, it is a an unavoidable noise and therefore a fundamental limit for ADCs. As it only depends on k_B, T and C, it is referred to as kTC noise.

2.2.3 Jitter

For the reconstruction of a signal or further processing it is assumed that every sample is taken in equidistant steps. In real-world scenarios however this is not the case. There are several effects that influence the exact sampling point of a signal. Static effects like slope of the sampling clock, parasitics of the traces off- and on-chip going from the clock to the sampling switch or buffer delays, cause only a static delay by shifting every sample by the same amount. They therefore produce no error in the sampled signal. An exception make time-interleaved ADCs that use multiple ADCs in parallel to convert a signal to the digital domain. Here, the delay of the clock signals leading to the individual ADCs, has to be reduced to sufficient levels either by careful design and layout or mitigated by calibration stages.

Time-varying effects have a much more severe impact on the quality of the signal. They are caused for example directly by the noise coming from circuits like buffers used in the clock path or are picked up by the clock lines from other nearby traces and circuits. The quality of the clock source is also a major contributor to sampling uncertainties. For very high frequencies a mismatch of the clock line going into the chip also causes deterioration and is mitigated by moving from a square wave signal as clock signal to a sinusoidal clock signal instead which is rectified on-chip. All time-varying effects can be summed up to one single term which is referred to as jitter.

To calculate the resulting noise caused by jitter, first a simple sinus function is defined as

$$v(t) = V_0\,\sin(2\,\pi\,f_{sig}\,t). \tag{2.10}$$

V_0 is here the amplitude of the input signal voltage and f_{sig} is the input signal frequency. Forming the derivation

$$\frac{d\,v(t)}{d\,t} = 2\,\pi\,f_{sig}\,V_0\,\cos(2\,\pi\,f_{sig}\,t) \tag{2.11}$$

and taking the RMS of it

$$\left(\frac{d\,v(t)}{d\,t}\right)_{rms} = \frac{2\,\pi\,f_{sig}\,V_0}{\sqrt{2}} \tag{2.12}$$

yields the average slope of the sinus. Substituting in, $\Delta\,v_{rms}$ is the RMS voltage error which the jitter produces and $\Delta\,t_{rms}$ is the RMS time value the sampling point diverges from the ideal value. With this, the term results in

$$\frac{\Delta\,v_{rms}}{\Delta\,t_{rms}} = \frac{2\,\pi\,f_{sig}\,V_0}{\sqrt{2}}. \tag{2.13}$$

Often, $\Delta\,t_{rms}$ is represented by σ_j. The final equation for the voltage error through jitter concludes to

$$\Delta\,v_{rms} = \frac{2\,\pi\,f_{sig}\,V_0\,\sigma_j}{\sqrt{2}}. \tag{2.14}$$

It should be underlined that the frequency f_{Sig} here is the signal frequency and not the sampling frequency. Accordingly, the effect of jitter has less effect on low-frequency signals, while at very high frequencies it becomes the limiting factor for the resolution.

2.3 Fundamental Characterization Units

2.3.1 Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio of the power of a signal and the noise that affects the signal quality. Harmonic distortions are not taken into account here. It is defined as

$$\text{SNR} = 20\,\log_{10}\left(\frac{\text{RMS value of FS signal wave}}{\text{RMS value of noise}}\right). \tag{2.15}$$

Its unit is the decibel, dB in short. FS stands for full scale. In the following, the SNR for the previously described main noise sources is calculated and its impact contextualized.

2.3.1.1 SNR for Quantization Noise

The SNR for the quantization noise is calculated assuming a sinus wave input. To arrive at the RMS of a sinus signal, the following equation has to be solved

$$v_{sin,rms} = \sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} (V_0\, \sin(\omega\, t))^2 dt}. \tag{2.16}$$

V_0 is here the amplitude of the signal. With the help of the relation

$$\sin^2(x) = \frac{1}{2}\,(1\, -\, \cos(2\,x)) \tag{2.17}$$

the integral can be solved. The equation can now easily be resolved to

$$v_{sin,rms} = \sqrt{V_0^2\,\frac{1}{2}} = \frac{V_0}{\sqrt{2}}. \tag{2.18}$$

With the amplitude expressed as a multiple of the quantization interval q in the form of $V_0 = \frac{q\,2^N}{2}$ the RMS voltage for a sinus signal is finally given as

$$v_{sig,rms} = \frac{q\,2^N}{2\,\sqrt{2}}. \tag{2.19}$$

Inserting this and the equation for the RMS quantization noise into 2.15, the expression changes to

$$\begin{aligned} \mathrm{SNR_{quant}} &= 20\,\log_{10}\left(\frac{\frac{q\,2^N}{2\,\sqrt{2}}}{\frac{q}{\sqrt{12}}}\right) \\ &= (6.02\,N - 9.03 + 10.79)\,dB \\ &= (6.02\,N + 1.76)\,dB. \end{aligned} \tag{2.20}$$

6.02 dB stems from the doubling in precision with every bit, -9.03 is the amount subtracted for using a sinus wave as input and 10.79 is added, because the RMS value of the quantization noise $\frac{q}{\sqrt{12}}$ is much smaller than the static quantization error q compensating for the statistically too pessimistic derivation from $6.02\,N$ alone. Equation 2.20 can also be used to derive a equation for the effective number of bits (ENOB) as

$$\mathrm{ENOB} = \frac{\mathrm{SNR_{dB}} - 1.76\,dB}{6.02\,N\,dB}. \tag{2.21}$$

The SNR in this equation includes noise from all sources. Therefore, it measures the difference between the SNR of ideal quantization noise which calculates the amount of physical bits, and the actual SNR to get the reduced amount of bits, called ENOB. The correction factor for the quantization noise is still applied as it accounts for the augmentation from the statistical distribution of the quantization noise which would otherwise lead to a too-high ENOB.

2.3.1.2 SNR for Jitter

The SNR for jitter noise is given by

$$\mathrm{SNR}_{\mathrm{jitter}} = 20\,\log_{10}\left(\frac{v_{sig,rms}}{v_{jitter,rms}}\right). \tag{2.22}$$

With $v_{sig,rms} = V_0/\sqrt{2}$ being the RMS voltage of a sinus wave, the equation becomes

$$\mathrm{SNR}_{\mathrm{jitter}} = 20\,\log_{10}\left(\frac{\frac{V_0}{\sqrt{2}}}{\frac{2\,\pi\,f_{sig}\,V_0\,\sigma_j}{\sqrt{2}}}\right) = 20\,\log_{10}\left(\frac{1}{2\,\pi\,f_{sig}\,\sigma_j}\right). \tag{2.23}$$

Figure 2.4 illustrates the effect of clock jitter on the SNR of an ADC plotted over the input signal frequency. Three different clock jitter values were chosen as an example in which 10 ps stands for a low-quality reference clock and 100 fs is a value of highest precision. As the trend for high-performance ADCs continues, it is clearly visible that at high signal frequencies, jitter becomes the dominant source of noise. To stay above an ENOB of 10 bit or an SNR above 62 dB which is generally regarded as the lower limit for high resolution, jitter values below 1 ps are necessary for signal frequencies above 100 MHz. These requirements are difficult to achieve and shift a great portion of the design effort towards the clock source and distribution. One should also keep in mind that this is only the SNR attributed to the jitter noise and other noise source reduce the resolution further so that in general the SNR of jitter noise should be higher than the ultimately needed overall SNR.

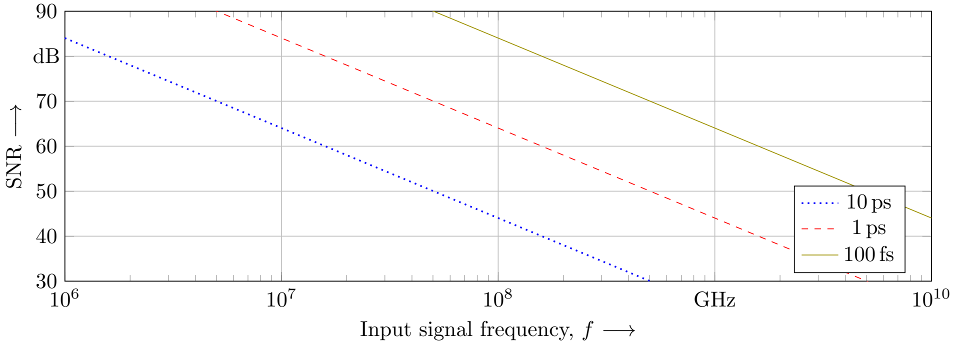


Figure 2.4: Maximum reachable SNR for different values of jitter plotted over the input signal frequency.

2.3.1.3 SNR for kTC Noise

The SNR for kTC noise is calculated by

$$\mathrm{SNR}_{\mathrm{kTC}} = 20\,\log_{10}\left(\frac{v_{sig,rms}}{v_{kTC,rms}}\right). \tag{2.24}$$

With $v_{sig,rms} = V_0/\sqrt{2}$ being the RMS voltage of a sinus wave, the equation resolves to

$$\mathrm{SNR}_{\mathrm{kTC}} = 20\,\log_{10}\left(\frac{\frac{V_0}{\sqrt{2}}}{\sqrt{\frac{k_B\,T}{C}}}\right) = 20\,\log_{10}\left(V_0\sqrt{\frac{C}{2\,k_B\,T}}\right). \tag{2.25}$$

This time, the SNR is also dependent on the magnitude of the input signal. Figure 2.5 shows the limit of the SNR caused by kTC noise plotted over the sampling capacitance of an ADC assuming a signal amplitude of 0.5 V. Additionally, the black stair plot shows the resolution in integer ENOB steps as a rough guideline for the needed capacitance. As a side note, choosing a capacitance close to the lower bound for the respective ENOB leaves less design margin for other noise sources, threatening the intended resolution target. While for lower capacitance values an increase has a large effect on the overall noise generated (mind the logarithmic representation here), it diminishes further when a higher SNR is required. The consequence is a high area consumption on-chip for the sampling capacitor alone and a high power consumption. Therefore, it makes sense after a certain SNR to increase the magnitude of the input signal, although it has a quadratic effect on the power consumption, compared to the linear influence on power consumption of the capacitance. Note that the power consumption to charge a capacitor follows the relation $P \propto C\,V^2$. Unfortunately, in modern process technologies, the maximum available supply voltage is limited to very low levels, typically around 1 V. This dilemma may be circumvented by introducing new design techniques. An upcoming method is omitting the sampling stage altogether by using so called continuous time ADCs [6]. Another method leverages kTC noise cancellation to keep the sampling capacitance size small [7] [8].

2.3.1.4 Combined Overall SNR

To arrive at a term to describe the SNR for all aforementioned noise sources, the power of these has to be combined as follows

$$\mathrm{SNR}_{\mathrm{all}} = 10\,\log_{10}\left(\frac{P_{sig,rms}}{P_{kTC,rms} + P_{quant,rms} + P_{jitter,rms}}\right). \tag{2.26}$$

As a remark, it is switched back to power here, because only the power for RMS adds, not the voltage. Transforming this equation to align its shape with the others and describe all noise

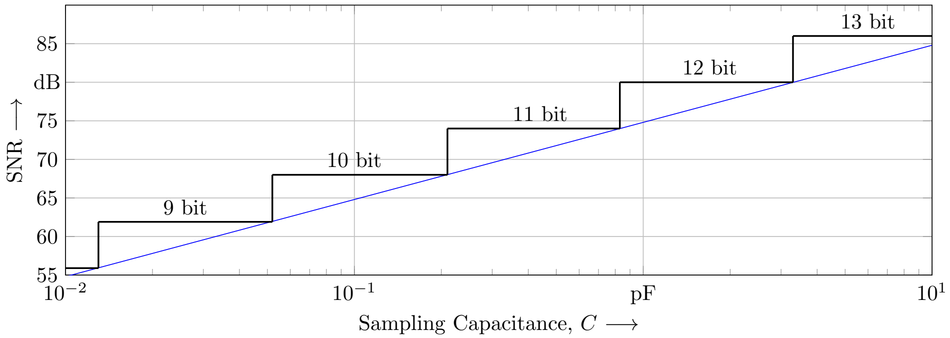


Figure 2.5: SNR caused by kTC noise plotted over the sampling capacitance of an ADC and a signal amplitude V_0 of 0.5 V. The stair plot shows the resolution in integer ENOB steps as was done in [9].

sources as SNR yields

$$\begin{aligned}
\mathrm{SNR} &= 10\,\log_{10}\left(\frac{P_{sig,rms}}{P_{kTC,rms}+P_{quant,rms}+P_{jitter,rms}}\right)\\
&= -10\,\log_{10}\left(\frac{P_{kTC,rms}+P_{quant,rms}+P_{jitter,rms}}{P_{sig,rms}}\right)\\
&= -10\,\log_{10}\left(\left(\frac{v_{kTC,rms}}{v_{sig,rms}}\right)^2+\left(\frac{v_{quant,rms}}{v_{sig,rms}}\right)^2\left(\frac{v_{jitter,rms}}{v_{sig,rms}}\right)^2\right)\\
&= -10\,\log_{10}\left(10^{\frac{-SNR_{kTC}}{10}}+10^{\frac{-SNR_{quant}}{10}}+10^{\frac{-SNR_{jitter}}{10}}\right).
\end{aligned} \tag{2.27}$$

2.3.2 Total Harmonic Distortion

The total harmonic distortion (THD) describes the ratio of the sum of the powers of the harmonic components to the power of the fundamental of the input signal. Its equation describes the relation as follows

$$\mathrm{THD} = 20\,\log_{10}\left(\frac{\sqrt{V_2^2+V_3^2+\ldots+V_n^2}}{V_1}\right). \tag{2.28}$$

V_1 is the fundamental and all higher V are harmonics respectively. Harmonics are caused by nonlinearities in a device and are always positive integer multiples of the fundamental frequency which is the original input signal frequency. Harmonics and aliased harmonics are determined by $|\pm K\, f_{sample} \pm n\, f_{sig}|$, where n is the number of the harmonic and $K \in \mathbb{N}$. This is illustrated in Fig. 2.6 showing the fundamental of a signal at 10 MHz and its second, third and fifth harmonic at 20 MHz, 30 MHz and 50 MHz respectively. THD is usually specified in decibel relative to the carrier (dBc), or decibel relative to full scale (dBFS). The first describes the power ratio of a signal to a carrier signal, in this case the fundamental. The latter also compares to the power of the fundamental, but assumes that a full-scale signal is applied. As the spectrum is usually normalized to the full-scale signal, dBFS thus always relates to 0 dB.

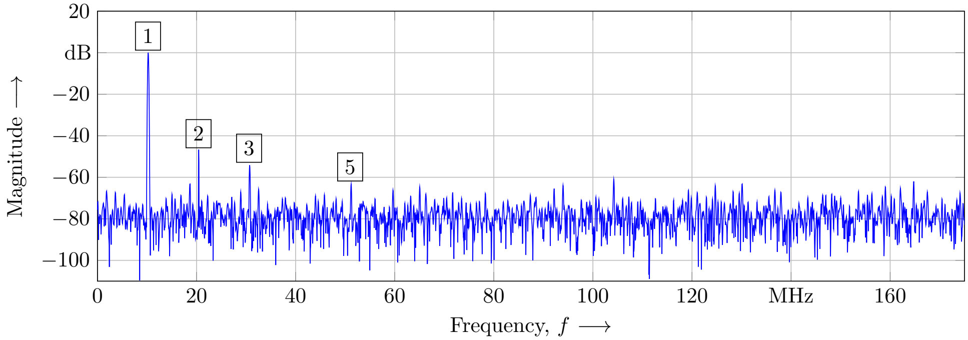


Figure 2.6: Spectrum of a signal highlighting the fundamental and harmonics.

2.3.3 Signal-to-Noise-and-Distortion Ratio

To arrive at the most complete measure of the dynamic performance of an ADC, the sum of the noise and harmonics, excluding direct current (DC) is considered for the signal-to-noise-and-distortion ratio (SNDR). In mathematical terms, it is described by

$$\mathrm{SNDR} = 10\,\log_{10}\left(\frac{P_{sig,rms}}{P_{noise,rms} + P_{dist,rms}}\right). \tag{2.29}$$

SNDR is usually plotted over frequency. For ADCs with very high resolution, the input signal often needs to be refined, for example by a bandpass filter, to not have an effect on the measured performance. This makes a sweep difficult, but at least a number at low frequency and at high frequency, close to the maximum bandwidth of the ADC, should be given.

2.3.4 Dynamic Range

The dynamic range (DR) is a measure of the range of the input signal power for which useful outputs can be expected from an ADC. It describes the ratio between a full-scale input signal and the noise floor level in the spectrum. It is therefore specified in decibel. A mathematical expression is given as

$$\mathrm{DR} = 10\,\log_{10}\left(\frac{P_{sig,rms,max}}{P_{sig,rms,min}}\right). \tag{2.30}$$

Here, $P_{sig,rms,max}$ is measured for a full-scale input signal and $P_{sig,rms,min}$ describes the minimum detectable signal. A common used definition is the signal power at the point when SNDR is 0 dB.

It is still used in ADCs that do not have a physical representation of the targeted resolution in bit, like oversampling and noise-shaping ADCs. Otherwise, a more common and useful parameter to define the minimum detectable signal in the frequency domain is given with the adaption described in the following section.

2.3.5 Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is an indicator for the smallest detectable signal distinguishable from other spectral components in the bandwidth. It is an important metric in communication applications and describes the ratio of the RMS value of the signal to the largest spectral noise component or harmonic which are called spurs. As equation, it is expressed as follows

$$\mathrm{SFDR} = 10\,\log_{10}\left(\frac{P_{sig,rms}}{P_{spur,max,rms}}\right). \tag{2.31}$$

Usually, the second or third harmonic is the limiting factor for the SFDR. In more complex applications, like systems on a single chip, other components can create spurs that have a bigger impact than the harmonics itself.

2.3.6 Differential Nonlinearity

The diferential nonlinearity (DNL) is a DC characteristic and measures the deviation from the ideal step width for one digital code of the ADC between adjacent codes. Mathematically, this is expressed as following

$$\mathrm{DNL(k)} = \frac{w(k) - w_{ideal}}{w_{ideal}}, \quad w(k) = X(k+1) - X(k). \tag{2.32}$$

$w(k)$ is the width for the currently investigated digital code. It is defined by the transition point $X(k+1)$ from the current code to the next digital code, minus the transition point $X(k)$ from the last code to the current code. w_{ideal} represents the ideal code width which is 1 LSB. Figure. 2.7a illustrates different DNL errors. In general, for positive DNL errors the step width increases, for negative DNL errors the step width decreases. At DNL = -1 the step for the current code disappears completely, leading to a missing code in the ADC output. With this definition, the DNL for ADCs cannot decrease lower than -1. A DNL >1 can be an indicator for a non-monotonicity, as seen around the code "100" in Fig. 2.7a. Monotonicity is crucial for some applications, e.g in control loops, where otherwise instabilities can occur. To assure the operation of an ADC without missing codes and non-monotonicities, $|DNL| < 1$ has to be fulfilled for all values. A diagram showing an example how a measured DNL is usually presented can be seen in Fig. 2.8a. An 8 bit ADC was used here to plot the DNL error in LSBs for every possible ADC code.

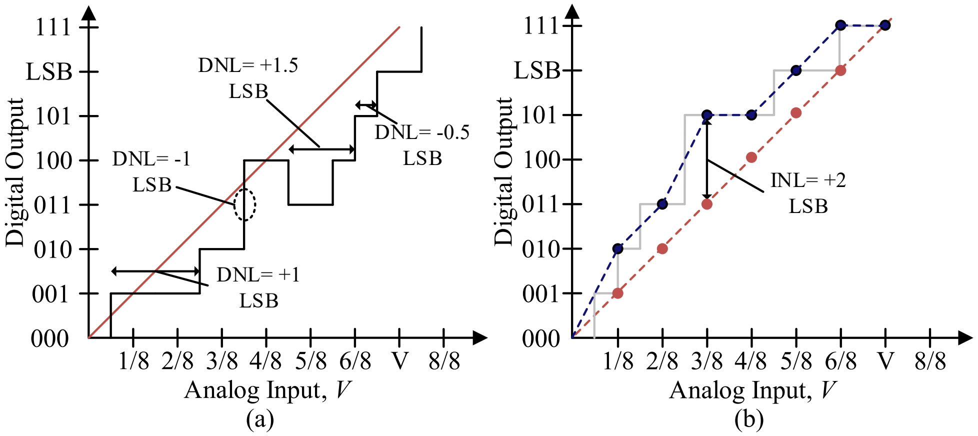


Figure 2.7: (a) A DC output characteristic of an ADC showing different DNL errors.
(b) A DC output characteristic of an ADC showing the integral nonlinearity (INL) error of the output in blue compared to the ideal transfer curve shown here in red.

2.3.7 Integral Nonlinearity

Another measure of the nonlinearity is the integral nonlinearity (INL). Here, the output transfer characteristic of an ADC is compared to a straight line. In general, there are different methods to define this line. In the first, the unadjusted INL, the ideal output characteristic of the ADC is used. This results in the raw, absolute error produced at every step. A more common approach is the so called endpoint INL. It draws the reference line starting at the origin and ending at the full-scale output of the ADC after it was corrected for gain and offset errors by trimming out the endpoint errors at the zero and full-scale codes. With this the INL at the starting point and the end point is therefore also zero. As virtually all ADCs exhibit offset and gain errors and they are easily correctable, it is a reasonable method. It still shows the true, absolute error that can be expected from the ADC. Best-fit INL is the third method. Here, the straight line is fitted with standard curve fitting techniques in such a way that the overall error for all codes is minimized. With this only the relative error is considered. It highlights the distortion in an ADC at the expense of absolute precision and is therefore more meaningful for AC applications. Figure 2.7b shows an exemplary nonlinear output characteristic. For the analog input voltage "3/8" which ideally responds to the digital output "011" the ADC puts out the code "101" which produces an absolute error of 2 LSB. This can also be expressed with this equation

$$\mathrm{INL(k)} = \frac{C_{ADC}(k) - C_{ideal}(k)}{w_{ideal}}, \quad k = 2 \ldots N. \tag{2.33}$$

Here, $C_{ADC}(k)$ describes the current output code and $C_{ideal}(k)$ the ideal code of the ADC. An alternative method to obtain the INL is by summing the calculated DNL errors up until the currently investigated code:

$$\mathrm{INL(k)} = \sum_{i=1}^{k-1} \mathrm{DNL(i)}, \quad k = 2 \ldots N. \tag{2.34}$$

Notice, that for the calculation of the INL, the constraints INL(0) = not defined and $\mathrm{INL}(1) = 0$ apply. A diagram showing an example how a measured INL is usually presented can be seen in Fig. 2.8b. An 8 bit ADC was used here to plot the INL error in LSBs for all ADC codes.

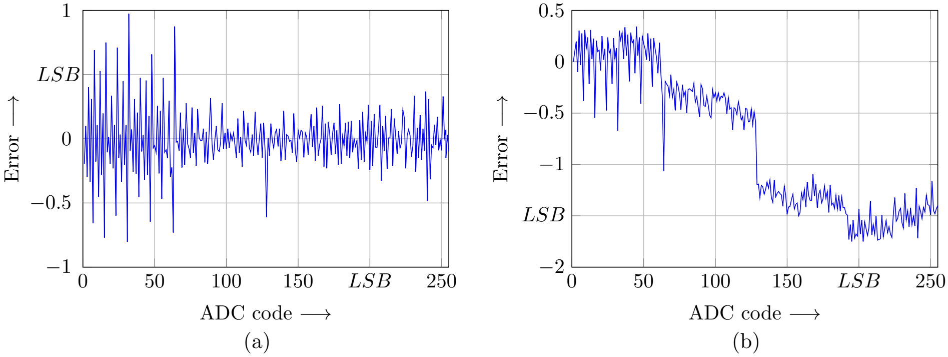


Figure 2.8: (a) Exemplary DNL of a 8 bit ADC. (b) Exemplary INL of a 8 bit ADC.

2.3.8 Figure of Merit

In the past various figure of merits (FoMs) have been introduced to easily and compactly compare the performance of an investigated device on the basis of a single number. For analog circuits, and in particular for ADCs, there are many different aspects to consider, when defining performance. Among these are power consumption, resolution, sample rate, area, yield, power supply rejection ration, analog bandwidth and process technology. Processing all these metrics into a single FoM is an impossible challenge. The two FoMs that prevailed and are used nowadays, therefore use only three, arguably the most impactful, parameters, namely power consumption, resolution and sample rate. For the same reason, it is advisable to compare ADCs through FoMs only, if they lie in the same field of requirements. In general, FoMs show their usefulness by indicating a trend in the development of ADCs. For closer comparisons, all characteristics should be considered. The two most popular FoMs are the Walden figure of merit ($\mathrm{FoM_W}$) and the Schreier figure of merit ($\mathrm{FoM_S}$). In technical reports it has become standard to give both despite their significantly different approach. They are introduced in the following.

Walden Figure of Merit - It was first described by Robert H. Walden in 1999 [10]. Power consumption, resolution and sample rate are considered for it and a linear relation is assumed. Nowadays the inverse of the initially conceived equation is used and described as

$$\mathrm{FoM_W} = \frac{P}{f_s\, 2^{\mathrm{ENOB}}}, \quad [\mathrm{FoM_W}] = \frac{\mathrm{J}}{\text{conv. step}}. \tag{2.35}$$

Its unit is defined as energy in Joule per conversion step. Originally, to calculate the $\mathrm{FoM_W}$ an effective resolution bandwidth greater than a quarter of the sample rate was required and the SNR at low frequency was used. This changed nowadays to the use of the SNDR at full bandwidth. Investigating ADCs with a high resolution or sample rate, the linear relation to power consumption diminishes, as other effects, like thermal or power supply noise compensation, take up a disproportionate amount of the overall effort. In general, the FoM_W favorably skews towards mid resolution below 8 bit, where performance is neither limited by noise on the one hand or feature size in technology, e.g. matching constraints or minimum size of transistor, on the other hand [11].

Schreier Figure of Merit - It was introduced by Richard Schreier in 2005 and is expressed in dB using the dynamic range rather than the ENOB of an ADC as in the FoM_W [12]. The modulated FoM_S [13] that became established, is in the form of

$$\text{FoM}_\text{S} = \text{SNDR} + 10\,\log_{10}\left(\frac{BW}{P}\right), \quad [\text{FoM}_\text{S}] = \text{dB}. \tag{2.36}$$

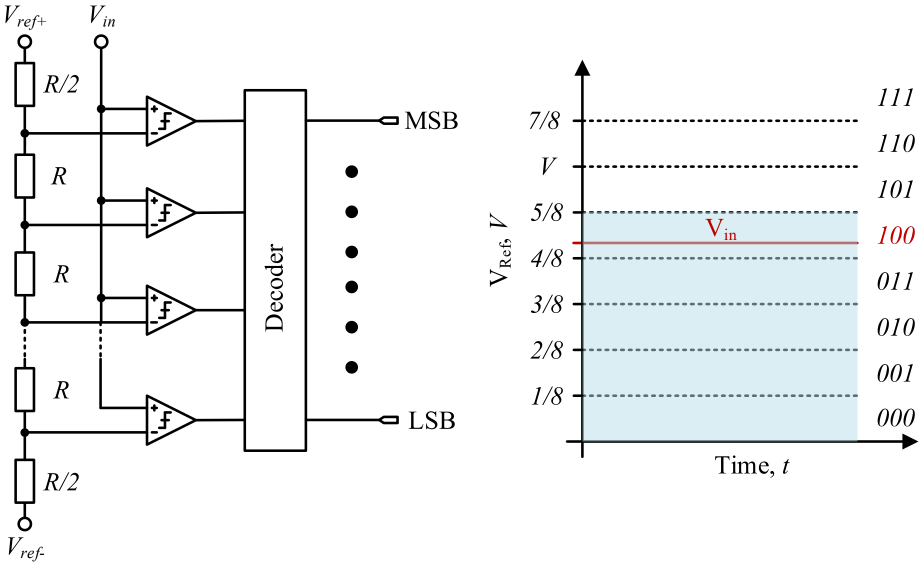
Here, the dynamic range is replaced by the SNDR to consider all effects decreasing the resolution. Its accurate units would be dB/J, but the J is dropped. A trend investigation found empirically that ADCs with mid to high resolution closer to the technological limits, exhibit a power consumption increase quadrupling per effective bit [14]. This matches well with the 6 dB per bit increase in the FoM_S for which reason it gained its popularity and is now a standard performance indicator.

2.4 ADC Types

Over the years, the steadily decreasing analog design space in progressing technology nodes led to many new developments producing different sub ADC types, hybrid combinations of ADC types or even completely new ADC types. The latest appearance is a completely time-based ADC [15]. A comprehensive coverage of all ADC types would be out of scope for this thesis though. For this reason, the following section only gives a brief overview about the classical architectures of ADCs that are the basis for most designs and are still actively researched.

2.4.1 Flash ADC

The flash ADC, also called direct-conversion ADC, derives its name from its way of conversion which happens for all bits in one time step, or more loosely in an instant [16, p. 147]. Its basic structure can be seen in Fig. 2.9a. A linear voltage ladder is used to generate reference voltages which are compared against the input signal with the help of comparators. The resulting thermometer code is converted to binary representation by an additional decoder. An illustration of the conversion principle is shown in Fig. 2.9b. Flash ADCs can be very fast reaching sample rates in the upper gigasample per second range [17]. The downside is the required amount of comparators needed which doubles for every additional bit of resolution implemented. For a higher resolution it therefore has a very high area and power consumption limiting practical implementations to 8 bit. Flash ADCs are nowadays mainly used in high-speed receivers that do not need high resolution like in wireline communication [18] [19]. Lately, they are replaced by heavily time-interleaved successive approximation register (SAR) ADCs due to their superior technology scaling [20] [21].

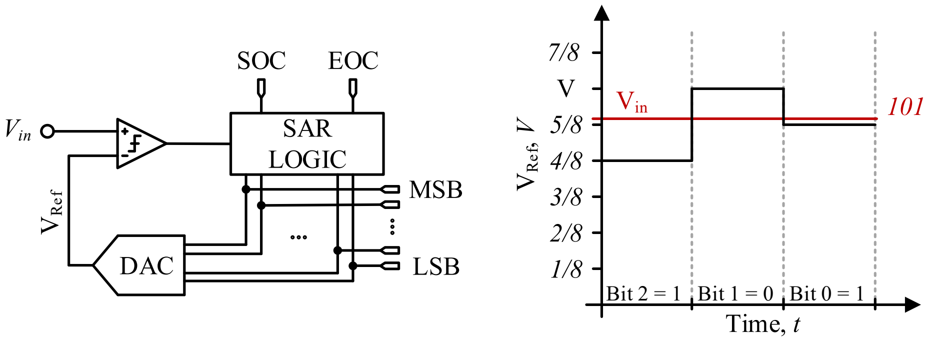


(a) (b)

Figure 2.9: (a) Structure and (b) conversion principle for a flash ADC.

2.4.2 SAR ADC

The successive approximation register ADC converts an analog signal to the digital domain in a recursive way approximating the digital representation in a binary search fashion [16, p. 178]. Figure 2.10 illustrates the general structure and conversion process. With the help of a comparator, the input signal is compared to half of the maximum signal input voltage in a first step. If the analog signal voltage is greater, the first bit is set to one and a digital-to-analog converter (DAC) sets the reference voltage to 3/4 of the maximum signal input voltage for the conversion step. This procedure is continued until the desired resolution is achieved. Figure 2.10b shows the conversion process for a 3 bit ADC. The reference voltage nowadays is usually generated in a capacitive way subtracting a respective amount of charge from the sampled input signal. Through this, SAR ADCs are very power-efficient. To keep the needed reference clock frequency low, it is usually operated in an asynchronous mode which means, it times the individual conversion steps independently of the global reference clock thereby reducing the overall complexity and power consumption of the chip [22]. Additionally, as the comparator is the only analog component in a SAR ADC, it scales very well with modern process nodes reducing the area footprint and power consumption even further. A drawback poses the recursive nature. For every additional bit of resolution an extra conversion step is executed which reduces the sample rate proportionally to the resolution. A general limit to the maximum resolution achievable without additional tuning or calibration is furthermore given by the matching quality of the capacitors in the used technology process. It is usually limited to around 10 bit [23]. SAR ADCs were typically used in general purpose scenarios whenever medium resolution and medium sample rate are sufficient. Lately, this architecture serves as the basis for hybrid combinations extending its range of application in all domains (see


SOC
EOC
V_{in}
V_{Ref}
SAR LOGIC
MSB
LSB
DAC
7/8
V
5/8
4/8
3/8
2/8
1/8
V_{in}
101
V_{Ref}, V
Bit 2 = 1
Bit 1 = 0
Bit 0 = 1
Time, t

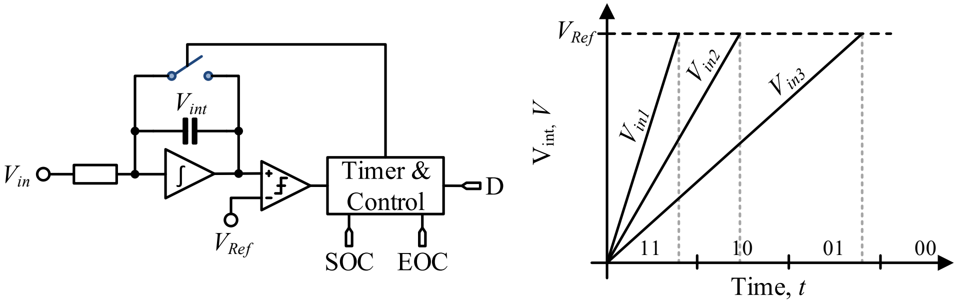
(a) (b)

Figure 2.10: (a) Structure and (b) conversion principle for a SAR ADC.

section 2.5).

2.4.3 Slope ADC

A slope, or integrating, ADC operates without a DAC generating reference voltages to compare the input signal against [16, p. 200]. Instead, it converts an analog signal into a digital representation by measuring the time until a voltage ramp proportional to the input signal voltage reaches a reference voltage. An illustration of the structure and the basic operation is shown in Fig. 2.11. At the beginning of the conversion, a timer is started. To generate the ramp an integrator is used that produces a linear output voltage ramp with the slope depending on the input signal voltage. This is fed to a comparator that stops the timer after the voltage ramps reaches a reference voltage. This architecture is able to reach a high resolution with low complexity, but has only low maximum achievable sample rates. This is due to the fact that the counter has to run very long up to $t_{max} = 2^{\text{Resolution}}$. For this reason, slope ADCs were used mostly for DC applications, but are lately replaced by sigma-delta ADCs. Nowadays, their target application is found in CMOS image sensors [24] [25] [26] [27], where they trade favorably compared to other ADCs in terms of resolution, power consumption and complexity.

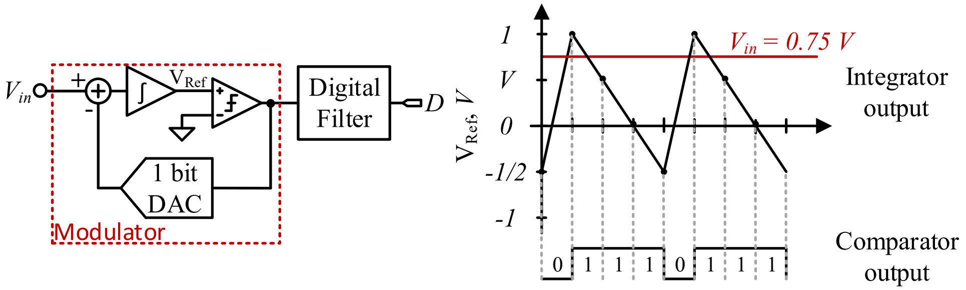

V_{int}
V_{in}
Timer & Control
D
V_{Ref}
SOC
EOC
V_{Ref}
V_{int}, V
V_{in1}
V_{in2}
V_{in3}
11
10
01
00
Time, t

(a) (b)

Figure 2.11: (a) Structure and (b) conversion principle for a slope ADC.

2.4.4 Sigma-Delta ADC

The sigma-delta ADC lends its name from the likewise called sigma-delta modulation [16, p. 253]. Its general structure and theory of conversion is illustrated in Fig. 2.12. An input signal voltage is summed with a positive or negative reference voltage coming from a 1 bit DAC. This is fed into an integrator which produces a linear ramp proportional to its input. A clocked comparator checks in periodical time steps, if the ramp signal from the integrator is positive or negative. As long as the ramp voltage is positive, a digital one is streamed into the digital filter and the DAC in the feedback loop subtracts the positive reference voltage from the input signal voltage. If the ramp voltage is negative, a digital zero is streamed into the digital filter and the DAC subtracts a negative reference voltage. The data stream is finally converted to a digital representation by a digital lowpass filter averaging the stream. Note, in Fig. 2.12b the sigma-delta ADC is already in its steady state. At the start of the conversion, the pattern will look different. Furthermore, the chosen input signal voltage here generates a simple, fast converging pattern. Different input voltages will take considerably longer to converge. In general, the resolution of a sigma-delta ADC depends also on the size of the averaging digital filter. Two effects combine in a sigma-delta ADC to enhance the resolution. The first is called oversampling which samples a signal at a higher sample rate than the Nyquist theorem requires, and thereby spreads the quantization noise also over a higher bandwidth. Filtering then increases the resolution. For every additional bit, the sampling frequency has to be increased by four following $f_{os} = 4^{\text{Resolution}} \times f_s$. The second effect arises from the system response of the modulation scheme which can be described as $H(z) = 1 - z^{-1}$, shifting quantization noise from lower frequencies up to higher frequencies which is then removed by the digital filter. This is called noise shaping. Through this, sigma-delta ADCs can reach very high resolutions. However, the nature of this conversion does not allow a high sample rate and introduces also a high latency in the signal conversion. Sigma-delta ADCs displaced slope ADCs in DC measurement equipment applications due to their superior resolution. They became popular however in audio processing applications as they are able to achieve a very high resolution over a wider kilohertz range [28] [29] [30].



(a) (b)

Figure 2.12: (a) Structure and (b) conversion principle of a sigma delta ADC.

2.4.5 Pipelined ADC

Pipelining is a technique used to increase the throughput by splitting the process of conversion and distributing it over multiple subsequent stages [16, p. 184]. A simple representation build out of three stages totaling 13 bit can be seen in Fig. 2.13a. Every stage of a pipelined ADC consists of a smaller sub ADC that resolves a part of the incoming input signal. In this case, the first stage converts 4 bit. Subsequently, the analog representation of these four bits, generated by a DAC, is subtracted from the original input signal, creating an analog residuum signal that is handed over to the next stage. To alleviate the requirements for the next stage the residuum voltage is amplified to utilize the whole dynamic range, the supply voltage permits alleviating noise requirements. Note, that usually one bit overlap between the stages is implemented which means that the amplifier amplifies the residuum to a maximum of half the supply voltage. Through this, offsets occurring naturally in the individual stages have no effect on the output other than a global offset, as long as they do not extend over a certain limit. This is not considered in the illustration in Fig. 2.13b to improve clarity. The last stage consists only of a sub ADC as a residuum is not needed anymore. The individual stages start to convert a new input signal or residuum as soon as they are finished with the old to maximize throughput. Therefore the bits of the earlier stages need to be buffered and correctly aligned with bits from the later stages to assemble the complete digital representation. Strictly speaking, a pipelined configuration can be implemented with various other types of ADC architectures as sub ADC and therefore is more a topology than an architecture. Historically though, pipelined ADCs were always implemented with flash sub ADCs and were treated as their own architecture.

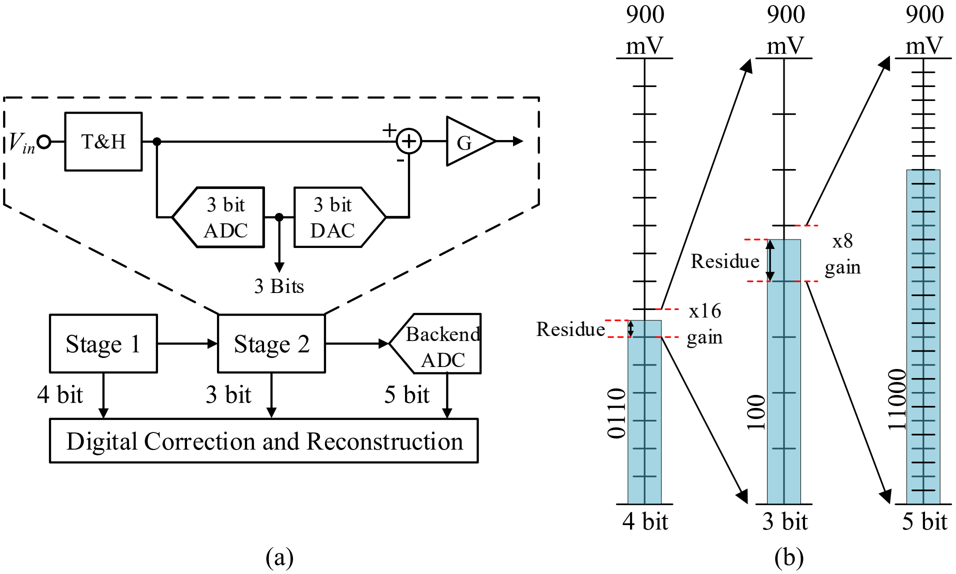


Figure 2.13: (a) Structure and (b) conversion principle of a pipelined ADC.

Through the division of the conversion process, this architecture is able to reach high resolution at high sample rates. Disadvantageously, the latency is increased and, while the complexity for the individual sub ADCs is reduced, the requirements shift towards the sub DACs generating the residue which have to fulfill the linearity demands for all remaining bits. Nowadays, the bottleneck is the amplifier to magnify the residue for the next stage. The classic operational amplifier in feedback mode loses its capabilities in smaller process nodes and viable solutions consume an over proportionally big amount of power at high sample rates. To counteract this, new amplifier architectures, like ring amplifiers [31] [32] and fully dynamic amplifiers [33] [34] were introduced and combined with complex digital calibration methods. The progress of pipelined ADCs is mainly driven by the rapidly increasing bandwidth needs of wireless communication [35] [36].

2.4.6 Time-Interleaved ADC

In time-interleaving multiple individual ADCs are used in parallel taking turns to sample the same input signal [16, p. 174]. Figure 2.14 illustrates the structure and mode of operation. As can be seen, the individual ADCs sample the signal only at a fraction $1/M$ of the overall sample rate depending on the total amount M of parallel ADCs used. Through this, it is possible to reach very high sample rates even in older slower process nodes. Time-interleaving, first mentioned in [37], is another method that is more a topology but treated like an architecture in the classification. In theory, time-interleaving scales linearly in power with sample rate. In practical implementations however differences in the conversion process of the individual ADCs reduce the performance and need to be addressed. Among these are gain, offset and timing skew errors which create spurs in the spectrum [38]. Gain and offset errors are compensated comparably easy, while timing skew is more difficult to handle and requires complex digital detection and digital or analog calibration circuits [39]. For time-interleaved ADCs of high resolution all these errors have a considerable influence on the overall performance and need precise correction tracked as well as adjusted over time [40]. This quickly leads to a significant power overhead and must be taken into account to assess the viability. Furthermore it should be noted that the buffer driving the time-interleaved ADC, be it on-chip or off-chip, needs to operate at the full speed of the input signal.

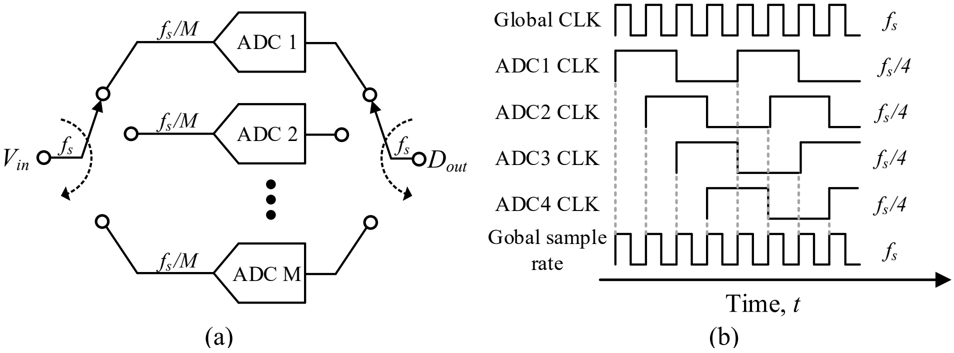


Figure 2.14: (a) Structure and (b) conversion principle of a time-interleaved ADC. The example assumes a four times time-interleaved ADC.

Moderate time-interleaving is used in high resolution applications, like wireless communication, to push the sample rate further [34] [41]. With more modern process node, heavy time-interleaving for moderate resolution also became a viable option. Its development is mainly driven by wireline communication applications [42].

2.5 State of the Art

The subsequent information relies on a database of ADC publications which is managed and extended by Professor Murmann of Stanford University [43]. It ranges from 1997 to 2023 as of the writing of this thesis and lists publications of the ISSCC and VLSI circuit symposium; the conferences with the highest impact factor in the field of integrated electronic circuits. Although not all ADC publications are considered, it gives a representative overview about the performance trend as a publication in ISSCC and VLSI usually implies that it is better than any other in one field.
Figure 2.15 shows the $\mathrm{FoM_W}$ plotted over the sample rate. For sigma-delta ADCs twice the bandwidth set by the digital filter is used as maximum sample rate to arrive at a fair comparison possibility. The red curve traces a rough performance envelope. Until 10 MHz it is relatively flat which indicates a linear relationship between sample rate and power consumption. In this region the minimum energy per conversion step needed is limited by manufacturing precision. This means that, e.g. transistor or capacitance size can not be reduced further due to mismatch constraints. New records for energy efficiency will be set by publications that find more effective schemes to circumvent these manufacturing limits. The ADCs with the lowest $\mathrm{FoM_W}$ reported are SAR ADCs [44] [45]. They both utilize dynamic comparators with novel solutions to reduce the power consumption per cycle even further. Additionally, in [44] which is manufactured in a 90 nm process, a novel switching scheme is used in the DAC to generate the reference voltages. [45] which is manufactured in a 65 nm process, implements a scheme to reduce the sampling capacitance close to the theoretical noise limit without mismatch penalties. Beyond 10 MHz and starting to take full effect around 100 MHz an increase of the $\mathrm{FoM_W}$ can be seen which implies that the power scales with the square of the frequency. An explanation for this is the reduced transconductance efficiency g_m/I_D with increasing transit

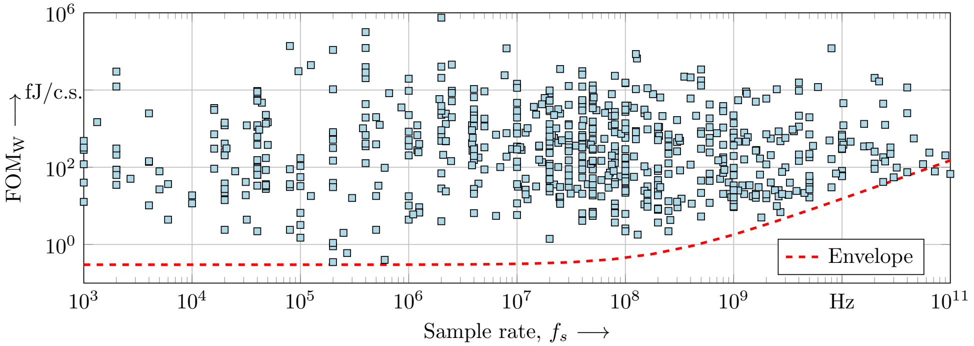


Figure 2.15: $\mathrm{FoM_W}$ plotted over sample rate for ADCs published in ISSCC and VLSI circuit symposium from 1997 to 2023, and performance envelope [43].

frequency f_T of the transistor [46] in the respective process node. This is underlined by the two publications of [47] and [48] that fall notably below the envelope. Both are manufactured in a very modern process technology node, with [47] using a 7 nm and [48] employing a 5 nm node, and therefore naturally reach higher transit frequencies. As architecture, they implement a time-interleaved SAR ADC. The ADC of [48] achieves the highest reported sample rate of 112 GSPS and is manufactured in a 5 nm process. Among other techniques, it uses an inductive clock distribution network with jitter filtering to arrive at a $\mathrm{FoM_W}$ of 74.6 fJ/conv. step.
For completeness, a diagram with the $\mathrm{FoM_S}$ plotted over the sampling rate is shown in Fig. 2.16 based on the same data set as before. Other ADCs dominate in this figure as $\mathrm{FoM_S}$ emphasizes

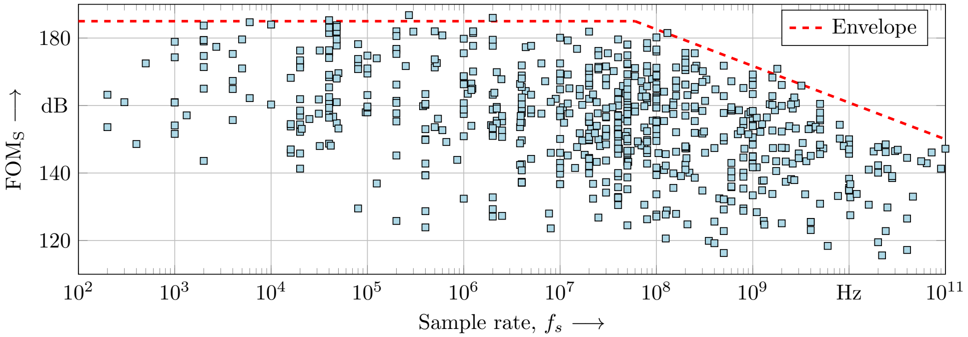


Figure 2.16: $\mathrm{FoM_S}$ plotted over sample rate for ADCs published in ISSCC and VLSI circuit symposium from 1997 to 2023, and performance envelope [43].

the effort needed to overcome noise limitations in resolution. Apart from this, the same trend as with $\mathrm{FoM_W}$ is visible. The envelope curve stays flat until a certain point. In this case it extends until 60 MHz compared to Fig. 2.15 which is attributed to inaccuracies in generating the envelope. It reinforces the observation that this region is limited by manufacturing precision. Beyond 60 MHz the envelope decreases with 10 dB per decade as the $\mathrm{FoM_S}$ also assumes only a linear relation between power consumption and sample rate which does not hold for very high frequencies. In [11] a theoretical maximum limit was calculated for the $\mathrm{FoM_S}$. As basis serves the minimum energy needed to drive a sampling capacitor with an ideal class-B amplifier [49] [50] which can be described mathematically as

$$\frac{P}{f_s} = 8\,k\,T\,\mathrm{SNR}. \tag{2.37}$$

Inserted in the equation for the $\mathrm{FoM_S}$ this results in the following upper limit

$$\begin{aligned} \mathrm{FoM_{S,max}} &= \mathrm{SNR} + 10\,\log_{10}\left(\frac{f_s/2}{P}\right) \\ &= \mathrm{SNR} + 10\,\log_{10}\left(\frac{1}{16\,k\,T\,\mathrm{SNR}}\right) = 192\,\mathrm{dB}. \end{aligned} \tag{2.38}$$

This number will never be reached, since it disregards all other sources for increased power consumption. However, there are two publications in recent years that come close to this upper limit [51] [52]. A hybrid ADC in a 90 nm is presented combining the SAR with the sigma-delta architecture in [51]. By implementing an time-domain integrator that does not need an operational amplifier, it is able to run at a supply voltage of only 0.4 V. At a sample rate of 270 kSPS and an ENOB of 11.9 bit, it consumes 638 nW arriving at a FoM_S of 186.8 dB. There are two additional noteworthy ADCs surpassing the envelope in the noise limited region. [53] presents a pipelined SAR ADC in a 28 nm process with an ENOB of 11.8 bit at a sample rate of 130 MSPS and a power consumption of 0.82 mW that reaches a FoM_S of 181.5 dB. Among others, two methods especially have a big impact. The first boosts the gain bandwidth of the residue amplifier by introducing a two-phase amplification with level shifting. The second method reduces the energy needed for the first decision of the second sub ADC by splitting the most significant bit (MSB) capacitance into smaller segments and enable a bypass window algorithm to skip decisions. Publication [54] accomplishes a FoM_S of 170.9 dB at an ENOB of 9.69 bit and a sample rate of 1.8 GSPS with a power consumption of 7.55 mW with a similar approach. A time-interleaved pipelined architecture with a backend SAR ADC is employed. The first seven sub stages use a pre-sampling scheme to improve conversion efficiency in combination with an operational amplifier as residue amplifier that obviates the need of a tail current source and a common-mode feedback scheme.

Finally, Fig. 2.17 plots the SNDR over the bandwidth for ADCs in the aforementioned data set. It gives an overview about the current state for the highest input bandwidth as well as SNDR, and also the combination of both, regardless of efficiency reached. Noteworthy is the ADC presented in [55] which has the highest SNDR at least in the investigated data set. In a 1 kHz bandwidth it reaches an SNDR of 118.1 dB which translates into an ENOB of 19.3 bit, and has a power consumption of 280 µW. The employed architecture here is called zoom ADC and combines a SAR with a sigma-delta architecture. The SAR ADC produces a coarse 5 bit conversion which is subsequently used by the sigma-delta ADC to arrive at a finer resolution. Additionally, the operational amplifiers used in the sigma-delta ADC are inverter-based to reduce power consumption. The ADC with the highest input bandwidth on the other hand is presented in [56]. Pipelining and time-interleaving with SAR ADCs as basis is employed here. It has an ENOB of 6.8 bit at the Nyquist frequency with a sampling rate of 32 GSPS and a power consumption of 199 mW. Note, that the maximum analog input bandwidth is considerably higher with 39.8 GHz than the sample rate. This is useful in applications in which undersampling is a viable solution. The measured ENOB is 5.98 bit. For this achievement, extensive effort was put into the design of a wideband interleaver, with analog timing skew and bandwidth

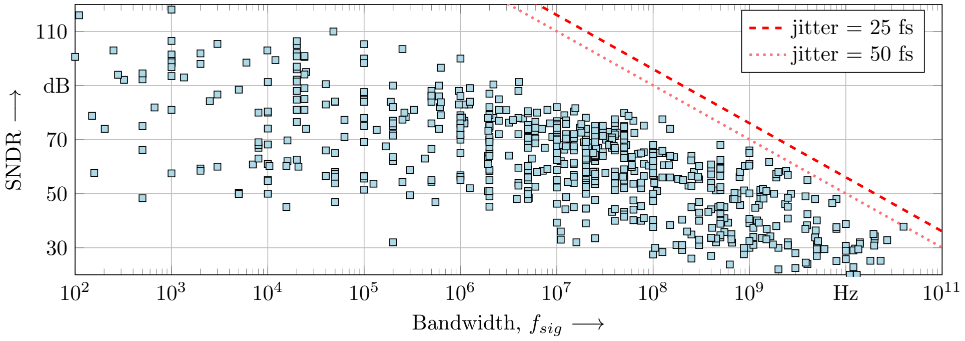


Figure 2.17: SNDR plotted over sample rate for ADCs published in ISSCC and VLSI circuit symposium from 1997 to 2023, and jitter noise limitations on SNDR for a jitter of 25 fs and 50 fs [43].

mismatch correction, to accurately distribute the signal to the individual time-interleaved branches. With this a jitter of 25 fs including the external clock source and all on-chip circuitry was reached which is the best reported value in the investigated literature. Translated to SNDR this would allow a maximum of 44.1 dB leaving a margin of about 6 dB, or 1 bit respectively, for errors from other sources when compared to the actual reached SNDR of 37.8 dB of the ADC. Continuing with 25 fs as the lowest reported jitter, its limit for achievable SNDR is plotted in Fig. 2.17 as a general perspective for the current trend. If [56] is regarded as an exceptional outlier, for the remaining high-performance ADCs a reasonably well fitting upper limit for the achievable jitter, assuming again a margin of 6 dB, is 50 fs; also plotted in Fig. 2.17. They match the slope of the drawn line remarkably well indicating that jitter noise is the main barrier for ADC developments with high sample rate. Furthermore, it can be derived that the state-of-the-art jitter noise is between 25 fs and 50 fs. The investigation of jitter noise being the main limiting at high bandwidths is continued in more detail in [11] also pointing out a slower progress in the bandwidth-resolution product than in other fields, e.g. energy efficiency.
Table 2.1 summarizes the main parameters of noteworthy ADC developments with outstanding achievements described in more detail in this section before. From left to right ADCs with the lowest $\mathrm{FoM_W}$, highest $\mathrm{FoM_S}$, highest sample rate, highest ENOB and highest input bandwidth are listed. An interesting observation can be drawn from the "architecture" row here. All developments listed here use the SAR ADC either directly or as a hybrid in combination with another architecture. This trend is underlined if we use Fig. 2.17 and highlight all publications that involve SAR ADCs as is done in Fig. 2.18. Out of the 646 publications 202, or 31.2 %, include a SAR ADC covering all design spaces of the other ADC architectures. Looking at more recent years, this is even stronger pronounced, with 154 out of 304 publications, or 51.3 %, utilizing the SAR architecture. While also research is liable to trends, there are actually strong reasons for the dominance of SAR ADCs in the latest developments. One reason is its superior energy efficiency and area footprint. With increasing demands for higher bandwidth and resolution, mostly coming from communication applications, the ADC complexity has a big impact on the overall power consumption. Applications for the internet of things (IoT) or biomedical devices, have a very limited power budget, also demanding very high energy efficiency. Another reason is a consequence of the aggressive scaling in process technology nodes catering mainly to digital circuits. With transconductance of transistors decreasing, a reduced supply voltage and

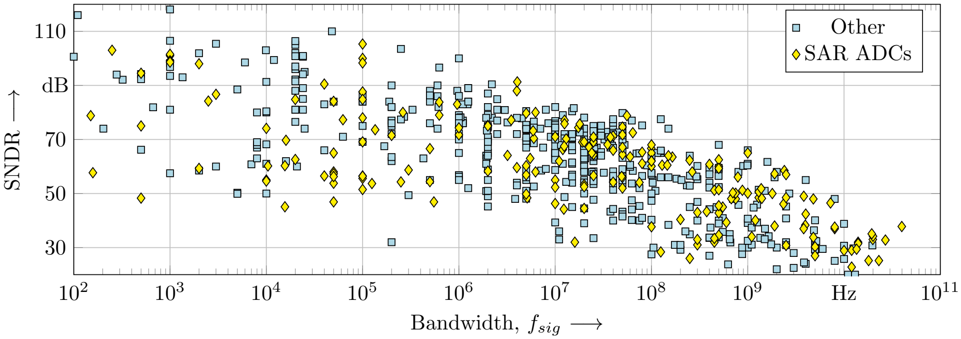


Figure 2.18: SNDR plotted over sample rate for ADCs published in ISSCC and VLSI circuit symposium from 1997 to 2023 with SAR ADCs highlighted which make up 31.2 % of the total publications [43].

Table 2.1: ADCs with best performance in one category among publications in ISSCC and VLSI circuit symposium from 1997 to 2023 [43].

	[45]	[51]	[48]	[55]	[56]
Architecture	SAR	SAR SD[a]	TI[b] SAR	SAR SD[a]	TI[b] PI[c] SAR
Technology	65 nm	90 nm	5 nm	160 nm	14 nm
Supply voltage	0.7 V	0.4 V	0.9 V	1.8 V	0.8 V
Time-interleaving	1x	1x	64x	1x	48x
Resolution	10 bit	13 bit	6 bit	20 bit	10 bit
Max f_{in}	99.9 kHz	134.9 kHz	10 GHz	1 kHz	39.8 GHz
ENOB	9 bit	11.9 bit	4.5 bit	19.3 bit	6 bit
SFDR	66 dB	90.4 dB	-	-	48.2 dB
Sample rate	200 KSPS	270 KSPS	112 GSPS	2 MSPS	32 GSPS
Power consumption	38 nW	638 nW	189 mW	280 µW	199 mW
Area	0.04 mm^2	0.059 mm^2	-	0.25 mm^2	0.16 mm^2
FoM$_W$	0.35 fJ/c.-s.	0.6 fJ/c.-s.	74.6 fJ/c.-s.	216.9 fJ/c.-s.	98 fJ/c.-s.
FoM$_S$	180.6 dB	186.8 dB	143.6 dB	185.8 dB	147.8 dB

[a] SD = Sigma delta

[b] TI = Time-interleaved

[c] PI = Pipelined

at the same time a stagnating threshold voltage decrease, the design margin for analog circuits is more and more limited. Novel analog designs cope with these restrictions. An example are new amplifier architectures that omit the use of traditional operational amplifiers. The SAR ADC however has the advantage that it uses only very little analog circuits in its core by nature.

Chapter 3

Concept for a Software-Configurable ADC

3.1 Vision

The concept of a software-configurable ADC developed in this thesis can be seen in Fig. 3.1. It is comprised of multiple smaller sub ADCs arranged in a matrix-like form. In the example, three concatenated ADC in a row form a pipelined ADC for increased resolution. The sub ADCs are also parallelized to enable time-interleaving for increased sample rate or, in combination with input signal multiplexing, to read out multiple channels. With this, the resolution and sample rate, but ultimately the power consumption, can be adjusted to fit a wide range of applications. If, for example, the resolution demands are low, a column of ADCs can be switched off and bypassed. Because the former stages in a pipelined ADC consume more than the latter, a significant amount of power can be saved by shutting off these first. Such a configuration is shown in Fig. 3.1 through the grayed out sub ADCs indicating deactivation. Regarding the sample rate, most ADCs are inherently able to support a reduced sample rate. Therefore, if the application does not require the highest sample rate, it is simply reduced by altering the sample clock frequency down to a certain threshold. Below the threshold it is more effective to switch off complete rows as auxiliary digital circuits enhancing the performance for time-interleaving can also be switched off.

Continuing the thought, an ultimate version of a software-configurable ADC uses all individual sub ADC cells individually. This would allow for even more, albeit less resolution, channels. There could also be low resolution channels next to high-resolution channels, or a partially time-interleaved configuration with two rows combined for maximum sample rate and others with the base sample rate catering to slower signals.

Legitimization for this approach is drawn from the ever increasing complexity of the signals to be detected conflicting with the exponential increase in design effort, verification and cost in more modern process technology nodes. Overall, two niches were identified that this concept fills. First and most importantly, it enables complex projects on a smaller budget. The ADC is among the most complex blocks on a chip and its functionality poses a high risk to the overall success of a project. But also other circuit blocks on the chip consume a lot of effort in modern process nodes and with higher integration factors the amount of elements to verify increases. A modular approach to chip design with individual more generic blocks, fitting a wider range of applications, combined, may be the only way to go forward. This applies especially to research which traditionally has to cope with significantly smaller budgets than industry. A second domain can be rapid prototyping. While a generic approach will never reach the same performance as a dedicated development, deploying it as placeholder facilitates fast verification of the general concept in a project prior to the building of the final system.

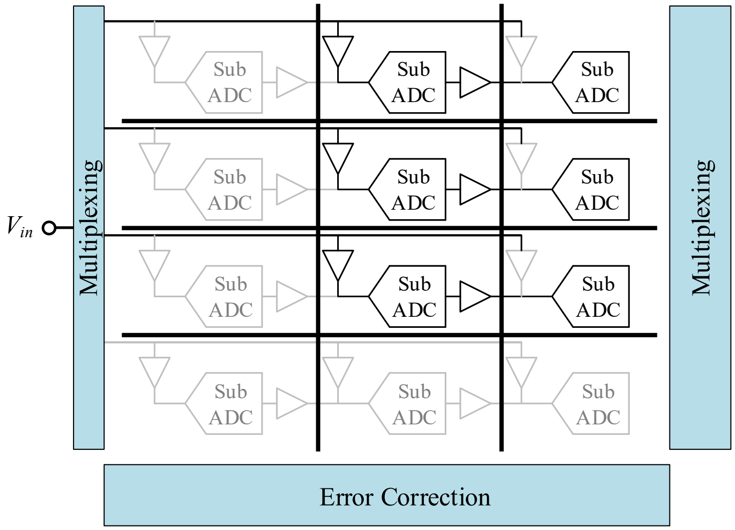


Figure 3.1: Concept of a software-configurable ADC with concatenated sub ADCs for increasable resolution and parallel sub ADCs for increasable sample rate.

The downside to this concept are first and foremost the area and power consumption overhead associated with the software-configurability. Furthermore, the multiple feed-ins of the input signal at critical points, the different buffers needed and the ability to switch off or combine individual cells, rows and columns increase the complexity further and are little investigated so far. This has a high initial development effort in effect. Mitigating these downsides is the prime challenge to make this concept competitive with dedicated, non-generic ADC solutions.

3.2 First Iteration of a Software-Configurable ADC

This thesis is a first step providing the basic research to investigate the feasibility of a software-configurable ADC concept as presented in the section before. The effort is very difficult to assess as no prior experience or literature exists in this field of development. Hence, a reduced, first ADC was conceptualized, developed, brought to tapeout and measured. It is the subject of this thesis and focuses on identifying weak spots and bottle necks. It may further serve as basis for continued development enhancing the software-configurability.
The figure 3.2 shows the schematic for the first implementation concept. The shown configuration was chosen as a compromise between the given time frame and a maximum of information that can be drawn from it for future developments. It consists of two sub ADCs in a pipelined configuration. If only a moderate resolution is needed in the target application, a so called low-power mode with a resolution of 8 bit can be used in which the first stage sub ADC is bypassed and the residue amplifier is switched off to reduce power consumption. For the full resolution, a so called high-precision mode, converts the signal through both sub ADCs. With one bit overlap for error correction a total resolution of 11 bit is thus reached.

The same input buffer is used for both modes in this first concept due to time constraints at the cost of decreased power efficiency. Since this is only a proof of concept, it is negligible here. The two implemented sub ADCs exhibit a large imbalance in the bit distribution with the first sub ADC converting only 4 bit and the second sub ADC converting a total of 8 bit. This setting which will be explained in more details later on evolved from the fact that the first sub ADC needs a longer time per bit as its reference voltage has to settle to higher precision. This is something that might be applicable in the final software-configurable ADC as well having the right-most column of ADC cells differ from the rest through an increased resolution, increasing the flexibility in configuration even further. Additionally, support for a second channel is included by a second, parallel set of pipelined sub ADCs that can also be switched off independently.

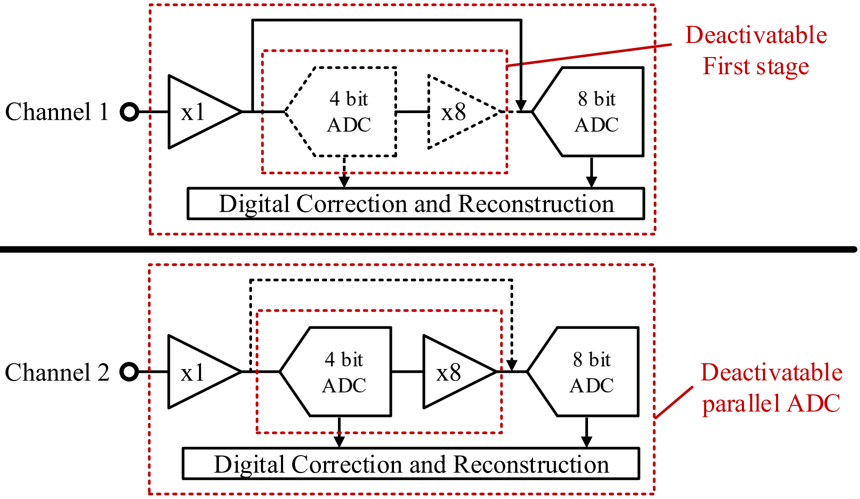


Figure 3.2: Schematic of the first implemented version of a software-configurable ADC.

For the sub ADCs the SAR ADC architecture was chosen. The literature research shows the dominance of SAR ADCs in all application areas. Its superior area and energy efficiency is a corner stone of the generic software-configurable ADC concept. A SAR ADC's mostly dynamic circuits consume no power in idle when no conversion is happening. This means that it scales inherently with sample rate and needs no dedicated circuits to power it down and only the clock signal needs to be suppressed. Due to the energy efficiency of the SAR ADC, it is also favorable in a pipelined ADC configuration to convert as many bits as possible in one stage. This however has a direct impact on the overall highest sample rate. Nowadays the main limiting factor is the gain bandwidth product of amplifiers which dictates the smallest residue voltage that can be recovered to a full-scale signal at a given sample rate. The resolution of 4 bit in the first stage therefore is an optimum found for this application between energy efficiency of the SAR ADC, the maximum sample rate and the restrictions of the residue amplifier.

3.3 Process Technology Choice

For this pilot project a 28 nm bulk CMOS process technology is used. It was established in 2011 and is therefore a very mature and well characterized technology with a high yield. Research however only just started to migrate to this more modern process technology (see section 1.1). The choice can be attributed to two reasons. The first is more of universal nature. The increasing integration factor and energy efficiency is the key enabler for this concept of a generic software-configurable ADC allowing it to compete with dedicated solutions. Furthermore, it is the last silicon bulk node before more complex manufacturing processes, namely FinFET [57] and FDSOI [58], have to be deployed to control unwanted side effects in even smaller technology nodes. Therefore, to a large extent, traditionally used design methods can be used keeping the effort tolerable.

The second reason is more application driven with particle detector experiments as its target field. With 65 nm bulk CMOS being the state of the art [2], 28 nm bulk CMOS is the discussed successor for future detector integrated electronics, when highest performance is needed [3]. Its high integration factor allows the implementation of powerful digital signal processing on-chip, while analog performance and conventional design methodologies largely stay valid. As it is still a planar bulk silicon process, manufacturing costs are still manageable and the design effort stays at an acceptable level for small-scale prototype chips. Furthermore, 28 nm processes from two different manufacturers were investigated extensively for total ionizing radiation dose impact and compared against 65 nm and 130 nm by CERN. It shows a significantly higher radiation hardness than currently used process technologies. In contrary to older nodes, smaller transistor lengths here also have a positive impact on the radiation hardness which allows 28 nm to take full advantage of the technology shrink [59].

Chapter 4

First ADC Chip

A first chip was manufactured as a pre-development to get familiar with the new process technology used for the first time at the institute. It acted as a pilot project to assess the benefits and drawbacks migrating from a previously used 65 nm node to a 28 nm process technology. The scientific purpose of the project which was done in cooperation with an external research partner, is to detect high electromagnetic interference without taking damage or disruption of the detection while being exposed to the electromagnetic field itself. Such a use case occurs in magnetic resonance imaging for example. To this end a SAR ADC was implemented for the digital conversion. As only a qualitative signal detection for this first version was necessary, the implemented SAR ADC can be seen as a pre-development of a sub ADC for the concept of a pipelined, software-configurable ADC. The architecture of all implemented circuit blocks was kept simple purposefully throughout the chip to increase the success rate for correct operation and ease verification in the laboratory and error analysis.

This chapter focuses on the development of the SAR ADC only as the discussion of the whole chip would be out of scope for this thesis and is furthermore not relevant for the concept presented herein.

4.1 Overview SAR ADC

Figure 4.1 shows an overview of the main blocks used in a SAR ADC. Deviations from the shown composition exist to some extent, but the one shown is the most common and the one used for the implementation in the ADCs in this thesis. For the illustration a differential structure was chosen, because it is the most prominent. Single-ended designs are used only rarely, e.g. in ultra-low power applications like biomedical monitoring. The individual blocks will be explained in more detail subsequently. Here, only a short summary and the relation between the blocks is given.

Track-and-Hold - The input signal going to the ADC is usually buffered through an input buffer stage as it eases signal feed-in at high frequencies and allows also accurate sampling from weak sources. As precise and fast amplifiers are difficult to design in new process nodes and are very power hungry, some designs choose to implement off-chip buffering. For the switches typically a bootstrapped architecture is used which keeps the gate source voltage and therewith the resistance of the transistor constant to reduce harmonics and to keep the overall resistance in the signal path low. The buffer and the switches together with a sampling capacitance form a so called track-and-hold circuit. In a SAR ADC, the sampling capacitor is merged with the capacitive DAC described next.

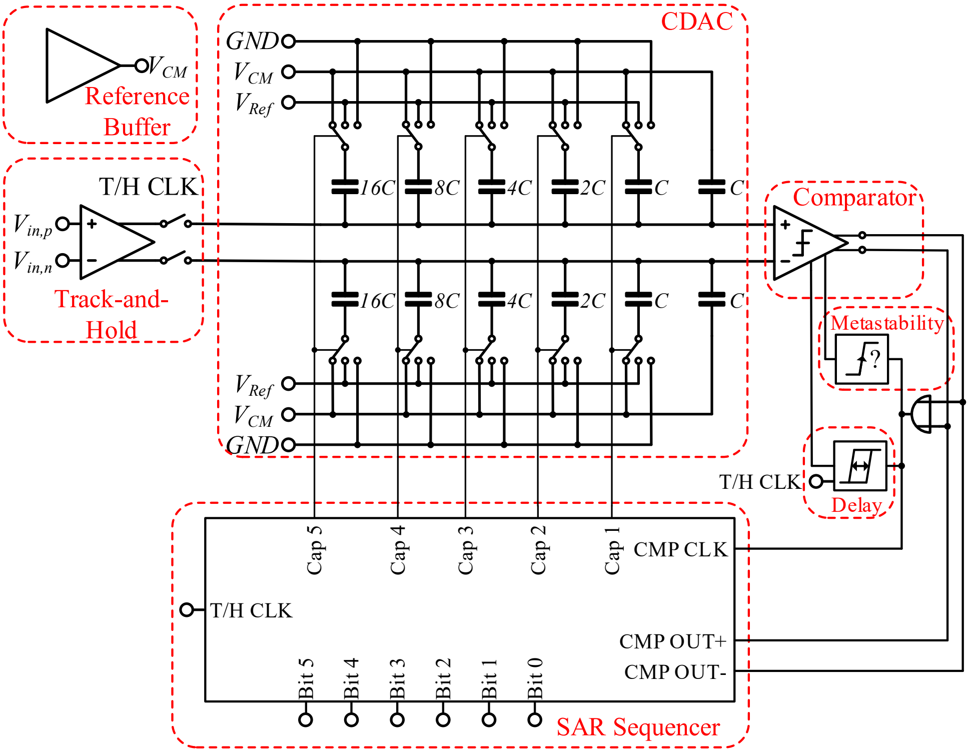

Reference Buffer
V_{CM}
CDAC
GND
V_{CM}
V_{Ref}
16C
8C
4C
2C
C
C
T/H CLK
$V_{in,p}$
$V_{in,n}$
Track-and-Hold
Comparator
Metastability
Delay
T/H CLK
Cap 5
Cap 4
Cap 3
Cap 2
Cap 1
CMP CLK
T/H CLK
CMP OUT+
CMP OUT-
Bit 5
Bit 4
Bit 3
Bit 2
Bit 1
Bit 0
SAR Sequencer

Figure 4.1: An overview about the main blocks comprised in a SAR ADC.

Capacitive DAC - The most dominant form to generate reference voltages used in the conversion process is with a capacitive digital-to-analog converter (CDAC). The reference voltage is subtracted or added directly to the input signal which allows to use the implemented capacitors both for sampling and for conversion. There are many different switching schemes tailored to various specialized use cases; the depicted one is only one example.
Comparator - After every conversion step a comparator decides whether the positive input signal minus or plus the current reference voltage is greater than the negative input signal minus or plus the current reference voltage which determines the current bit. A dynamically clocked comparator is usually used which consumes no static power when no decision is needed.
Delay Element- In an asynchronous design which is shown here, the individual conversion steps are timed by the SAR ADC itself. For this, the comparator output is used to indicate the end of the current conversion step, whereupon the next conversion step can be started. The required settling time for the reference voltage is adjusted by a delay element clocking the comparator activation. For synchronous designs no delay element is needed and the activation of the comparator is done from outside via a dedicated clock. This has to be as many times faster than the sample rate as the number of bits to convert in one cycle.
Metastability Detector - If the voltages at the positive and the negative input of the comparator are very close to each other, the decision time can be very long and exceed the allocated

time frame for a conversion step. This behavior of the comparator is called metastability. In an asynchronous operation a metastability detector catches these errors and forces a decision. This causes then only an LSB error instead of ruining the whole sample. In a synchronous mode, this metastability detector is not needed as the external clock dictates a hard limit for the maximum decision time. At the end of it, a decision of the comparator can be enforced then as well.

Sequencer - To coordinate the process flow in the SAR ADC a state machine is implemented which starts the conversion cycle at the respective edge of the global sampling clock, controls the switching in the CDAC for new reference voltages, ends the conversion cycle and saves the bit representation of the input signal for handover for further processing. There is no fixed name for this block in the literature; in this thesis it is called *sequencer*.

Reference Buffer - Some switching schemes for the CDAC utilize an additional initial reference voltage. In the case shown here, it is equal to the common-mode voltage V_{CM} which is half of the supply voltage. For this a dedicated buffer is usually implemented.

4.2 Technical Specifications

As the target application for the first chip does not impose strict requirements on the SAR ADC, these are instead derived from the design effort accomplishable in a given time frame and which implementations help assess potentials as well as limitations for the architecture in the next chip.

As the SAR ADC is a pre-development for a sub ADC in the future software-configurable concept, its physical resolution was set to 6 bit. The expected ENOB is 5 to 5.5 bit. It is a conservative estimate due to lack of experience, but not uncommon in high-speed designs.

The resolution and speed are closely connected to each other in a SAR ADC due to its recursive nature of conversion. First simulations and estimates concluded at an upper boundary of 500 MSPS for this first investigation. The lower boundary was set to 300 MSPS, because layout dependent parasitic elements make up a significant portion of the overall performance in small nodes such as 28 nm used here. In the following, calculations and considerations however are still done under the assumption of a sample rate of 500 MSPS or a sample period of 2 ns, respectively. The overall timings in the SAR ADC are illustrated in Fig. 4.2. For the first chip a 50 % duty cycle was implemented to keep the complexity low. The sampling phase which is also used to reset all blocks in the ADC thus has a relaxed duration of 1 ns. Likewise, the conversion phase also takes place in 1 ns. The comparator resolving time budget was determined in first investigations to 50 ps. With six bits to be resolved this leads to a total time of 300 ps for the combined comparator decision times. For the CDAC settling time of the reference voltage a duration of 100 ps was determined. Because the first bit does not need a reference voltage adaption, in sum a total of 500 ps is allocated to the CDAC settling. Overall the conversion cycle needs therefore only 800 ps leaving 200 ps as design margin and to lower the effect of metastability events.

Optimizing for power consumption has least priority in this first study and is of minor concern. Using literature as orientation, a power budget for the SAR ADC in the single-digit milliwatt range was set.

Full-scale input range amplifiers are realizable only at very low input frequencies, because the

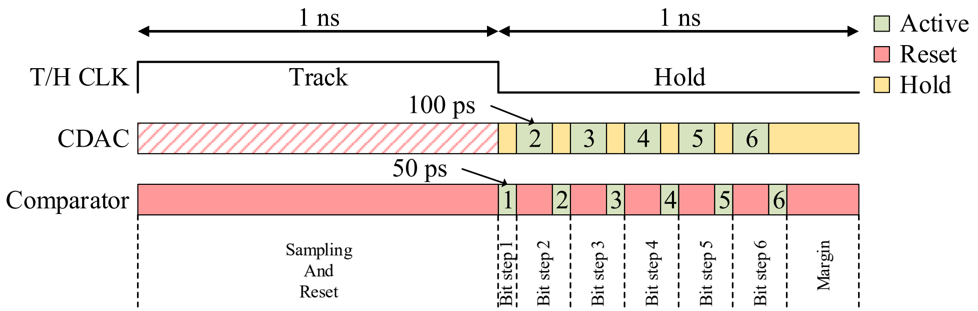


Figure 4.2: Illustration of the sample and conversion cycle timings of the implemented SAR ADC.

output transistors fall out of saturation at the upper and lower end of the supply voltage. To relief the burden and increase the design margin for high frequency operation, the single-ended input voltage range was defined to 450 mV peak-to-peak which is half of the supply voltage of 900 mV for core devices in this process technology.
The sampling capacitor in the CDAC is over-dimensioned with a value of 1.8 pF. For the given differential maximum input voltage range of 900 mV peak-to-peak, this would relate to an ENOB of 12 bit with enough margin for other error sources according to Fig. 2.5. This decision was done to investigate the implications of using the SAR ADC implemented here as a first stage sub ADC in a pipelined ADC as needed for a future software-configurable ADC. Furthermore, it tests the limits of input buffers with high resolution at high sample rates in the used 28 nm process technology.

4.3 Asynchronous Operation

While a synchronous design has the advantage of a simpler conversion cycle timing, it increases the overall power consumption in the chip considerably. This is because the clock driving the conversion cycle has to run at a significantly higher speed than the sample clock to process all individual conversion steps in time. This increases the demands on the clock generation significantly. For this reason an asynchronous design is chosen. It might need a one-time calibration of the delay and metastability detector for optimal operation speed, but this initial effort is outweighed by the superior power efficiency of an asynchronous design which is even more important for high-speed applications. .

4.4 Capacitive Digital-To-Analog Converter

The CDAC is the most sensitive part in a SAR ADC. Apart from power and area consumption, attention has to be paid to the mismatch the individual capacitors in the CDAC exhibit and the thermal noise that is generated in combination with the capacitors. Noise coupling into the CDAC by reference voltage sources and their overall precision is an additional disruptive factor.

The charge injection through transistors used as switches and the kickback noise coming from the comparator plus its dynamic offset changes also has to be considered to arrive at the final accuracy of the CDAC.

Numerous different kinds of CDACs have been developed catering all to different application needs. Among them one can differentiate in a first step between so far only little investigated charge-sharing and the dominant well characterized charge redistribution CDACs. Among popular modifications is the split-capacitor technique dividing the CDAC into two parts connected by a series capacitor which reduces the total amount of capacitors needed. A non-binary CDAC implements redundancy for bit decisions mitigating dynamic offset changes and incomplete reference settling [60] [61]. 2-bit-per-cycle architectures uses multiple CDACs and comparators in parallel to increase the sampling rate [62].

In the following the conventional CDAC will be discussed in detail to explain the operation principle, as well as the two most prominent switching schemes which are also used in the SAR ADCs described in this thesis.

4.4.1 CDAC Switching Scheme

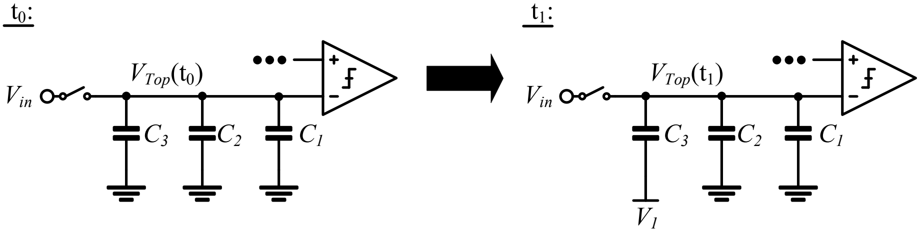


Figure 4.3: Principle theory for the capacitive DACs.

Charge redistribution CDACs, first described in [63], are the most popular architecture for reference voltage generation in SAR ADCs due to their power-efficiency and low complexity in implementation and operation control. Their principle of operation can be explained with the help of Fig. 4.3. Initially, at a time t_0, the charge at the side connected with the comparator and the input sampling switch, in the following called top side, $Q_{Top}(t_0)$, can be calculated as

$$Q_{Top}(t_0) = V_{Top}(t_0)\ (C_3 + C_2 + C_1)\,. \tag{4.1}$$

V_{Top} is here the voltage at the negative input of the comparator. In a next time step t_1 the voltage at the side facing away from the comparator, in the following called bottom side, is changed for capacitor C_3. In the example it is charged from ground to V_1. The charge $Q_{Top}(t_1)$ can then be calculated to

$$Q_{Top}(t_1) = \big(V_{Top}(t_1) - V_1\big)\ C_3 + V_{Top}(t_1)\,C_2 + V_{Top}(t_1)\,C_1. \tag{4.2}$$

Since the charge at the top side is insulated, it stays the same and the following relation holds

$$Q_{Top}(t_1) = Q_{Top}(t_0). \tag{4.3}$$

Therefore, as the charge stays the same, the voltage at the topside $V_{Top}(t_1)$ has to change which can be derived finally as

$$V_{Top}(t_1) = V_{Top}(t_0) + V_1 \left(\frac{C_3}{C_1 + C_2 + C_3} \right). \tag{4.4}$$

If a binary scaling with $C_1 = C_2$ and $C_3 = 2\,C_2$ is implemented, the new voltage at the top $V_{Top}(t_1)$ becomes

$$V_{Top}(t_1) = V_{Top}(t_0) + V_1 \left(\frac{1}{2} \right). \tag{4.5}$$

This scheme thus allows to implement the binary search algorithm needed for the SAR ADC architecture.

Throughout the years many different switching schemes were invented. As reference for comparison, it was established to use a 10 bit differential version of [63]. Its switching scheme is as follows. In a first step, the input signal is sampled on the bottom plates of the capacitors. The top plates are connected to a common-mode voltage. After the sampling phase, the top plates are disconnected. On the side of the CDAC connected to the positive input of the comparator, the first capacitor, responsible for the MSB conversion, is switched to a voltage V_{Ref}, often set equal to the supply voltage, while all other capacitors on the positive side are connected to ground. On the side connected to the negative input of the comparator, the capacitors are switched in reverse, with the MSB capacitor connected to ground and the rest connected to V_{Ref}. Subsequently, the comparator determines the first bit. If the first bit is a one, the second capacitor on the positive side is connected to V_{Ref} and the second capacitor on the negative side is connected to ground. If the first bit is a zero however, while the second capacitor on the positive side is again connected to V_{Ref}, the first capacitor on the positive side is also switched to ground now. Similarly on the negative side, the second capacitor is again connected to ground, the first capacitor however is switched also from ground to V_{Ref}. This scheme continues for all following bits. The drawback of this switching implementation is that it dissipates a lot of energy for a down transition, when the comparator determines a zero bit, as it changes the voltage on two sets of capacitors.

Another switching scheme is called monotonic switching [64]. Its aim was to improve the energy efficiency compared to the conventional CDAC structure. The signal is now sampled on the top side of the capacitors, while the bottom side is connected to a reference voltage V_{Ref}. After the sampling, the top side capacitors are disconnected from the signal source and the bottom side of the individual capacitors are only switched down from V_{Ref} to ground. For the first bit there is no switching needed. Thereafter, if the comparator determined a one for the first bit, the first capacitor on the positive side of the CDAC is switched to ground. If the comparator determined a zero, the first capacitor on the negative side is switched to ground. With this scheme no prior capacitors need to change voltage anymore. The control of the switches is also simpler reducing the complexity in the sequencer and only n-type metal-oxide semiconductor (NMOS) transistors can be used during conversion which have a higher mobility than p-type metal-oxide semiconductor (PMOS) transistors. Finally, this switching scheme in general needs only half the capacitors in total for the same amount of implemented resolution in bits. A severe drawback however is its decreasing common-mode voltage during every conversion step converging towards zero. This causes a dynamically changing offset error in the comparator which reduces the effective precision. A slight variation can be applied to

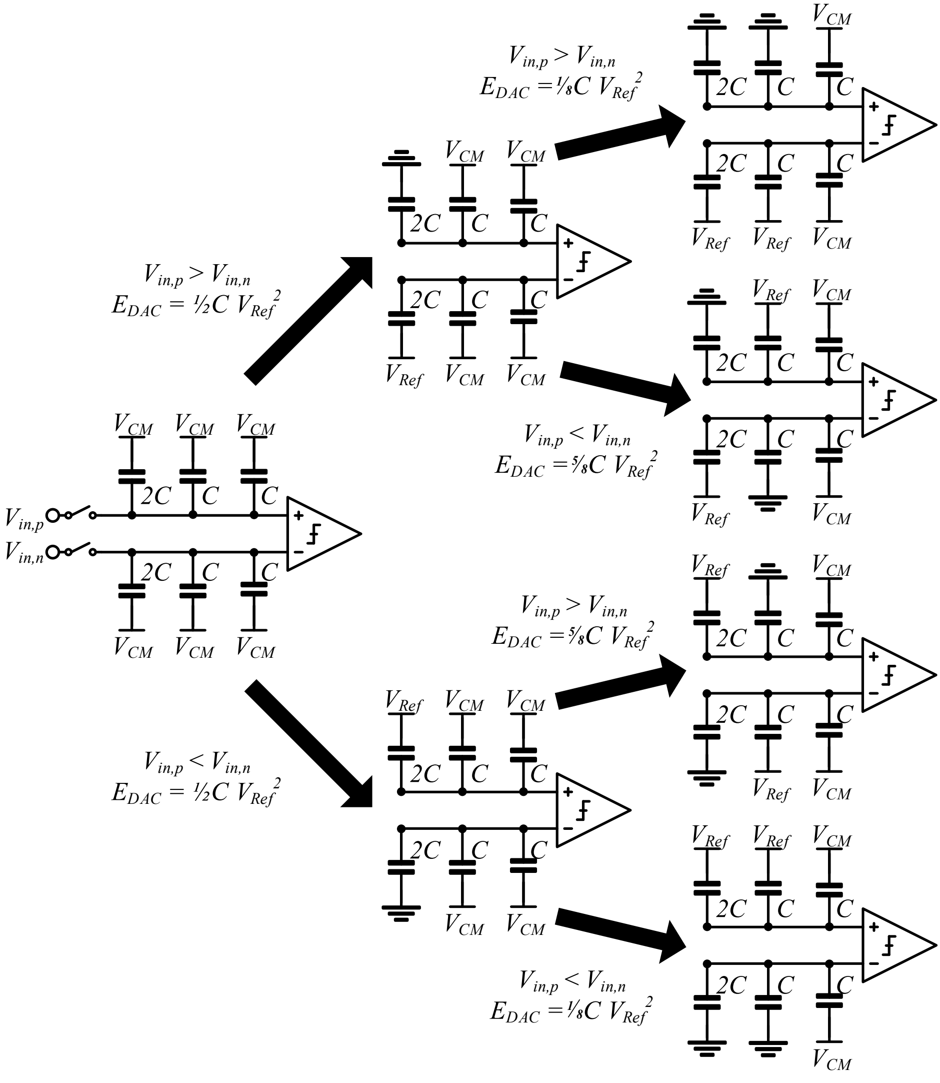

V_in,p > V_in,n
E_DAC = ⅛C V_Ref^2
V_CM
2C
C
C
V_Ref
V_Ref
V_CM
V_CM
V_CM
V_in,p > V_in,n
E_DAC = ½C V_Ref^2
V_CM
V_CM
V_CM
2C
C
C
Vin,p
Vin,n
V_Ref
V_CM
V_CM
V_Ref
V_CM
V_in,p < V_in,n
E_DAC = ⅝C V_Ref^2
V_Ref
V_CM
V_Ref
V_CM
V_in,p > V_in,n
E_DAC = ⅝C V_Ref^2
V_Ref
V_CM
V_CM
V_in,p < V_in,n
E_DAC = ½C V_Ref^2
V_Ref
V_CM
V_Ref
V_Ref
V_CM
V_Ref
V_CM
V_CM
V_in,p < V_in,n
E_DAC = ⅛C V_Ref^2
V_CM

Figure 4.4: Principle of the switching scheme for a V_{CM}-based CDAC.

this scheme by connecting the bottom side of the first capacitors on the positive and negative side to ground instead of V_{Ref} during sampling and reverse-switch them to V_{Ref} during conversion. By this, the common-mode voltage change is halved in comparison to the standard monotonic switching scheme and converges to the common-mode voltage.

The V_{CM}-based CDAC switching scheme improves the energy efficiency further [65]. This is accomplished by introducing a second reference voltage, usually the common-mode voltage V_{CM}, as the starting position for the subsequent conversion cycles. An illustration of the conversion cycle for this switching scheme is shown in Fig. 4.4. The signal is also sampled on the top plates of the capacitors as in the monotonic switching scheme which allows to determine the first bit directly without any voltage change in the capacitors. The bottom plate is connected to V_{CM} during sampling. In the conversion phase, after the first bit is found, the capacitors on the negative and positive side of the CDAC responsible for the next bit are switched oppositely to V_{Ref} or ground respectively. If, for example, the comparator determined a one for the first bit, the first capacitor on the positive side is switched from V_{CM} to ground and the first capacitor on the negative side is switched from V_{CM} to V_{Ref}. This procedure is continued until all bits are determined. The progression of the individual voltage levels after every conversion step is also illustrated in Fig. 4.5a. The energy dissipation for every conversion

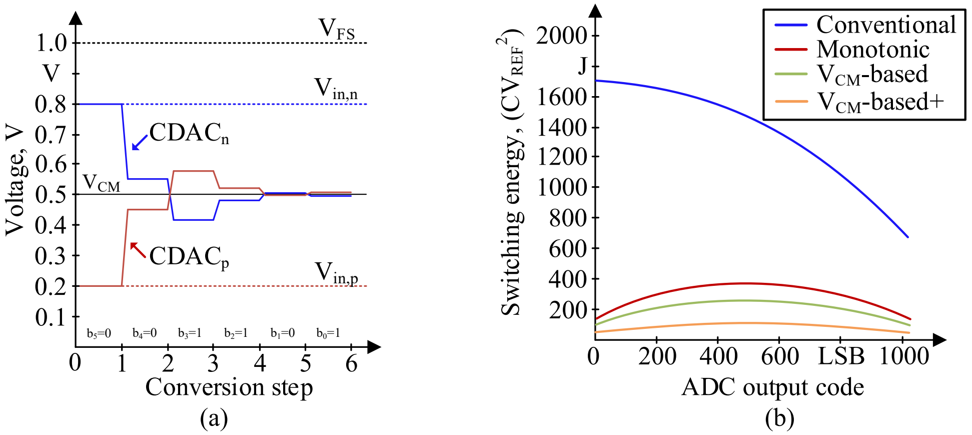


Figure 4.5: (a) Progression of the voltage on the top side of the CDAC and the negative side of the CDAC for the V_{CM}-based switching scheme for a 6 bit ADC. (b) Switching energy for different switching schemes plotted for every output code of a 10 bit ADC.

step is shown in Fig. 4.4. It can be derived with the equation

$$\begin{aligned} E &= \int_0^T i(t)\, V_{Ref} dt = -V_{Ref} \int_0^T -\frac{dQ}{dt} dt \\ &= -V_{Ref}\, C \left[\left(V_T(T) - V_B(T) \right) - \left(V_T(0) - V_B(0) \right) \right]. \end{aligned} \tag{4.6}$$

Here, $V_T(T)$ and $V_B(T)$ are the final voltage on the top and bottom plate of the capacitor at the end of the charging process. $V_T(0)$ and $V_B(0)$ are the initial voltage on the top and bottom plate of the capacitor at the start of the charging process. As an example, the energy dissipated after the capacitor determined a one for the first bit can be calculated in the following way. The first capacitor on the bottom side of the CDAC is switched from V_{CM} to V_{Ref}. Its energy is therefore calculated to

$$\begin{aligned} E &= -V_{Ref}\,2\,C\,\left[\left(V_{in,n} + 0.5\,V_{CM} - V_{Ref}\right) - \left(V_{in,n} - V_{CM}\right)\right] \\ &= 0.5\,CV_{Ref}^2. \end{aligned} \tag{4.7}$$

The remaining capacitors on the bottom side of the CDAC also dissipate energy which can be calculated to

$$\begin{aligned} E &= -V_{CM}\,2\,C\,\left[\left(V_{in,n} + 0.5\,V_{CM} - V_{CM}\right) - \left(V_{in,n} - V_{CM}\right)\right] \\ &= -0.25\,CV_{Ref}^2. \end{aligned} \tag{4.8}$$

On the top side, the first capacitor is only discharged from V_{CM} to ground dissipating no energy, but the remaining capacitors' energy dissipation can be calculated in the same way as before to

$$\begin{aligned} E &= -V_{CM}\,2\,C\,\left[\left(V_{in,p} - 0.5\,V_{CM} - V_{CM}\right) - \left(V_{in,p} - V_{CM}\right)\right] \\ &= 0.25\,CV_{Ref}^2. \end{aligned} \tag{4.9}$$

It can be seen here that the energy from the non-switching caps on the top side and the bottom side of the CDAC compensate each other. This charge-recovery is a major contributor to the increased energy efficiency of this switching scheme. Furthermore, it relaxes the current driving requirements for the source providing the common-mode voltage. The total energy dissipation for the second bit is thus $0.5\,CV_{Ref}^2$. All these calculations are done under the assumption that V_{CM} is half of V_{Ref}. Otherwise charge-recovery would lose its fully compensating effect. The precision of the ADC is however not affected by the accuracy of the V_{CM} source as its value is canceled out through the differential signal processing. It only needs to stay constant during the conversion cycle. Aside from the superior energy efficiency, the common-mode voltage is not shifted in this switching scheme in contrast to the monotonic switching scheme which keeps the offset of the comparator static and increases precision. A drawback of this switching scheme is the need for additional switches for the second reference voltage and control of these which increases complexity. Pre-charging the bottom side of the capacitors to V_{CM} is also linked to more effort in modern process nodes as both NMOS and PMOS transistors exhibit a high resistance around half of the supply voltage. Furthermore, a generator for the second reference voltage is needed that consumes additional power and chip area.

A modification to the V_{CM}-based CDAC switching scheme utilizes also the last capacitor which is normally statically connected to one voltage to achieve a binary weight distribution [66]. It is henceforth called V_{CM}-based+ switching scheme. Switching only the positive or negative side capacitor from V_{CM} to ground allows to resolve one more bit with the same amount of total capacitors. In other words, with this implementation the number of capacitors, and thereby the energy dissipation, can be halved again in comparison to the pure V_{CM}-based switching scheme. The common-mode voltage will change for the LSB decision increasing the impact of the dynamic offset from the comparator again however. As it changes only by the small amount of half the LSB voltage, its impact can be countered with a more robust comparator design. An even more serious drawback is that the V_{CM} now has an effect on the precision and needs to be precisely half of the reference voltage V_{Ref} as there is no more complementary switching on the top or bottom side of the CDAC negating deviations.

Table 4.1: Properties of most prominent switching schemes and the switching scheme adopted in this thesis for the CDAC in SAR ADCs. The values given in this table are calculated assuming a 10 bit resolution of the ADC.

	Average switching energy [C V^2]	Total unit capacitors	Static V_{CM}	V_{CM} precision needed
Conventional [63]	1363.3	2048	yes	no
Monotonic [64]	255.5	1024	no	no
V_{CM}-based [65]	170.1	1024	yes	no
V_{CM}-based+ [66]	84.9	512	not for LSB	yes
This work	84.9	512 + 1	not for LSB	no

The table 4.1 summarizes the different properties of the presented switching schemes. For the energy dissipation, it has become common practice to assume an implemented resolution of 10 bit in the CDAC. This alleviates comparisons between different switching schemes. The switching scheme used in the implemented SAR ADC of this chapter is also prematurely added to the table for a better comparison overview. Furthermore, the switching energy for every output code of an ADC with 10 bit resolution for all presented switching schemes is illustrated in Fig. 4.5b.

4.4.2 Implementation

A schematic of the implemented CDAC can be seen in Fig. 4.6. It adopts the V_{CM}-based switching scheme with a modification to the last bit. There are switching schemes that dissipate even less switching energy, but are more complex to implement and have higher demands for accuracy in the remaining circuit blocks. Therefore, the V_{CM}-based switching scheme offers the best tradeoff between energy dissipation, resolution and speed. The sampling capacitor value needed in the CDAC to reach a certain kTC noise performance is usually composed of many small unit capacitors. Starting with one unit capacitor C_U for the LSB and going up in size in binary steps by implementing multiple unit capacitors in parallel. This ensures a high matching rate in the physical layout of the CDAC. In this implementation however, the starting capacitor has a value of $^1/_2\ C_U$. It is formed by placing two capacitors in series whereby the matching accuracy is not reduced. Thus the amount of unit capacitors is halved plus one for the series capacitor. The second half-unit capacitor needed for binary proportions of the capacitors in the CDAC is omitted in this implementation as parasitic capacitance in the final physical layout will have a greater effect anyway. This is illustrated by the grayed out capacitors in Fig. 4.6. The switching for the LSB capacitors was also modified with only either the positive CDAC or the negative CDAC capacitor switching from the reference voltage to ground. This saves to a minor degree additional switching transistors and control circuits of these, but its main purpose is the investigation how much small common-mode voltages changes affect the precision of the ADC for future implementations. In contrary to the V_{CM}-based+ switching scheme, it imposes

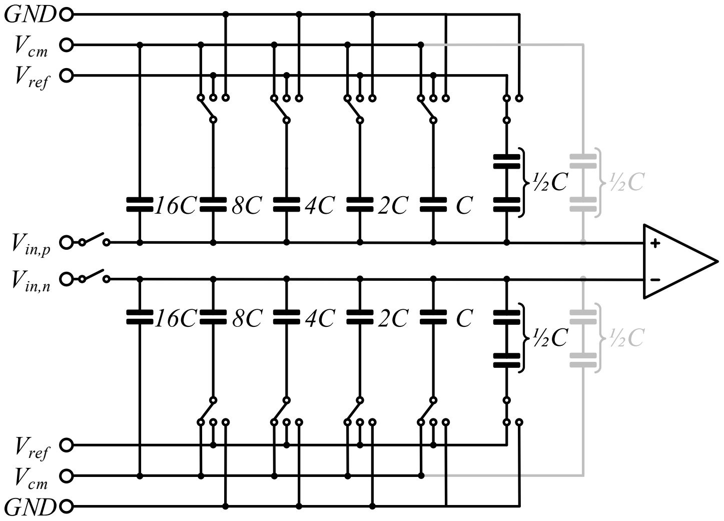


Figure 4.6: Modified V_{CM}-based switching scheme implemented in the SAR ADC in this thesis. The grayed out capacitors are omitted in design and layout as parasitic elements have a larger effect.

no accuracy requirements on the common-mode voltage source. There are two ways to adjust the voltage range of a CDAC to the maximum voltage range of the input signal. Either the reference voltage can be adjusted or further capacitors can be added, as was done for this implementation which act as reference voltage attenuation. The theory behind this can be explained with the help of Fig. 4.1. Here, the first capacitors with the size 16 C used usually for the conversion of the second bit are not switched on the bottom side but are connected statically to V_{CM}. The capacitor ratio is thus changed so that when the conversion starts with the capacitors with size 8 C, the signal is compared to a quarter of the reference voltage and not half of it as before. The main advantage of this implementation is that the full overdrive of the switching transistor for the charging of the capacitors is maintained maximizing speed. Furthermore, no additional, power-hungry buffer for the generation of the reference voltage is needed and instead the reference voltage can be set to the supply voltage. The main drawback however is the increased size of the CDAC which in this case uses twice the amount of unit capacitors.

The capacitor size of the CDAC is specified to have a total amount of 1.8 pF or 900 fF in the positive and the negative side of the CDAC respectively. Therefore, the area of the CDAC is determined by the capacitance per area parameter of the process technology. Reducing the total amount of capacitors through different switching schemes in this case mainly helps to reduce the wiring overhead for control and increases matching. A unit capacitor size of 28 fF is chosen as it can be layouted in a quadratic form which is beneficial for matching. With this and a total number of 63 capacitors a capacitance of 1.764 pF is reached which is deemed close enough to the targeted capacitance. With a 500 MSPS sample rate and an even time distribution between the sampling and the conversion phase, all 6 bit need to be converted in 1 ns. As the first bit needs no charge redistribution in the capacitors, this gives a total of six comparator decisions and five capacitor charge redistributions that need to settle to the required voltage accuracy. The implemented switching scheme utilizes three switches at the bottom plate of the capacitors. One is used to charge the bottom side of the capacitor during sampling to V_{CM}. NMOS transistors are used here, as they show a better resistance around the common-mode voltage of 450 mV. As the gate-source voltage and with it the resistance of the transistor changes throughout the charging process, the dimensions for the transistors were derived from simulations. They are relaxed however by the longer time frame of 1 ns in the sampling phase. The other two switches are an PMOS transistor, charging the capacitor to the supply voltage, and a NMOS transistor, discharging the capacitor to ground, during the conversion phase. Their resistance needed for a settling time of 100 ps can be calculated with the following equation

$$V_C(t) = V_{Supply} + \left(V_{Start} - V_{Supply}\right) e^{-\frac{t}{RC}}. \tag{4.10}$$

It describes the charging process of a capacitor C with a charging voltage of V_{Supply} through a series resistor R from a certain starting voltage V_{Start} to a voltage V_C. Solving for R the equation becomes

$$R = \frac{t}{C \ln\left(\frac{V_{Supply} - V_{Start}}{V_{Supply} - V_C}\right)}. \tag{4.11}$$

With $V_C = V_{Supply} - \frac{V_{Supply}}{2^N}$ being the value to which the voltage on the capacitor has to settle and $V_{Start} = V_{CM} = {}^1\!/_2\, V_{Supply}$ the equation finally resolves to

$$R = \frac{t}{C \ln\left(2^{N-1}\right)}. \tag{4.12}$$

With the resolution N chosen as 12 to stay consistent with the specifications and the size of a unit capacitor of 28 fF, the resistance of the transistors therefore has to be 468.4 Ω to settle in 100 ps.

The layout of the CDAC has a crucial impact on the overall accuracy which the ADC can reach. This is even more stressed in modern process technology nodes in which parasitic elements significantly reduce the overall performance of a circuit. Extensive care has to be taken to create an equal environment for all sensitive circuit parts. Figure 4.7 shows the distribution of the individual capacitors of the CDAC. It can be divided into two parts, because only the capacitors on the negative side $\mathrm{CDAC_n}$ and respectively only the capacitors on the positive side $\mathrm{CDAC_p}$ have to match to each other. The common-centroid layout technique was applied as it offers the best immunity against mismatch factors. Additionally, gaps in the layout were filled up and the perimeter was surrounded by so called dummy elements which are not-connected capacitors with identical dimensions. It ensures that all used capacitors are exposed to the same surrounding conditions during manufacturing. A drawback of this arrangement is the different length of the wires connecting the capacitors with the control switches. This can be mitigated by implementing additional insulating layers at the bottom and the top of the capacitors [67]. For the given implementation, the large size of the individual unit capacitors alone makes the influence of the wires negligible. The measured area on chip is 94.5 µm in width and 36 µm in height.

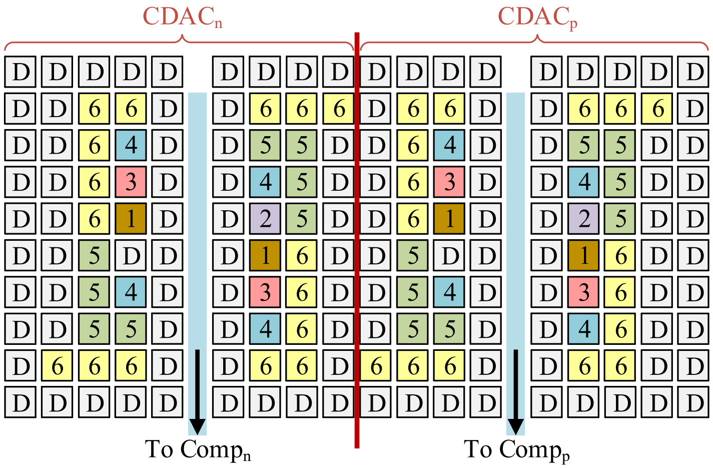


Figure 4.7: Illustration of the common-centroid distribution of the capacitors in the CDAC and additional dummy elements to create even manufacturing conditions for all unit capacitors.

4.5 Comparator

4.5.1 The Dynamic Latch-Based Comparator

For comparators in ADCs the dynamic, latch-based comparator has become the dominating architecture. It is able to attain a very high speed due to positive feedback, has high energy efficiency as it dissipates no static power and offers rail-to-rail output. Its general principle was first described with the now called strong-arm comparator [68] [69] which is shown in Fig. 4.8. The operation is divided into two operations. During the reset phase the CLK signal is low, transistor M1 is switched off and the auxiliary transistors M8, M9, M10, M11 reset the latch by forcing the output and intermediate nodes XP, XN to the supply voltage. In the second phase which is called regeneration phase, the CLK signal goes high and M1 is conducting. M2 and M3 start to discharge the nodes XP and XN and subsequently the output nodes. The input voltage thereby controls the speed at which the discharge happens. As soon as the threshold voltage of either M6 or M7 is reached, the respective branch starts to activate the positive feedback in the other branch and the latch regenerates.

With decreasing supply voltage in modern process technology nodes, the strong-arm comparator's many stacked transistors make it challenging to tune its performance. Additionally, the speed, noise and offset all depend on the input common-mode voltage. To overcome these issues, a two-stage latch-based comparator was invented called double-tail comparator [70]. It separates the input stage from the latching stage generating an extra degree of freedom in the design space. The first stage can thus be optimized for low offset, noise and also gain to suppress inaccuracies of the latch stage. The second stage can focus on fast latch regeneration with reduced dependency on the common-mode voltage. Additionally, the cascaded input stage protects the input of the comparator better from kickback noise which arises from the sudden voltage change in the latch coupled back unevenly through mismatch into the input ports.

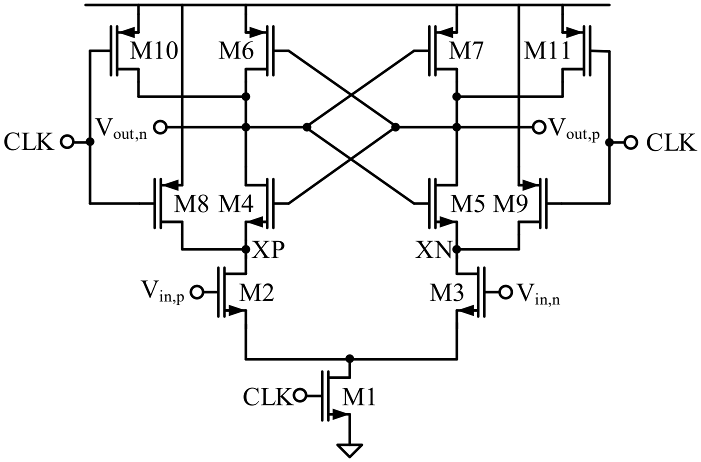


Figure 4.8: Schematic of a strong-arm, dynamic latch-based comparator [68] [69].

Furthermore, it is better suited for low supply voltage environments due to a reduced transistor stack [71].

4.5.2 Implementation

Figure 4.9 shows a modified version of the comparator presented in [72] which has an energy efficiency advantage over the original implementation. Additionally, in the first stage a cascode for the input transistors was added. This increased the gain and also reduced the kickback coming from the latch. Furthermore, the switching transistor in the tail was omitted and the cascode transistors are used instead to change from reset to regeneration phase. This compensates for the otherwise increased transistor stack and also mitigates the voltage kick coming from the switching transistor in the tail coupling through the input transistors into the input ports of the comparator. Instead a resistor $R1$ was added in the tail to limit the current flow and improve the gain of the first stage. In the reset phase now, M3 and M4 are switched off. M11 and M12 are charged to the supply voltage by the transistors M5 and M6. Transistors M13, M14, M15 and M16 reset the latch by pulling the output to ground and providing a defined potential at the drain of M11 and M12. In the regeneration phase M5 and M6 are then switched off, M3 and M4 are switched on and the first stage discharges the gate-source capacitance of M11 and M12 with a speed depending on the respective input voltage. As soon as the threshold voltage of transistor M11 or M12 is reached, the respective branch in the latch is charged until the threshold voltage of M7 or M8 is reached and the latch regenerates.
Figure 4.10 illustrates the output characteristic of the implemented dynamic comparator. A differential voltage of +20 mV was applied to the input around a common-mode voltage of 450 mV. The nodes XP and XN, shown in the violet and olive graph, discharge at different slopes building up an increasing difference in voltage. At 0.58 ns, transistors M1, M2, M3 and M4 fall out of saturation and the discharge curves flatten accordingly. The voltage at the outputs of the comparator, drawn in red and blue, increases both in the beginning, because

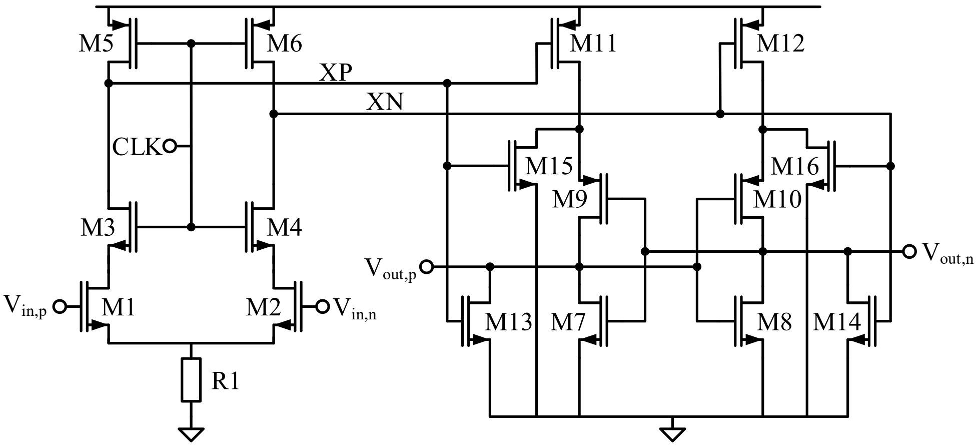


Figure 4.9: Schematic of the double-tail latched comparator implemented in the SAR ADC of this thesis.

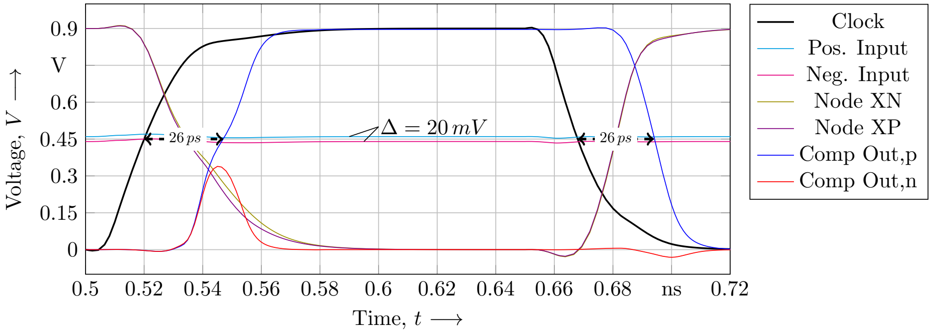


Figure 4.10: Simulated output characteristic of the comparator for a differential input voltage of 10 mV and common-mode voltage of 450 mV.

the threshold voltage of neither M7 or M8 is reached yet. At 0.54 ns, M8 starts to conduct, pulls down $V_{out,n}$ to ground and $V_{out,p}$ is pulled up to the supply voltage. The delay from the incoming clock signal to the regenerated output of the comparator is 26 ps in this case. This value varies depending on the input voltage applied to the comparator which can be arbitrarily small in theory. Practically, the noise of the comparator sets a limit to the smallest voltages seen by the input transistors. Apart from the regeneration delay, the reset time also has an influence on the duration one bit conversion steps of the SAR ADC takes. It should be kept as low as possible too, but as the reset transistors M13, M14, M15 and M16 increase the total load in the second stage, they cause a tradeoff between regeneration and reset time. The reset of the comparator can run in parallel to the settling of the reference voltage in the CDAC and therefore has a relaxed timing due to the high accuracy implemented in the CDAC. The reset delay for this implementation finally coincidentally resulted in 26 ps. The worst-case offset was determined with a Monte Carlo simulation over 1000 runs to 10 mV. All values were obtained by simulation with an extracted schematic, meaning all parasitic elements from wiring etc. are considered. The area on the chip needed for this comparator implemented is 9 µm in width by 8 µm in height.

4.6 Sequencer

4.6.1 The classical Sequencer

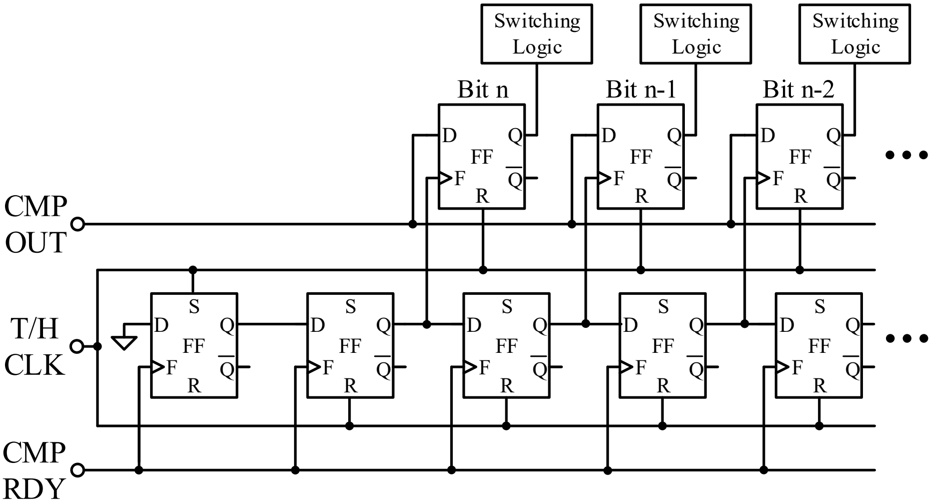


Figure 4.11: Classical sequencer built mainly out of D flip-flops (DFFs) [73].

The most straight-forward implementation for the control logic uses mainly DFFs [73]. A variation of it can be seen in Fig. 4.11. Here, a shift register is used built with DFFs propagating a logic high value. This activates and subsequently deactivates a memory register and additional switching logic step by step for the currently investigated bit. Although a sequencer consists only of digital circuits, it is usually not synthesized by hardware description languages and built out of full custom circuits. This is done to have maximum control over the properties and tune it to have minimum delay to increase the overall sample rate as well as to minimize the power consumption of the sequencer.

4.6.2 Implementation

The classical sequencer has a high transistor count as DFFs belong to the more complex digital circuits. This increases area on chip and power consumption. Additionally, it has a long critical path delay from the comparator output to the switching logic which first has to wait for the enable signal from the shift register and then has to propagate through the memory register. To alleviate these problems a sequencer was implemented as shown in Fig. 4.12. It shows only

one cell responsible for one bit sequence plus one start DFF on the bottom left. They can be concatenated for an arbitrary amount of bits. As long as the global sampling clock is in a high state, the sequencer is in reset mode and all circuit blocks are in a pre-defined state. Notice, that the transmission gates for the first bit and switching logic block are already passing the comparator output. Since it is in a low state during the settling of the current investigated bit, this causes no erroneous behavior. Thus when the global sampling clock goes in a low state and thereby starts a new conversion cycle, the signal of the comparator is directly altering the state of the relevant switching logic. This principle is continued in all following cells for the subsequent conversion steps. The switching logic is implemented through S-R latches in such a way that all three switches on the bottom side of the capacitors in a V_{CM}-based CDAC are addressed. The S-R latches consist of cross-coupled NOR logic gates which function also as buffers between comparator and CDAC. An additional S-R latch saves the resulting bit for this conversion step. It is not reset by the global sampling clock and only overwritten by the next conversion cycle. The timing restraint for handover of converted data for further digital processing is relaxed by this. To enable the next cell for the next conversion cycle, a sort of clock gating with the help of additional OR logic gates is implemented which closes the transmission gates of the current switching logic and opens the transmission gates of the next with the reset of the comparator. The final cell in this SAR ADC is slightly altered as it only needs to activate switches on one side of the CDAC.
From the comparator signal to the switching logic a delay between 64 ps and 96 ps is simulated

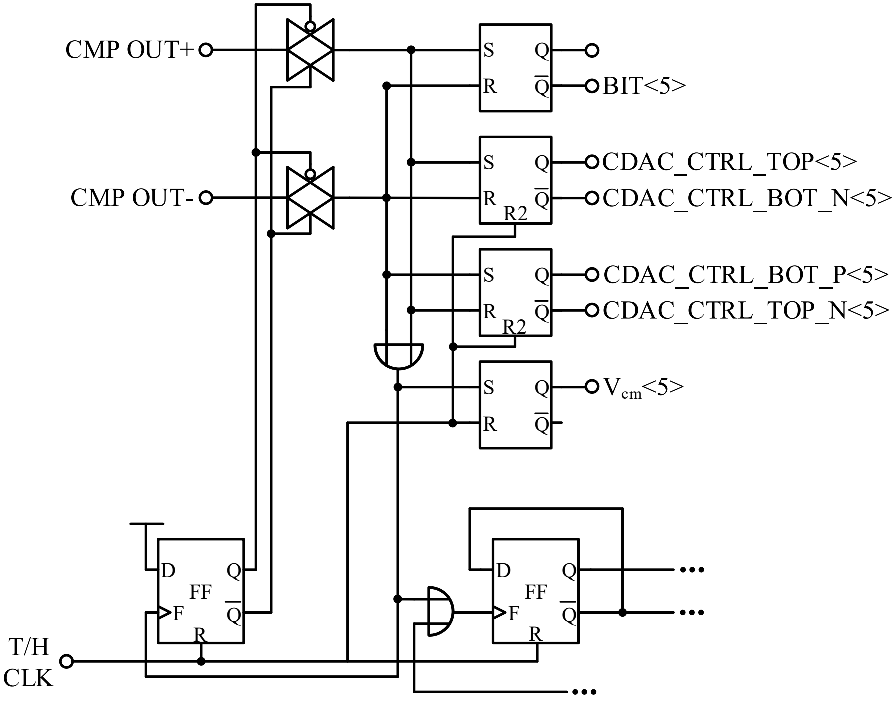


Figure 4.12: One cell of the implemented sequencer responsible for one conversion step plus one start DFF on the bottom left in the figure.

depending on the currently converted bit in after extracted view with parasitics. The measured area on chip is 46 µm in width by 5 µm in height.

4.7 Input Buffer

4.7.1 Specifications

For the input buffer a classical operational amplifier approach was chosen despite the challenging analog design space in modern process technologies. First simulations showed that for the given demands, it is still feasible. The requirements are summarized in Table 4.2. Parameters relieving the design constraints are the unity loop gain, a maximum nyquist input frequency of 250 MHz and a single-ended input signal amplitude of 225 mV. The precision of the input buffer however has to be very high for a resolution of 12 bit which translates to a gain error of 0.024 %. The open-loop gain A_0 needed for this value can be calculated with following equation [74, p. 276]

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \beta A_0}. \tag{4.13}$$

As the loop gain is one, the feedback factor β is also one. The open-loop gain then simply results in

$$A_0 = \frac{1}{\frac{V_{in}}{V_{out}} - 1} = 4095 \mathrel{\widehat{=}} 72\,\mathrm{dB}. \tag{4.14}$$

For the needed bandwidth this is difficult to achieve in modern process technologies. It should be noted that for the input buffer a reduced open-loop gain simply results in an attenuated input signal and therefore is tolerable. But a high open-loop gain also reduces the impact of process, voltage and temperature (PVT) variations on the closed-loop gain and decreases harmonic distortion coming from the amplifier [74]. Therefore, some of the open-loop gain can be sacrificed for better performance in other parameters, but careful monitoring of all variables has to be done so the input buffer is not becoming the bottle neck for the ADC performance. The settling time is limited to 1 ns and a high bandwidth and slew rate are needed, because the non-continuous track-and-hold operation demands a charging from the lowest to the highest voltage or vice versa in the worst case. This is intensified by the high single-ended load capacitance of 900 fF. A rough estimation for the closed-loop bandwidth needed in the operational amplifier, neglecting the slew rate, can be achieved with the equation

$$V_{out}(t) = V_0 \left(1 - e^{-\frac{t}{\tau}}\right) u(t). \tag{4.15}$$

It describes the step response of a linear feedback system with V_0 being the final voltage and $u(t)$ being the step excitation. Solving for τ and $t > 0$ with the condition $u(t) = 1$ for $t > 0$ the equation resolves to

$$\tau = \frac{-t}{\ln(\text{gain error})}. \tag{4.16}$$

Table 4.2: Specifications for the input buffer of the implemented SAR ADC. The high requirements to the gain error are derived from investigations for a future use in a high-resolution, pipelined ADC.

Parameter	Value
Voltage gain	1
Gain error	0.024 %
Single-ended output swing	225 mV
Single-ended input swing	225 mV
Load capacitance	900 fF
Settling time	1 ns
Max. input frequency	250 MHz

With the relation $f_{3dB} = \frac{1}{2\pi\tau}$, the 3-dB bandwidth for this implementation has to be at least $f_{3dB} = 1.33$ GHz. This can be used as orientation during the design phase. The offset of the input buffer will be small due to the loop gain of one and therefore have only a negligible effect on the performance of the ADC. It is not the focus during the design procedure.

4.7.2 Implementation

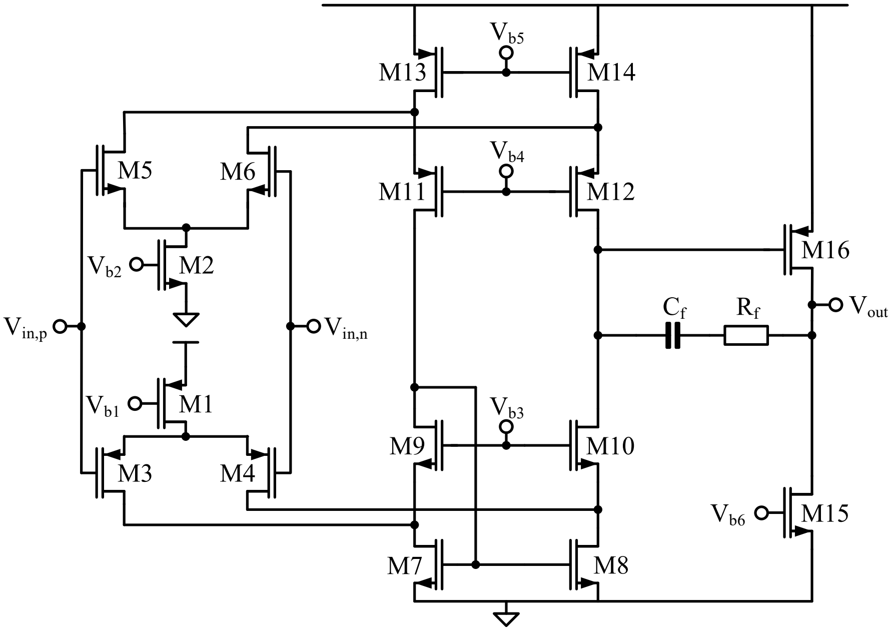


Figure 4.13: Schematic of the implemented input buffer for the implemented SAR ADC.

Due to the high open-loop gain and output swing needed, a two-stage architecture has to be deployed. Its schematic can be seen in Fig. 4.13. A pseudo-differential setup is used, meaning two individual input buffers are used for the positive and the negative input of the ADC. On the one hand this simplifies the design especially under the time constraint it is developed, because no common-mode feedback loops need to be implemented. On the other hand and more importantly, the influence of a common-mode voltage change on the performance of the ADC should be investigated and can be easily applied in a pseudo-differential setup which has no common-mode rejection. The first stage is a folded-cascode topology [74, p. 355]. While a telescopic operational amplifier [74, p. 351] has lower power dissipation, higher gain, higher pole frequencies and lower noise, it needs five transistor stacked which prohibits a robust implementation in modern process technologies. Additionally, the input signal range of the input buffer is very large. The folded-cascode topology can be expanded for this as shown in Fig. 4.13. Instead of using only the NMOS transistor pair M5 and M6 together with the NMOS transistor M2 as the input of the operational amplifier, in parallel a second pair of PMOS transistors M3 and M4 together with the PMOS transistor M1 are used. Now, if the input common-mode falls below a certain threshold which pushes M2 out of saturation and thereby reduces the gain, the PMOS input pair M3 and M4 together with M1 takes over which stays in saturation for low voltages. Linear scaling in simulation showed an optimum bias current for all branches of the folded-cascode first stage of 150 µA. The second stage is a common-source amplifier to maximize the output swing. It utilized a PMOS input transistor and a NMOS load transistor as simulations showed a favorable gain for this setup. The bias current is adjusted to 3.3 mA to cope with the high load capacitance. The feedback resistor R_f and capacitor C_f ensure frequency stability.
Figure 4.14 shows the bode plot of the loop gain and the phase margin of the input buffer. It reveals an open-loop gain of 58.9 dB which is lower than calculated in the specifications. The chosen topology shows a hard limit with regards to the other requirements here. As speed is of higher priority, the attenuation of the input signal is accepted as it can be countered with a higher input signal amplitude fed in to the input buffer. The unity-gain bandwidth is 4 GHz

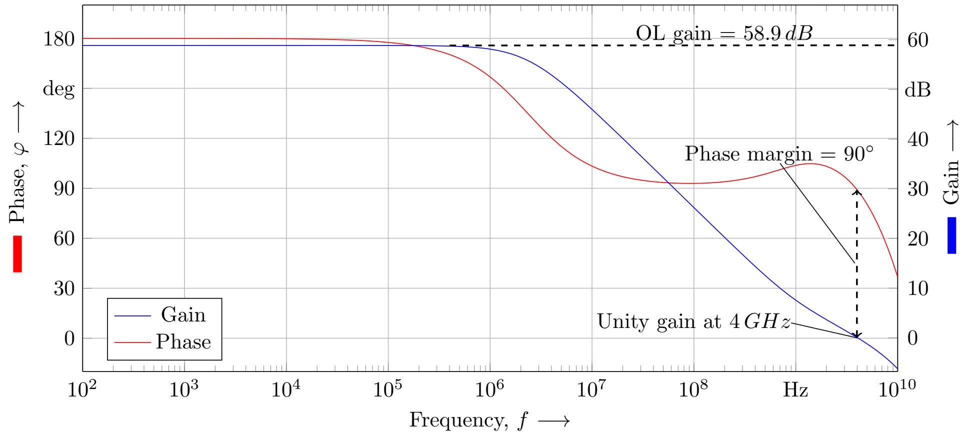


Figure 4.14: Gain and phase margin of the input buffer for the implemented SAR ADC.

which indicates that the 3-dB bandwidth of the input buffer with a gain of one will suffice the requirements. The phase margin is 90°. This is in line with the typical margin of 60° specified in literature for an unconditionally stable operation. However, the concept of phase margin is well suited for small signal analysis, this amplifier however experiences large voltage steps and does not follow the classical analysis anymore [74, p. 419]. Therefore, also the transient behavior with a maximum voltage step as excitation was investigated to find the optimum in both operation regions. For this, mainly the feedback resistor and capacitor were adjusted. Figure 4.15 shows the final step response of the input buffer without and with layout dependent parasitic elements. There is a dramatic increase in the required settling time from around 1 ns to 2.2 ns for a 12 bit precision. This would deteriorate the overall performance in terms of sample rate significantly. For a 6 bit precision however, the required settling time reduces to 1.2 ns again. While this is still outside of the specifications, it is close enough considering the time constraints. Further optimizations would include multiple cycles of redesigns and physical layout adjustments. A stable operation was verified in simulation with an extracted view together with a Monte Carlo simulation over temperature. The dynamic power consumption was simulated to 3 mW and the area on chip is 49 µm in width by 31 µm in height.

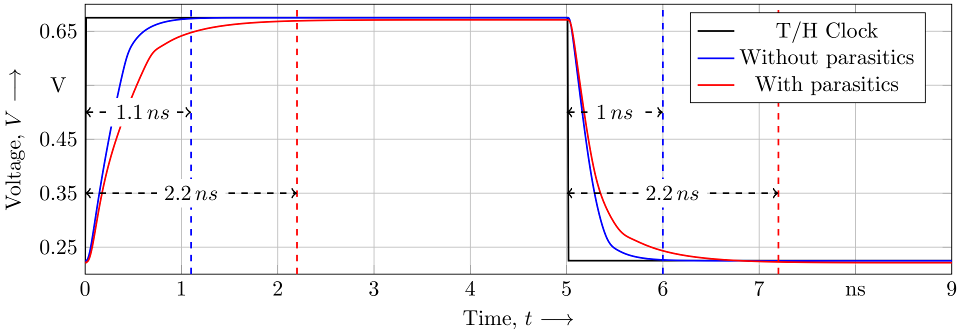


Figure 4.15: Step response of the input buffer for the implemented SAR ADC.

4.8 Bootstrapped Switches

4.8.1 Fundamentals

Using a simple transistor as track-and-hold switch, it is always in the ohmic region. The current flowing through it for a NMOS transistor can therefore be describes as

$$I_{DS} = \mu_n C_{ox}^{'} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right). \tag{4.17}$$

Here, μ_n is the mobility of the charge carriers in the transistor. $C_{ox}^{'}$ is the capacitance of the insulating layer between gate contact and transistor channel substrate per unit area. W and L are are the physical width and length of the transistor. V_{GS} is the gate-source voltage, V_{th}

is the threshold voltage and V_{DS} is the drain-source voltage of the transistor [74, p. 14]. With $R_{on} = \frac{V_{DS}}{I_{DS}}$ the equation becomes

$$R_{on} = \frac{1}{\mu_n C'_{ox} \frac{W}{L} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right)}. \tag{4.18}$$

This shows that the resistance of the switch has a strong input signal voltage dependency through V_{GS} which introduces distortion in the signal. Besides, it also only allows a maximum input signal voltage of $V_{GS} - V_{th}$ to stay on. A transmission gate which deploys a parallel PMOS transistor to the NMOS transistor, allows a full-scale signal voltage range, but also experiences resistance modulation especially at voltages around half of the supply voltage which is even more pronounced in modern process technologies. As a rule of thumb, a transmission gate as switch for analog signals allows a maximum ENOB of 6 bit [75].
To overcome this problem, implementations aimed at keeping the gate-source voltage constant and independent of the input signal voltage which culminated in the prototype for the bootstrapped switch that is used nowadays [76]. Here, a capacitor is charged to the supply voltage in the hold phase and connected in series with the input signal voltage from the source to the gate of the switch transistor during the sampling phase. This keeps the gate-source voltage constant at the maximum possible value.

4.8.2 Implementation

The implemented bootstrapped switch can be seen in Fig. 4.16. It is a modification of [77]. The core loop is formed by the transistors M1, M3, M4 and the capacitor C1. M1 is the pass transistor carrying the input signal to the sampling capacitor in the CDAC. M3 and M4 switch the pre-charged C1 in series with the input signal voltage and apply it to the gate of M1 ensuring a stable maximum gate-source voltage of 900 mV independent of the input signal voltage. M2 is added as it reduces harmonic distortion. In the hold phase, when $V_{CLK,P}$ is low and $V_{CLK,N}$ is high, M11 and M13 charge C1 to the supply voltage. M15 pulls the gate of M1 to ground and switches off M1 during this time. M14 is cascoded with M15 to prevent the gate-drain voltage of M15 to exceed the supply voltage which improves the reliability of the circuit. M5, M6 and M7 form the control circuit to switch on M4. Initially when $V_{CLK,P}$ goes high transistor, M6 pulls the gate of M4 to the ground potential, but as M3 applies the input signal voltage to the source of M6 it loses its driving capability. For this M5 is placed in parallel to M6 which is driven in the same bootstrapped way as M1 and therefore ensures that the gate-source voltage of M4 is also always 900 mV in the sampling phase. M3 which originally was connected to the same node as M1 is now controlled by M12, M8, M9 and M10. This reduces the capacitance connected to the node of M1 significantly as M3 needs a bigger width so the input signal voltage can effectively redistribute charge on C1. With this ultimately the size of C1 can be reduced, because the capacitive voltage division between C1 and the capacitance at node M1 is decreased. This enables a higher bandwidth of the bootstrapped switch as C1 can be made smaller, decreases the power consumption and also the area on the chip. Taking equation 4.16 into consideration again, the output resistance of the input buffer and the resistance of the bootstrapped switch together can be calculated with

$$\tau = RC = \frac{-t}{\ln(\text{gain error})}. \tag{4.19}$$

It should therefore not exceed 133 Ω. On the other hand minimizing the resistance of the bootstrapped and by this making the switch too large also has an impact on the bandwidth as the input buffer needs to drive the capacitors in the bootstrapped switch as well. An optimum was finally found with a resistance of 50 Ω of M1.
The bootstrapped switch occupies a comparatively large area in layout on the chip of 41.4 µm in width by 27.7 µm in height. This is attributed to the capacitor C1 needed for the bootstrapping action and the fact that many transistors have their bulks connected to their drain to prevent too high voltages at all nodes of the transistors.

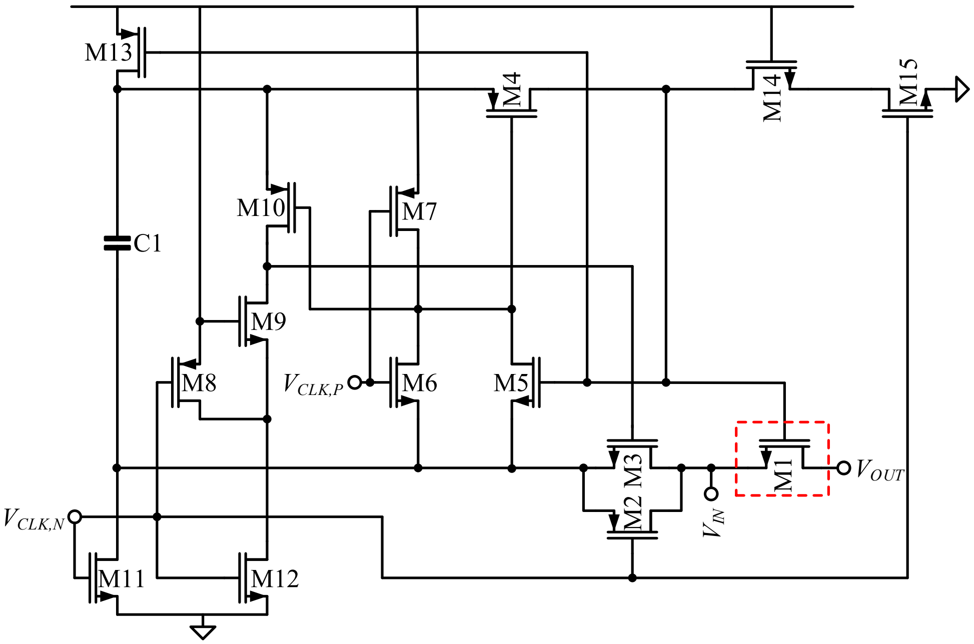


Figure 4.16: Schematic of the implemented bootstrapped switch for the implemented SAR ADC. Highlighted is the bootstrapped switch passing the input signal from the input buffer to the CDAC.

4.9 Delay Element

4.9.1 Introduction

For an asynchronous operation of the SAR ADC a delay is needed which sets the time in between conversion steps and allows the CDAC to settle to the needed precision in the reference voltage. A delay for a digital circuit is usually built out of multiple concatenating inverters. Digitally adjustable delay lines use whole elements, in this case additional inverters that can be added to or removed from the delay line. This results in a coarse delay adjustment. Adjusting a delay in analog is done by changing the controlling voltage or current in the circuit. With this a fine adjustment can be realized. Ideally the value for the delay is known and static so there is no need for coarse adjustments. To account for deviations in all circuits directly involved in the speed of the SAR ADC and in the delay itself due to parasitic elements as well as process variations, a delay with an analog adjustment mechanism was implemented.

4.9.2 Implementation

The schematic of the implemented delay line can be seen in Fig. 4.17. Here additional transistors M6, M7 and M12 in series with the normal inverter delay elements are used acting as current sources to limit the maximum current that can flow. This topology is called current-starved inverter. M1, M2 and M3 together with M6, M7 and M12 form a current mirror which is fed with an external current I_{bias}. Adjusting this current directly alters the delay properties. The inverters are only current-starved on one side. There are two phases the comparator goes through, one being the reset phase, the other being the regeneration phase. After the comparator regenerated and produces a bit decision for the current conversion step, it needs to reset before it can produce a new bit decision. This happens as fast as possible. After the comparator is reset, the delay determines the remaining time given to the CDAC to settle before

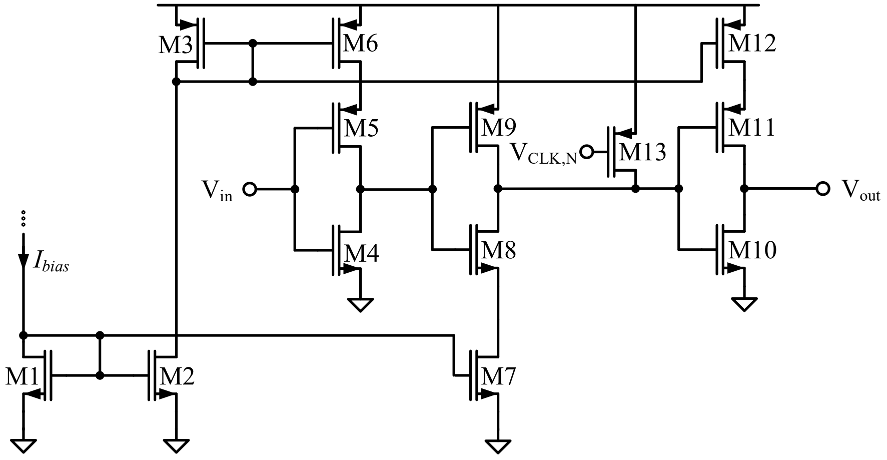


Figure 4.17: A current starved inverter line as delay element for the implemented SAR ADC.

the comparator is activated again. This also means that while the time given to the CDAC for settling is 100 ps, the adjustable delay through the delay element needs to be shorter. The total delay in the comparator control loop is composed of the delay of the comparator reset, the fast propagation time through the delay element, the propagation time of the OR logic gate that is producing a clock signal from the outputs of the comparator, and then finally the delay from current-starved delay line operation (see Fig. 4.1). A nominal simulation showed therefore that the needed delay is around 60 ps. An additional transistor M13 is implemented to break the conversion loop cycle. It is activated by the global sampling clock and holds the comparator in the reset mode.

The current I_{bias} which controls the delay element is adjusted by an eight bit current DAC. Its schematic can be seen in Fig. 4.18. It consists of a binary-weighted current mirror bank with an additional shift circuit. With a simple current mirror bank only the largest transistor would be $2^{8-1} = 128$ times the size of the smallest transistor which makes the needed area on chip also very large. With the shifting circuit the current is divided by eight in this case. Choosing M4 appropriately, the maximum ratio between transistors is now reduced to 8:1. With this, an output current between 0 µA and 80 µA with a minimum step size of 0.31 µA can be generated and fed to the delay element.

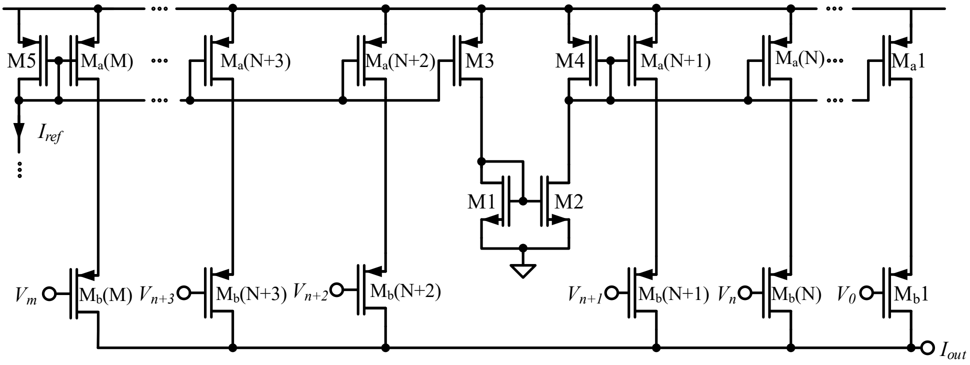


Figure 4.18: An adjustable current mirror used to control the current available in the current starved inverters of the delay element.

The simulated, adjustable propagation time in the delay element plotted for the useful range can be seen in Fig. 4.19b. All parasitic elements extracted from the physical layout were considered here. The nominally useful adjustment range's lower limit is at the configuration word 200 which corresponds to a bias current of 62.5 µA, for a delay of 44 ps. Below, the current-starved inverters are not limited by the bias current anymore and the delay is limited by the load. It is therefore constant. The upper limit is defined for the configuration word 240 which corresponds to a bias current of 75 µA, for a delay of 128 ps. Above, the granularity for the configuration of the delay is too low to have any usefulness for the configurability. Figure. 4.19a shows the delay now plotted over the whole configuration range. The grayed-out regions highlight the areas that have little use for the SAR ADC under nominal conditions. The large bias current range is implemented to compensate a shift of the operation region of the delay element due process variations. As the inverters used in the delay have minimal dimensions, they are very susceptible to process variations. The area on chip of the delay element is 18 µm in width by

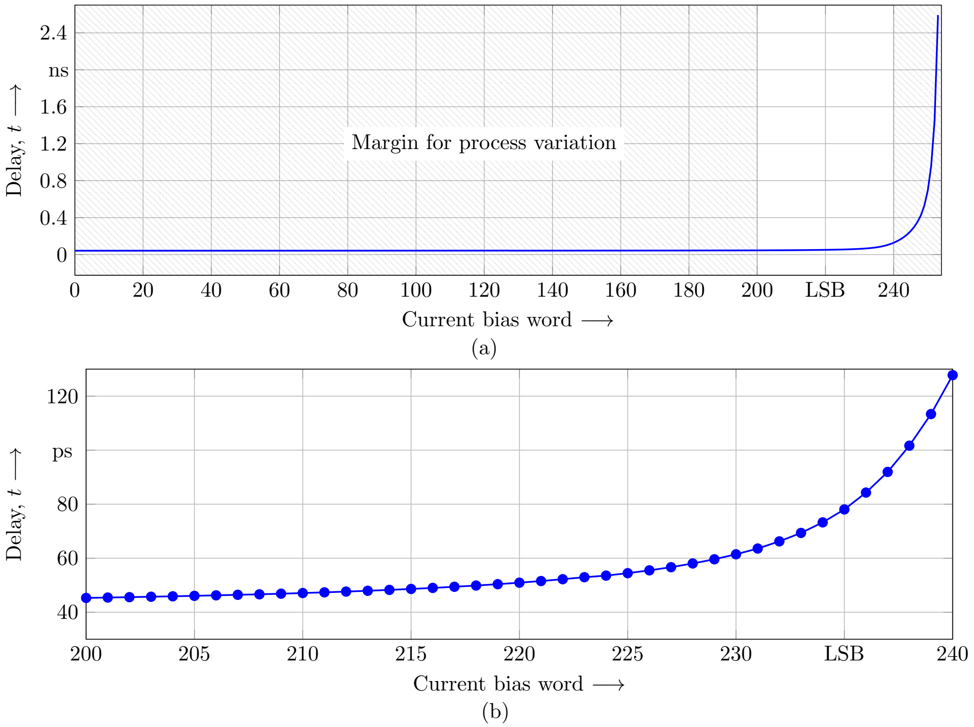


Figure 4.19: (a) Propagation time of the delay element plotted over bias current for the full configuration range. (b) A zoomed-in range showing the needed delay.

3.6 µm in height. For the 8 bit current DAC an area of 50 µm in width by 7 µm in height is needed.

4.10 Metastability detector

The metastability detector for this ADC is implemented as a second loop that runs in parallel to the regular timing loop of the SAR ADC. Its circuit is essentially the same as for the delay element. A further description is therefore refrained from.

It is also triggered by the comparator output. As long as there is no metastability event in the comparator and a decision stays in the bounds of the given time frame, the metastability detector is reset before activation. Otherwise, upon a certain time delay, it forces a decision in the comparator by pulling the latch in the second stage in one direction. As there is no direct readout of the adjusted delay in the metastability detector, a correct setting can be very tedious. For this, metastability has to be enforced in the comparator with a certain input signal voltage and then the detector has to be tuned until the metastability is successfully mitigated. The extra design margin in the regeneration of the comparator and the settling time in the CDAC eases the precise adjustment of the metastability detector as only very heavy cases of metastability taking considerable amount of time have to be intercepted.

The area on chip of metastability detector is similar to the delay element with 16 µm in width by 2 µm in height. For the current DAC again an area of 50 µm in width by 7 µm in height is needed.

4.11 Reference Buffer

This SAR ADC design has no high demands on the reference buffer as neither precision in the accuracy of the generated voltage nor a high driving capability is needed which is further alleviated by additional bypass capacitors. To keep the overall design effort low and maximize the time for more crucial circuit blocks, a pre-existing operational amplifier architecture was reused which derives the common-mode voltage of 450 mV with a resistor divider from the supply voltage. For future developments, this part can be optimized. A more detailed description is at this point out of scope and therefore omitted. The area on chip needed is 50.6 µm in width by 77 µm in height.

4.12 Layout

Figure 6.26 shows a layout screenshot of the 6 bit SAR ADC. Highlighted are the individual components described before. The dimensions are given in width x length.

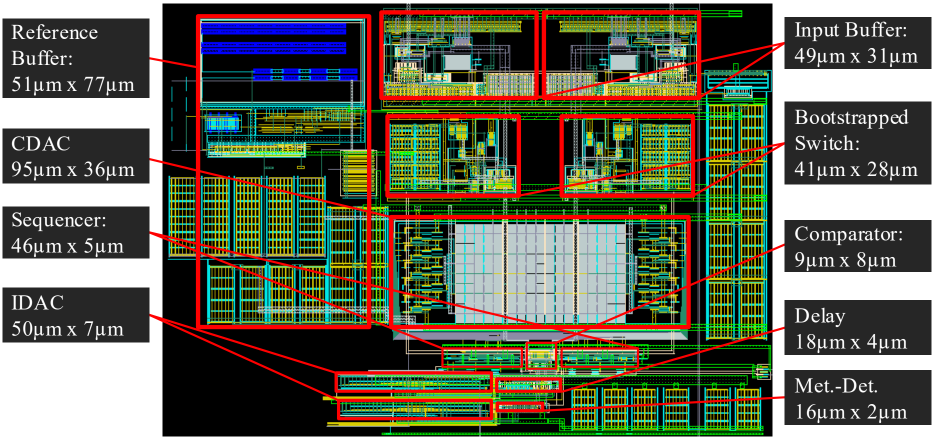

Reference Buffer: 51µm x 77µm
CDAC 95µm x 36µm
Sequencer: 46µm x 5µm
IDAC 50µm x 7µm
Input Buffer: 49µm x 31µm
Bootstrapped Switch: 41µm x 28µm
Comparator: 9µm x 8µm
Delay 18µm x 4µm
Met.-Det. 16µm x 2µm

Figure 4.20: Layout screenshot of the implemented SAR ADC with its individual components highlighted.

Chapter 5

Measurement Results of First ADC Chip

5.1 Printed Circuit Board

The chip is fabricated in a single-poly-eight-metal 28 nm bulk CMOS process. Its 1 mm by 1 mm silicon area is packaged in a quad-flat no-leads (QFN) package with 32 wire bonded output pads. The package has a size of 5 mm by 5 mm. A close up photo of the package with the lid removed is pictured on the right side of Fig. 5.1. On the die the top-most metal layer, in this case aluminum, is visible. It was spread over the whole chip for increased protection of the underlying circuits. A printed circuit board (PCB) was designed at the institute for the verification of the chip and can be seen on the left side of Fig. 5.1. It is split up into two separate parts. One, called daughterboard, carries the chip and has only few dedicated inputs for crucial signal paths. The remaining electric connections are fed-in over a connector on the backside of the PCB. It is pushed into its counterpart on the motherboard. This serves as the basis for all remaining, necessary connection from the measurement equipment, namely power supply and communication interfaces. With this, changing the chip sample, e.g. for investigations of process variation, is greatly alleviated.

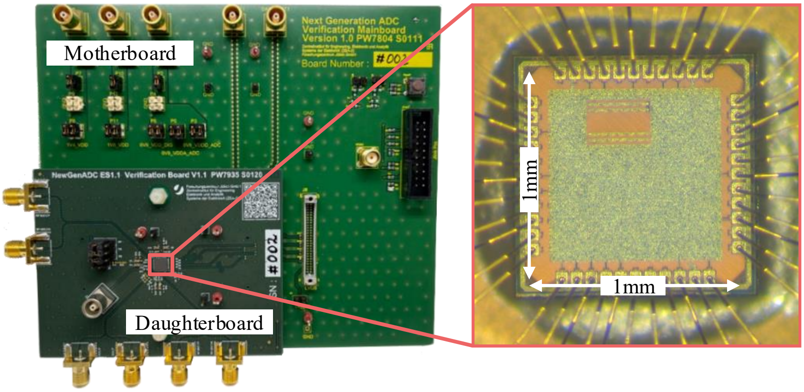

Motherboard
Next Generation ADC
Verification Mainboard
Version 1.0 PW7804 S0111
Board Number : #002
NewGenADC ES1.1 Verification Board V1.1 PW7935 S0120
#002
Daughterboard
1mm
1mm

Figure 5.1: Illustration of the PCBs split into motherboard and daughterboard for the chip with the SAR ADC on the left. Close up of the packaged chip with the lid removed on the right.

5.2 Measurement Setup

The measurement setup can be seen in Fig. 5.2. The reference clock for the chip is generated by a Rohde und Schwarz SMBV100B signal generator. A balun converts it into a differential signal. On the PCB a series capacitor acts as a DC block, so the bias point for the clock buffer on the chip can be chosen independently. It is set by a resistive divider on the PCB to 450 mV. To be able to sweep the input signal frequency, the waveform generator 33600A from Keysight was used. 20 dB attenuators were used to shift the range of the waveform generator to the level of the ADC and retain its resolution. Unfortunately, the maximum available frequency is therefore 120 MHz which is below the nyquist frequency of the ADC. Signal generators, like the SMBV100B from Rohde und Schwarz, produce strong harmonics which would require a tunable bandpass filter for frequency investigations. For DC measurements the precision source B2911A from Keysight is used.
In total three different supply voltages are needed. One connection uses 900 mV for the ADC and auxiliary analog circuits that cause no noise or high load on the supply. A second 1.4 V supply is used for the high-speed low voltage differential signaling (LVDS) data interface. The third supply voltage of 1.8 V is used for digital circuits, like the joint test action group (JTAG) communication interface. For these supply voltages the DC power analyzer N6705C from Keysight is deployed.

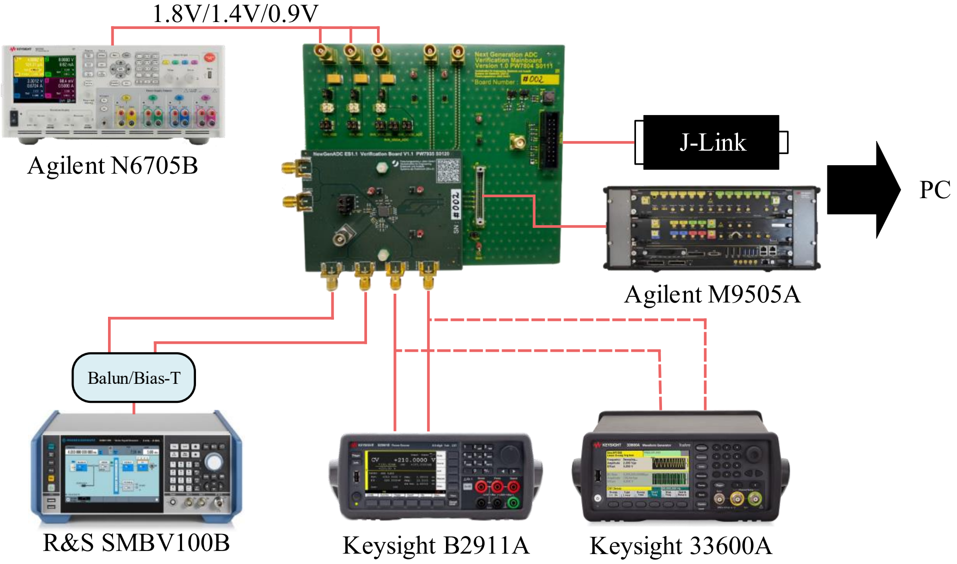


Figure 5.2: Measurement setup for the implemented SAR ADC.

To program the chip via the JTAG communication standard a SEGGER J-Link adapter is used to connect the chip to the computer. The ADC data samples are read out over the LVDS interface and captured by the M9095A logic analyzer from Keysight which is then transferred to the computer. Processing and evaluation of the ADC data is finally done on the computer with scripts written in the software MATLAB from MathWorks.

5.3 Delay Line Configuration

In a first step, after the general functionality of the chip and all its circuit blocks was verified, the optimal delay line configuration is investigated. For this, relaxed settings with a sample rate of 100 MSPS, an input signal frequency of 1 MHz and an input signal amplitude of 401 mV are chosen to not conceal the effect of the delay line configuration. A signal amplitude of 401 mV corresponds to a reduction of 1 dB of the full-scale signal amplitude of 450 mV. This is a frequently chosen value to prevent clipping. The digital configuration word for the delay line was then swept from "128", representing the midpoint for the adjustable bias current to "0" which represents the value for the highest bias current and therefore the shortest delay. When a reduction of the SNDR is noticeable the sweep is stopped and the previous value is taken as the ideal configuration setting for the delay line of the investigated sample. This investigation needs to be executed once per sample as only process variations and mismatch need to be compensated. The temperature has an even effect on all circuits. If the delay is shortened by lower temperature so is the settling time in the CDAC for example. A more conservative value for the delay line configuration may be chosen which then allows to use one setting for all chips without prior investigation. This simplifies the implementation of the chip in other applications at the cost of a reduced maximum sample rate. As the effective settling time for 6 bit is greatly relaxed, there was no deterioration observable in the performance of the ADC even for a delay setting of "0" for three different chips.

5.4 Maximum Sample Rate

After the optimal delay line configuration is found, the maximum sample rate of the implemented SAR ADC is investigated. The input signal frequency is adjusted to 10.99 MHz while the amplitude is kept as before at an amplitude of 401 mV. The sample rate was swept in 50 MSPS steps starting at 50 MSPS until 450 MSPS. At every point the SNDR and SFDR is measured. The result can be seen in Fig. 5.3. The achieved SNDR stays relatively flat over 36 dB until 350 MSPS with a maximum of 36.3 dB for 50 MSPS. The SFDR shows the same characteristic

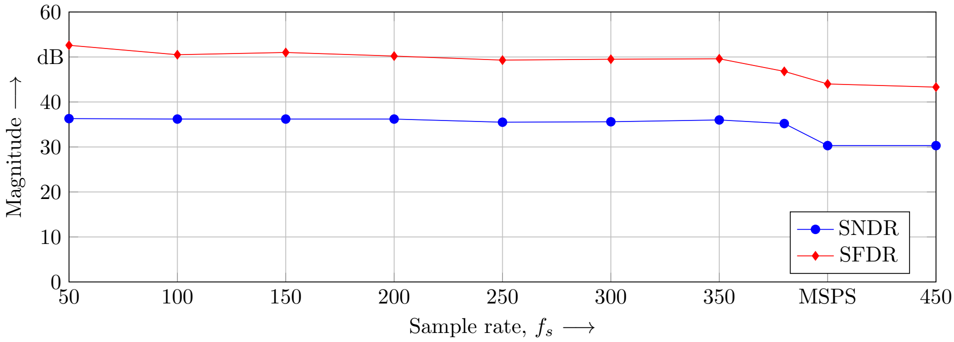


Figure 5.3: Measured SNDR and SFDR plotted over the sample rate of the implemented SAR ADC.

staying above 49 dB until 350 MSPS with a maximum of 52.6 dB at 50 MSPS. At 400 MSPS there is a sudden step-like drop in the SNDR and SFDR reducing by 6 dB. This is because the given time frame for the conversion cycle of the SAR ADC is now too short to fit the last conversion step for the LSB of the SAR ADC which is interrupted by the global sampling clock forcing the ADC back into sampling mode.

5.5 Power Consumption

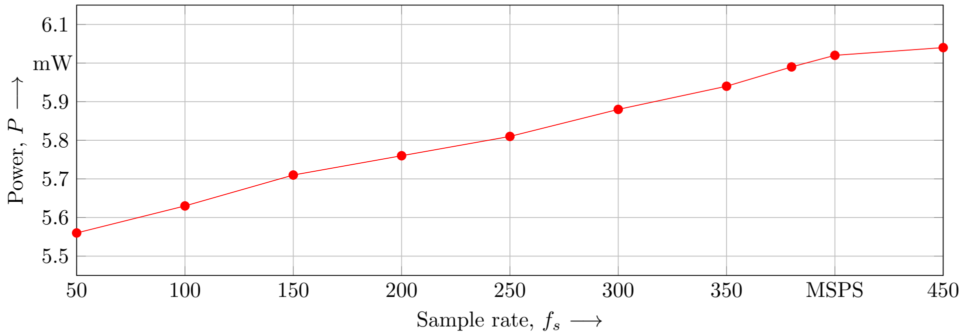


Figure 5.4: Measured power consumption plotted over the sample rate of the implemented SAR ADC.

Figure 5.4 shows the power consumption of the SAR ADC plotted over the sample rate including the input buffer, but excluding the reference buffer for the generation of the common-mode voltage as it is not optimized for its application. As before the sample rate was swept in 50 MSPS steps starting at 50 MSPS and ending at 450 MSPS. A great portion of the overall power consumption is static caused by the high bias current of the input amplifiers. Extrapolating the curve in Fig. 5.4 to 0 MSPS, the approximate share of the input buffers to the total power consumption can be approximated to 5.48 mW. The remaining circuits of the SAR ADC exhibit a linear scaling with the sample rate. For the sample rate of 350 MSPS, showing the best performance, the power consumption of the ADC core is 0.46 mW (the static power contribution of the input buffer is subtracted here).

5.6 Maximum Input Signal Frequency

With the highest sample rate of 350 MSPS found, subsequently the input signal frequency was swept for a full characterization of the AC performance of the ADC. To keep the correlation between sample rate and input signal frequency as low as possible a starting value of 10.99 MHz was chosen and then incremented in 10 MHz steps to a maximum of 119.99 MHz which is the maximum available input frequency of the used waveform generator. The results are shown in Fig. 5.5. The SNDR has a maximum of of 36.1 dB at 10.99 MHz and stays consistently above 33 dB until 119.99 MHz. Similarly the SFDR stays above 42 dB until 119.99 MHz and has a maximum of 50.5 dB at 30.99 MHz.

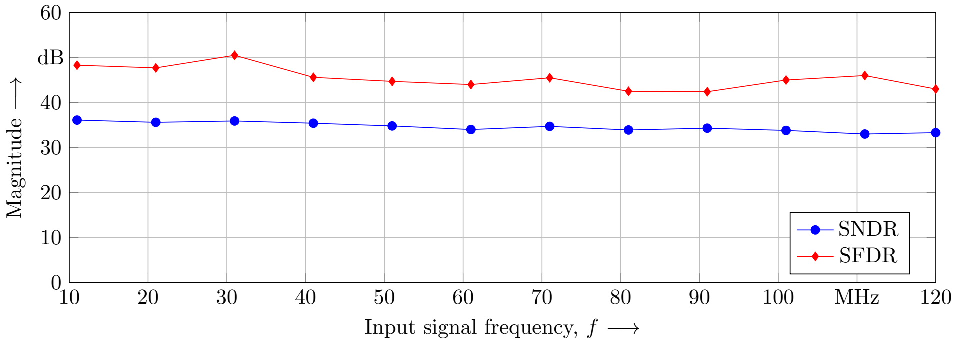
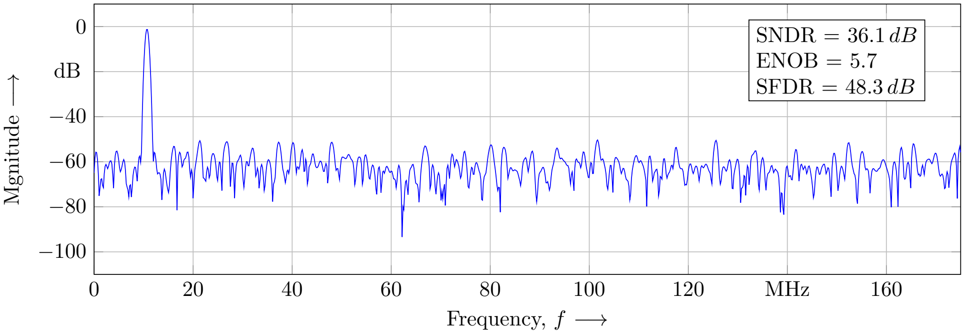
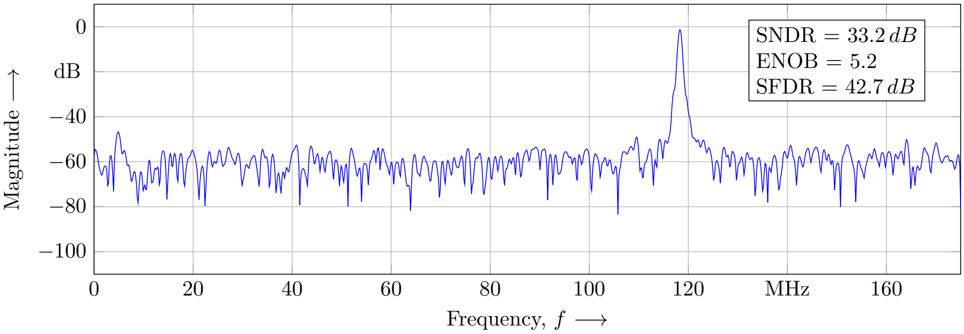


Figure 5.5: Measured SNDR and SFDR plotted over the input signal frequency of the implemented SAR ADC.

Figure 5.6a shows the spectrum of the ADC for a sample rate of 350 MSPS and a low frequency input signal of 10.99 MHz, Fig. 5.6b shows the spectrum of the ADC at a high frequency input signal of 119.99 MHz.



(a)



(b)

Figure 5.6: Measured spectrum of the implemented ADC at a sample rate of 350 MSPS. (a) Spectrum for a low frequency input signal of 10.99 MHz. (b) Spectrum for a high frequency input signal of 119.99 MHz.

5.7 DNL and INL

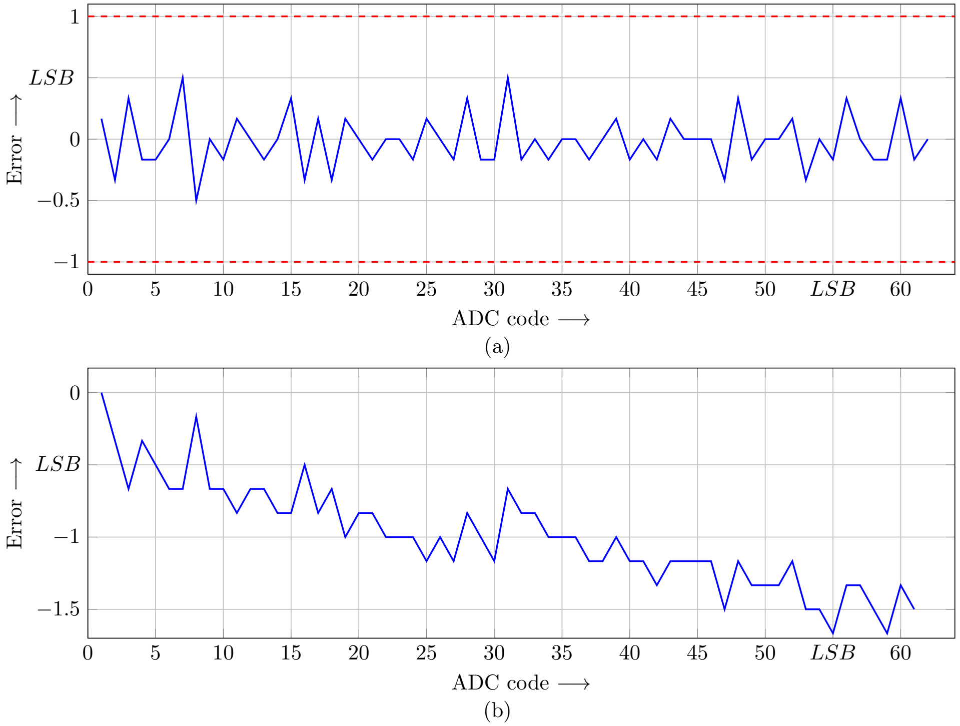


Figure 5.7: (a) Measured DNL and (b) measured INL of the implemented SAR ADC.

Subsequently the DNL and INL of the ADC were measured. The step size here was chosen to 100 µV to precisely capture the transition points for every LSB. The results are illustrated in Figure 5.7. The DNL lies within 0.51/+0.5 LSB. As its absolute stays below 1 LSB the ADC is therefore monotonic and has no missing codes. The INL lies within -1.6/+0 LSB. The typical jumps around $^{1}/_{4}$, $^{1}/_{2}$ and $^{3}/_{4}$ of the full-scale input range of the ADC are not seen here. At these values the most unit capacitors have a charge redistribution and mismatch in between the unit capacitors has the largest impact. However, through the large unit capacitor size in combination with the low overall resolution of the ADC of 6 bit these jumps are suppressed.

5.8 Performance Summary

Concluding the measurements, Tab. 5.1 shows a summary of the key parameters used nowadays to evaluate the performance of ADCs.

Table 5.1: Performance summary for the implemented 6 bit SAR ADC.

Parameter	Value
Architecture	SAR
Technology	28 nm
Supply Voltage	0.9 V
Resolution	6 bit
Max Amplitude	0.44 mV
SNDR @ 11 MHz	36.3 dB
SNDR @ 120 MHz	33.3 dB
SFDR @ 11 MHz	50.5 dB
SFDR @ 120 MHz	43 dB
Sample rate	350 MSPS
Power consumption	0.46 mW
Area	0.04 mm^2
FoM$_W$	35.8 fJ/c.-s.
FoM$_S$	149.1 dB

5.9 Discussion of the First Chip ADC

The measurement of the 6 bit SAR ADC of the first chip showed results in line with the specifications. The minimum ENOB stays above 5 bit over a frequency range of 120 MHz for a sample rate of 350 MSPS. The power consumption of the ADC core, neglecting the input and reference buffer power, scales linearly with the sample rate for a maximum of 0.46 mW at a sample rate of 350 MSPS.

With a resolution of 6 bit, the technological properties do not pose limits to the performance goals yet. On an architectural level the modified $V_{CM}+$-based switching scheme showed no negative impact on the performance. Therefore a transfer to future designs is pursued investigating its potential in more complex circuits. The measurement results showing no complications also reinforced the reliable operation of the comparator which allows an implementation in future designs. The sample rate however was severely impacted. In that regard, the parasitic elements extracted from the physical layout altered the behavior significantly compared to simulations without parasitics. This is especially visible in the sequencer which is a main factor of the diminished sample rate. Here, an optimized architecture or layout will have a strong influence on the maximum achievable sample rate. The required settling time of the input buffer suffices for the 6 bit SAR ADC, but for a higher resolution the settling time of 2.2 ns would dominate the sample and hold cycle. The same applies to the static power consumption of the input buffer which is by far the largest contributor to the overall power consumption. A pipelined, software-configurable ADC would profit strongly from an optimized performance in the input buffer.

Overall the design, manufacturing and measurement of a first SAR ADC gave valuable insights to working with a more modern process technology node as 28 nm bulk CMOS. The SAR ADC showed convincing power efficiency and area scaling attributed to its mostly digital nature.

Chapter 6

Second ADC Chip

A second chip was designed and manufactured having a first version of a software-configurable ADC as described in chapter 3.2 at its core. Additional circuitry completes the chip or simplifies the investigation of the ADC. A clock driver is implemented to feed in an external high-precision clock signal and regenerate its fidelity on chip. Static random-access memory (SRAM) which can store 8168 ADC samples was added to the chip to have a simple, low-power method to read out ADC data from the chip. For this and for programming the configuration registers of the chip, a JTAG communication interface is available. Alternatively, ADC data can be read out via a high-speed real-time LVDS communication interface.

6.1 Technical Specifications

The target specifications for the sample rate is kept at 300 MSPS to 500 MSPS. With this, similar margins and timings for the conversion cycles are maintained and the design can capitalize from the experience gained from the previous chip.

The resolution of the ADC is a product of many design iterations. For the high-resolution mode it culminated in an implementation of 11 bit. The goal for the ENOB is set to 10 bit as this marks the border for high resolution in general. The physical resolution of the low-power mode is 8 bit and the ENOB is expected to lie between 7 bit and 7.5 bit based on the results of the previous chip.

The maximum amplitude of the input signal voltage was increased to 0.6 V differentially for this ADC to utilize the design space for the given supply voltage as much as possible and maximize the SNDR. With this, the sampling capacitance can be reduced. It is chosen here to 0.92 pF which corresponds to an SNR of 76 dB and lies at the upper end of a an integer representation ENOB of 11 bit (see Fig. 2.5). This ensures enough margin for noise from other sources. If the amplitude was kept at 0.45 V as in the first chip a significantly higher sampling capacitance of 1.6 pF would have to be implemented to arrive at the same SNR.

The absolute power consumption is secondary for this first concept of a software-configurable ADC. Of priority is that a discernible difference in the power consumption between the individual nodes is observable. Also the ADC should maintain the linear scaling effect with sample rate.

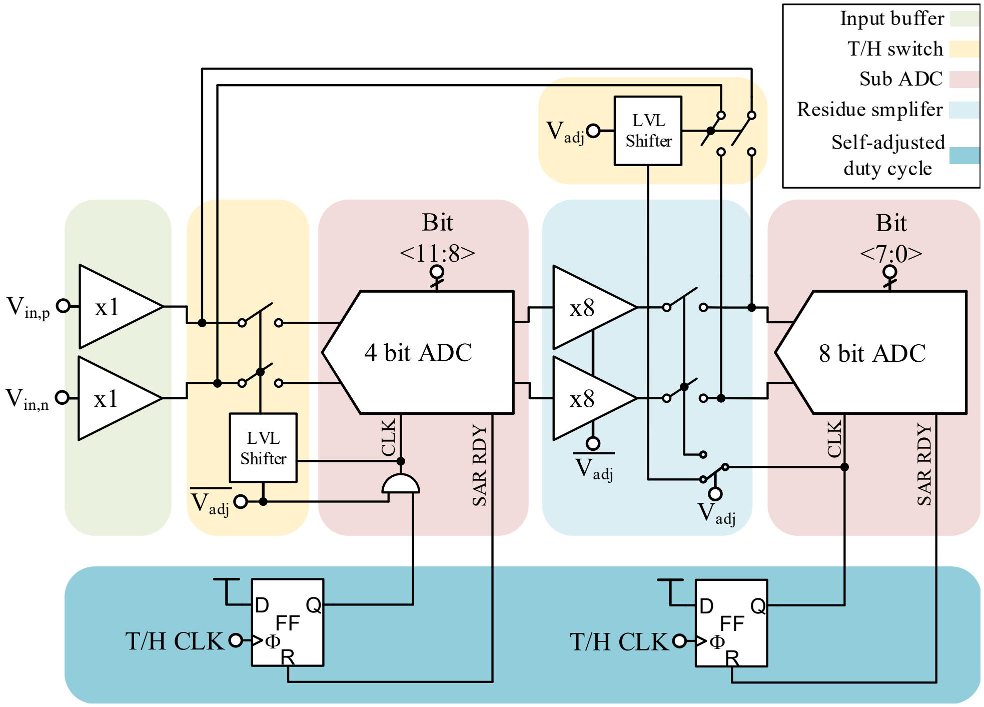

Input buffer
T/H switch
Sub ADC
Residue smplifer
Self-adjusted duty cycle
$V_{in,p}$
$V_{in,n}$
x1
x1
LVL Shifter
$\overline{V_{adj}}$
V_{adj}
LVL Shifter
Bit <11:8>
4 bit ADC
CLK
SAR RDY
x8
x8
V_{adj}
V_{adj}
Bit <7:0>
8 bit ADC
CLK
SAR RDY
T/H CLK
D
Q
FF
Φ
R
T/H CLK
D
Q
FF
Φ
R

Figure 6.1: Overview about the main components in the software-configurable ADC.

6.2 Overview Pipelined SAR ADC

An overview about the different main components the software-configurable ADC consists of is shown in Fig. 6.1. This implementation uses pseudo-differential input buffers again. They reuse the old implementation of the first chip to a major degree, only the second stage is modified to provide a higher output signal amplitude. Two sets of track-and-hold switches are used. This allows to bypass the first stage of the pipelined ADC and feed the input signal directly into the second stage which enables the configurability in resolution. These switches are not bootstrapped, but use 1.8 V transistors to implement a low-resistance switch. They are driven by high-speed level shifters. Two sub SAR ADCs with one bit overlap achieve a total of 11 bit physical resolution. The first sub ADC's design priority is precision, whereas the second sub ADC is tailored for speed. Residue amplification is realized with pseudo-differential ring amplifiers. This architecture maximizes gain-bandwidth product available for the ADC. The global sampling clock is modified through a few simple additional digital circuits in such a way that the duty cycle between sampling and conversion phase is now automatically adjusted. This allows an optimal utilization of the available sample period.

The following sections will describe key features of the implemented pipelined ADC that enable the software configurability, but also enhance the performance on an architectural level in comparison to conventional, pipelined ADCs.

6.2.1 First Stage Bypass

To realize a first version of a software configurability in resolution, two sets of track-and-hold switches are implemented which are oppositely activated and deactivated respectively through V_{adj}. With this, the first stage can be bypassed enabling the low-power mode with a resolution of 8 bit. Increasing the overall design complexity by bypassing the first stage instead of using it as standalone ADC for the low-power mode has two reasons. Firstly, the first stage needs to fulfill the precision requirements for the total resolution of the pipelined ADC. It has therefore an accordingly higher power consumption and settling time with reasonably sized switching transistors. Secondly, the sample rate specifications and the achievable gain-bandwidth product of the residue amplifier limit the gain factor which can be implemented and therefore the smallest residue that can be processed for the second stage.

The high driving requirements for the first stage make the implemented input buffers suboptimal drivers for the second stage and reduce the overall power efficiency of the low-power mode. This will be addressed in future iterations of the software-configurable ADC concept.

The residue amplifier is put into standby mode reducing its power consumption to almost zero during the low-power mode. Also for the first stage, the input clock signal is interrupted and held at a constant zero. Power consumption is reduced to almost zero as no static current is drawn in the SAR ADCs apart from the delay element.

6.2.2 Residue Interleaving

In a conventional pipelined ADC the conversion procedure is as follows. First an input signal is sampled onto the capacitors in the CDAC of the first SAR ADC stage. After it has finished its conversion, the residue is then transferred via the residue amplifier onto the next SAR ADC stage. During this period, the first stage has to hold the determined residue as a reference for the amplifier and can not start a new sampling phase. Thus, there exists some dead time in the pipelined ADC, because the residue amplifier can not operate independently of the first stage. The timing for a conventional pipelined ADC is illustrated in Fig. 6.2a. Here, it is assumed that both stages take 1 ns for their conversion cycle. Likewise, for the sampling on the first stage and for the residue amplification onto the second stage a time of 1 ns is assigned. With this distribution, a conventional pipelined ADC needs 3 ns to convert one sample which translates to a sample rate of approximately 333 MSPS. To remove the dead time and maximize the throughput of the presented, pipelined ADC, a residue interleaving scheme was implemented as can be seen in Fig. 6.3. The attenuation caps used to adjust the input range of the CDAC are now doubled and used in an alternating fashion. A typical operation cycle is described as follows. Initially, the switch pair S_4 and S_8 is closed and connects attenuation capacitor B to the CDAC. After the sampling and conversion phase are finished, S_4 and S_8 open and the switch pair S_1 and S_5 closes connecting the attenuation capacitor A to the CDAC. The CDAC's composition stays thus preserved and is ready for the next sample, while simultaneously the last residue is stored on attenuation capacitor B. Switch pair S_3 and S_7 is subsequently used to connect the capacitor to the residue amplifier. The switches S_5 and S_8, realized with transmission gates, add a voltage-dependent parasitic capacitance component to the CDAC due to the nature of their gate-source/gate-drain capacitors. This effect however is also present in the comparator as its input transistors which are also directly connected to the CDAC add a voltage-dependent parasitic capacitance through gate-source capacitors as well. The impact of this is therefore

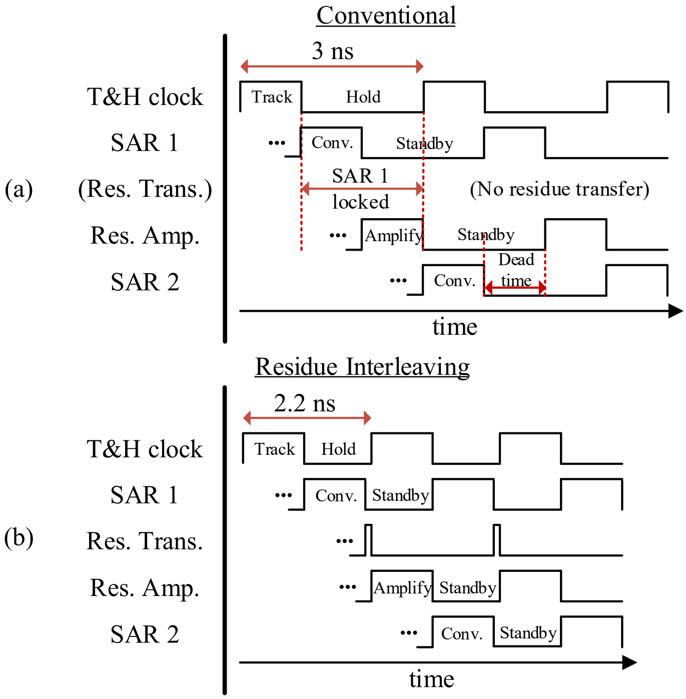

Conventional
3 ns
T&H clock
Track
Hold
SAR 1
Conv.
Standby
(a)
(Res. Trans.)
SAR 1
locked
(No residue transfer)
Res. Amp.
Amplify
Standby
SAR 2
Conv.
Dead
time
time
Residue Interleaving
2.2 ns
T&H clock
Track
Hold
SAR 1
Conv.
Standby
(b)
Res. Trans.
Res. Amp.
Amplify
Standby
SAR 2
Conv.
Standby
time

Figure 6.2: (a) Conversion timing of a conventional pipelined ADC. (b) Conversion timing of a pipelined ADC with the proposed residue interleaving.

well understood and included in performance investigations.

The remaining switches also affect the accuracy of the residue due to their voltage-dependent behavior, but more so through an effect called charge injection. Here the remaining charge in the channel moves to the drain and source nodes when the transistor is switched off. As it is dependent on the gate-source voltage, the amount of charge is not predictable and thus distorts the residue. To preserve the accuracy in the residue, a switching scheme as seen in Fig. 6.4 is utilized [74, p. 570]. It illustrates a well-established charge-based amplifier with a bottom-plate switching scheme. After sampling on capacitor C_1 is done via S_1 and S_2, at first switch S_1 opens injecting a constant charge onto the bottom plate of C_1. It is constant because also the gate-source voltage for this switched is fixed. S_2 opens next injecting an arbitrary amount of charge on the top plate of C_1. Finally, S_3 and S_4 close and start the amplification process. As charge injected from S_2 is removed by S_4 again as soon as it connects to a fixed potential, no error occurs. S_3 produces only a constant error as it is connected to the virtual ground node X of the operational amplifier. As the voltage-dependent junction capacitance of S_1 and S_3 experience only small voltage changes across the switch, the resulting non-linearity is negligible

With residue interleaving the residue amplifier effectively also becomes an independent part of the pipeline. Its impact is illustrated in Fig. 6.2b. The conversion phase and the sampling/residue amplification phase for both stages now run sync. There is a small overhead with the extra time for the residue transfer here assumed to 200 ps. However, with the timing defined before

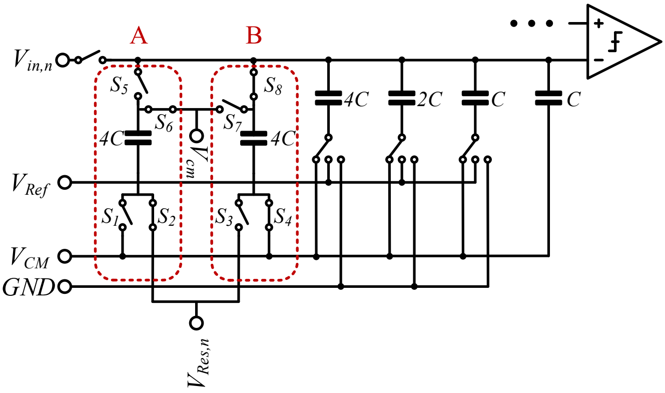


Figure 6.3: Implementation of residue interleaving in the CDAC of a SAR ADC.

for sampling/amplification and conversion of 1 ns each, the total sample period reduces now to only 2.2 ns which translates to a sample rate of approximately 455 MSPS.

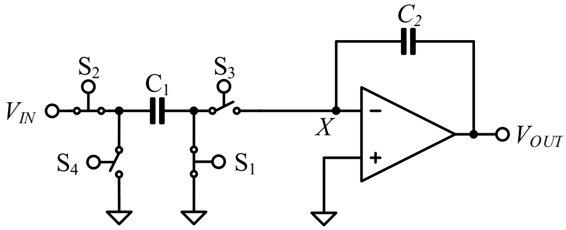
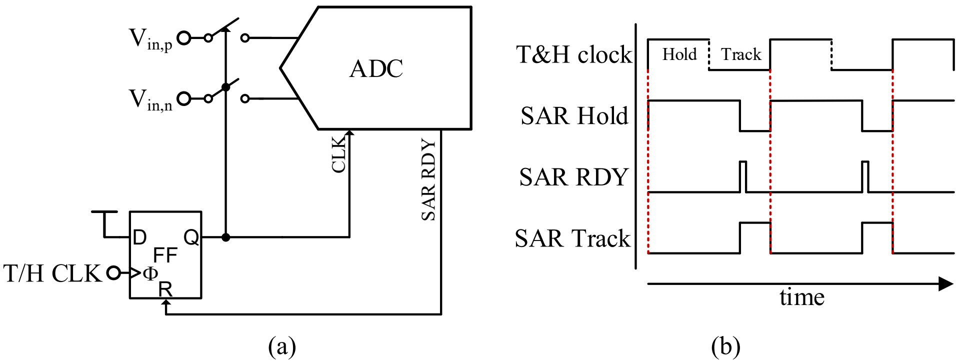


Figure 6.4: Principle of accurate amplification in a charge-based amplifier with bottom-plate sampling.

6.2.3 Self-Adjusted Duty Cycle

For SAR ADCs in particular there can be a significant imbalance between the time needed for sampling an input signal voltage on the sampling capacitor and the time needed to convert the signal to the digital domain. It is therefore common to adjust the duty cycle of the global sampling clock skewing it so that conversion phase has more time at the cost of reduced sampling time. This approach however needs additional circuitry and finding the right configuration for the duty cycle can be a lengthy process, especially in pipelined ADCs.
Figure 6.5a shows an implementation for a self-adjusted duty cycle. Here the global sampling clock is not directly fed into the SAR ADC but into a DFF. This DFF triggers only on a rising edge producing a high output voltage. This starts the conversion phase. A falling edge of the sampling clock however is ignored. Instead after the SAR ADC has finished its conversion, the *SAR RDY* signal generated internally by the SAR ADC is used to reset the DFF to a low output voltage. This starts the sampling phase. With this scheme the ADC adjusts the duty cycle itself,



(a) (b)

Figure 6.5: (a) Basic implementation method for a SAR ADC with a self-adjusted duty cyle.
(b) Diagram of the internal signals for a SAR ADC with a self-adjusted duty cyle.

while the global sampling clock retains its even duty cycle. This is also illustrated in Fig. 6.5b. For the software-configurable ADC in its high-precision mode, this self-adjusted duty cycle has only a minor effect on the overall sample rate in this implementation, because the conversion time for the sub ADCs and the time for the residue amplification were found to be very similar. It still offers better robustness against metastability events as it can offset a longer conversion phase with a sampling phase in which not the most critical charge redistribution requirements arise. Additionally, both sub ADCs can have individual, independent duty cycle adjustments which increases flexibility even further. For the lower-power mode the impact is significant. The sampling time here is considerably shorter than the conversion phase due to the small sampling capacitance and the lower settling requirements. The increased metastability robustness applies here as well.

6.2.4 1.8 Volt Switches

Bootstrapped switches have an outstanding resistance consistency over input voltage, but their driving circuitry has an area consumption on chip which accounts for a significant overall footprint of the ADC. As a large capacitor has to be driven, the power consumption increases accordingly as well. A decisive disadvantage for this ADC implementation is the increased integration complexity into the CDAC. The required switching scheme here makes a distributed input switch approach necessary.

In the used process technology also 1.8 V switches are available which are usually used at an interface of the chip to provide a more robust signal and for legacy reasons to offer the ability to connect to devices made with older process nodes. Using these 1.8 V transistors as a pass transistor for the input signal of the ADC with a minimum input voltage of 150 mV and a maximum input voltage of 750 mV has the advantage of much smaller resistance modulation through V_{GS}. With the higher overdrive compared to a 0.9 V switch the non-linearity caused by the input switch is reduced. Figure 6.6 shows the resulting resistance of a 1.8 V NMOS transistor for the input range of the ADC. Its highest resistance of 79 Ω for the maximum input

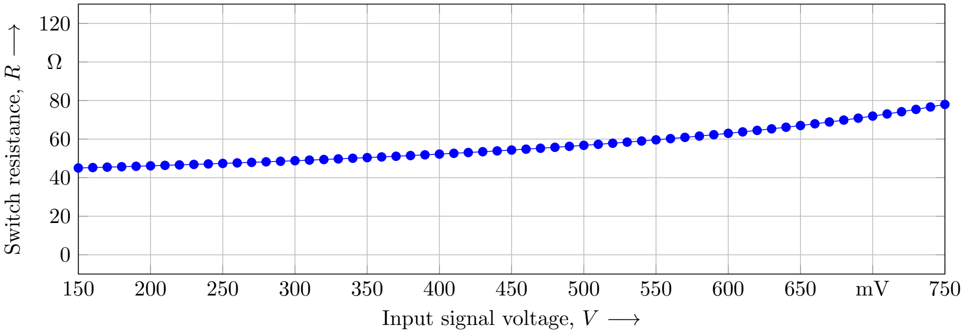


Figure 6.6: Diagram of the resistance change over voltage for a 1.8 V switch used as sampling switch for the given input signal amplitude.

signal voltage fulfills the settling requirements for the high-precision mode. While there is a slight voltage dependency visible in the resistance characteristic of the 1.8 V switch, for the maximum input frequency of 250 MHz this design choice produces no spectral components and satisfies the resolution requirements.

The global clock signal is in the 0.9 V supply voltage domain. It is therefore converted to the 1.8 V supply voltage domain by high-speed level shifters as illustrated in Fig.6.7 and then fed to the sampling switches. Here a 1.8 V PMOS transistor pair latch M5 and M6 is driven by a

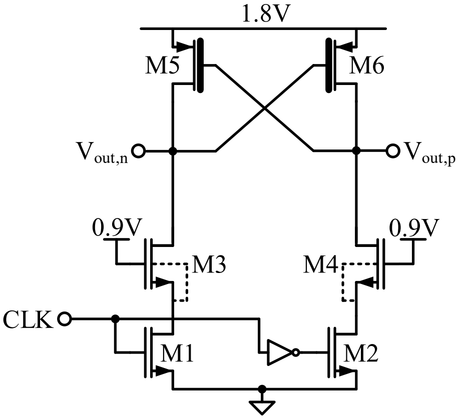


Figure 6.7: Schematic of the high-speed level shifter used to convert the global clock signal to the 1.8 V domain.

cascode of 0.9 V NMOS transistors. The cascode transistors M3 and M4 are powered with the full supply voltage of 0.9 V. Through this, even if a voltage of 1.8 V is present at the drain of M3 or M4, their gate will always see a maximum voltage difference of 0.9 V. Simultaneously they protect the input transistors M1 and M2 from breakthrough. With a rising drain potential of M1 or M2 the gate-source voltage of M3 or M4 is diminished stopping current flow. As all cascode transistors have the same dimensions, they also have the same nominal leakage current which ensures that the drain of M1 and M2 never goes higher than 900 mV.

6.3 Input buffer

For the input buffer, to a large fraction the old design from the first chip was reused (see section 4.7). To account for the new requirements with regard to an open-loop gain of 72 dB and a maximum input amplitude of 300 mV, the second stage was exchanged. Instead of a common-source amplifier an inverter stage is now implemented. The PMOS and NMOS here need less overdrive and provide a higher gain at high and low voltages. The static current consumption is also decreased due to the dynamic driving capability of an inverter. Additionally, the area on chip is reduced by removing the large current source transistor, and its bias circuits, of the common-source amplifier. A considerable drawback is the lack of power supply rejection ratio within this topology. It is a consequence of the shrinking design space for analog circuits in modern process technologies and this tradeoff is accepted in other components of the ADC as well, e.g. the residue amplifier. This drawback is compensated here by dedicated quiet supply lines. The final design of the modified input buffer can be seen in Fig. 6.8. Its loop gain and phase margin are shown in the bode plot of Fig. 6.9. The achieved open-loop gain of 78 dB is sufficient for a resolution of 11 bit for the ADC plus some additional margin for other error sources. The phase margin with 73.8° lies above 60° and therefore also fulfills the requirements for a stable operation in a small-signal analysis. With a unity gain point located at 4 GHz, the input signal with a maximum input frequency below 250 MHz will be reproduced correctly. As gain and phase margin investigations mainly apply to the small-signal behavior, the transient step response is also analyzed with an extracted view over Monte Carlo and temperature simulations. It showed a stable behavior in all cases. Figure 6.8 highlights the transient response in more

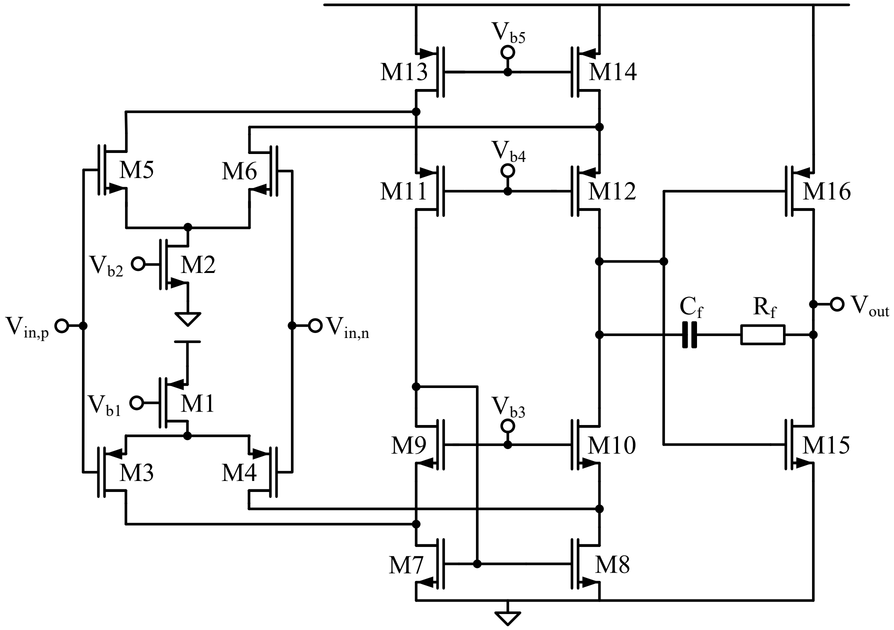


Figure 6.8: Schematic of the input buffer used in the software-configurable ADC.

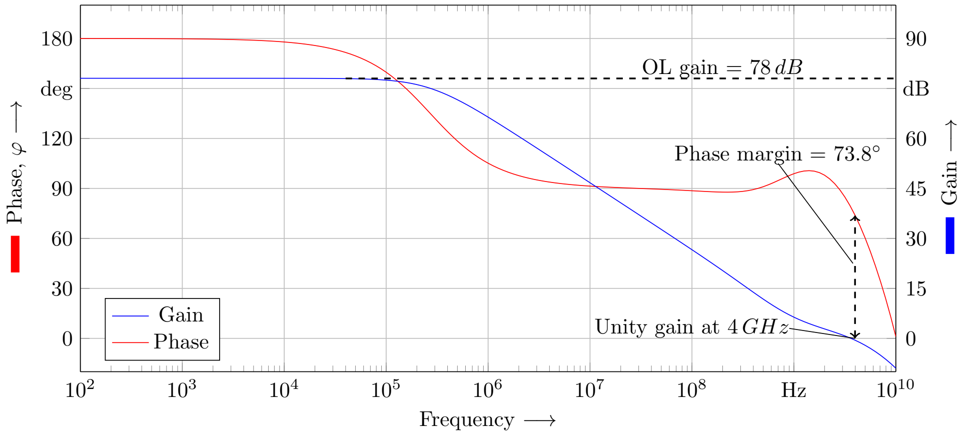


Figure 6.9: Gain and phase margin of the implemented input buffer for the software-configurable ADC.

detail, also with regards to the severe impact of parasitic post-layout elements. Interestingly, the settling time for the modified input buffer has similar timings for the rising and falling edge as the input buffer of the first chip and also shows the same deterioration through parasitics. It should be noted however that the maximum peak-to-peak voltage increased to 600 mV. Nonetheless, the assumption can be made that the deterioration comes from the first, folded-cascode stage which is the same in both designs. This is especially remarkable as the layout for the modified input buffer in comparison to the buffer of the first chip was strongly optimized. This could be an indicator for a general limitation of this implementation of an operational amplifier architecture. Due to time constraints no further optimizations were undertaken. The general functionality of the ADC has priority over the maximum sample rate in this project. The Monte Carlo simulation over 1000 runs furthermore yielded a maximum expectable offset of -15/+15 mV with a standard deviation of 4.5 mV. Because of the reduced capacitor load and the inverter stage, the static power consumption of the input buffer reduces to 1.11 mW. The area needed on chip is 36.2 µm in width by 19.8 µm in height.

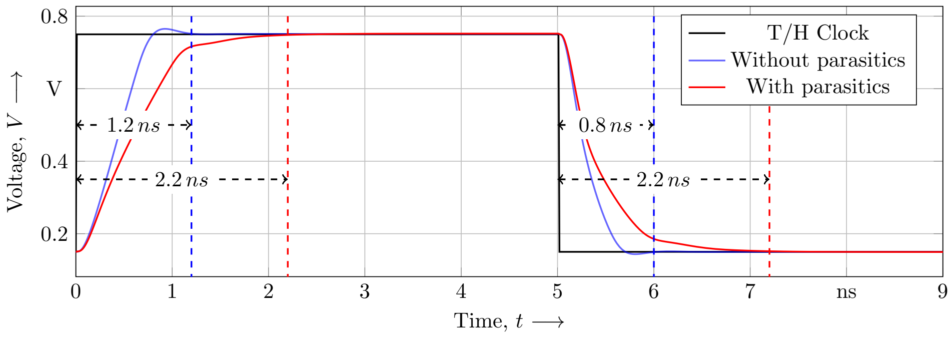


Figure 6.10: Step response of the input buffer used in the software-configurable ADC for a maximum voltage step size.

6.4 Metastability

It is argued in [78] that metastability events with large magnitude reducing the sample by more than 2 bit are extremely rare and do not significantly affect the bit error rate. Its impact is therefore in the same order of magnitude as thermal noise in the comparator. Instead it is advised to use the extra timing margin for metastability to optimize the comparator performance. Furthermore, the merit of dedicated metastability detectors is questioned as its presence will load the comparator and increase its decision time. Because of the steep tradeoff between the bit error rate due to metastability and the timing of the comparator, the theoretical benefit of a metastability detector is nullified. The metastability detector itself will also introduce difficult-to-solve race conditions. Finely adjusting the metastability detector to an optimal point in time to intervene the regular timing loop is a complex task involving time-intensive measurements which are unique for every chip.

On the basis of these observations, it was decided to omit a dedicated metastability detector in the design of this ADC. There is however conceded some margin in the conversion cycle timing in the initial design considerations as middle ground. As it is easy to create or remove extra margin for metastability in an asynchronous SAR ADC by simply adjusting the sample rate, an optimized operation speed can be investigated later in long-term measurements in the laboratory.

6.5 Sequencer

The same sequencer topology is used in both sub ADC stages of the pipelined ADC, only the number of concatenated switching cells is different. An illustration is given in Fig. 6.11 It was further optimized in comparison to the sequencer of the first chip and now contains no transistor heavy DFFs anymore. To activate and deactivate the respective stages in the sequencer now combinational logic is used. The S-R latches were also exchanged by inverters acting as an additional buffer for the control signal, plus a small cross-coupled inverter to latch the comparator decision for the currently investigated conversion step. This reduces the propagation delay further. Its operation theory is as follows. The first cell has a small modification compared to all following cells, because it is not locked in the beginning of the conversion cycle. A comparator decision is directly fed into the inverter latches and then feeds into a *NOR* logic gate. This disables all inverter latches. It also feeds into a three-input *NOR* gate of the next cell which is then unlocked as soon as the additional *OR* gate, seen at the bottom of the illustration which also feeds into the three-input *NOR* gate, is putting out a low value after the comparator is reset again. For the next comparator decision there is no race condition as the comparator signal is going into the bottom *OR* gate and the inverter latches at the same time. The locking signal however first still has to go through the three-stage *NOR* gate before it disables the inverter latches. For all subsequent cells now an *OR* is used at the outputs of the inverter latches to lock the respective cell. Monte Carlo simulations over temperature with an extracted view ensured that the sequencer is robust and reliably works. From the comparator signal to the switching logic now a consistent delay of only 23 ps is simulated in comparison to the 64 ps to 96 ps of the sequencer for the first chip. The area on chip is 14.9 µm in width by 5.5 µm in height for the 4 bit first stage ADC and 23 µm in width by 5.5 µm in height for the second stage 8 bit ADC.

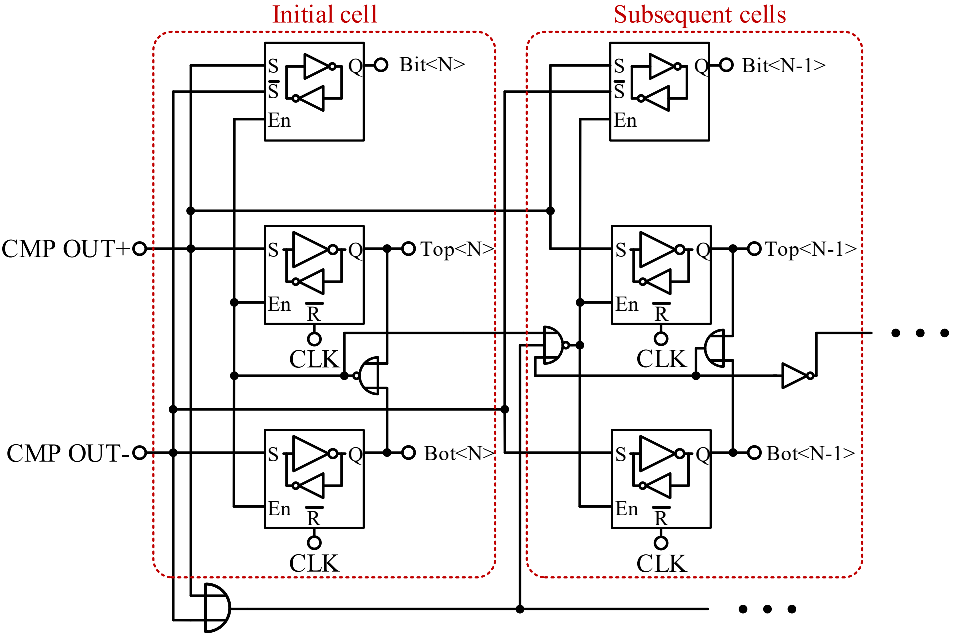


Figure 6.11: General structure of the sequencer used in both sub ADCs of the pipelined ADC.

6.6 First Stage SAR ADC

6.6.1 CDAC

The first stage SAR ADC resolves the first four bits of the pipelined ADC. This configuration was found in an iterative process and yielded an optimum between the settling requirements in the CDAC, the gain-bandwidth of residue amplifier and the target sample rate. Matching requirements for the capacitors are also relaxed, because the total sampling capacitance is divided into a smaller amount of unit capacitors. For the CDAC of the first stage SAR ADC again the V_{CM}-based switching scheme is used, because of its superior accuracy, speed and energy efficiency tradeoff. In contrast to the CDAC of the first chip the last capacitor pair is not used for an additional bit in resolution to preserve the common-mode voltage consistency and maintain the high resolution requirements of the pipelined ADC. There are however other modifications implemented to increase the performance described in the following.

The first modification is illustrated in Fig. 6.12. Bottom-plate sampling, similar to the residue transfer scheme shown in Fig. 6.4, is applied to reject errors from charge injection of the input sampling switches. For this, the switches connecting the top side of the capacitors with the common-mode voltage V_{CM} open first after the sampling phase is finished. Only after this the switches at the bottom side connecting the capacitors with the input signal voltage are opened. Finally, to restore the sampled signal at the top side of the comparator for the subsequent conversion cycle, the bottom side of the capacitors is connected to V_{CM}. The last capacitor necessary for a binary weight distribution, and also the attenuation capacitors, now need an

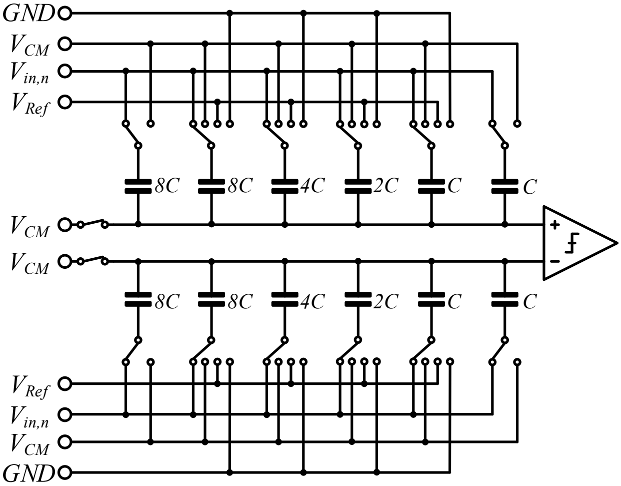


Figure 6.12: Schematic of a CDAC utilizing a V_{CM}-based switching scheme with bottom-plate switching.

initial charge redistribution. The attenuation capacitance contributes a third of the overall capacitance of the CDAC reducing the input voltage range to two thirds of the reference voltage which is the supply voltage of 900 mV. With a common-mode of 450 mV, the CDAC allows thus a voltage going from 150 mV to 750 mV single-endedly. It should also be noted that the first bit in the conversion step cannot be converted immediately anymore as it is the case in top-plate switching schemes. First, the input signal has to be transferred from the bottom-plate to the top-plate and settle to the required accuracy.
In a next step, the unit capacitors were split into two parallel half-sized capacitors as shown in

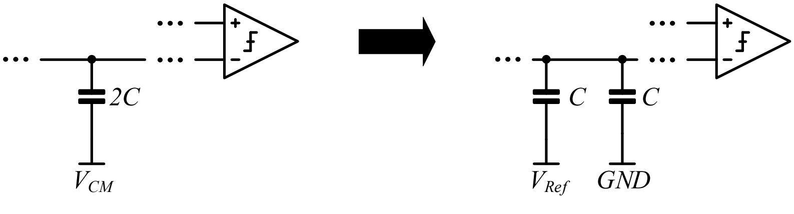


Figure 6.13: Principle of splitting a single capacitor driven by a common-mode voltage V_{CM} into two individual capacitors driven by V_{Ref} and GND for an equivalent behavior.

Fig. 6.13. Driving these with GND and V_{Ref}, assuming that $V_{CM} = {}^1\!/\!_2\, V_{Ref}$, results in the same behavior as driving a single normal-sized capacitor with V_{CM}. The advantage of this adaption is that we avoid the driving difficulties of NMOS and PMOS switches around V_{CM} for this process technology. It is especially important as with the bottom-plate switching scheme, before the conversion cycle starts, the bottom side of all capacitors has to be charged to V_{CM}. Additionally, these switches are also used during the conversion cycle which reduces the total amount of

switch transistors in the CDAC. Finally, the requirements on the reference buffer for the V_{CM} generation stays low, because for the bottom plate of the capacitors it is derived directly from V_{Ref} which is the supply voltage in this ADC. As a drawback, the total amount of capacitors is now increased by a factor of two. In this implementation the CDAC size is set by kTC noise, therefore no size penalty has to be conceded.
Figure 6.14 shows the final CDAC structure combining the bottom-plate V_{CM}-based switching scheme with the residue interleaving through the attenuation capacitors. All capacitors are split into oppositely driven pairs as shown before in Fig. 6.13, but for better overview it is not included here. There is also some simple logic needed which is triggered by the global sampling clock as well as the *SAR RDY* signal and controls the process flow of the residue transfer. With a total sampling capacitance of 0.92 pF and 48 unit capacitors which are again split into two, the capacitance for the unit capacitor results in 9.58 fF. The timings in one conversion cycle of the first stage SAR ADC are illustrated in Fig. 6.15. Some additional steps have to be considered here in contrast to the standalone ADC of the first chip. Firstly, the initial step during the conversion cycle transfers the sampled input signal from the bottom plate to the top plate as it is necessary with bottom-plate sampling. Secondly, there is one additional redistribution step needed in the CDAC to generate the residue for the next stage to convert and have an

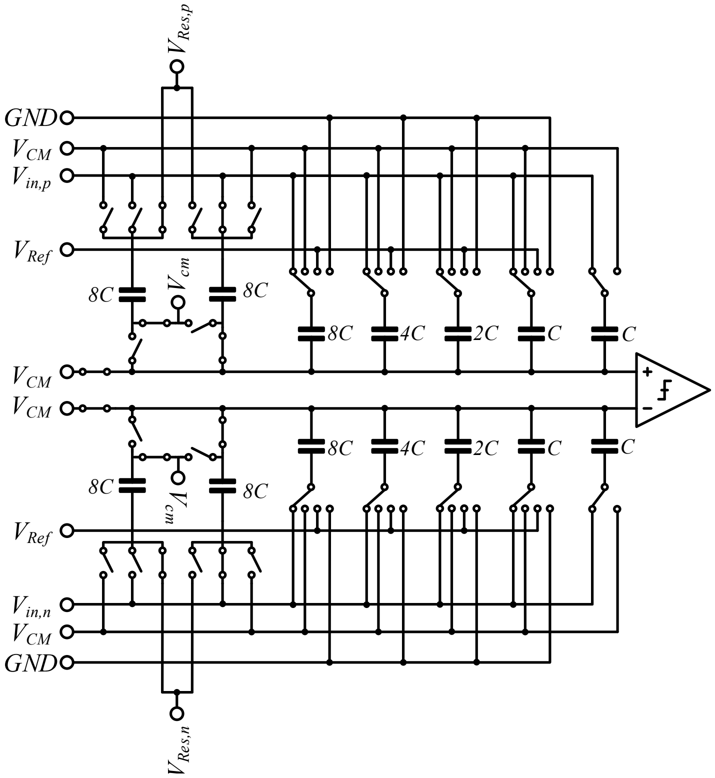


Figure 6.14: Final schematic of the first stage ADC CDAC combining the bottom-plate V_{CM}-based switching scheme with the residue interleaving through the attenuation capacitors. Not shown is the capacitor splitting for better overview.

overlap of one bit. Finally, the interchanging of the attenuation capacitors for residue transfer is also attributed to the conversion cycle. A total of 900 ps is needed for the conversion cycle, if for the comparator regeneration again a timing of 50 ps, for the settling of the CDAC after each conversion step again a timing of 100 ps and for the residue transfer a timing of 200 ps is chosen. With a margin of 100 ps for layout dependent parasitic effects and for metastability events, this fits well into the targeted conversion period specification of 1 ns. All switches are dimensioned accordingly in the same manner as described in section 4.4 for the CDAC of the first chip's ADC.

An outline of the capacitor distribution as implemented in the CDAC of the first stage SAR ADC can be seen in Fig. 6.16. Due to the small unit capacitance a two-dimensional matching scheme was applied here with interdigitated capacitors. Therefore, two split capacitors are combined with all needed switches to make one layout cell similar as described in [79]. Adding dummy capacitors and switches at the edges, this creates a uniform environment for all unit capacitors. There are also no wires running under or in between the capacitors anymore. Additionally, capacitors needed to adjust the gain of the ring amplifier (see Fig. 6.20) are outsourced and integrated into the CDAC layout. This was done to achieve the best matching between the attenuation capacitors and ring amplifier capacitors which are responsible for the accuracy of the amplified residue signal. The ring amplifier capacitors are based on the same unit capacitors as the rest of the CDAC for non-disruptive insertion. The used area on chip here is 77.1 µm in width by 72 µm in height.

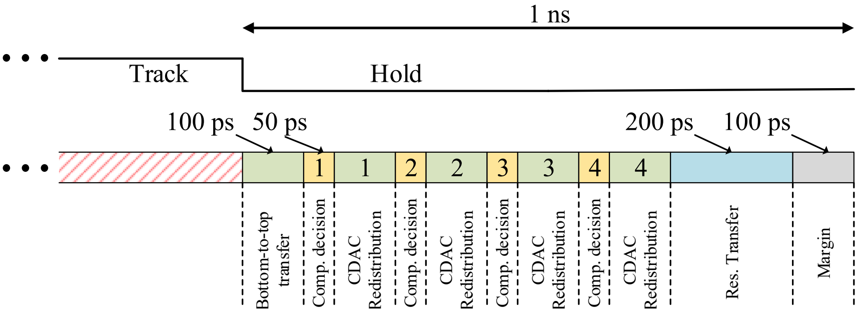


Figure 6.15: Timing for the first stage SAR ADC.

6.6.2 Comparator

The comparator of the first chip (see section 4.5) was completely reused for the first stage SAR ADC. It has sufficient speed, noise properties and precision for the resolution of four bit. Furthermore, its switched cascode stage and removed tail switch offer superior kickback noise performance which is needed because the CDAC of the first stage ADC has to fulfill the precision requirements of the whole pipelined ADC.

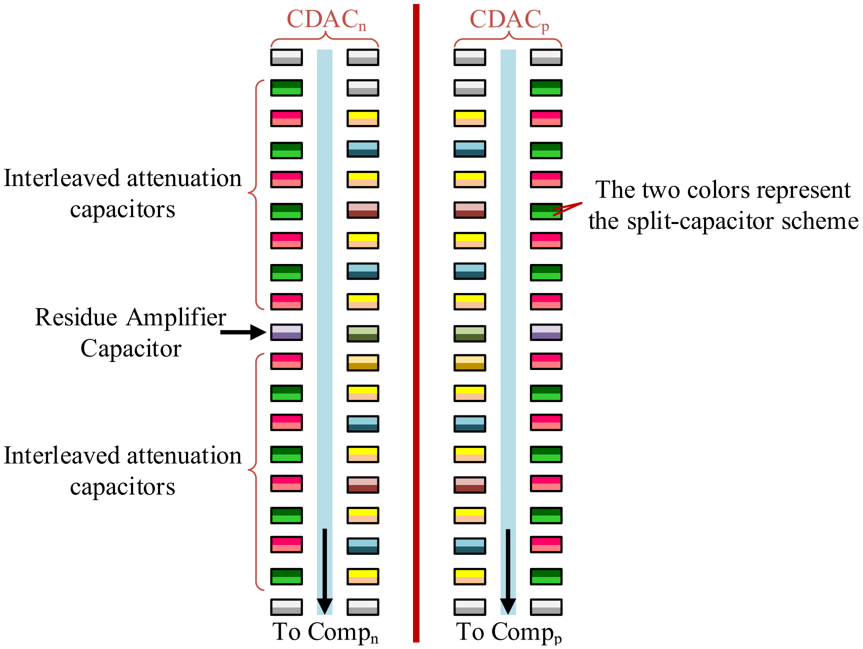

CDAC$_n$
CDAC$_p$
Interleaved attenuation capacitors
Residue Amplifier Capacitor
Interleaved attenuation capacitors
The two colors represent the split-capacitor scheme
To Comp$_n$
To Comp$_p$

Figure 6.16: Illustration of the interdigitated capacitor distribution in the CDAC of the first stage SAR ADC.

6.7 Delay Element

In an effort to decrease the minimum of the adjustable delay, the component count in the delay element was reduced. Its basic structure can be seen in Fig. 6.17. To create a time delay, a capacitor C_{Par} is discharged by an adjustable small current until the trip point of an inverter is reached. A fast reset signal on the other hand is generated by a PMOS pull-up transistor with full overdrive. Another PMOS pull-up transistor is activated by the internal *CLK* signal of the sub SAR ADC and stops the comparator at the end of the conversion cycle. The capacitor C_{Par} is not inserted as a dedicated capacitor, but forms out of parasitic elements from the transistors and the wiring between them. This causes the delay to have a stronger non-linear tuning behavior, but available dedicated metal capacitors increased the needed current for the wanted considerably even at their minimum size. With the chosen implementation, the bias current stayed in an acceptable range between 25 µA and 60 µA to arrive at the needed propagation delays. The bias current is supplied again by a binary-weighted current DAC similar to the one shown in Fig. 4.18. Its range was however reduced to five bit resulting in a current range of 0 µA to 80 µA with a minimum step size of 2.5 µA. The delay element for the first stage SAR ADC has a minor modification to also delay the initial decision of the comparator. This is done to allow the CDAC with bottom plate switching scheme to settle after the samples input signal is pushed from the bottom plate to the top plate for the subsequent conversion cycle. Furthermore, the bias current coming from the current DAC is halved again to accommodate the higher needed overall settling time in the first stage. Figure 6.18 shows the adjustable

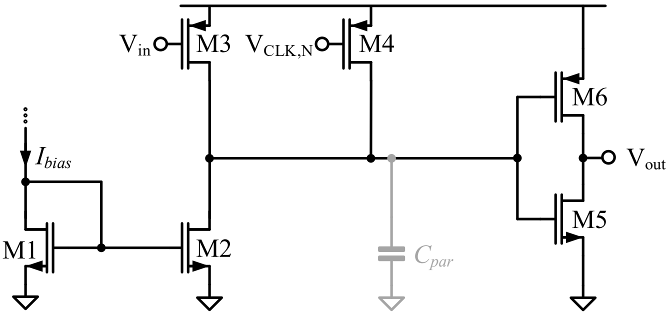


Figure 6.17: Basic schematic of the delay implemented in the SAR ADC stages of the pipelined ADC.

propagation delay over the respective configuration word in LSB for the delay element of the second stage SAR ADC. The nominal tuning range starts at 33.1 ps for a configuration word of "10" which translates to a bias current of 25 µA and ends at 49.3 ps for a configuration word of "24" which translates to a bias current of 60 µA. Again there is added some margin on both ends of the adjustable delay to account for deviations through process variations. The used area on chip is 4.4 µm in width by 2.2 µm in height for the delay element and 17 µm in width by 4.2 µm in height for the 5 bit current DAC for both ADC stages.

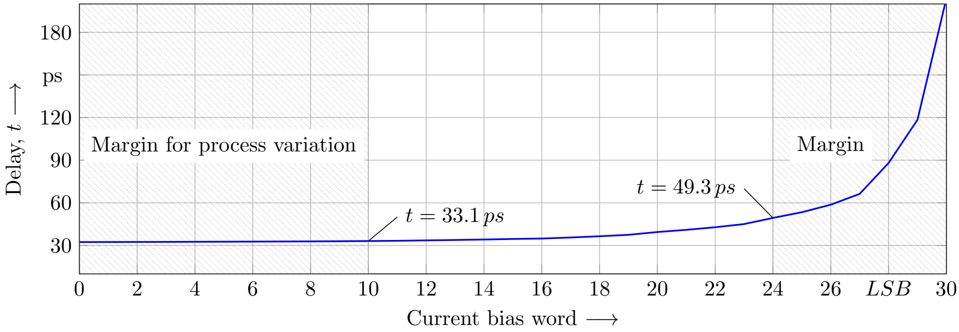


Figure 6.18: Propagation time of the delay element plotted over the configuration word for the 5 bit current DAC.

6.8 Residue Amplifier

6.8.1 The Ring Amplifier

The open-loop output resistance of an amplifier is maximized in CMOS technologies to achieve a high voltage gain. As implementing extremely big resistors on chip is not feasible, a resistive feedback network can dominate the output resistance of an amplifier and therefore limit the overall accuracy [74, p. 539]. Using capacitors instead of resistors in the feedback network, offers an area-efficient way out of this predicament depending on the application. Moreover, in discrete-time applications using feedback capacitors, the open-loop gain of an amplifier is not limited if the output voltage is given enough time to settle. That is why the residue amplifier for the implemented pipelined ADC utilizes a switched-capacitor topology as shown in Fig. 6.4 in Section 6.2.2.

Fulfilling the target requirements for this pipelined ADC necessitates the use of an alternative amplifier than traditionally used operational amplifiers. In modern process technology nodes their gain suffers too much from the decreasing transconductance and power supply voltage. As the residue amplifier has become the bottle neck in pipelined ADCs, alternative amplifier architectures are more and more investigated. To give a complete overview and to underline the effort undertaken in recent years, the most successful are named in the following. The zero-crossing based amplifier deploys a comparator which controls two current sources that charge the capacitive load to the desired value [80]. A dynamic amplifier similarly integrates an input voltage dependent current on a capacitor until a reference voltage is reached [81]. Simply using conventional amplifier architectures in open-loop configuration is also investigated [82]. While these amplifiers show superior performance in regard to efficiency and bandwidth, their open-loop nature makes them very susceptible to PVT variations. A robust operation therefore requires complex background calibration methods diminishing the advantages.

Another alternative amplifier architecture is the so-called ring amplifier which was introduced in 2012 in [83]. Since then its property to function in closed-loop environments and therefore good PVT robustness made it very popular and well-researched. Its original schematic can be seen in Fig. 6.19. At its core it consists of a three-stage inverter-based amplifier and offers therefore high gain even at very low supply voltages. In a feedback network however three concatenated inverters, resembling a ring oscillator, are not stable and cause oscillation. To attain a stable amplification, it is modified by splitting the path to the last inverter stage and imprinting an offset V_{OS} in the capacitors C2 and C3 for the bottom transistor M7 and the top

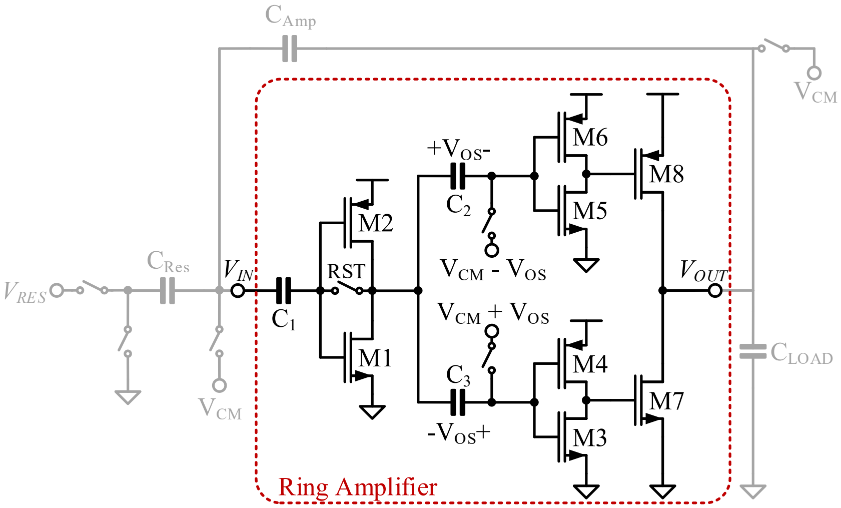


Figure 6.19: Schematic of a ring amplifier in a switched-capacitor feedback network.

transistor M8. Through this, a range of input voltages is created in which neither M7 or M8 conduct a current. If this dead zone is large enough, the ring amplifier operates by slewing to, stabilizing and finally locking into a steady state. C1 and the *RST* switch are used to cancel the most critical offset of the first inverter stage. The input-referred value of the dead zone $\epsilon_{V_{IN}}$ defines the overall accuracy of the ring amplifier. It can be described as

$$-\left|\frac{V_{DZ}}{2\,A_1}\right| \leqslant \epsilon_{V_{IN}} \leqslant \left|\frac{V_{DZ}}{2\,A_1}\right|. \tag{6.1}$$

Here, $V_{DZ} = 2\,V_{OS}$ and A_1 is the final settled small signal gain of the amplifier (ignoring finite gain effects of the later stages). In the initial slewing phase, either M7 or M8 act as maximally-biased current sources charging the load capacitor while the complementary transistor of the third stage inverter is in off-state. This maximizes energy efficiency and increases the speed of the amplifier. After the trip point of the first stage inverter is reached, the slewing phase stops. Due to the inherent delay through the three stages, there is some overshoot beyond the dead zone, which causes a charge in the opposite direction. This is the stabilizing phase and it is affected by the propagation delay of the first and second stage inverters, the feedback factor, the load capacitor and the current of the third stage. The fundamental process behind the stabilization is the rapidly increasing output resistance of the ring amplifier as the input voltage closes in on the dead zone forming a dominant pole to stabilize the amplifier. In general the relation holds, the higher the accuracy of the ring amplifier the longer the stabilization phase lasts. Finally, the peak overdrive voltage fed back into the first stage generates a voltage not outside of the dead zone anymore. Thus both output transistors M7 and M8 are switched off and the ring amplifier enters the steady-state phase.

6.8.2 Implementation

Four bit are resolved in the first stage SAR ADC and the needed gain in the residue amplifier is therefore 16. With the implemented one bit overlap between both stages of the pipelined ADC however, the gain reduces to 8. This also means that the maximum residue signal amplitude reduces by half to 150 mV. The amplified residue needs to be exact enough to the LSB of the second stage. With seven resolved bits and a peak-to-peak differential voltage of 600 mV, this corresponds to a settling of the residue amplifier to within 4.69 mV, or respectively 2.34 mV if one bit overhead is considered for error margin from other sources. Expressed in gain error this leads to a value of 0.39 %. With the gain factor of 8 an open-loop gain of 67.25 dB is needed to achieve this performance. As open-loop gain is difficult to simulate in ring amplifiers, the transient settling behavior is used as performance indicator during design. For the settling time 1 ns is defined in the specifications. The load capacitance is determined by the requirements of the subsequent second stage SAR ADC and is here 96 fF for the positive and the negative side of the CDAC. The specifications are summarized in Tab 6.1.

The residue amplifier implemented in this design can be seen in Fig. 6.20. At its core it uses a modified ring amplifier following the design presented in [84]. Here, in the third inverter stage high-threshold voltage transistors are used to create the dead zone for a stable operation. As long as the threshold voltages of the transistors fulfill the constraint $V_{th,n} + |V_{th,p}| > V_{DD}$ the ring amplifier will reach a steady state. For the 28 nm process technology used in this work, this constraint can be met with the available transistor flavors. Splitting up the path

Table 6.1: Specifications for the residue amplifier.

Parameter	Value
Voltage gain	8
Settling accuracy	2.34 mV
Gain error	0.39 %
Single-ended output swing	300 mV
Single-ended input swing	37.5 mV
Load capacitance	96 fF
Settling time	1 ns

to the last inverter stage and inserting additional bias circuitry can be omitted by this which reduces the overall component count and the load on the first inverter stage. Additionally, now the entire ring amplifier can be auto-zeroed which cancels the difference between the global common-mode voltage and the internal common-mode voltage of the ring amplifier. A drawback is the reduced slewing current of high-threshold voltage transistors which is however mitigated by the orders of magnitude higher output resistance. Compensating the output current by increasing the size of the third stage transistors is in the end still beneficial. The ring amplifier of Fig. 6.20 has an additional transistor M1 which is used to power down the amplifier. For this, M1 pulls the first inverter to the supply voltage. This skews all inverters maximally in one direction so that no cross current is flowing. The common-mode voltage V_{CM} for auto-zeroing is supplied through transmission gates as the load of C_2, C_{amp} and C_{DAC} is small enough to ensure a fast settling. The feedback network and its capacitors C_1 and C_{amp}

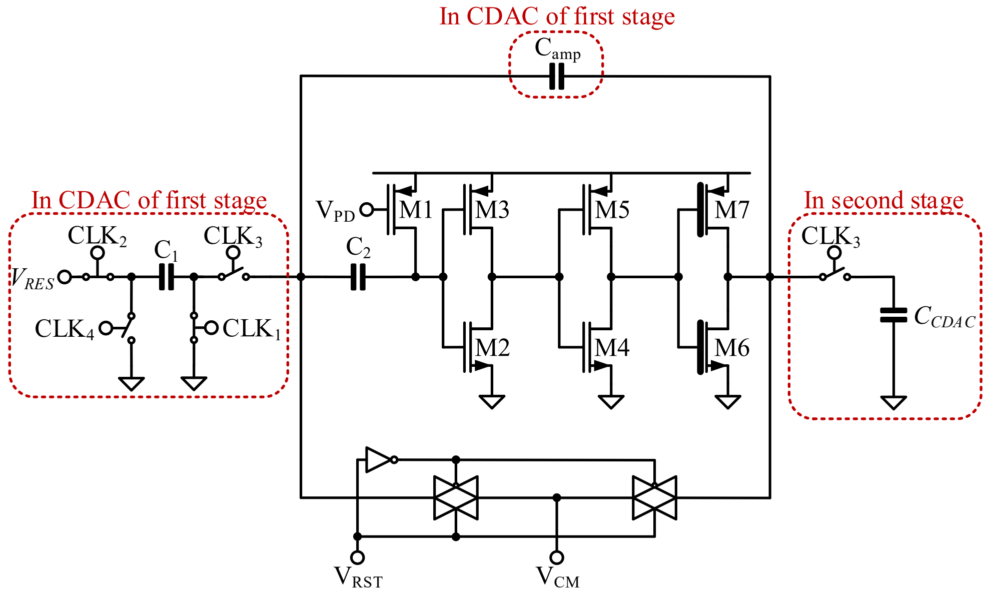


Figure 6.20: Schematic of the implemented residue amplifier with a ring amplifier at its core.

are outsourced into the CDAC for better matching. To maximize the gain-bandwidth of the residue amplifier, again a pseudo-differential arrangement was chosen duplicating the amplifier of Fig. 6.20.
The simulated settling behavior of the pseudo-differential residue amplifier with parasitic extraction is shown in Fig. 6.21. The maximum possible residuum voltage of 37.5 mV is applied to investigate the worst case settling time. After the ring amplifier is reset and the signal to perform the amplification is given, the residue amplifier needs approximately 1 ns to settle to the required accuracy. The acquired output signal has a reduced peak-to-peak voltage of only 295 mV instead of 300 mW. This can be traced back to the unavoidable parasitic capacitors manipulating the originally adjusted gain. It has however no impact on the overall accuracy of the ring amplifier and the linear gain error can be calibrated digitally in post-processing. The common-mode voltage of the output signal of the residue amplifier also shifts by a significant amount of 55 mV after parasitic extraction. This is absorbed by the one bit overlaps and halved gain implemented in the pipelined ADC. It was furthermore simulated under Monte Carlo and temperature variations in the full ADC environment to ensure it has no impact on the overall performance. The static power consumption of the residue amplifier is 1.4 mW and its core area on chip neglecting the feedback network is 39.1 µm in width by 8 µm in height.

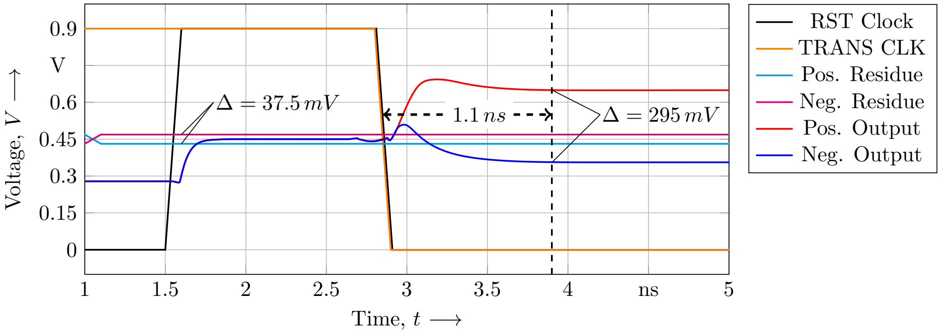


Figure 6.21: Settling behavior of the implemented residue amplifier with parasitic post-layout elements.

6.9 Second Stage CDAC

A first investigation estimated that during the conversion of the first four MSBs in the first stage, 8 bit can be converted in the second stage ADC due to the reduced settling requirements. The CDAC of the second stage SAR ADC therefore has to provide eight reference voltages for the 8 bit to be resolved. The basic schematic can be seen in Fig. 6.22. A monotonic switching scheme with reversely connected MSB capacitors is chosen as describes in Section 4.4. The main advantage for the pipelined ADC of this thesis is its very low complexity which eases design effort in the last stage and allows to put more focus on the correct timings and signal distributions in the first stage and its residue interleaving. The lower switching energy is compensated by the very small total sampling capacitance. Top-plate sampling is implemented to maximize the speed. For a resolution of 8 bit, charge injection from the sampling switches has no significant impact. Additionally, again the CDAC LSB capacitor is formed by two unit capacitors in series effectively starting at half a unit capacitor to reduce the total amount of capacitors needed. The second set of half-unit capacitors for a binary weighting in the CDAC is omitted as parasitics will have a larger effect anyway. Attenuation caps attenuate the maximum signal amplitude to 600 mV here, too. Calculating the sampling capacitance needed to satisfy kTC noise requirements plus one bit extra margin a value of 34.67 fF is obtained. Dividing this value by the 192 unit capacitors implemented in the CDAC would result in a unit capacitance of only 180 aF. In relation to this, parasitic capacitance has a significant impact on the actual implemented capacitance. Furthermore, process variation reducing the matching among the individual unit capacitors is severely magnified by their small dimensions. For this reason, a higher unit capacitor value of 1 fF was chosen. With this, the negative and the positive side of the CDAC each have a total capacitance of 96 fF. There are many intertwined aspects that need to be regarded as the CDAC is the central circuit block of a SAR ADC. In the end the unit capacitor size was chosen as an optimized compromise between matching, parasitic element resilience and feasibility in layout on the one hand and area as well as power consumption, loading of residue amplifier, and speed of the conversion loop on the other hand. For the comparator timing again a value of 50 ps is assumed. The settling time for the individual conversion steps is reduced to 50 ps here. In total, the conversion cycle therefore takes 750 ps for eight bits. Additionally, the CDAC top side needs to be reset to the common-mode voltage for the residue amplifier to operate correctly. For this, a duration of 100 ps is assigned. The remaining margin of 150 ps is accounted to performance loss due to parasitic effects and to metastability events. The area on chip is 22 µm in width by 61.5 µm in height. Figure 6.23 shows the layout structure that was applied to the CDAC of the 8 bit SAR ADC rotated by 90°. Again due to the small size of the unit capacitors an interdigitated two dimensional matching pattern was chosen. The attenuation capacitors are placed facing inwards which enables a close

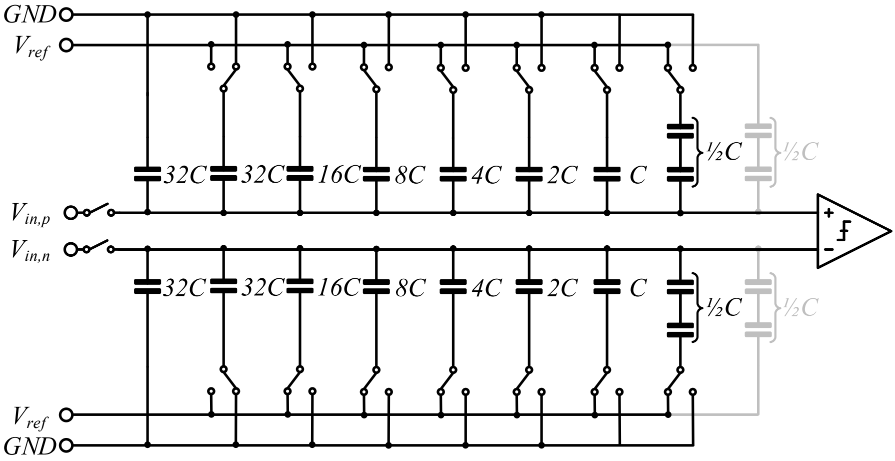


Figure 6.22: Schematic of the monotonic switching scheme with reversely connected MSB capacitors and half-unit capacitors for the second stage 8 bit SAR ADC.

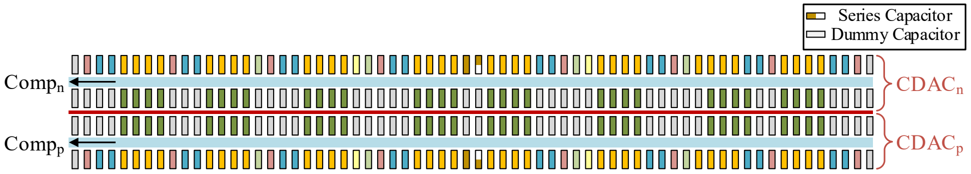


Figure 6.23: Illustration of the capacitor distribution in the CDAC of the second stage SAR ADC.

proximity between the positive and the negative side of the CDAC. The capacitors responsible for the generation of the reference voltages are placed facing outside which eases the wiring for the control logic and creates a very uniform environment. Dummy capacitors are also placed in between and on the perimeter to increase homogeneity.

6.10 Second Stage Comparator

While the demands on the CDAC of the second stage SAR ADC are decreasing, the demands on the comparator increase as it now needs to resolve a precision of 8 bit. The comparator of the first chip described in Section 4.5 showed an increased error rate in simulation hinting at too little gain in the first stage to activate the latch reliably in the given time frame. It was therefore modified as seen in Fig. 6.24. The tail switch transistor was reinstated for two reasons. The first being that it is easier to implement a high resistance which increases common-mode rejection. This alleviates the impact of the chosen switching scheme for the CDAC of the second stage ADC. Secondly, it allows to cross-connect the cascode transistors which increases the gain of the first stage. Clock feedthrough is however reintroduced with this, but simulations showed that it does not impact the overall accuracy of the 8 bit ADC. The second stage is adopted unaltered

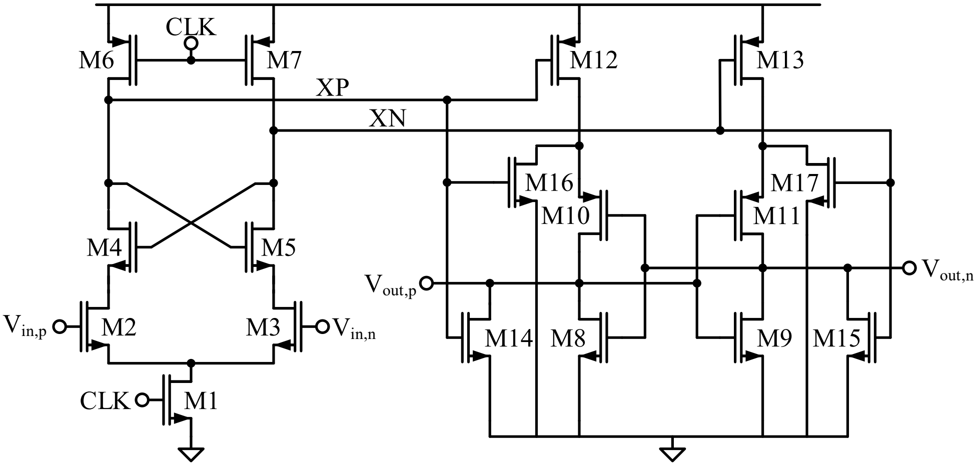


Figure 6.24: Schematic for the modified comparator for the second stage SAR ADC.

from the first-chip comparator. The operation principle for the modified comparator can be seen in Fig. 6.25. Here again an input of 20 mV differentially was chosen to be able to directly compare the behavior with the comparator of the first chip described in Section 4.5. The delay for a successful regeneration now increases to 42.8 ps. This is a consequence of the decreasing overdrive in the crosss-coupled cascode stage over time in contrast to the comparator of the first chip. The voltage between node XP and node XN however has now a significantly higher difference which leads to a more distinct switching direction for the second stage latch. The reset state is reached similar as before in 22 ps. The worst-case offset was determined with a Monte Carlo simulation over 1000 runs to below 10 mV. All values were obtained by simulation with an extracted schematic, meaning all parasitic elements from wiring etc. are considered. The area on chip needed for this comparator implemented is 8.2 µm in width by 5.4 µm in height.

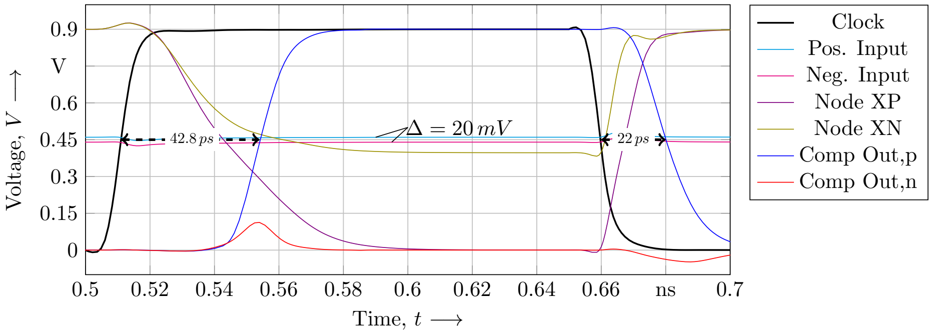


Figure 6.25: Output of the comparator implemented in the second stage SAR ADC.

6.11 Layout Overview

Figure 6.26 shows a screenshot of the layout of the software-configurable ADC. Highlighted are the individual components described before. The dimensions are given in width x length.

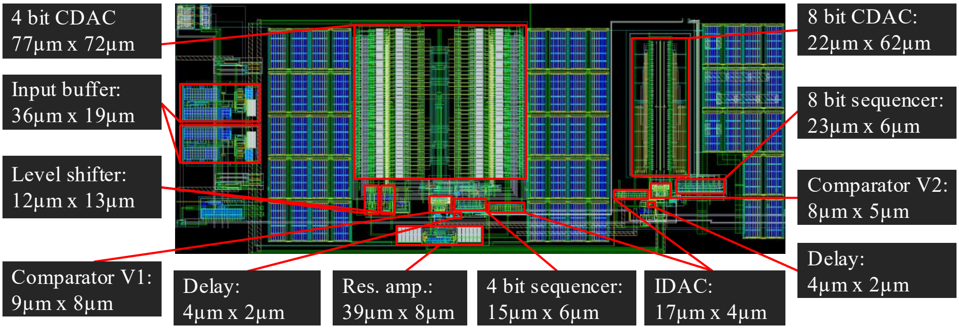

4 bit CDAC
77µm x 72µm
Input buffer:
36µm x 19µm
Level shifter:
12µm x 13µm
Comparator V1:
9µm x 8µm
Delay:
4µm x 2µm
Res. amp.:
39µm x 8µm
4 bit sequencer:
15µm x 6µm
IDAC:
17µm x 4µm
8 bit CDAC:
22µm x 62µm
8 bit sequencer:
23µm x 6µm
Comparator V2:
8µm x 5µm
Delay:
4µm x 2µm

Figure 6.26: Layout screenshot of the implemented software-configurable ADC.

Chapter 7

Measurement Results of Second ADC Chip

7.1 Printed Circuit Board

The process technology and metal stack configuration is kept as in the first chip development with a single-poly-eight-metal 28 nm process. Again a 1 mm by 1 mm silicon area die is processed and then packaged in a QFN package with 32 wire bonded output pads. The package has a size of 5 mm by 5 mm. The PCB design was done at the institute for this chip. It consists again of a motherboard for most of the connections and a detachable daughterboard carrying the chip itself and connections for the most crucial signals. It was adopted from the PCB of the first chip and only slightly modified to support the more individual power supply lines. Figure 7.1 shows the PCB of the daughterboard mounted on the motherboards on the left side and a close up of the package and the wire-bonded silicon die within on the right side.

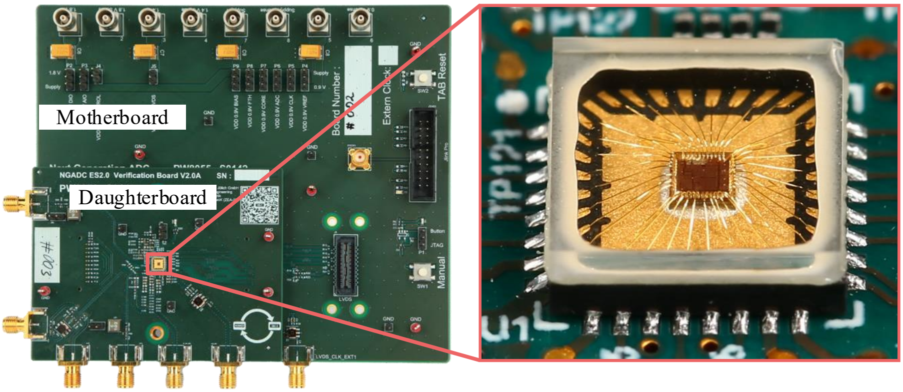


Figure 7.1: Measurement setup for the implemented SAR ADC.

7.2 Measurement Setup

The measurement setup also remains unaltered in comparison to the setup for the first chip and can be seen in chapter 5. The additionally needed supply voltages are also provided by the DC power analyzer N6705C from Keysight. To be able to sweep the input signal frequency, the waveform generator 33600A from Keysight was used. 20 dB attenuators were used to shift the range of the waveform generator to the level of the ADC and retain its resolution. Unfortunately, the maximum available frequency is therefore 120 MHz which is below the Nyquist frequency of the ADC. Signal generators, like the SMB100A from Rohde und Schwarz, produce strong harmonics which would require a tunable bandpass filter for frequency investigations.

7.3 Low-Power Mode Measurements

The low-power mode is characterized in the beginning as it uses the second stage of the pipelined ADC as standalone. Based on the found performance and configuration settings, the settings for the pipelined ADC in high-precision mode can be derived. Furthermore, this makes it easier to draw conclusion on the performance of the first stage, the residue amplifier and the residue interleaving.

7.3.1 Delay Line Configuration

In a first step, the minimum delay line configuration is found at which no performance degradation is observed. For this, a sample rate of 100 MSPS, an input signal frequency of 1 MHz and a differential input signal amplitude of 480 mV was chosen. The maximum signal amplitude differs from the nominal specified full-scale signal amplitude due to increased parasitic effects. Subsequently, the delay line configuration word was swept from "16", representing the mid-value of the adjustable delay, to "0", representing the shortest possible delay timing value. When a deterioration of the SNDR is noticeable, the sweep is stopped and the previous value is taken as the ideal configuration setting for the delay line of the investigated sample.
Multiple samples were tested and for all the delay line configuration could be swept down to "0" without any impact on the SNDR. This value is therefore kept for all following measurements. This indicates a systematic error which is traced back to the impact of parasitic elements dominating the overall delay.

7.3.2 Maximum Sample Rate

With the delay line configuration at "0", next the maximum sample rate is measured. Input signal and amplitude are kept at the same values as for the delay line configuration investigation. The sample rate is then swept with a step size of 50 MSPS from 5 MSPS which marks the lowest sample rate that could be successfully fed into the chip, to 600 MSPS. The results can be seen in Fig. 7.2 for two different samples. As they both show a similar characteristic, the curve trace is described in more detail on the basis of the first sample plotted in blue. The achieved SNDR stays relatively flat over 46 dB until 585 MSPS with a maximum of 47.4 dB for 405 MSPS. The SFDR shows a similar characteristic but has a maximum of 56.4 dB at 405 MSPS. After 585 MSPS the SNDR and SFDR are slowly declining. Because of the self-adjusted duty cycle, the typical one bit drop at increasing sample rates is not existent anymore. With higher sample rates, the sampling phase of the SAR ADC diminishes to a state at which the input signal is not sampled accurately anymore. The SNDR is therefore steadily reducing instead of abruptly

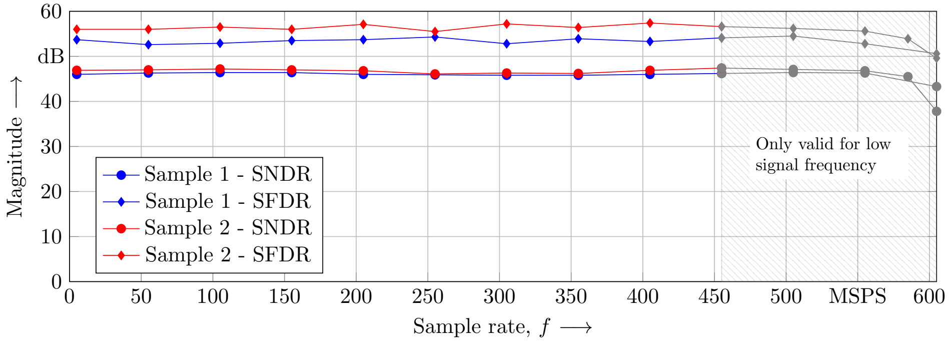


Figure 7.2: Measured SNDR and SFDR plotted over the sample rate for the second stage 8 bit SAR ADC for the low-power mode.

dropping. In case the sample rate is increased further and the sampling period is too small for the SAR ADC to finish its conversion cycle, the *SAR RDY* signal is not resetting the D flip-flop in time. Therefore the ADC stays in conversion mode and the next sampling cycle is not started but skipped leading to unpredictable behavior. This can be seen for sample 2 at a sample rate beyond 585 MSPS at which a strong decline in performance is visible.
With the self-adjusted duty cycle, the conversion phase timing stays fixed while the sampling phase timing is reduced for higher sample rates. This implicates that the SAR ADC can achieve a higher total sample rate for lower input signals which need a lower settling time during the sampling phase. While this may be suitable for some applications, e.g. for oversampling, the sample rate found with only a low-frequency input signal is not showing a complete picture. The measurement was therefore repeated with the maximum available signal frequency of 119.99 MHz. The maximum achievable sample rate reduced to 455 MSPS now. The remaining sample rate range shown in Fig. 7.2 is therefore grayed out.

7.3.3 Power Consumption

Figure 7.3 shows the power consumption of the SAR ADC plotted over the sample rate. Excluded are the input buffer, the reference buffer and the digital leaving only the ADC core itself. While the left-out blocks are essential for the correct operation of an ADC, they are not optimized for performance and skew the actual performance of the ADC. As before the sample rate was swept in 50 MSPS steps starting at 5 MSPS and ending at 600 MSPS. A linear scaling with the sample rate can be seen as expected from the mostly dynamic circuit elements of a SAR ADC. The sample rate range above 455 MSPS holding up only for low input signal frequencies is again grayed out. The power consumption offset extrapolated at 0 MSPS is 0.11 mW for sample 1 and 0.1 mW for sample 2. It increases linearly with an average step size of 0.05 mW to 0.61 mW for sample 1 and 0.59 mW for sample 2 at a sample rate of 455 MSPS. For sample 2 beyond a sample rate of 585 MSPS a sharp decline is visible. This is the point at which the conversion phase timing is larger than the global sampling period. Because of the self-adjusted duty cycling scheme, the ADC starts skipping samples which results in a reduced power consumption.

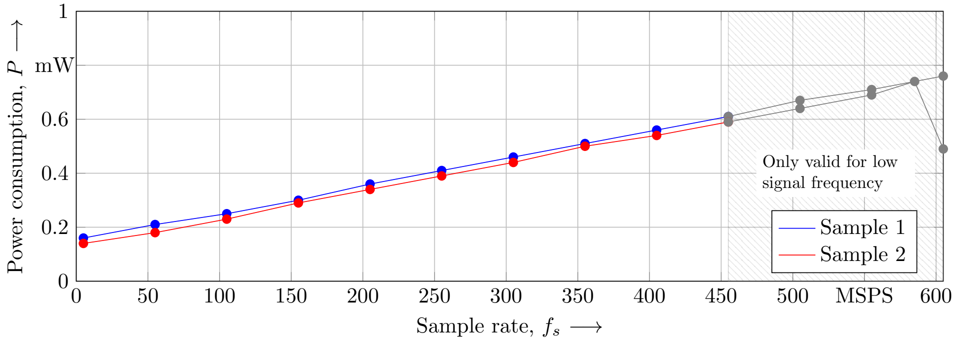


Figure 7.3: Measured power consumption plotted over the sample rate of the implemented second stage 8 bit SAR ADC for the low-power mode.

7.3.4 Maximum Input Signal Frequency

With the optimum delay line configuration and the maximum sample rate determined, now the maximum input signal frequency is investigated. For one measurement 8168 points are recorded. To have only full periods of the input signal sinus which reduces spurs in the spectrum, the precise input signal frequency is calculated with

$$f_{sig} = \frac{P f_s}{N}. \tag{7.1}$$

Here, f_{sig} is the input signal frequency, P is the number of periods contained in the total amount of recorded points N and f_s is the sample rate. With P being the free adjustment parameter, it is chosen such that the signal frequency is close to the wanted frequency for the investigated points.

The sample rate is adjusted to the before found 455 MSPS, the input signal amplitude is reduced to 428 mV which is −1 dB below the full-scale input signal amplitude to prevent clipping. The input signal frequency measurement is started at a value around 11 MHz and then incremented

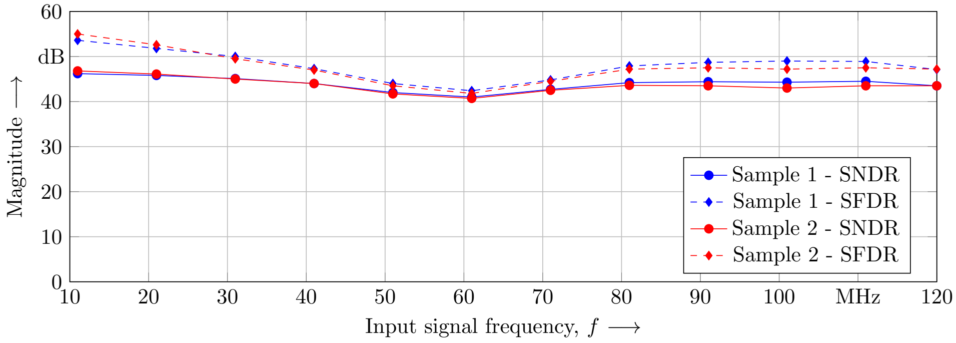
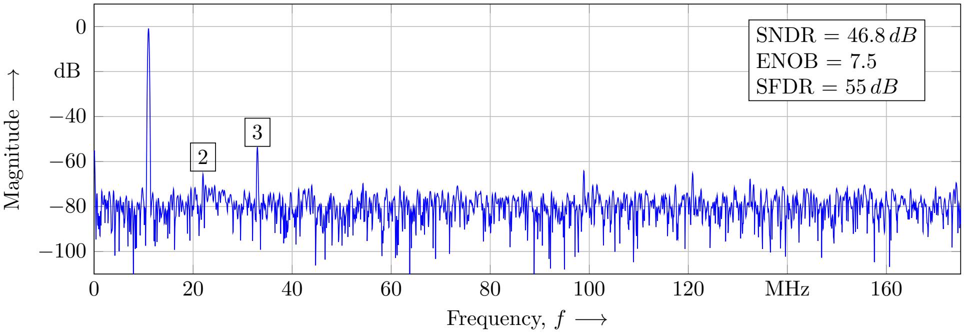


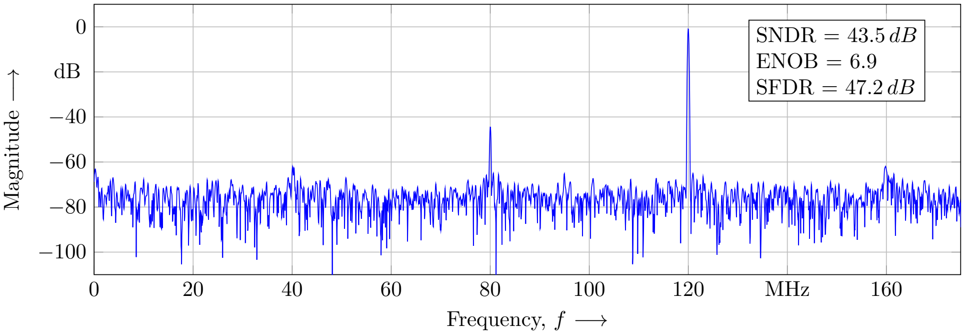
Figure 7.4: Measured ENOB and SFDR plotted over the input signal frequency of the second stage 8 bit SAR ADC for the low-power mode.

in 10 MHz steps to a maximum of around 120 MHz. The results are shown in Fig. 7.4 for two samples. Both samples show a similar characteristic. In the following it is therefore described on the basis of the results of sample 2. The SNDR has a maximum of 47.4 dB at 11 MHz and stays consistently above 41 dB for the whole investigated range. Similarly the SFDR stays above 42 dB and has a maximum of 56.4 dB at 11 MHz.

Figure 7.5 shows the spectra of the ADC for a sample rate of 350 MSPS. It was adjusted to be able to compare the characteristic with the results of the SAR ADC of the first chip as well as the ADC in high-performance mode. Figure 7.5a shows the spectrum for a low frequency input signal of 11 MHz, Fig. 7.5b shows the spectrum for the maximum available input frequency signal of 120 MHz. For both 8168 samples were recorded. For both spectra a strong harmonic is visible limiting the maximum SFDR.



(a)



(b)

Figure 7.5: Measured spectrum of the implemented second stage 8 bit SAR ADC at a sample rate of 350 MSPS. (a) Spectrum for a low frequency input signal of 11 MHz. (b) Spectrum for the maximum available input frequency of 120 MHz.

7.3.5 DNL and INL

Figure 7.6 shows the DC output characteristic of the ADC for a sample rate of 455 MSPS. Here, chip sample 2 is used to illustrate the DC behavior. The input voltage range was swept from the nominal, simulated minimum to maximum in a DC measurement with a high precision

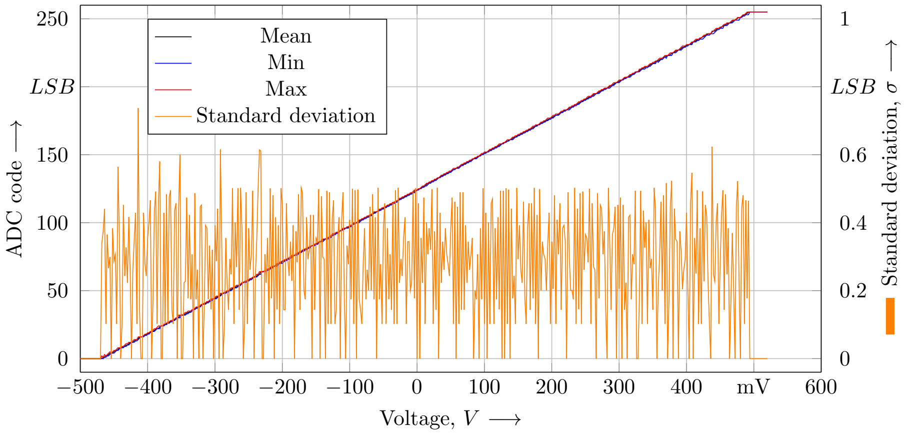


Figure 7.6: Measured output characteristic of the implemented second stage 8 bit SAR ADC.

voltage source and additional, discrete output noise filters. The step size for this was chosen to half the nominal LSB size which is 4.69 mV. Subsequently the mean of hundred sampled was formed and plotted beside the maximum and minimum found value for all samples. The standard deviation plotted in orange shows a correct behavior with an average value of 0.5 LSB. The input voltage range is lower than specified as the output of the ADC only starts rising at a voltage of −480 mV and clips already at a voltage of 490 mV. This can be explained by additional parasitic caps, e.g. from metal traces, connected the CDAC to the input signal. The maximum measured input range of the ADC is therefore 970 mV differentially and the LSB size of the ADC reduces accordingly to 3.79 mV. There is also an offset of 10 mV visible.
Subsequently the DNL and INL of the ADC were measured. The step size here was chosen to 100 µV to precisely capture the transition points for every LSB. The results are illustrated in Fig. 7.7. The DNL lies within -0.7/+0.9 LSB. As its absolute stays below 1 LSB the ADC is therefore monotonic and has no missing codes. The INL lies within -2.1/+0.4 LSB. Noticeable here are the jumps around $^1/_4$, $^1/_2$ and $^3/_4$ of the full-scale input range of the ADC. They can be explained by mismatch of the unit capacitors in the CDAC. At the mentioned points it is most pronounced as the most capacitors have a charge redistribution for these ADC codes.

7.3.6 Performance Summary

Concluding the measurements Tab. 7.1 shows a summary of the key parameters used nowadays to evaluate the performance of ADCs.

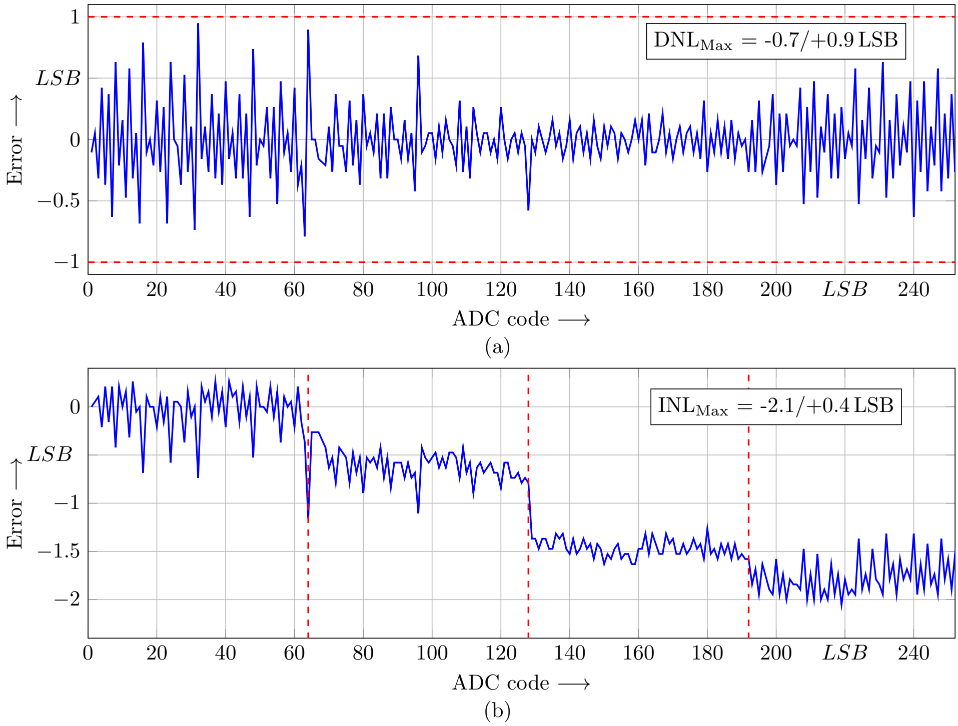


Figure 7.7: (a) Measured DNL and (b) measured INL of the implemented second stage 8 bit SAR ADC.

Table 7.1: Performance summary for the implemented 8 bit SAR ADC in standalone operation for the low-power mode.

Parameter	Value
Architecture	SAR
Technology	28 nm
Supply Voltage	0.9 V
Resolution	8 bit
Max Amplitude	485 mV
SNDR @ 11 MHz	47.4 dB
SNDR @ 120 MHz	43.5 dB
SFDR @ 11 MHz	56.4 dB
SFDR @ 120 MHz	47.2 dB
Sample rate	455 MSPS
Power consumption	0.59 mW
Area	0.0025 mm^2
FoM$_{\mathrm{W}}$	10.8 fJ/c.-s.
FoM$_{\mathrm{S}}$	162.1 dB

7.4 High-Precision Mode Measurements

For the high-precision mode the initial functionality test failed and the input signal could not be reconstructed from the converted digital samples. After intensive error search in the laboratory and in simulation, settings were found that put the ADC in a functional state which allows to recognize a reconstructed input signal qualitatively, although not the wanted performance in accuracy is reached. Very specific configurations had to be adjusted, whose impact cannot be traced back to one individual block on the chip. The sample rate for example has to be around 350 MSPS. In the following, only the effect of a change in the common-mode voltage of the input signal being fed directly into the ADC and an increase of the supply voltage for the first stage ADC is described in detail. This setting has a big impact on the performance of the ADC in high-performance mode and its influence is isolated to the ADC.
Due to this incorrect operation, there is a deviation from the usual verification pattern as was introduced in the measurements before. At first now the error and its correction are described. Furthermore, the previously identified configuration settings for the second stage SAR ADC are adopted for the following measurements.

7.4.1 Erroneous Output Characteristic

To understand the nature of the error occurring in the pipelined SAR ADC in high-precision mode, the DC output characteristic was investigated. For this, the nominal common-mode voltage of 450 mV was applied and the input signal was swept around it from −600 mV to 600 mV differentially. The step size was chosen to 100 µV to have an accurate representation of the LSB transition point. The sample rate is kept at 350 MSPS throughout all measurements. The result can be seen in Fig. 7.8. The output characteristic is strongly corrupted. In some locations however, for example between 80 mV and 144 mV, a finer step size granulation is visible. This is a first indicator that the pipelined operation works in principle. Furthermore, the error stays in the boundary of the current resolution of the first stage SAR ADC which suggests that it operates correctly without error. In combination with the previous measurements of the

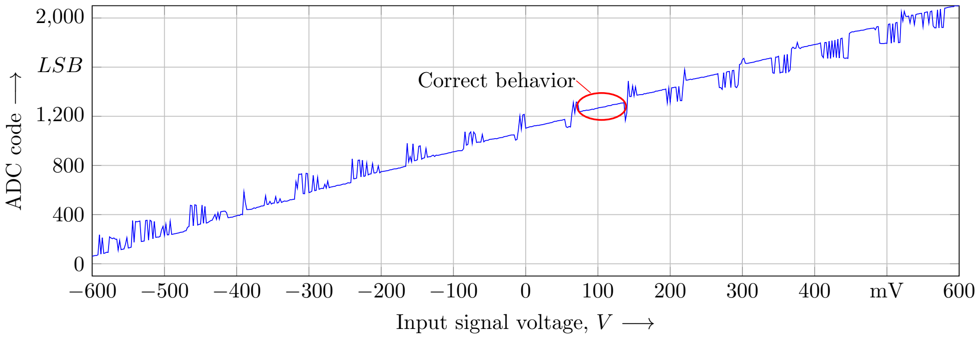


Figure 7.8: Measured erroneous output characteristic of the implemented pipelined 11 bit SAR ADC for the high-precision mode with the nominal common-mode voltage of 450 mV.

second stage SAR ADC which also showed a correct, error-free operation, the faulty behavior can be narrowed down to the residue transition or the residue amplifier. The severity of the measured error and the general sensitivity to common-mode voltage changes in the amplifier give a first lead to understand and compensate the error.

7.4.2 First Stage ADC Investigation

To eliminate the first stage SAR ADC as the source of error, it was also investigated on its own as standalone ADC. As the subsequent residue amplifier and second stage SAR ADC cannot be switched off independently, instead the last seven bit of the pipelined ADC are discarded. Only a short written summary of the most important performance parameters without visual representation is given here. As the first stage 4 bit SAR ADC is outperformed in every way by the second stage 8 bit SAR ADC, there is no reason for it to run in standalone and a detailed analysis has no merit.

The delay line configuration can be reduced to "0" without a performance deterioration. For the pipelined operation this value has no significance however, as the CDAC needs to settle to a precision of 11 bit and not just 4 bit as here. The pipelined ADC therefore needs a respectively higher settling time and the delay line configuration needs to be adjusted as a function of all relevant parts. The sample rate can be increased to the maximum specification of 500 MSPS without any impact on the performance observed. Likewise the input signal frequency causes no reduction in performance starting at for a maximum available frequency of 120 MHz. The maximum SNDR and SFDR measured are 24.5 dB and 36 dB. For the DNL and INL the maximum absolute values are 0.21 and 2.1. Finally, parasitic elements reduce the maximum differential input signal amplitude to 580 mV.

7.4.3 Impact of Input Common-Mode Voltage

As the input common-mode voltage is a parameter that has a direct influence on the behavior and the performance of the ADC, it was investigated next. There is an internally generated common-mode voltage which is used in the first stage SAR ADC and in the residue amplifier. If there is a mismatch between the input common-mode voltage and the internal common-mode voltage, the input signal's common mode and thus also the residue's common-mode voltage will be shifted in the CDAC by a certain amount. The difference between the common-mode voltage from the reference buffer used to auto-zero the residue amplifier, and the common-mode voltage of the residue will also be amplified by the residue amplifier. There is resilience against common-mode voltage shifts built into the pipelined ADC due to the one bit overlap and the halved residue amplifier gain, but also only to a certain degree. Figure 7.9 shows the SNDR as an indicator parameter plotted over an input common-mode voltage shift for three samples. The sample rate is kept at 350 MSPS, the input signal frequency is 128.5 kHz and the input signal amplitude is adjusted to 1.16 V differentially which is the measured full-scale range of the pipelined ADC. This is done to maximize the information that can be retrieved from this investigation. To make sure this is not the limiting factor, the delay line configuration was swept along side the input common-mode voltage sweep. For very low and for very large delay settings the SNDR dropped, but stayed constant otherwise for a wide delay range. Additionally, the supply voltage of the first stage SAR ADC was also varied slightly. It has also an impact on the final common-mode voltage generated in the CDAC of the first stage. The

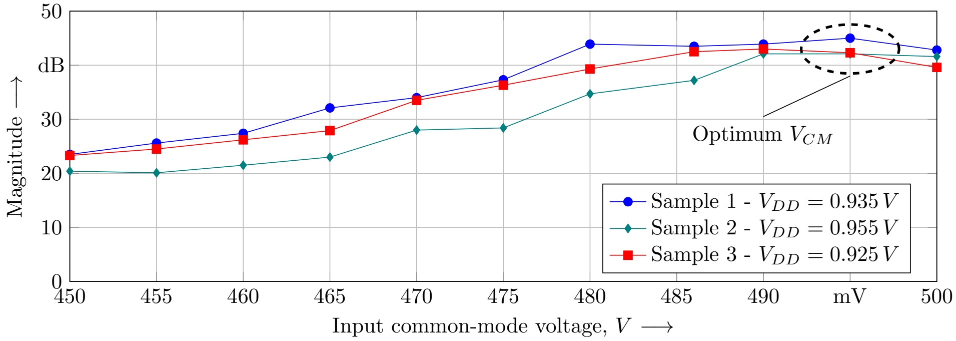


Figure 7.9: SNDR plotted over input common-mode voltage of the implemented pipelined 11 bit SAR ADC for three samples.

input common-mode voltage is adjusted from 450 mV to 500 mV in 5 mV steps. For all three samples there is the same trend visible. The performance of the pipelined ADC improves with an increased input common-mode voltage peaking around 495 mV. The maximum SNDR of 45 dB is achieved by sample one with an input common-mode voltage of 495 mV and a first stage ADC supply voltage of 935 mV. While this value is significantly smaller than the expected SNDR of an 11 bit ADC, it can be increased to 49 dB after calibration and therefore exceeds the maximum SNDR of the standalone second stage 8 bit ADC. It shows that the pipelined ADC operation works albeit only in a very limited fashion. The common-mode voltage sweep was also repeated single-endedly through the whole investigated common-mode voltage range on the negative side of the differential input for every increment on the positive side of the differential input. The outcome of this showed no improvement, but yielded the same maximum performance as before. On a side note, the input common-mode voltage sensitivity was also investigated for the second stage 8 bit SAR ADC in standalone. It showed superior resilience and there was no performance degradation observable over a range of −100 mV to 100 mV in common-mode voltage change.

Figure 7.10a shows the improved output characteristic of the implemented pipelined 11 bit SAR ADC for the high-precision mode for sample one with an adjusted common-mode voltage of 495 mV and an increased first stage ADC supply voltage of 935 mV. The black curve shows the average output code for the given differential input signal voltage generated from 100 successively recorded signal samples. The red curved shows the maximum and the blue curve shows the minimum value that occurred among the 100 signal samples. The orange curve with its y axis on the right side shows the standard deviation of the 100 signal samples from the average value. The mean output characteristic now shows a fine resolution granularity resembling the output of an 11 bit ADC. The maximum and minimum values deviate from the mean by -3/+3 LSBs indicating that there is increased noise existing in the system, but the standard deviation with a value between 1.8 and 2 puts this into perspective hinting at a typically smaller noise range. However, in certain intervals a larger standard deviation can be seen that has a more severe impact on the accuracy of the pipelined ADC. For a clearer view of the remaining error, Fig. 7.10b has a close up of the range between −100 mV and 0 mV. These large spikes are 128 LSBs apart which means that they occur after all bits of the second stage

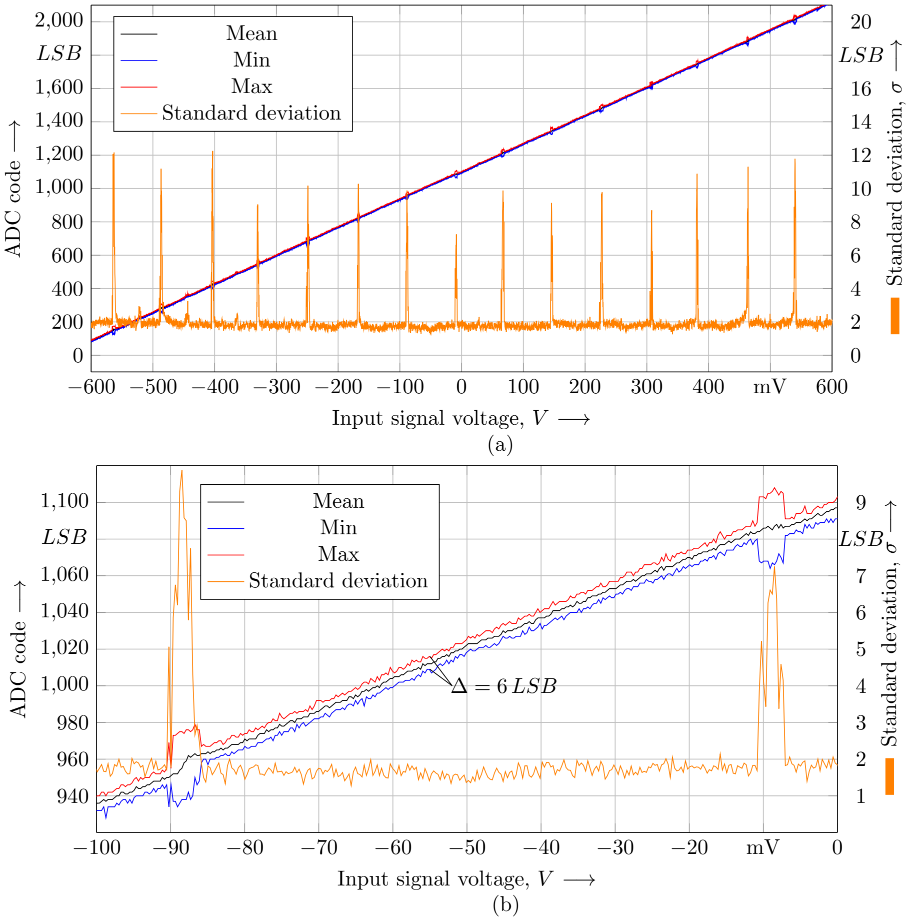


Figure 7.10: (a) Improved output characteristic of the implemented pipelined 11 bit SAR ADC for the high-precision mode with an adjusted common-mode voltage of 490 mV. (b) Close up between −100 mV and 0 mV highlighting the large standard deviation every 128 LSBs.

ADC are cycled through and a bit of the first stage ADC changes. This is a typical error seen if there is a gain error in the residue amplifier. In this case the error with a standard deviation of 7 to 12 LSBs is too large and the maximum and minimum values show a significant increase which cannot be explained by a gain error.

7.4.4 Power Consumption

With the limited amount of investigation space an extensive measurement of the power consumption of the sample rate is not possible or meaningful. The power consumption is therefore investigated only for the pipelined ADC in the functional state at a sample rate of 350 MSPS.

With a power consumption of 2.23 mW the differential input buffer holds the largest share on the total power consumption. Due to the many different implementation possibilities of an ADC frontend, e.g. low-noise amplifier, transimpedance amplifier or input buffer, the power consumption is usually only given for the core ADC. This is also adopted here. A distribution of the overall power consumption of the core pipelined ADC on the respective sub blocks is illustrated in Fig. 7.11 excluding the input buffer, the reference buffer and digital processing circuits. The first stage SAR ADC has the highest power consumption with 1.71 mW, then the residue amplifier follows with 1.31 mW followed finally by the second stage SAR ADC with 0.43 mW. The total power consumption thus sums up to 3.45 mW.

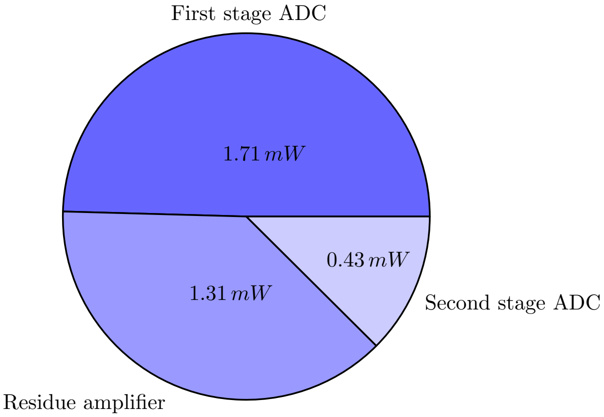


Figure 7.11: SNDR plotted over input common-mode voltage of the implemented pipelined 11 bit SAR ADC for three samples. The total power consumption thus sums up to 3.45 mW.

7.4.5 SNDR and SFDR

To give a complete overview, albeit under the constraint of the limited performance, the maximum SNDR and SFDR were investigated. The input signal amplitude is adjusted such that the reconstructed output signal shows an amplitude 1 dB below the full-scale range which translates to a differential amplitude of 1.03 V. The delay line configuration is kept at "16" and the sample rate is kept at 350 MSPS. The input signal frequency is adjusted to 11 MHz To arrive at the highest retrievable performance, additionally a simple look-up table based off-chip calibration was implemented. For this a high number of periods from the original reconstructed output signal of the ADC is compared against a fitted ideal sinusoidal signal. The difference between the ideal sinus and the ADC output for every ADC code is captured and finally averaged to obtain a correction value for the respective ADC code. With this a maximum SNDR of 46.9 dB is measured which corresponds to an ENOB of 7.5 bit. The maximum SFDR found is 55.2 dB. Figure 7.12 illustrates the performance again by plotting the spectrum of the ADC. It shows that the limiting factor for the SFDR is the third harmonic.

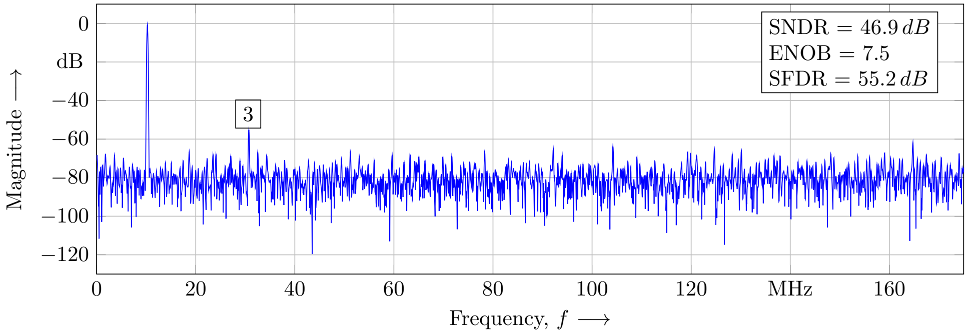


Figure 7.12: Measured spectrum of the implemented pipelined 11 bit SAR ADC for the high-precision mode with an input signal frequency of 10.99 MHz.

7.4.6 DNL and INL

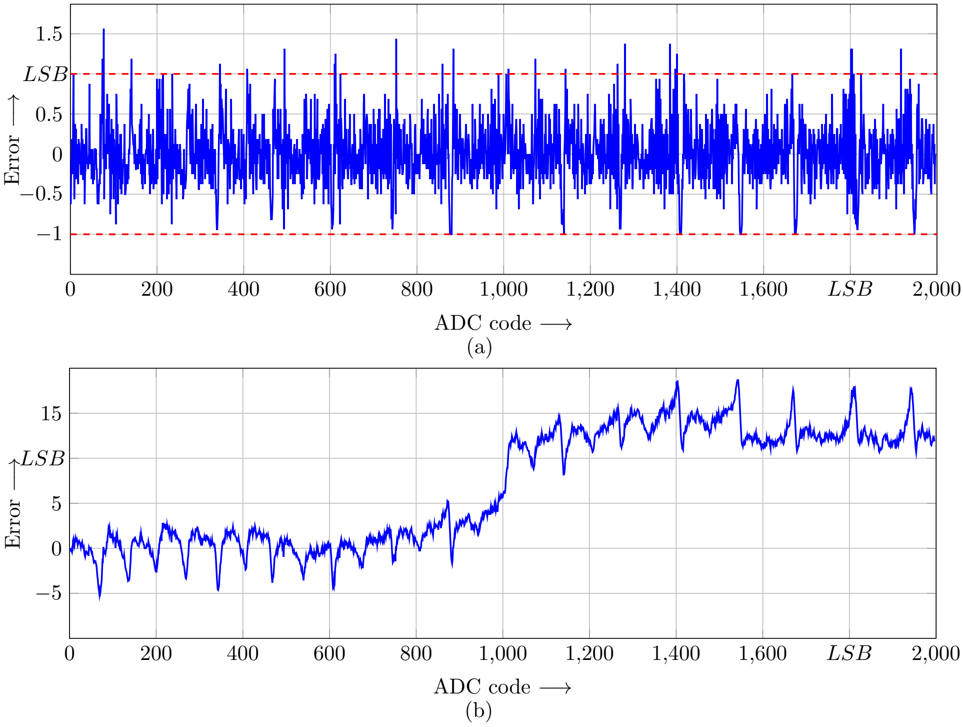


Figure 7.13: (a) Measured DNL and (b) measured INL of the implemented pipelined 11 bit SAR ADC for the high-precision mode at a sample rate of 350 MSPS.

The DNL and INL of the pipelined ADC were also measured and are presented here for completeness. The step size here was chosen to 100 µV to precisely capture the transition points for every LSB. The results are illustrated in Figure 7.13. The DNL mostly lies within

-0.5/+1 LSB which would attest a decent performance. But also here the strong corruption of the output characteristic in regular intervals is clearly visible. The INL lies within -5/+18 LSB. The large jump around the ADC code "1024" is partly due to the structure of the CDAC in a SAR ADC as here the most capacitor have a charge distribution. Mismatch of the unit capacitors in the CDAC has its largest impact here. The other spikes visible are a combination of the gain error, the INL of the second stage ADC and the corrupted signal similar as seen in the DNL as well as the output characteristic.

7.4.7 Performance Summary

Concluding the measurements Tab. 7.2 shows a summary of the key parameters used nowadays to evaluate the performance of ADCs.

Table 7.2: Performance summary for the implemented pipelined 11 bit SAR ADC for the high-precision mode.

Parameter	Value
Architecture	SAR
Technology	28 nm
Supply Voltage	0.9 V
Resolution	11 bit
Max Amplitude	0.58 V
SNDR @ 11 MHz	46.9 dB
SFDR @ 11 MHz	55.2 dB
Sample rate	350 MSPS
Power consumption	3.45 mW
Area	0.016 mm^2
FoM_W	54.4 fJ/c.-s.
FoM_S	154 dB

7.5 Discussion of Second Chip ADC

7.5.1 Low-Power Mode

The measurement results for the low-power mode which deploys only the second stage 8 bit SAR ADC, show satisfactory results. The targeted sample rate of 500 MSPS in the specifications is not reached with a maximum measured sample rate of 455 MSPS, but shows a significant improvement over the first chip SAR ADC resolving two more bit at a faster sample rate. Noticeable is that the delay line configuration can be set to "0" providing the smallest delay without a degradation of the SNDR. Parasitic elements in the physical layout distributed over the whole SAR cycle loop reaching from the comparator to the delay line, the sequencer and also especially the wiring between the individual components were underestimated. It might be advantageous to leave out the delay element completely for low resolution SAR ADCs as their presence alone adds a delay that is larger than needed. Comparisons with other ADC developments with similar resolutions and manufactured in the same or close process technology nodes achieve significantly higher sample rates in the GHz-range showing the full potential that can be achieved [79] [85]. With advanced process technologies such as 28 nm parasitic elements reach the same order of magnitude as transistor elements. The discrepancy in sample rate is mainly attributed to the layouts which were done in the traditional way focusing on mismatch and area efficiency. For improvements, more radical approaches for layouting must be investigated prioritizing speed.

The ENOB is 7.5 bit at a low input signal frequency of 11 MHz and 6.9 bit for a high input signal frequency of 120 MHz. These are acceptable levels for an 8 bit ADC hard limited by quantization noise. A loss of one half to one full bit is normal especially for high-performance ADCs. For the 10 bit ENOB accuracy of the pipelined ADC an ENOB of over 6 bit is needed which is achieved. The ENOB therefore meets the specifications.

The input signal amplitude is nominally specified to 600 mV. Measurements showed a deviation by 125 mV for an actual input signal amplitude of only 485 mV. This is a significant difference that needs to be addressed in future developments. The amplitude should be used at its maximum capacity, as it provides an effective method to increase SNR. The cause is here as well the underestimated impact of parasitic elements in the physical design. With the implementation chosen it is however easy to correct. For this, the nominal amount of attenuation capacitors can be reduced to mitigate the attenuating influence of parasitic capacitor elements.

The total power consumption of the second stage 8 bit SAR ADC core is 0.59 mW at the maximum sample rate of 455 MSPS. There is little room for improvement in the design regarding power consumption without compromising at parameters like resolution or sample rate. Marginal headroom exists for example in the buffering chains of some signals or in the bias current for the delay element, but the gain versus effort exhibit a poor ratio. More importantly for this chip and the concept that is investigated, is the linear scaling behavior which the ADC core features convincingly.

7.5.2 High-Precision Mode

The high-precision mode which uses the pipelined, two-stage 11 bit SAR ADC is not operating correctly under nominal conditions. Specific configurations were found during verification in the laboratory that restore the general functionality albeit a significantly reduced performance. Among other universal chip configurations the sample rate has to be at a fixed 350 MSPS. For the ADC regarded individually the input common-mode voltage has a direct impact on the performance and has to be increased to 495 mV to achieve a state with a recognizable output characteristic. The performance can be improved further by increasing the power supply voltage of the first stage SAR ADC which also finally has an impact on the common-mode voltage prevailing in the CDAC. This erroneous behavior persisted over three samples and temperature changes hinting at a systematic error. Although there is some robustness against common-mode voltage changes built in the design of the pipelined ADC, at a deviation of -/+30 mV from the nominal voltage of 450 mV, simulations showed a performance breakdown. A Monte Carlo simulation over 1000 runs for the reference buffer revealed a worst case deviation surpassing the limit of 30 mV for the common-mode voltage. While this apparently contradicts the conclusion from the measurements hinting at a systematic error, investigations in the layout of the reference buffer revealed a weakness which significantly boosts the probability of a common-mode voltage deviation.

With the workaround, the maximum ENOB of 7.5 bit of the pipelined ADC is in the same range as the maximum ENOB of 7.5 bit of the standalone second stage 8 bit ADC. As a consequence, using the high-performance mode in applications is not feasible. However, this first version of a software-configurable is not primarily designed for a specific application, but rather to gain experience and investigate the feasibility of the concept. From this perspective, the corrected operation shows that the residue transfer and amplification, and therefore the pipelined ADC works in principle as the signal is passing through all the stages.

The power consumption of the pipelined ADC core at a sample rate of 350 MSPS is 3.45 mW. As with the second stage ADC, the possibilities to increase the power efficiency in the first stage are exhausted to a large degree without compromising on other performance parameters. The residue amplifier contributes a high static power consumption offset to the otherwise highly linear scaling of the SAR ADCs with the sample rate. At lower sample rates, its contribution is the dominating factor for the power consumption. To mitigate this, the residue amplifier could be modified such that the the power-down function also activates after the residue amplification process is finished.

Chapter 8

Conclusion and Outlook

This thesis proposes and investigates the concept of a software-configurable ADC. It tackles the major challenges of future developments in integrated electronics for research applications. While a generic approach will never reach the same performance as a dedicated development, its ability to adjust in resolution, sample rate and therewith ultimately in power consumption makes it suitable for a broad range of application fields. This more generic approach to IC design is regarded as the only way to use modern process technology nodes in research. Their development cost would otherwise exceed the budget of individual research groups. Instead, more generic, interchangeable blocks of a system are developed and shared in the community. For the concept of a software-configurable ADC, multiple smaller sub ADCs are arranged in a matrix-like grid, leaning on existing topologies of pipelining and time-interleaving to enable the configurability in resolution and sample rate. As key enabler the SAR ADC architecture was identified which scales very well with technology nodes and has superior energy efficiency compared with other ADC architectures.

For the elaboration of the concept presented in this thesis two chips were manufactured. The first chip was a pilot project marking the transition to a more modern 28 nm bulk CMOS technology process for the institute. The main focus here was to identify the potential and also the drawbacks of the technology as well as to gather experience in the design of SAR ADCs. In conclusion, the merit for digital circuits is significant which also benefits the performance of SAR ADCs due to their digital nature. Analog design, with some concessions, is also still viable as seen by the input buffer which is built using a standard operational amplifier. The results are in line with the expectations. Based on this, concept developments and investigations are continued with the design and manufacturing of a second chip.

The second chip has a first version of a software-configurable ADC at its core. It features a low-power mode with a reduced resolution of 8 bit and a high-precision mode with a maximum resolution of 11 bit. The SAR architecture for the sub ADCs and the use of a ring amplifier as the residue amplifier provide high power efficiency and a linear scaling of the power consumption with the sample rate. While the low-power mode showed convincing results with a maximum ENOB of 7.5 bit and a maximum sample rate of 455 MSPS at a power consumption of 0.59 mW, the high precision mode exhibited a defective behavior. The general functionality could be restored by adjusting certain parameters, but the performance stayed below the anticipated results. However, as this chip is mainly a proof of concept without a dedicated application, the overall functionality has priority over the quantitative performance. Even with the limited operation range, a positive conclusion can be drawn from this development. The area increase to implement a software configurability is minimal in the ADC core. In low-power mode with the first stage ADC and the residue amplifier deactivated the power can be reduced by 83 %.

Also in low-power mode the maximum sample rate can be increased beyond the sample rate of the high-precision mode expanding the application space. The second chip therefore serves as basis for continued research and investigation on SAR ADCs, pipelined ADCs and also on the concept of a software-configurable ADC.

A software-configurable ADC with only two stages is less meaningful, as the effort to create two separate ADCs instead, one ADC with 8 bit and one ADC with 11 bit, is still manageable. But the more individual application cases with specific needs in terms of resolution, sample rate and power consumption, arise, the more a dedicated development for every single use case loses its feasibility; at least in the research community with limited resources. Neglected in this thesis as it would be out of scope, it should be kept in mind that high-performance ADCs also need various digital support circuits like a calibration which has to be redesigned for every dedicated application as well. How well the software-configurability scales beyond a two-stage pipelined ADC design is therefore a crucial next step. The first possible direction would be to add an additional sub ADC to the pipelined ADC increasing the configurable resolution range. The main challenge here is to achieve a high common-mode rejection ratio as the residue now has to pass through two amplifiers and deviations are magnified accordingly. The second possible direction would involve the implementation of a parallel ADC for time-interleaving. The design focus here lies on the precisely synchronous distribution of the input signal and the global reference clock determining the track and hold phase. For this, a combination of analog and digital calibration methods needs to be implemented. A more general observation made during the measurement of the second chip which was trimmed more towards a higher performance than the first chip, is the significant impact of parasitic elements in the physical layout on the overall performance in a 28 nm process technology. For future developments, advanced layout techniques could be investigated moving away partly or completely from the conventional layout rules for certain designs.

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Curriculum Vitae

Lukas Krystofiak

Academic Degree	Master of Science in Electrical Engineering
Date of Birth	30.08.1990
Place of Birth	Cologne, Germany

Professional Experience

10.2018 - 06.2023	Doctoral Researcher at Central Institute of Engineering, Electronics and Analytics, Electronic Systems (ZEA-2) - Forschungszentrum Jülich GmbH, Jülich, Germany
04.2017 - 08.2017	Internship at Fraunhofer Institute for Microelectronic Circuits and Systems, Duisburg, Germany
10.2016 - 02.2017	Research Assistant at Chair of Integrated Analog Circuits and RF Systems - RWTH Aachen University, Aachen, Germany

Education

10.2015 - 04.2018	Master of Science in Electrical Engineering, RWTH Aachen University, Aachen, Germany
10.2011 - 09.2015	Bachelor of Science in Electrical Engineering, RWTH Aachen University, Aachen, Germany

Publications and Conferences

Journal Publications

L. Krystofiak, F. Rössing, A. Zambanini, C. Grewing and S. van Waasen, "Towards a generic receiver chain for particle detectors," Journal of Instrumentation, vol. 17, no. 5, May. 2022, Art. no. C05025, DOI. 10.1088/1748-0221/17/05/C05025.

Conferences and Workshops

L. Krystofiak, A. Zambanini, C. Grewing and S. van Waasen, "A Software-Scalable ADC in 28nm CMOS for Detector Readout," DPG Spring Meetings 2023, Dresden, Germany, March 2023

L. Krystofiak, F. Rössing, A. Zambanini, C. Grewing and S. van Waasen, "Progress of Integrated Receiver Electronics," 3nd High-D Consortium, February 2023

L. Krystofiak, F. Rössing, A. Zambanini, C. Grewing and S. van Waasen, "Progress of Integrated Receiver Electronics," 2nd High-D Consortium, September 2022

L. Krystofiak, F. Rössing, A. Zambanini, C. Grewing and S. van Waasen, "Concept of a software-adaptable receiver chain for particle detectors," SEI-Tagung-2021 Studiengruppe Elektronische Instrumentierung, October 2021

L. Krystofiak, F. Rössing, A. Zambanini, C. Grewing and S. van Waasen, "Towards a Software-Adaptable Receiver Chain for Particle Detectors," Topical Workshop on Electronics for Particle Physics (TWEPP), April 2021

Master Thesis Supervision

F. Freye, "Development of a fast digital interface (SERDES) with clock recovery",Master Thesis, Integrated Analog Circuit and RF Systems, RWTH Aachen University, March 2021

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