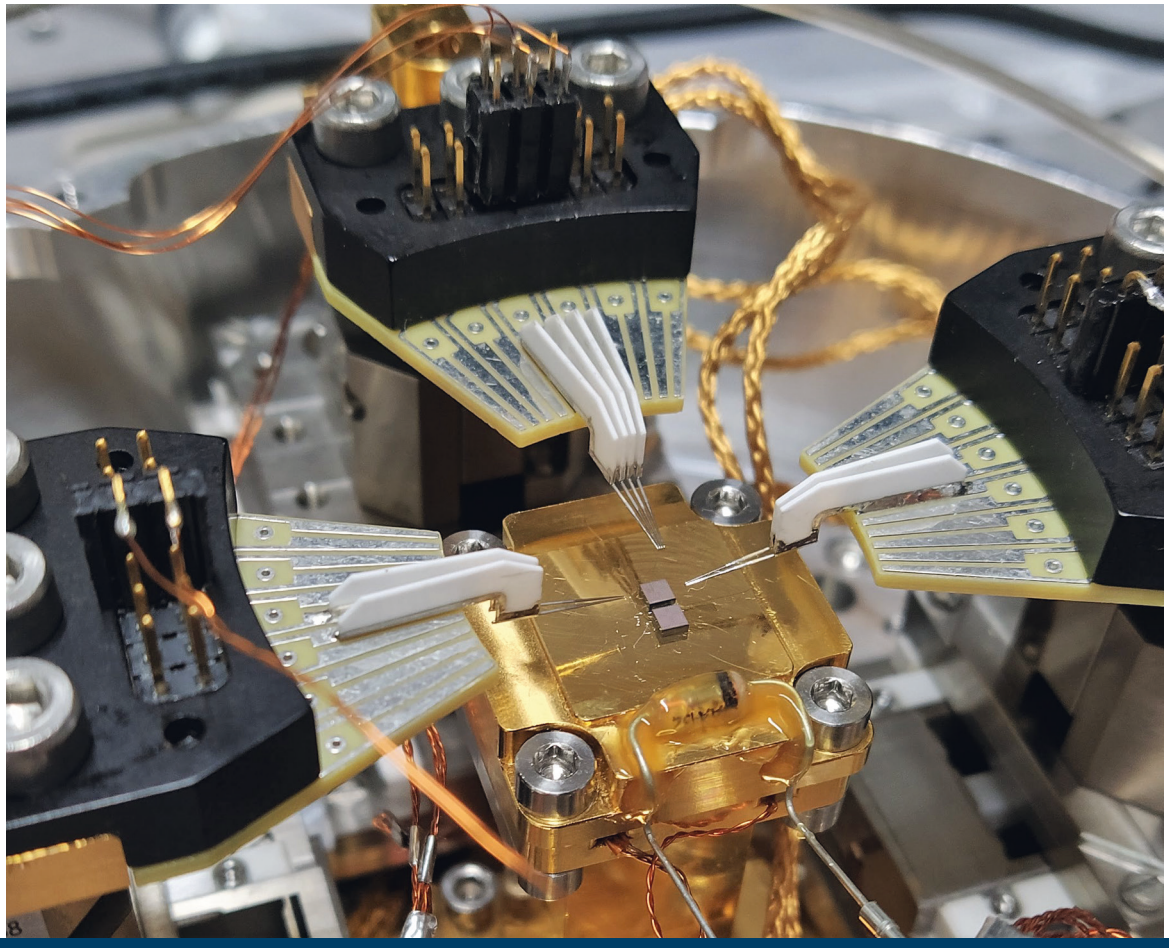

DC and RF characterization of bulk CMOS and FD-SOI devices at cryogenic temperatures with respect to quantum computing applications

Anton Artanov

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Abstract

Quantum computing is a research topic gaining popularity for a few decades, and interest to it significantly increased over recent years. A universal quantum computer is expected to lead to various breakthroughs in science, medicine, and economics. Specific tasks could be solved by a universal quantum computer exponentially faster than by any modern high-performance computer system. Possible applications include search algorithms for unordered databases, improved cryptography methods, protein folding simulations, and quantum chemistry research.

However, most of the proposed quantum processors need to be operated in deep cryogenic temperatures below 1 K. The necessity of millions or even billions of quantum bits for universal quantum computer realization causes various challenges, connected with the requirements for individual qubit biasing, control, and readout, as well as thermal decoupling of the system from the room temperature environment. One of the possible solutions is the development of cryogenic integrated circuitry, being able to perform these tasks directly at the lowest temperature stage. In turn, the design of such circuitry is complicated by the absence of cryogenic models and lack of knowledge in the cryogenic operation of standard complementary metal-oxide-semiconductor (CMOS) technologies.

This work is focused on the cryogenic characterization of single devices, fabricated in 65 nm bulk CMOS and 22 nm fully depleted silicon-on-insulator (FD-SOI) technologies, which are very promising for low-temperature applications according to prior publications in the scientific literature.

First of all, a new cryogenic test setup has been implemented and characterized, according to the requirements for upcoming low-temperature measurements. One of its configurations includes a probe station, that allows performing DC and RF needle probing at temperatures down to 6.5 K and frequencies up to 20 GHz.

Capacitors, diodes, and single transistors, including native transistors, have been characterized in DC at 6.5 K for 65 nm bulk CMOS technology. In the case of 22 nm FD-SOI technology, the main focus was on RF characterization of specially designed transistor array structures. The small-signal equivalent circuit elements have been extracted with measured frequencies up to 20 GHz.

Special attention was given to the cryogenic electro-thermal characterization of transistor-like structures in both fabrication technologies. Self-heating effect for both structures has been investigated. It was shown, that single CMOS devices can heat up locally up to several tens of kelvins. The influence of embedding on thermal behavior has been determined and modeled.

The obtained data prompt the development of new cryogenic electrical and electro-thermal models for modern CMOS technologies, in order to help IC designers in the development of electronics for quantum computing and other cryogenic applications.

Zusammenfassung

Das Quanten-Computing ist ein Forschungsthema, das seit einigen Jahrzehnten an Popularität gewinnt, und das Interesse daran hat in den letzten Jahren erheblich zugenommen. Es wird erwartet, dass ein universeller Quanten-Computer zu verschiedenen Durchbrüchen in Wissenschaft, Medizin und Wirtschaft führen wird. Bestimmte Aufgaben könnten mit einem universellen Quanten-Computer exponentiell schneller gelöst werden als mit jedem modernen Hochleistungscomputersystem. Zu den möglichen Anwendungen gehören Suchalgorithmen für ungeordnete Datenbanken, verbesserte Verschlüsselungsmethoden, Proteinfaltungssimulationen und quantenchemische Forschung.

Die meisten der vorgeschlagenen Quantenprozessoren müssen jedoch bei tief kryogenen Temperaturen unter 1 K betrieben werden. Die Notwendigkeit, Millionen oder sogar Milliarden von Quantenbits für eine universelle Quanten-Computer-Realisierung zu verwenden, bringt verschiedene Herausforderungen mit sich, die mit den Anforderungen an die Vorspannung einzelner Qubits, die Steuerung und das Auslesen sowie die thermische Entkopplung des Systems von der Raumtemperaturumgebung zusammenhängen. Eine der möglichen Lösungen ist die Entwicklung kryogener integrierter Schaltungen, die diese Aufgaben direkt auf der niedrigsten Temperaturstufe ausführen können. Die Entwicklung solcher Schaltkreise wird jedoch durch das Fehlen kryogener Modelle und das mangelnde Wissen über den kryogenen Betrieb von standardmäßigen komplementären Metall-Oxid-Halbleiter (CMOS) Technologien.

Diese Arbeit konzentriert sich auf die kryogene Charakterisierung einzelner Bauelemente, die in 65 nm Bulk CMOS und 22 nm Fully-Depleted-Silicon-on-Insulator (FD-SOI) Technologien hergestellt werden, die nach früheren Veröffentlichungen in der wissenschaftlichen Literatur sehr vielversprechend für Tieftemperaturanwendungen sind.

Zunächst wurde ein neuer kryogener Testaufbau aufgebaut und charakterisiert, der den Anforderungen für anstehende Tieftemperaturmessungen entspricht. Eine der Konfigurationen umfasst eine Probe-Station, die es ermöglicht, DC und RF Messungen mit Kontaktierung per Probing-Nadeln bei Temperaturen bis zu 6,5 K und Frequenzen bis zu 20 GHz durchzuführen.

Kondensatoren, Dioden und Einzeltransistoren, einschließlich nativer Transistoren, wurden in DC bei 6,5 K für eine 65 nm Bulk-CMOS-Technologie charakterisiert. Im Falle der 22 nm FD-SOI-Technologie lag der Schwerpunkt auf der HF-Charakterisierung speziell entwickelten Transistor-Array-Strukturen. Die Kleinsignal-Ersatzschaltbildelemente wurden bei Frequenzen bis zu 20 GHz extrahiert.

Ein besonderes Augenmerk wurde auf die kryogene elektrothermische Charakterisierung von transistorähnlichen Strukturen in beiden Fertigungstechnologien gelegt. Der Selbsterhitzungseffekt wurde für beide Strukturen untersucht. Es wurde gezeigt, dass sich einzelne CMOS-Bauelemente lokal bis zu einigen zehn Kelvin aufheizen können. Der Einfluss der Einbettung auf das thermische Verhalten wurde bestimmt und modelliert.

Die gewonnenen Daten zeigen ein großes Potential zur Entwicklung eines neuen kryogenen elektrischen und elektrothermischen Modells für moderne CMOS-Technologien, um integrierte Schaltungsentwickler bei der Entwicklung von Elektronik für Quantencomputer und andere kryogene Anwendungen zu helfen.

Contents

List of Figures

List of Tables

Acronyms

BNC	Bayonet Neill–Concelman
BOX	Buried oxide
CMOS	Complementary metal-oxide-semiconductor
DAC	Digital-to-analog converter
DC	Direct current
DCO	Digitally controlled oscillator
DUT	Device under test
FD-SOI	Fully depleted silicon on insulator
HPC	High performance computing
IC	Integrated circuit
IV	Current-voltage
LHe	Liquid helium
LN_2	Liquid nitrogen
MFCMU	Multi frequency capacitance measurement unit
MIM	Metal-insulator-metal
MOSFET	Metal-oxide-semiconductor field-effect transistor
NMOS	n-type metal-oxide-semiconductor
PCB	Printed circuit board
PDK	Process design kit
PID controller	Proportional-integral-derivative controller
PMOS	p-type metal-oxide-semiconductor
PTFE	Polytetrafluoroethylene
QC	Quantim computing
qubit	Quantum bit
RF	Radio frequency
RMS	Root mean square
RT	Room temperature
SHE	Self-heating effect
SMU	Source measure unit
SSEC	Small signal equivalent circuit
TDR	Time domain reflectometry
VCO	Voltage-controlled oscillator
VNA	Vector network analyzer

Chapter 1

Introduction

1.1 Motivation

Quantum computing (QC) is a trending topic for the last four decades. The realization of a universal quantum computer is expected to lead to many breakthroughs in science, medicine, and economics. The history of QC started in the 80-s with the works of Paul Benioff [1], who proposed a quantum mechanical model of the Turing machine, as well as Yuri Manin [2] and Richard Feynman [3], who proposed the ideas of quantum computation. Since then, numerous quantum algorithms have been proposed [4] and quantum processors with several tens of qubits have been implemented [5, 6, 7]. In particular, QC could help to improve cryptography systems, machine learning algorithms, and simulations for different kinds of quantum systems. All these kinds of tasks could be solved exponentially faster than by any of the modern high-performance computer systems (HPC), which are not able to solve them from today's point of view.

However, in order to get closer to building a universal quantum computer, significant challenges must be overcome. Most of the proposed quantum bit (qubit) concepts and implementations require deep cryogenic environments for their operation. These conditions are fulfilled by dilution refrigerators, which can provide temperatures as low as few mK. Nevertheless, the cooling power budget of such machines is limited to few milliwatts at 100 mK. Biasing, operation, and read-out electronics of the qubits are usually performed by room temperature electronics, which leads to a huge amount of DC and RF wiring, going all the way from room temperature (RT) to the lowest cryogenic stage. That situation causes high heat flow, making the cooling less efficient, and hinders the opportunity to scale up the system. Like classical computers require millions of bits for proper operation, quantum computers require millions of qubits [8], and this becomes impossible with the current room-temperature electronics approach.

A proposed solution is local classical circuitry, that brings control and read-out to the lowest temperature stage, next to the qubits themselves [9]. This approach requires reliable integrated circuit (IC) technologies, that are able to work at deep cryogenic temperatures. Complementary metal-oxide-semiconductor (CMOS) integrated circuits seem to be a good candidate for this purpose, due to large experience in design and fabrication. First low-temperature measurements of CMOS field-effect transistors (MOSFETs), were published in 1968 [10, 11], and interest in this topic has recently increased due to new cryogenic applications, such as outer-space devices [12, 13], scientific instruments [14] and particularly quantum computing [15, 16].

This work is focused on DC and RF characterization of single devices, fabricated with modern bulk CMOS and fully depleted silicon-on-insulator (FD-SOI) technologies, in a cryogenic environment, as a contribution to the growing global research in this area. It includes building and verification of the measurement closed-cycle cryogenic setup according to the gathered requirements, design of single device test structures, and experiments using a cryogenic needle probing approach. DC, RF, and electro-thermal analysis of the single device structures, including transistors, diodes, capacitors, and self-heating structures, have been performed and the performance of those devices at different ambient temperatures is compared.

1.2 Structure of this work

Chapter 2, following this introduction chapter, introduces quantum computing and reviews the current state of cryogenic CMOS research.

In chapter 3, different approaches for cooling methods are considered and their strengths and weaknesses are discussed. Moreover, gathered requirements for the planned measurements are discussed, the chosen approach for the setup is explained and setup verification results are described.

Chapter 4 describes the chosen 65 nm bulk CMOS and 22 nm FD-SOI technologies, as well as the design of the test chips and approaches taken during the design in order with respect to future measurements.

Chapter 5 presents and compares the results of room temperature and cryogenic DC single device characterization for both technologies, as well as capacitor measurements.

In chapter 6, the cryogenic high-frequency characterization of transistor arrays in FD-SOI technology is described, including small signal equivalent circuit parameter extraction and an attempt of high-frequency noise measurements.

Chapter 7 focuses on the electro-thermal behavior of CMOS devices at cryogenic temperatures and describes the self-heating effect in bulk-CMOS and FD-SOI technologies.

Chapter 8 concludes this work with a summary of the achieved results and outlook.

Chapter 2

Fundamentals

2.1 Quantum computing

Quantum computing is a type of computation that is essentially different from classical computing. It uses the properties of quantum states, such as superposition, interference, and entanglement, to perform calculations. Universal quantum computers, which remain hypothetical at the present time, should be capable of solving certain computational problems exponentially faster than classical computers. Among them are search algorithms for unordered databases [17], improvements in cryptography by the implementation of prime factorization [18], quantum chemistry in catalyst research [19], and protein folding simulations [20].

In this section, the fundamental principles of quantum computing and basic units of quantum information are described.

2.1.1 Dirac notation

Dirac notation, also referred to as bra-ket notation, is usually used for the mathematical description of quantum states in quantum mechanics. Dirac notation describes vectors in a complex Hilbert space [21].

A ket has the form $|V\rangle$. Mathematically it represents a vector v in a complex vector space V, and physically it represents a state of some quantum system. A bra is of the form $\langle f|$. Mathematically it denotes a linear form $f : \mathrm{V} \longrightarrow \mathbb{C}$, i.e. a linear map that maps each vector in V to a number in the complex plane $\mathbb{C}$. Letting the linear functional $\langle f|$ act on a vector $|v\rangle$ is written as $\langle f|v\rangle \in \mathbb{C}$.

A bra vector $\langle V|$ is the adjoint of the associated ket vector, so:

$$|V\rangle = \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} = [v_1^* \; v_2^* \; \cdots \; v_n^*]^\dagger = \langle V|^\dagger \tag{2.1}$$

A quantum mechanical particle is described by the corresponding wave function $\psi(\vec{r}, t)$ in space $\vec{r}$ and time t, which can be determined by the Schrödinger equation [22]:

$$j\hbar\frac{\partial}{\partial t}\psi(\vec{r}, t) = \left[-\frac{\hbar^2}{2m}\Delta + V(\vec{r})\right]\psi(\vec{r}, t) \tag{2.2}$$

2.1.2 Quantum bits

A quantum bit (qubit) is the basic unit of quantum information. Like classical bits, that describe information in a binary numerical system, they have two separate states - "1" or "0". However, classical bits can only take one of these values, while qubits are allowed to be in a coherent superposition of both states simultaneously. This property is fundamental for quantum mechanics and quantum computing.

The wave function $|\psi\rangle$ of a qubit with its two orthogonal basis vectors $|0\rangle$ and $|1\rangle$ can be described as

$$|\psi\rangle = c_0\,|0\rangle + c_1\,|1\rangle\,, \tag{2.3}$$

where c_0 and c_1 are complex coefficients, which satisfy the condition $|c_0|^2 + |c_1|^2 = 1$. $|c_0|^2$ and $|c_1|^2$ can be physically interpreted as the probabilities of the qubit to be projected into one of the states $|0\rangle$ or $|1\rangle$ by a measurement.

2.1.3 Bloch sphere

A common way to represent the quantum state space of a qubit is a Bloch sphere. It can be derived from eq. 2.3, leading to [23]:

$$|\psi\rangle = e^{j\gamma}(cos\frac{\theta}{2}\,|0\rangle + e^{j\phi}sin\frac{\theta}{2}\,|1\rangle), \tag{2.4}$$

where θ, ϕ and γ are real numbers. As the common phase γ does not have observable effects and physical significance, it is neglected. Therefore, eq. 2.4 transforms into

$$|\psi\rangle = cos\frac{\theta}{2}\,|0\rangle + e^{j\phi}sin\frac{\theta}{2}\,|1\rangle\,. \tag{2.5}$$

Hence, the state of a qubit can be reproduced as a point on a three-dimensional sphere, also called the Bloch sphere (Fig. 2.1). However, there are several limitations to this approach, e.g. there is no representation of a multi-qubit system. Nevertheless, it provides an acceptable model for visualization and understanding of single-qubit operations.

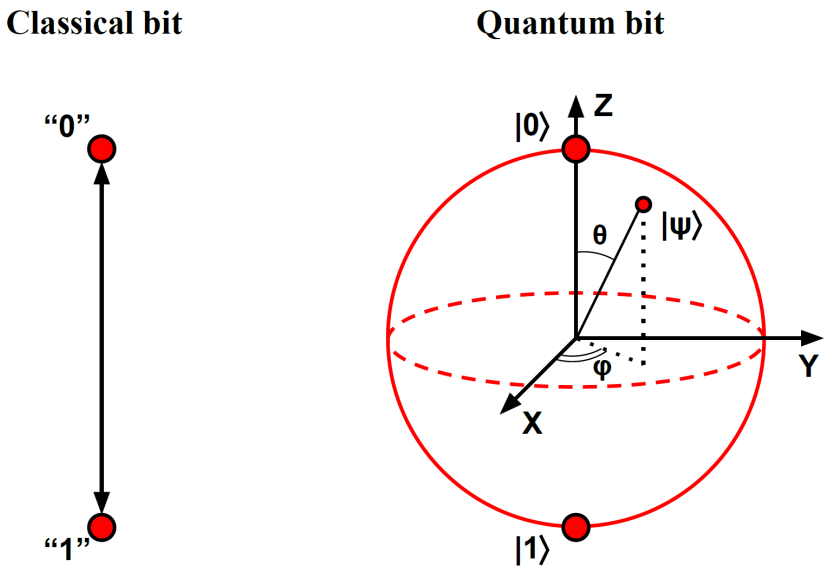


Figure 2.1: Geometric representation of the available states for a classical and a quantum bit.

2.1.4 Quantum computer requirements

The conditions, which are necessary for constructing a quantum computer, were proposed by David DiVincenzo in 2000 [24]:

1. A scalable physical system with well-characterized qubits
2. The ability to initialize the state of the qubits to a simple fiducial state
3. Long relevant decoherence times
4. A "universal" set of quantum gates
5. A qubit-specific measurement capability

These conditions define in an abstract way the requirements for the physical implementation of the qubits, as well as the environmental conditions and infrastructure of a quantum computation device.

A qubit can be physically represented by any two-level quantum-mechanical system, which meets the DiVincenzo conditions. There are several physical principles, based on which two-level systems to various degrees were successfully realized. In trapped ion qubits, the single ions in RF Paul traps are used as quantum bits [25, 26, 27, 28]. By interaction with the laser, the ions can be prepared in a specific qubit state, or be read. Spin qubits use the intrinsic spin degree of single electrons, confined in quantum dots [8, 29, 30, 31, 32]. There are also some implementations of qubits, based on superconductivity effects, like charge or flux qubits [33, 34, 35].

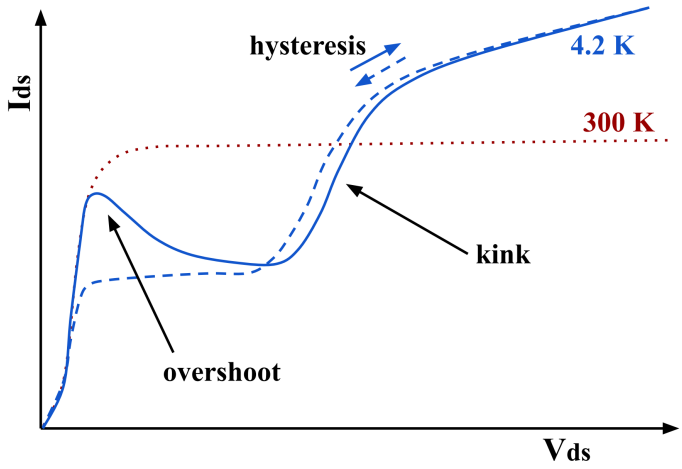


Figure 2.2: Parasitic cryogenic effects in 0.7 μm CMOS. Adopted from [39].

Almost all kinds of qubits must be operated at deep cryogenic temperatures, usually of few hundred millikelvins or even lower. That is needed to protect the state of the qubit from destruction by thermal fluctuations. That necessity also limits the thermal budget of the design of a universal quantum computer.

In order to fulfill the DiVincenzo criteria, millions or even billions of physical qubits are required for a universal quantum computer. Up to 1000 physical qubits are needed per each logical qubit in order to implement error correction schemes [8]. This rises the necessity for local classical cryogenic control electronics to be able to solve scaling challenges, like reducing the number of cables, going from room temperature equipment down to the lowest temperature stage. One of the promising approaches is the use of standard CMOS technologies for the design of custom control electronics, which is able to work at deep cryogenic temperatures close to the operating qubits [8, 9, 36].

2.2 Cryogenic CMOS

Due to the fact, that CMOS technologies are usually not used at cryogenic temperatures, standard semiconductor process design kits (PDKs), are typically provided only for temperatures not lower than - 40 °C. Currently, several scientific groups are performing research in order to provide cryogenic models for standard IC design [37, 38].

In addition to changes in internal parameters, such as threshold voltage V_{th}, transconductance g_m, or subthreshold swing S_{s-th}, the transistor is also subject to some parasitic cryogenic effects. Kink, overshoot, and hysteresis effects appearing in 0.7 μm CMOS at 4.2 K have been shown in [39] in 2009 (Fig. 2.2).

The kink effect is explained by self-polarization due to impact ionization by hot carriers. At room temperature impact ionization is normally able to flow off via the bulk contact of the substrate. However, at cryogenic temperatures, the substrate becomes high-ohmic due to

dopant freeze-out, and it blocks the bulk current flow. This also leads to a shift in threshold voltage V_{th} due to self-polarization-induced bulk-source voltage. In [37] the flatting out in the current jump is explained as an effect of the bulk-source junction diverting most of the current flow and thus gradually saturating bulk current.

The overshoot in the transition of linear to saturation region at temperatures below 15 K is the result of slow ionization processes of the dopants and slow recharging of interface traps at the substrate-to-oxide transition border, hence, delaying the formation of the depletion layer [39, 40].

Measurements of transistor characteristics in CMOS processes of 0.16 µm and 40 nm at 4 K are shown in [37]. The absence of kink behavior is shown for both CMOS processes (thin-oxide FETs in 0.16 µm and all FETs in 40 nm), and only two thick-oxide NMOS transistors show a kink in the I-V curve, which is explained by the fact, that they are very similar to 0.35 μm devices.

The authors further support the statement that the kink is only present in older technologies, i.e. feature sizes larger than 0.35 µm and at temperatures below 100 K. Hysteresis is also only present for thick-oxide FETs in 0.16 µm. According to [37], this effect is insignificant for nanometer nodes, as hysteresis is caused by kink behavior, which leads to the difference of threshold voltage V_{th} during transistor turning on and off.

An overshoot behavior is also not present in modern CMOS technologies, reported in [37, 38].

Cryogenic temperatures also lead to increased carrier mobility in semiconductors, as well as an increase in threshold voltage and steepness of subthreshold slope in CMOS. Carrier mobility increases due to reduced electron-phonon scattering at low temperatures [41], which causes an increase in transconductance g_m [42].

There are different explanations for the threshold voltage increase in cryogenic CMOS. In [37] it is explained by channel dopant freeze-out and according required ionization energy playing a major role. In [42] the authors insist on the temperature dependence of the bulk Fermi potential as well as in the temperature-dependent density of interface traps close to the band edge.

In [43] the authors characterized commercial 40 nm bulk CMOS devices at 50 mK ambient temperature. Classical MOSFET behavior with some cryogenic improvements has been shown. Moreover, some quantum mechanical effects are present, like Coulomb blockade oscillations for low drain-source voltages and close-to-threshold voltages.

Non-planar and non-bulk CMOS technologies, like FinFET [44], 28 nm FD-SOI [45, 46, 47], 22 nm FD-SOI [48], 14 nm SOI FinFET [49], Gate-All-Around Nanowire MOSFETs [50], are also under test at cryogenic temperatures. The opportunity to control the threshold voltage and tune it at cryogenic temperatures is especially promising for FD-SOI processes in terms of a first improving step towards cryogenic IC development [51].

Passive elements, like capacitors and inductors, show only minor changes at cryogenic temperatures [52]. Some resistors, like polysilicon and p-active resistors, also show stable operation over the whole temperature range, while n-well resistors show a huge increase in electrical resistance [16].

One of the issues with the cryogenic behavior of CMOS technologies is the transistor mismatch. It is reported to commonly deteriorate by a factor of 1.2 to 2 [53]. In [54] the authors performed extensive research on the characterization and modeling of mismatch in 40 nm CMOS at cryogenic temperatures. They make a conclusion that the Pelgrom scaling law [55] holds valid also in cryogenic temperatures down to 4.2 K. Current-factor variability increases by 75 % and threshold-voltage variability mostly remains constant. Moreover, the authors use a Croon model to reflect and predict this cryogenic drain current mismatch.

Regardless of extensive cryogenic CMOS research, being performed by many scientific labs all over the world, reliable CMOS device models for such important characteristics as AC-, RF-, and noise behavior at temperatures below 230 K still do not exist. Those characteristics are still subject to an active research and have not been thoroughly investigated yet [56, 57].

Chapter 3

Cryogenic measurement setup

Helium is the chemical element with the lowest boiling temperature of - 4.2 K. It was first liquified by the dutch physicist Heike Kamerlingh Onnes in 1908 [58]. He also used reducing the pressure technique in order to achieve lower temperatures, which in turn led him to the observation of the superfluidic behavior of liquid helium and to the discovery of superconductivity in mercury. These fundamental discoveries brought Kamerlingh Onnes the 1913 Nobel Prize in Physics and opened incredible opportunities for the development of such fields as superconductive electronics and low-temperature physics. Single-photon detectors, magnetic resonance imaging, terahertz receivers, and various quantum bit implementations became possible with further technological development.

In order to develop electronics, which has to work next to the qubit in a quantum computer, single elements should be characterized at temperatures close to the qubit operation environment. The newly-designed integrated circuit (IC) then should be also tested in appropriate cryogenic conditions.

The first step in order to make this dissertation possible was the development and verification of the cryogenic testing environment. That process included gathering the requirements, analysis of the possible solutions, and finally implementing all the ideas into a working cryogenic testing instrument.

3.1 Cooling methods

In this section, various cooling methods would be considered. Here the number of options is limited by the lowest temperature not lower than liquid helium boiling temperature. There are more advanced cooling methods, that can provide lower temperatures, like dilution refrigerators or helium circulation loops, but they are not considered here due to limited setup temperature requirements for keeping handling easy and cost in a reasonable range.

3.1.1 Immersion into a cryogen

This method is the simplest and historically first. The device under test (DUT) is fully immersed in liquid gas and is cooled by convection, happening in the cryogen. Usually, liquid nitrogen (LN_2) (77 K) or liquid helium (LHe) (4.2 K) are used for this purpose.

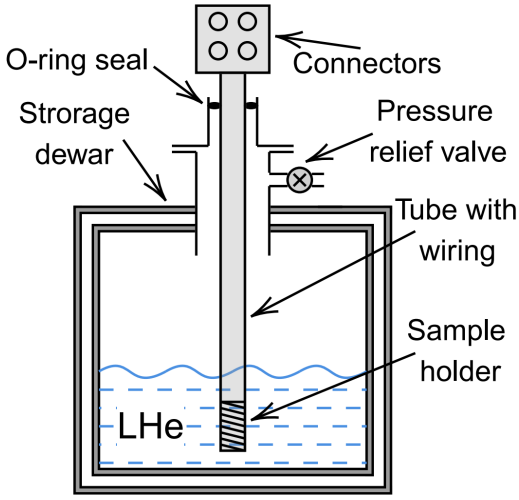


Figure 3.1: Scheme of a dipstick measurement.

Experiments with LN_2 are much simpler. This gas is a main component of the air, so there is no need to build a special infrastructure for collection - it can be collected from the air and liquified. While it needs a special storage vessel - a Dewar flask (often called just "dewar"), the measurement volume with DUT could be less thermally isolated. The drawback is the relatively high boiling temperature and the necessity to have an access to the liquefier or liquid gas supplier.

LHe needs more effort in order to operate it. Apart from the more advanced dewar, which often has a layer of liquid nitrogen in order to block the radiation from the walls, it needs special infrastructure for gas collection, as helium is relatively rare. Moreover, the experiment should be conducted within the storage flask, as LHe evaporates instantly when exposed to room temperature RT.

In order to test the DUT in the storage flask, a dipstick should be designed (Fig. 3.1). Usually it is a tube made of stainless steel, as it has a quite high thermal resistance and mechanical rigidity. On one side of the tube, there is a sample holder with the DUT, on another side – the connectors, and all the needed DC and RF cables are placed inside the tube.

This configuration is quite convenient for small DUTs, that do not require optical accessibility, mechanical stability, or preliminary tests. The cooling power is very high due to full contact with LHe. The consumption of LHe is also lower than during any other method, as there is no need in moving LHe and there is only a small piece of mass that should be cooled down. The measurement speed is a big advantage, as it takes only few minutes to cool down or warm up the DUT. There is also an opportunity to control the temperature by keeping the DUT above the LHe level in the vapors. The method also provides relatively high flexibility, as the dipsticks are easy to design for different required applications.

The drawbacks are the limited size and complexity of the cooled part of the setup: the width of the dewar's neck is usually not more than 12 cm in diameter. This method also excludes most

of the optical, low vibration, needle probing experiments, allowing mostly simple electrical measurements with fixed cabling connections.

3.1.2 Bath cryostat

In order to conduct more complex experiments, bath cryostats are used (e.g. Fig. 3.2).

High vacuum is created inside the cryostat in order to get rid of the convection and frost on the walls of the instrument. LN_2 is needed to create a 77 K stage in order to block RT radiation, make the temperature inside more stable, and slow down the evaporation of LHe. The measured sample in this case is placed in vacuum on a coldplate, which is cooled directly by the LHe.

Bath cryostats provide more space for the DUT and additional needed equipment. The working space is limited mostly by the design of the cryostat. The ability to make optical windows or mechanical positioners allows one to perform experiments in optics or implement moving parts in the setup. The cooling power is mostly limited by the thermal conductivity of the coldplate.

On the other hand, bath cryostats require a turbomolecular pump in order to create high vacuum inside, infrastructure for moving LN_2 and LHe from storage dewars into the cryostat, and collection of the helium gas. Each measurement requires 5-7 liters of LHe. The operation of the cryostat itself requires some expertise as operations with liquid gases are potentially dangerous. Few hours are required to bring the cryostat into operation, as the pumping, filling first with nitrogen and then helium are long processes and require almost constant presence of a specialist nearby. The setup stays cold as long as there is LHe inside, so it limits the measurement time up to 1 day and slows down the warming up if it is needed to be done soon. Temperature control is almost impossible, as any source of heat will significantly increase the LHe consumption.

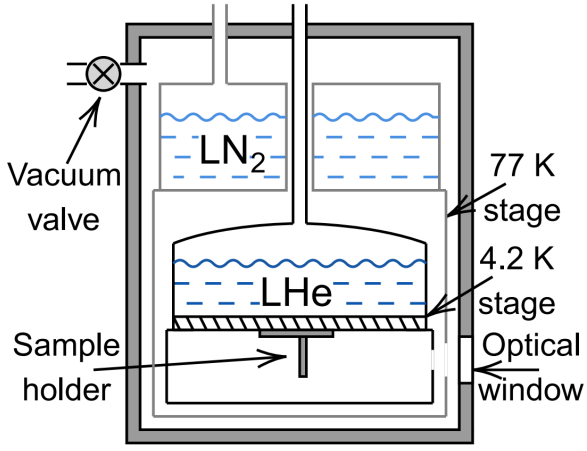


Figure 3.2: Scheme of a bath cryostat.

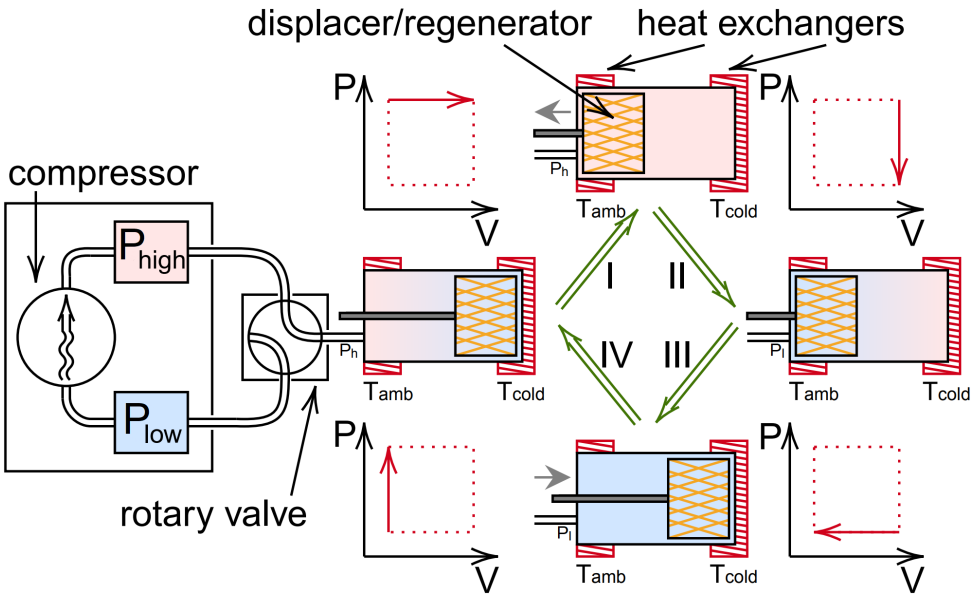


Figure 3.3: Scheme of a Gifford-McMahon cryocooler working principle.

3.1.3 Closed-cycle cryostat

There are several types of closes-cycle cryocoolers, like Stirling [59], Gifford-McMahon (GM) coolers [60], or pulse tubes [61], which work with helium as a working body and provide the temperature of boiling LHe or even lower. As the setup used for this work operates with the GM cycle, the principle of work of this cryocooler is briefly described here.

The principle scheme of a GM-cryocooler is schematically shown in Fig. 3.3. It consists of a compressor, a mechanical switch valve that provides switching between a high-pressure inlet and a low-pressure exhaust, a working cylinder with heat exchangers, a displacer and a regenerator. Often the displacer and regenerator are combined in one component.

The sequence of operation is the following:

I) *High-pressure intake* – The high-pressure inlet is open, warm volume is full of high-pressure gas. The displacer moves to the left of the cylinder, filling the cold volume with high-pressure gas and displacing the gas in the warm volume to the cold volume.

II) *Expansion* – With the displacer at the left of the cylinder, the inlet is closed and the exhaust is open. This produces an expansion of the gas in the cold volume from the high to the low pressure. During this process, the gas that remains in the cold volume is cooled to provide the refrigeration effect.

III) *Exhaust* – With the opened exhaust, the displacer is moved to the right of the cylinder, exhausting all gas from the cold volume and filling the warm volume with low-pressure gas.

IV) *Pressure buildup* – The inlet opens, cold high-pressure gas fills the warm volume.

Closed-cycle systems are easier to operate, as the whole process of cooling down can be automated. They do not require liquid gases or special infrastructures, except electricity and often water cooling for the compressor. The duration of the experiment is not limited.

The main drawbacks are large electrical power consumption and a relatively long time of cooling down. The cooling power is also much lower than that of bath cryostats.

3.2 Requirements

In order to make a decision on the setup design, the requirements for planned test cases should be gathered during the discussions with all the future users of the setup, understanding the needs for their experiments, explanation of the features and challenges during cryogenic measurements. As a result, detailed plans for future measurements have been developed and the list of minimum requirements for different test cases has been completed (table 3.1).

The first requirement, that would narrow out the options, is the temperature. Several preliminary measurements and later more detailed research [38, 62, 63] showed that the most drastic changes in semiconductor structures in modern technologies are happening at temperatures above 10 K. That means, that the tests done at 10 K should show almost the same result as those at lower temperatures. This fact led to the decision to aim for LHe temperature setups, as they are simpler and much cheaper than those for lower temperatures.

There were various tasks, required to be solved by the cryogenic setup. First of all, the designed and fabricated integrated circuits, like DC and pulse digital-to-analog converter (DAC), voltage-controlled oscillator (VCO), or digitally controlled oscillator (DCO), should be measured at the lowest temperature. This test case usually implies the packaging of the IC, placing it on a printed circuit board (PCB) with the following wire connections with soldering or pin headers. Although, due to the required big amount of DC and RF wiring, this test case is quite simple, as it does not require any moving parts or optical access, and it can be implemented in any of the above-described cryostats.

The second test case is much more challenging: the DC and RF characterization of single devices. That means that the single CMOS devices should be separately designed with their terminals connected to the pads for bonding or needle probing. Metal wire bonding would be a sufficient and quite simple solution for DC characterization, while proper RF characterization with de-embedding and parasitic extraction requires RF-needle probing.

While the first test case can be done with a dipstick technique, the needle probing station can be based only on a bath or closed-cycle cryostat. Taking into account, that the lab does not have LHe infrastructure and low power requirements for the electronics, the preference should be given to closed-cycle ones.

Ready solutions for needle-probing, based on any of the principles, are already available on the market. At the same time, the working area of such solutions is intended only for wafer probing, there is no space for PCB mounting, and that makes it impossible to perform the first test case.

Definition	Requirement
Minimum temperature	10 K
Cooling power	>100 mW
Coldplate size	70 x 70 mm^2
DC-cable resistance	<100 Ω
RF-cable chain attenuation	<10 dBm
RF-cable impedance	50 Ω
Microwave signal frequency	20 GHz
Cryogenic RF probe positioners	3 pcs
Travel range X x Y x Z	10 x 10 x 5 mm^3
Size of a single sample	2x2 mm^2
1.1. DCDAC	
Number of DC-cables	35 pcs
Number of coaxial cables	0 pcs
1.2. PulseDAC	
Number of DC-cables	22 pcs
Number of coaxial cables	1 pcs
1.3. VCO	
Number of DC-cables	15 pcs
Number of coaxial cables	2 pcs
1.4. DCO	
Number of DC-cables	12 pcs
Number of coaxial cables	2 pcs
2.1 Needle probing	
Number of DC-cables	10 pcs
Number of coaxial RF cables	2 pcs

Table 3.1: List of the test cases and requirements.

Moreover, a cryogenic setup is always a big investment in the lab, and it is always planned to use for several years or even decades. From that point, it is unreasonable to buy the instrument only for current activities - it should be flexible enough to be transformed into another setup for other possible future test cases.

Therefore, a new cryogenic instrument should be designed to be efficient enough to fulfill the current requirements and needs, and flexible in order to be adjusted for future applications.

Based on those requirements, the basic concept was developed, and after some discussions and negotiations, was implemented by engineers of the company attocube systems AG, based on the attoDRY800 instrument [64].

3.3 Setup description

attoDRY800 is a GM-based cryogenic setup, mounted into an optical table (Fig. 3.4). The black box is a vacuum shroud. There is an optical window on top of it, so the microscope can be used to control the position of the probes.

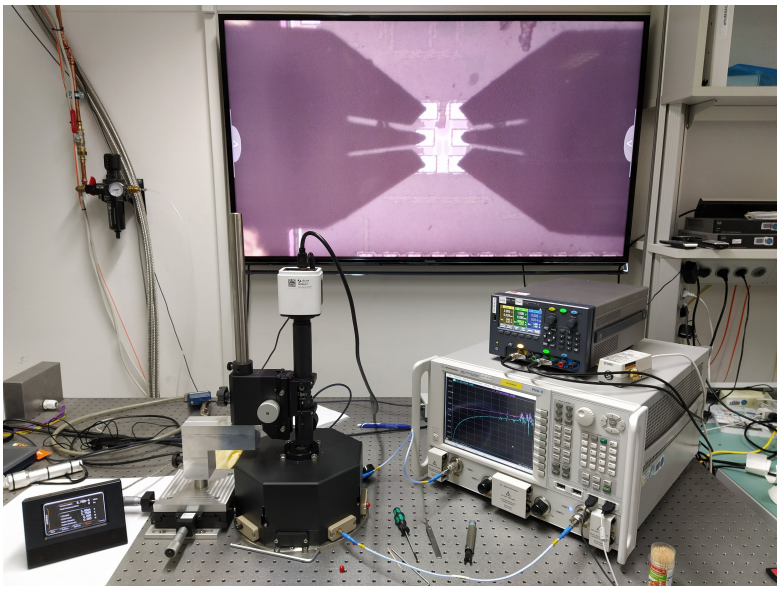
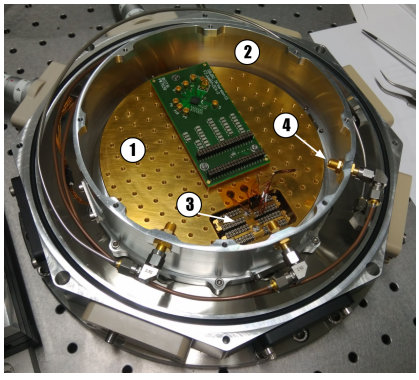
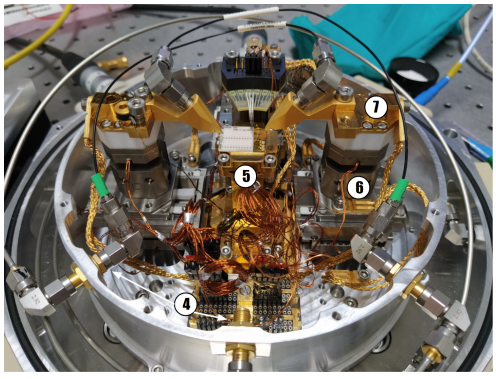


Figure 3.4: Photo of the cryostat in operation.



(a) all-purpose



(b) probing station

Figure 3.5: Two configurations of the cryosetup. 1 – coldplate on a 4 K stage, 2 – 60 K stage, 3 – DC connections, 4 – RF connections, 5 – sample holder on a 4 K stage, 6 – XYZ-stack of piezo-positioners, 7 – probe holder.

The setup has two cold stages (Fig. 3.5). The 60 K stage (2) has aluminum parts connected to it, so almost all the parts with gray color are at around 60 K. The 4 K stage (1) has copper parts, plated with gold, so all the "golden" parts are at around 4 K. According to the requirements, described in the previous section, it has two configurations: all-purpose cryostat (Fig. 3.5a) and probing station (Fig. 3.5b). The configurations are easily exchangeable, depending on what is needed during the experiment.

Setup (a) has a 15 cm diameter coldplate for PCB or any other cryogenic equipment. 3 – are pin headers, which are connected to 60 DC lines. All the lines are thermalized as each cold station by copper bobbins. 4 – are 3 K-connectors of the RF lines, which are thermalized at 60 K.

Setup (b) has a sample holder tower (5), where the sample can be mounted by thermally conductive glue. 3 XYZ-stacks of piezo-positioners (6) are attached to the 60 K stage. They use the stick-slip movement technique [65], which allows them to move even in a cryogenic environment. Probe holders (7) are attached to the positioners with a layer of PTFE in order to thermally isolate them. Copper braids are used to thermally connect the holders to the 4 K stage in order to bring their temperature closer to the sample one.

Any type of needle probes, that would fit the holder and dimensions of the setup, can be used for the measurements. Depending on the type and the measurement, it can be either connected with thin DC cables to the DC pin header or with flexible RF cables to one of the RF connectors.

The setup was modified according to the developed concept and has been never tested before. Therefore, some challenges were still to be solved after the installation.

First of all, the implemented stacks of piezo-positioners have not been used for needle probing before, therefore some time has been spent on the development of reliable measurement procedures. That was complicated by the stick-slip movement approach of the positioners. They provide smooth movement: one step during the stick phase is approx. 1 μm, the moving back during the slip phase can't be noticed in the microscope. That worked for rigid RF probes, however, 1 cm long DC probes might have the self mechanical frequency close to the moving one, causing the resonance and uncontrolled shaking of the needle during movement. That challenge was solved by tuning the moving frequency away from the resonance peak.

Another challenge was connected with the RF cables, which connect the 60 K stage and the RF probes. The application requires them to have low insertion losses and high thermal resistance, to be applicable for vacuum and cryogenic measurements, to be mechanically flexible at cryogenic temperatures, and to have stable RF parameters versus bending. The solution to that challenge is described in section 3.4.3.

3.4 Setup characterization

3.4.1 Thermal properties

Cooling down time is defined as the time from pressing the "base temperature" button to the achievement of the lowest possible temperature. It includes vacuum generation from

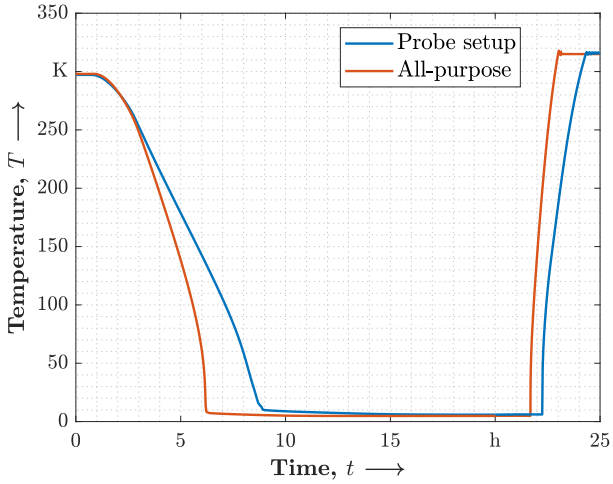


Figure 3.6: Full thermal cycle curves.

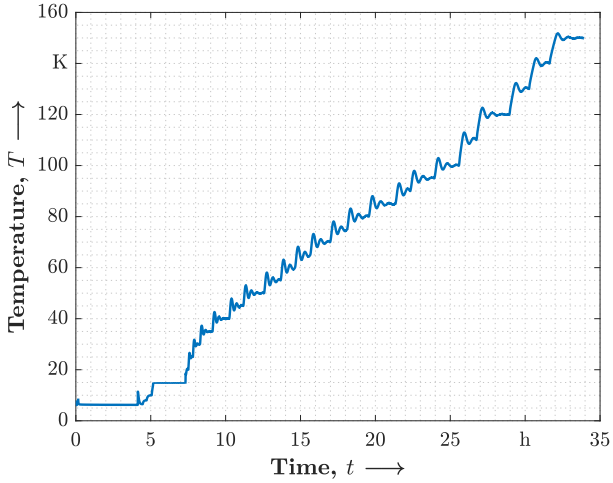


Figure 3.7: Temperature sweep curve.

atmospheric pressure down to 10^{-3} mbar and the process of temperature decrease. Warming up is the time from pressing the "sample exchange" button to the ability to open the cryo-chamber. Both of the processes are performed automatically, and that allows to perform cooling down during the night.

The temperature versus time curves for the whole cycle for both configurations are shown in Fig. 3.6. As the configurations have different thermal capacitance, the cooling down and warming up times are different. A lot of electrical wires also provide some thermal connection, which leads to the increase of the lowest temperature. As the positioners in the probing setup are connected to the 60 K stage, they have additional thermal links to the 4 K stage through

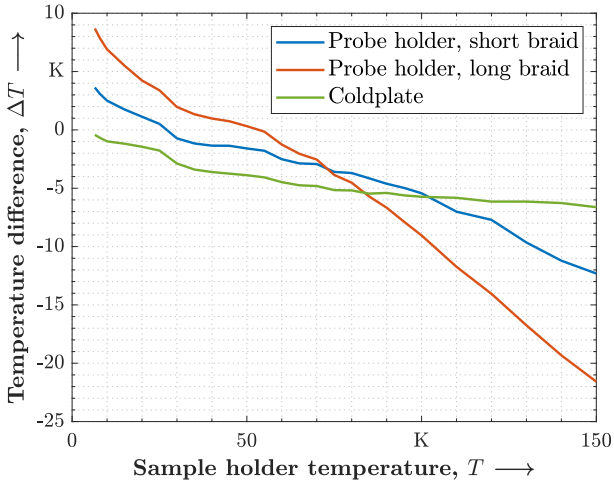


Figure 3.8: Temperature difference between the sample holder and other setup elements.

the cabling for the positioner drive and isolation under the needle holder. That increases the lowest possible temperature for this configuration by approx. 1 K.

For the all-purpose setup, it takes ca. 1 h to create the vacuum, then ca. 6 h to go below 10 K, and then ca. 5 h to go to the lowest possible 5 K. For the probing configuration, these numbers are 1 h, 9 h, 6 h, and 6 K, respectively. In order to increase the warming up an additional heater of 15 W is used. For the all-purpose and probing setup, the warming-up times are 2 h and 3 h, respectively.

The sample holders in both setups have the ability to vary the temperature with the use of a heater with max. 5 W, temperature sensor and proportional-integral-derivative controller (PID controller). The highest achievable temperature for this case is 150 K, but it can be improved up to room temperature (RT) with the use of an additional heater, helping the PID-controlled heater at higher temperatures. The temperature curve for a temperature sweep measurement is shown in Fig. 3.7. The temperature stabilization takes from several minutes below 20 K up to two hours at 120 K and higher. Ideally, this can be improved with PID values optimization at each temperature, but the tuning itself would take a huge amount of time, so it was decided to leave the values constant.

In order to bring the temperature of the probing needles closer to the temperature of the sample, the probe holders are thermally isolated from the positioners and connected to the 4 K stage with copper braids, although there is always a small difference in temperature between them. The thermal interactions become more complicated when the temperature sweep is performed: all the needle holders are connected with short or long copper braid, depending on the place of the stack, to the coldplate, where the sample holder tower is mounted. At the same time, the heater is placed close to the sample area, therefore the temperature increase there is higher than the temperature increase of the coldplate. As a consequence, the probes have higher temperatures at sample holder temperatures below around 50 K and lower temperatures as the base temperature increases (Fig. 3.8).

The estimation is that this temperature difference is negligible for the proposed measurements. The needle contact area is a few μm^2 for DC and a few tens of μm^2 for RF probes, which is much smaller than the coldplate contact area of a few mm^2, so in combination with the temperature difference that would provide a minor influence. Quite complicated local temperature behavior of the devices (see chapter 7) should be also taken into account.

3.4.2 DC properties

The cryosetup has 60 thermalized DC connections. From room temperature shroud down to the lowest temperature stage thin copper wires (30 twisted pairs) are used. They go through two bobbins, placed at both temperature stages of the cryostat in order to thermally isolate all the stages via proper cable thermalization. The connection of the measurement instruments to the DC lines is made via a breakbox with 30 bayonet Neill-Concelman (BNC) connectors, each providing 2 DC connections. The breakbox and the vacuum shroud are connected by twisted pair cables with Fischer connectors.

The whole chain of the wires provides a low resistivity connection of approx. 3 Ω. During the needle probing with multi-needle wedges fabricated by GGB industries, Inc. [66], on the aluminum pads, the measured contact resistance is approx. 1 Ω. As further measurements show, the current measurement limit is better than 1 nA.

3.4.3 RF properties

The instrument has 3 radio frequency (RF) lines. Semi-rigid coaxial cables (ULT05 by Keycom) are used between RT and 60 K stage, connected to both of them with feedthrough K-connectors. They are 45 cm long and made of stainless steel in order to reduce thermal conductance between the stages. This combination has only 2 dB attenuation at 20 GHz at RT.

Finding the proper RF cables to connect the 60 K stage connector and the needle probes was a challenge. Such cables should provide excellent high-frequency parameters, work at cryogenic temperatures, be flexible in order to be moved by the positioners, and be stable in terms of RF parameters in order to provide accurate measurement results.

There might be two approaches to that issue. The first one is a microstrip line on a flexible PCB. Usually, they are designed by research groups themselves, but there are also commercial options available (e.g. Cri/oFlex 2 DelftCircuits [67]). Although they have excellent flexibility, stability versus bending and almost negligible thermal conductivity, it is very difficult to match the connector and the line. Therefore, the S_{11} parameters of such cables are usually higher than -10 dB, hence, it is very difficult to use them for accurate device characterization. They also have high attenuation due to the nature of microstrip lines. Another approach is thin and flexible coaxial cables (e.g. StormFlex series from Teledyne Storm Microwave [68]). They have higher thermal conductivity and are sensitive to bending, but provide more adequate RF performance.

The test of several cable options has been performed. It was observed, that thinner cables provide better stability to bending than the thicker options: that happens due to smaller relative deformation in thin flexible cables compared to the thick ones. The aim was to find a

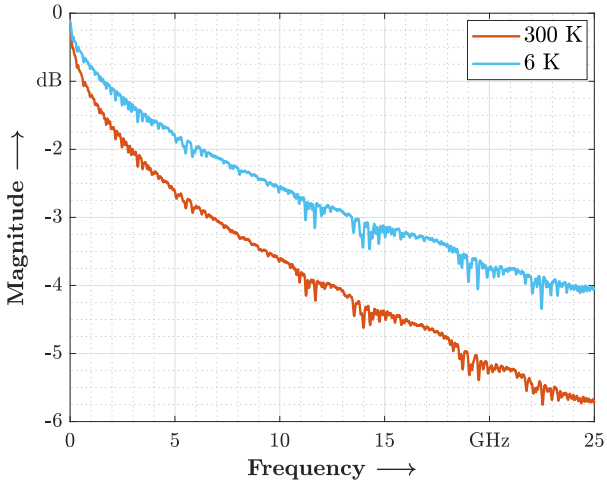


Figure 3.9: Insertion loss of the full RF chain from the connector on the vacuum shroud to the probe tip at 300 K and 6 K.

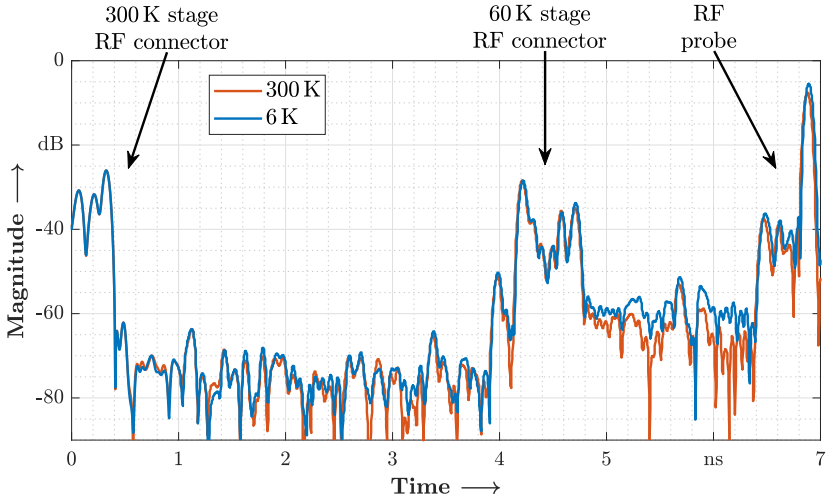


Figure 3.10: TDR measurements of the full RF chain from the connector on the vacuum shroud to the probe tip at 300 K and 6 K. Probe tip is open.

balanced option: thin enough to be flexible at cryo and stable to bending, but thick enough to have small insertion loss. Thermal conductivity also decreases with cable diameter. Using thermally low-conductive stainless steel as the main material for the cable makes the diameter requirements more relaxed.

The final choice was 21 cm long StormFlex034 cables [69] made of stainless steel. Due to the material and length, no influence on the probe holder temperature has been observed.

By forming a big loop (Fig. 3.5b) and due to the small thickness, it was possible to minimize the internal geometry changes, so the parameters kept stable during the positioner movement.

For RF probing |Z|-probes from Cascade Microtech [70] are used. The probes themselves, as well as calibration structures for them, are characterized down to cryogenic temperatures and have stable characteristics over the whole range. According to the specification, they provide a low insertion loss of 0.5 dB at 20 GHz and return loss better than 20 dB.

The measured S-parameters of the whole chain of several adapters, semi-rigid cable, flexible cable, and the probe are shown in Fig. 3.9. They are measured by the connection of the needles to the THRU calibration structure and gathering of the whole chain from one RF connector on the vacuum shroud to another one. As the chain in that case is symmetrical, the result is divided by 2. The insertion loss becomes smaller with a temperature decrease.

In order to characterize matching along the chain, time domain reflectometry TDR has been performed at 300 K and 6 K (Fig. 3.10). Both results show sufficient matching quality, with relative magnitudes of the reflected signal being below -25 dB at any RF connection.

3.4.4 Conclusions

During this stage of this project, a new cryogenic test setup was implemented and characterized. The flexibility and simplicity of modification of the setup allow performing a wide range of measurements. The requirements gathered for all the test cases are fulfilled (Table 3.2).

Personal contribution includes gathering the requirements and test cases, analysis of possible options and proposal of the setup concept, the test of several probing and cabling options in order to achieve the best DC and RF probing results as well as setup verification and measurement procedures development.

Definition	Requirement	Specification
Minimum temperature	10 K	6 K
Cooling power	>100 mW @ 10 K	≈ 1 W @ 10 K
Coldplate size	70 x 70 mm^2	ø15 cm (100 x 100 mm^2)
DC-cable resistance	<100 Ω	<5 Ω
RF-cable chain attenuation	<10 dB	<6 dB
RF-cable impedance	50 Ω	50 Ω
Microwave signal frequency	20 GHz	potentially up to 40 GHz
Cryogenic RF probe positioners	3 pcs	3 pcs
Travel range X x Y x Z	10 x 10 x 5 mm^2	20 x 20 x 5 mm^2
Area of sample holder	2x2 mm^2	20x20 mm^2
Number of DC-cables	35 pcs	60 pcs
Number of coaxial cables	3 pcs	3 pcs

Table 3.2: Comparison of the requirements and instrument specification.

Chapter 4

Test devices design

The metal-oxide-semiconductor field-effect transistor (MOSFET) was invented by Mohamed M. Atalla and Dawon Kahng at Bell Labs in 1959 [71, 72]. A year later they demonstrated n-type metal-oxide-semiconductor (NMOS) and p-type metal-oxide-semiconductor (PMOS) fabrication processes. These processes were combined by Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor into a complementary metal-oxide-semiconductor (CMOS) process in 1963 [73]. Just a year later, in 1964, General Microelectronics introduced the first commercial MOS integrated circuit [74].

Since then, with the improvement of the fabrication processes, decrease in the sizes of the devices, and the creation of new advanced architectures, CMOS-based electronics has become an essential part of our lives. The availability and reliability of modern integrated circuits make them excellent candidates for electronics in quantum computers.

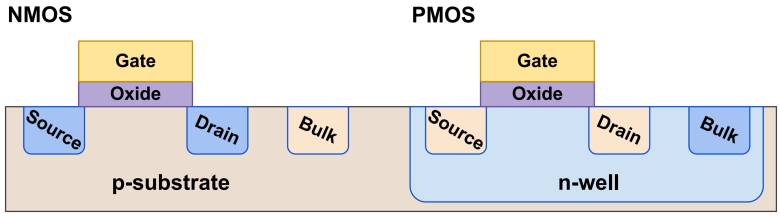
In this chapter, the choice of fabrication technologies for qubit control is explained and the device-under-test (DUT) design is described.

4.1 Fabrication technology choice

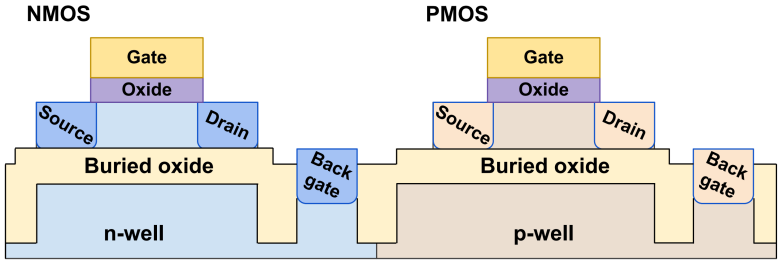
As discussed in previous chapters, cryogenic temperatures can be beneficial and disadvantageous for MOSFETs. Modern technologies with smaller nodes – less than 100 nm – show fewer cryogenic side effects [37].

Following this information, 65 nm bulk CMOS technology was chosen for the first generation of samples (Fig. 4.1a). It is a good compromise between the performance of digital as well as analog components and it allows us to minimize undesirable cryogenic effects. Two tapeouts have been performed using this technology: SQuBiC1 [75] with DC and RF digital-to-analog converters (DACs), as well as a digitally controlled oscillator (DCO) and a voltage-controlled oscillator (VCO), and SQuBiC2 - for single devices characterization.

Another technology, promising for cryogenic applications, is 22 nm fully depleted silicon on insulator (FD-SOI) (Fig. 4.1b). Due to a layer of buried oxide (BOX), the leakage current into the substrate should be much lower, hence, the power dissipation in the device decreases. BOX also reduces parasitic gate-bulk and drain-bulk capacitances, and that lowers the power consumption for the same operating frequency. Moreover, there is an opportunity to apply a back-gate voltage, that allows to shift the single device threshold voltage and tune it closer



(a) bulk CMOS



(b) FD-SOI

Figure 4.1: Schemes of MOSFETs in two technologies, used in this project.

to the room temperature one. That would significantly improve the capability of the circuit design for cryogenic electronics and decrease the power dissipation in the circuit.

4.2 SQuBiC2 – 65 nm bulk CMOS

The first tapeout for single device characterization was made in a 65 nm bulk CMOS technology. It was called "SQuBiC2" and consisted of two variants of dies, 2 x 2 x 0.8 mm^3 each. Both of them had more than 160 aluminum pads for DC needle probing, which were connected to the terminals of different single devices (Fig. 4.2), like transistors of different types and sizes, capacitors, diodes, resistors, and special self-heating structures. Each pad has 70 x 70 μm^2 dimensions, with a 70 μm distance between each of them. This pad configuration requires multi-needle DC probes with 140 μm pitch.

This design would allow the characterization of a big variety of devices separately from each other, using as small wafer area as possible. The lines from the pads to the devices' terminals are designed in a similar way with the same length and width, in order to simplify the measurements themselves and possible further parasitic extraction. The list of the device types is the following:

- MIM Capacitors – There are 3 metal-insulator-metal (MIM) capacitor structures, which have the same effective area: C1 – 1x 44.36 x 44.36 μm^2, C2 – 4x 22.18 x 22.18 μm^2 and C3 – 16x 11.09 x 11.09 μm^2. This difference was established in order to test the change in perimeter capacitance due to edge-to-edge effects.

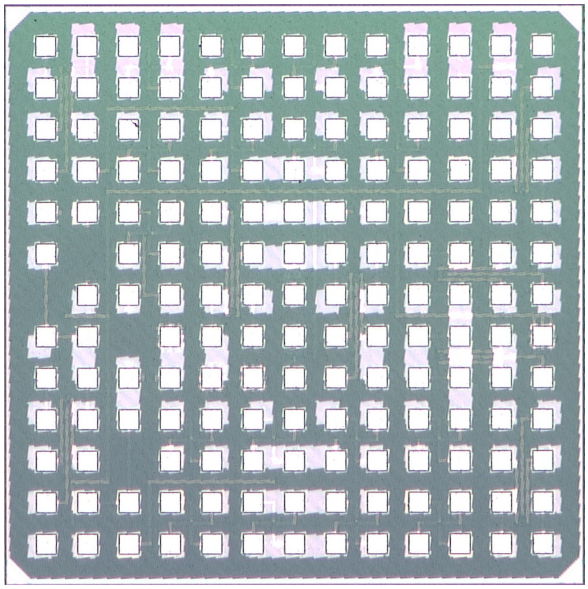


Figure 4.2: Photo of the SQuBiC2 chip, fabricated in 65 nm bulk CMOS technology.

- Diodes – There are 11 diode devices included in the design. They can be categorized into two groups: N-type diffusion inside substrate-based diodes (n-type diodes) and P+ diffusion inside N-well-based diodes (p-type diodes). All the devices have the same dimensions of 7.98 x 7.98 μm, the difference is in the type of the device.

- Transistors – 44 different transistor structures have been put on SQuBiC2 chips. They include core devices, IO devices, and native devices of several widths and lengths. The native devices are available only in an n-type variant, others have n- and p-type variants.

- Self-heating structures – Several wide and short transistor-like structures with 4 gate connections. Using 4-wire measurement the gate polysilicon resistance is measured and this value is calibrated on the ambient temperature, in order to perform local temperature measurement during transistor operation (chapter 7).

- Resistors – Several design types and sizes of polysilicon resistors.

- Metal lines – Several metal lines on different metal layers and of different lengths.

- Open and short pads – A set of opened and shorted pairs of pads were added in order to perform a de-embedding routine.

Not all of the devices, available on the chip, have been considered in this work. The exact device dimensions of most of the devices cannot be given due to non-disclosure limitations.

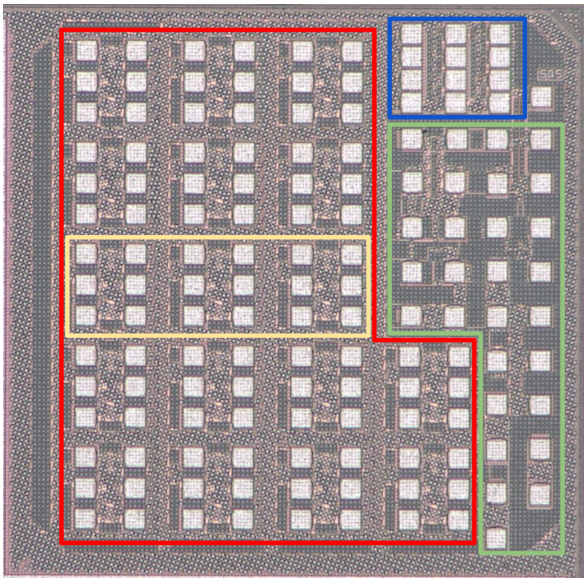


Figure 4.3: Photo of the SQuBiC5 chip, fabricated in 22 nm FD-SOI technology.

4.3 SQuBiC5 – 22 nm FD-SOI

The chip named "SQuBiC5" in 22 nm technology was designed in order to characterize single devices used for the latest generation of chips (Fig. 4.3). It is smaller than the previous one - only 1.4 x 1.4 x 0.25 mm^3.

Besides some chosen DC structures, most part of its area is used for structures for RF characterization up to 20 GHz. These structures have 6 pads, which can be connected with two Ground-Signal-Ground (GSG) probes from two opposite sides corresponding to the gate-source and drain-source ports of the transistors. The sizes of the structures are much smaller than the wavelength of the RF signal ($\approx$ 1.4 mm in silicon).

All the RF structures have as similar configurations of the pads and all the lines as possible for accurate de-embedding of the gathered data. Even the metal filling inside these structures, which is needed for the density requirements of the technology, is designed in the same way for all the structures.

Within the blue area, there are pads for the back gate, deep n-well, and substrate contacts. They are shared between all the devices on the chip, including RF and DC structures, in order to reduce the area occupied by each device. These pads are contacted by a separate DC-needle wedge from the top.

Within the red area in Fig. 4.3 there are 17 structures for RF needle probing. 13 of them are transistors, connected in parallel and forming arrays of 10. 4 of them are p-type and n-type thick oxide devices of two sizes. The other 9 are 3 different sizes of p-type low threshold voltage (V_{th}) transistor arrays, 3 different sizes of n-type low V_{th} transistor arrays with back gate terminal on a separate pad, and 3 same n-type transistor arrays, but with the back

gate connected to the ground (GND) terminal by a metal line on the chip. The gates of the devices are connected to the left signal pad and the drains - to the right ones. The sources are connected to the ground pads, which are then connected to the ground via a GSG probe.

While the source of an n-type device should be connected to the ground, the source of the p-type device should be connected to the positive voltage. That is not possible with the current configuration, as the ground needles of a GSG probe are connected to the ground of the setup. Instead, during the measurement, the voltages at all the other terminals - gate, drain, back gate, deep n-well as substrate – are reduced by the same value, which is equivalent to relative source voltage increase.

The exact device dimensions of the devices cannot be given due to non-disclosure limitations. For RF structures, 3 different size values have been used. The smallest one has a width W of 2.4 μm. The medium one has a 2 times larger length and $W = 4.8$ μm, hence, 4 times larger area. The large one has a 4 times larger area, than the medium one, $W = 9.6$ μm.

Within the yellow area, three de-embedding structures are placed – THRU, OPEN and SHORT. They fully reproduce the pads and metal lines of other RF structures, allowing the extraction of the parasitic capacitance of the pads (OPEN), as well as the series resistance and inductance of the lines (SHORT).

The devices are used in arrays in order to improve the accuracy of the measurement. The capacitances of the CMOS transistors are usually on the order of few fF, while the pad capacitance is more than 50 fF. Connecting them in parallel would increase total capacitance, improve the matching between the line and DUTs and make the parameter extraction simpler. The resulting parallel capacitances and transconductances should later be divided by 10 and parallel resistances and inductances multiplied by 10 in order to achieve the parameters of a single device.

The RF pads have 50 x 50 μm^2 dimensions with a 20 μm distance between them. The back gate, deep n-well, and substrate contacts have the same dimensions and a 50 μm distance between them. That requires RF probes with a 75 μm pitch and multi-needle DC probes with a 100 μm pitch.

The green area consists of a few DC structures, including some single n-type and p-type thick oxide transistors, a structure for self-heating effects investigation (presented in chapter 7), and other DC structures, which are not considered in this work.

4.4 Conclusions

Two chips for single device characterization in two different technologies - 65 nm bulk CMOS and 22 nm FD-SOI have been designed and taped out. The design was performed in accordance with the planned tests, which later have been successfully conducted.

Personal contribution includes participation in SQuBiC2 layout and deep involvement in SQuBiC2 RF part design, layout, and tapeout process under IC designer supervision.

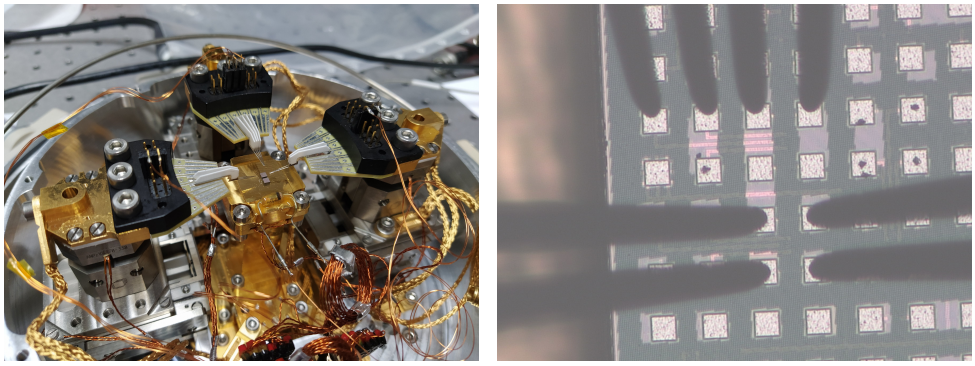
Chapter 5

DC characterization of single devices and capacitance measurements

5.1 Experiment description

The needle probing setup, used in this experiment, is described in section 3.3.

Multi-contact wedges, designed by GGB company, with a different number of needles (from 1 to 4) and pitch sizes (from 100 μm to 140 μm), depending on the measured device and distance between pads (Fig. 5.1), are used. These wedges are connected by thin copper cables with varnish isolation to the DC connectors of the setup. In the case of capacitance measurements, the same needles are used, but the wires are connected to RF connectors, in order to use well-shielded coaxial cables.



(a) photo of the setup (b) microscopic photo

Figure 5.1: Photos of the DC probing configuration.

The Keysight B1500A Semiconductor Analyzer instrument is used in order to perform all the measurements of this chapter. It has 5 source measure units (SMU) for precise voltage or current supply and measurement, as well as a multi-frequency capacitance measurement unit (MFCMU) for capacitance measurements.

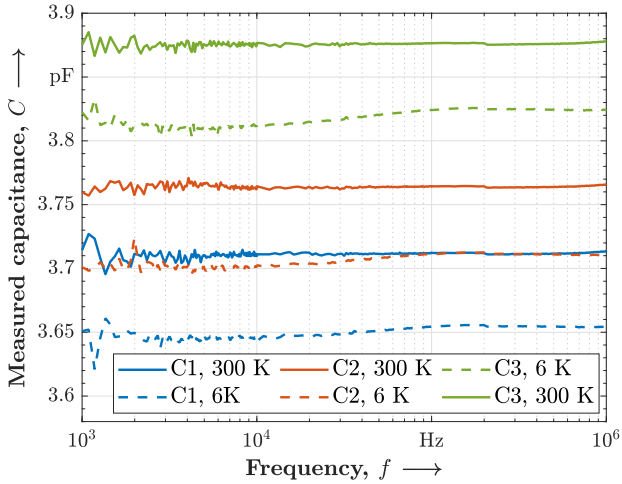


Figure 5.2: The results of the capacitance measurements at 300 K and 6 K, 65 nm bulk CMOS technology.

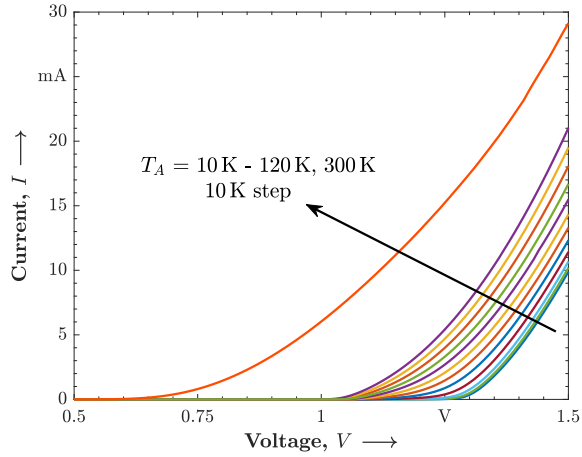
5.2 65 nm bulk CMOS MIM capacitors

The DUTs for capacitance measurements and pads for de-embedding are placed on the SQuBiC2 chip (section 4.2). There are 3 devices with the same effective area, but different perimeters (section 4.2): C1 – 1x 44.36 x 44.36 μm^2, C2 – 4x 22.18 x 22.18 μm^2 and C3 – 16x 11.09 x 11.09 μm^2. The nominal design value is 4 pF.

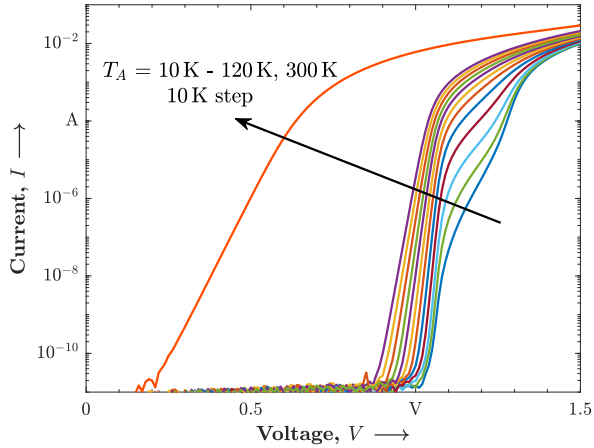
A multi-frequency measurement from 1 kHz to 1 MHz, using the MFCMU is performed. The measurement signal level is 50 mV root mean square (RMS). Calibration is done on the open pads of the chip, in order to de-embed pad, cable, and any other capacitances, except the measured one.

The results of the measurements are presented in Fig. 5.2. Indeed, the increase in perimeter length leads to an increase in total capacitance, although the difference between C1 and C3 is only 5.5 %. At the same time, the value of C1 is 7.5 % less, than nominal due to process variations during fabrication.

After cooling down to 6 K, all the devices show a decrease in capacitance by about 50 fF. All the cryogenic curves also show slight frequency dependency. Nevertheless, the temperature-dependent change is only approx. 1.5 %. Thermal contraction from 300 K to 6 K is less than 1 % for silicon and all common metals [76, 77], and permittivity change is less than 2 % [78], so a 1.5 % change in capacitance is reasonable. It is smaller than process variations and shouldn't significantly influence the IC design procedure and can be easily foreseen during the design phase.



(a) linear scale



(b) logarithmic scale

Figure 5.3: Measured IV characteristics for an n-type diode at different temperatures.

5.3 65 nm bulk CMOS diodes

The diode samples, measured in the framework of this chapter are briefly described in section 4.2.

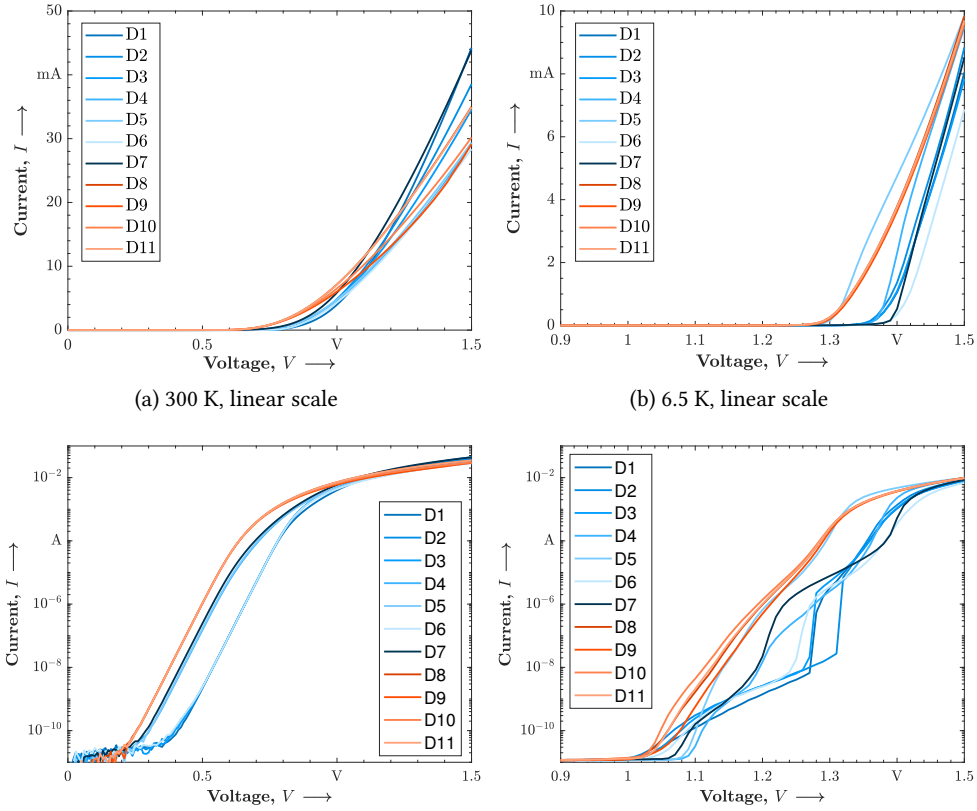
The current-voltage IV characteristic measurements have been performed using two SMUs. This measurement has been done for all the diodes at RT and 6.5 K. For one of the n-type diodes a temperature sweep measurement has been performed, the result is presented in Fig. 5.3.

It can be observed in Fig. 5.3, that the diode shows classical behavior down to about 70 K.

Similar to cryogenic MOSFETs, as in general described in section 2.2, the threshold voltage increases by 0.8 V, and steepness increases with the decrease in temperature. However, below 70 K the additional cryogenic effects appear. It leads to the flattening of the IV curve and adds additional kinks.

Very similar effects have been observed in the subthreshold region of CMOS transistors in [79], p. 37. The possible reason for that is the impact ionization, happening at voltages, close to the threshold.

The results for all the diodes are presented in Fig. 5.4 in both linear and logarithmic scales. Shades of red are chosen for N-type devices and shades of blue are for P-type. It can be observed, that parasitic cryogenic effects are more pronounced for P-type devices: some of them show bigger threshold voltage increase, and the IV curves have more kinks and steps.



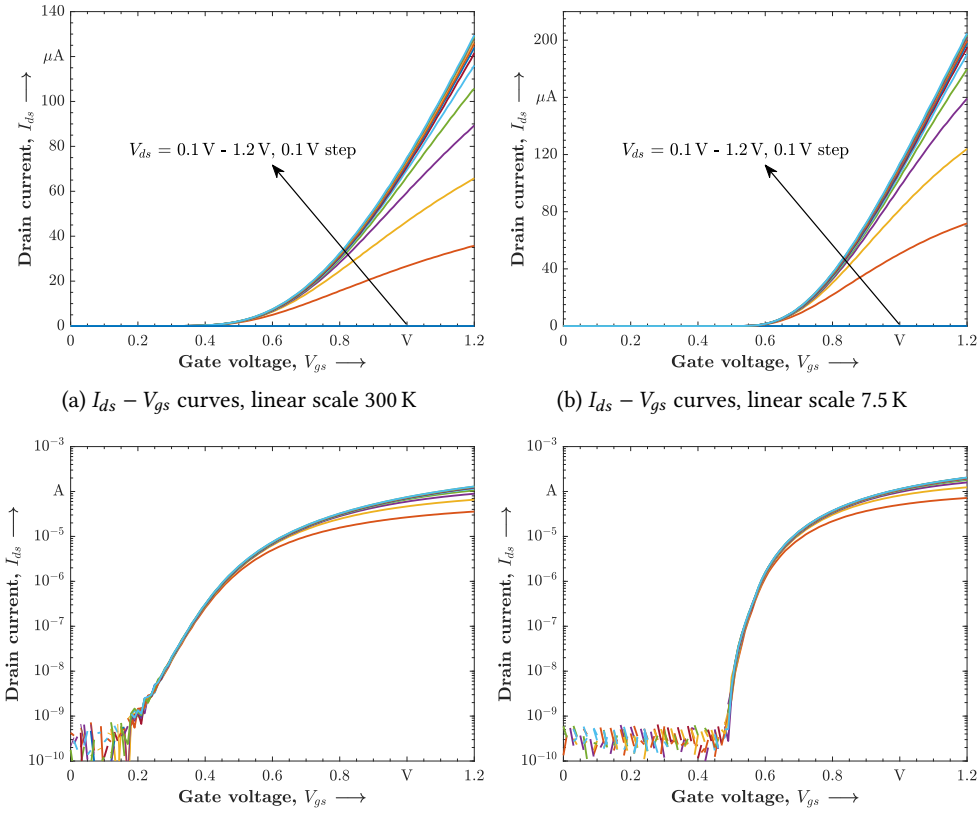
(a) 300 K, linear scale

(b) 6.5 K, linear scale

(c) 300 K, logarithmic scale

(d) 6.5 K, logarithmic scale

Figure 5.4: Measured IV characteristics for all the diodes. Shades of red – n-type, shades of blue – p-type.



(a) $I_{ds} - V_{gs}$ curves, linear scale 300 K

(b) $I_{ds} - V_{gs}$ curves, linear scale 7.5 K

(c) $I_{ds} - V_{gs}$ curves, logarithmic scale 300 K

(d) $I_{ds} - V_{gs}$ curves, logarithmic scale 7.5 K

Figure 5.5: Comparison of RT and cryogenic behaviors of an N-type device.

5.4 65 nm bulk CMOS transistors

The transistors, briefly described in section 4.2, have been measured within the framework of this chapter. The main features are presented in the example of n-type core devices with 1.02 μm width and 0.51 μm length (Fig.5.5).

Most of the cryogenic measurements showed no parasitic effects like kink, overshoot, or hysteresis. Some parameters, however, showed some changes with the decrease in temperature, in accordance with prior publications (section 2.2). The measured $I_{ds} - V_{gs}$ characteristics are presented in Fig. 5.5. As expected, threshold voltages V_{th} increase by around 0.1 V (Fig. 5.5a and 5.5b) due to temperature dependence of the bulk Fermi potential [42]. The subthreshold swing decreases with the decrease of temperature [62] from ca. 70 mV/dec down to ca. 20 mV/dec (Fig. 5.5c and 5.5d).

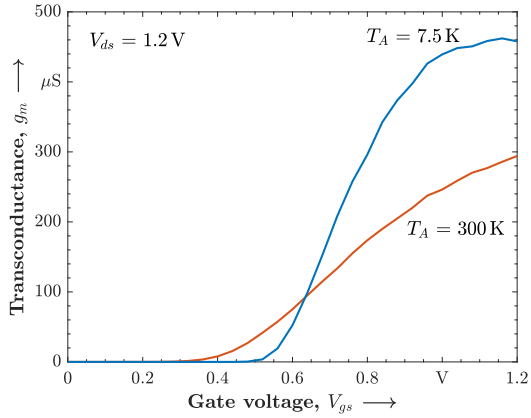
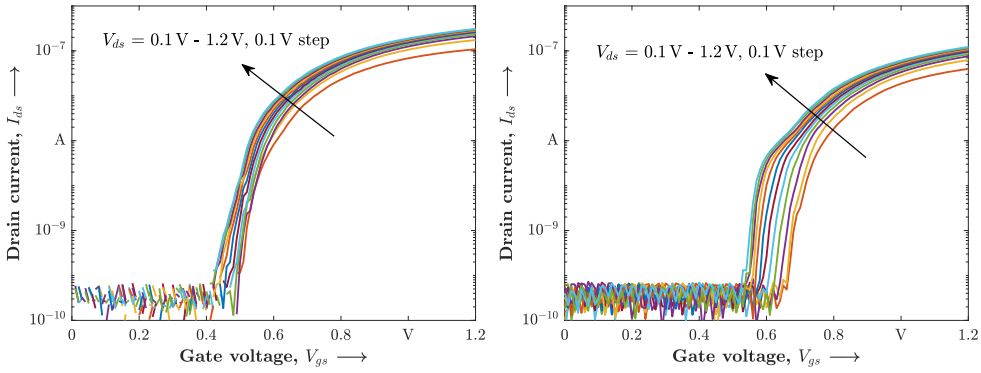


Figure 5.6: Comparison of transconductance g_m at RT and 7.5 K.



(a) N-type device

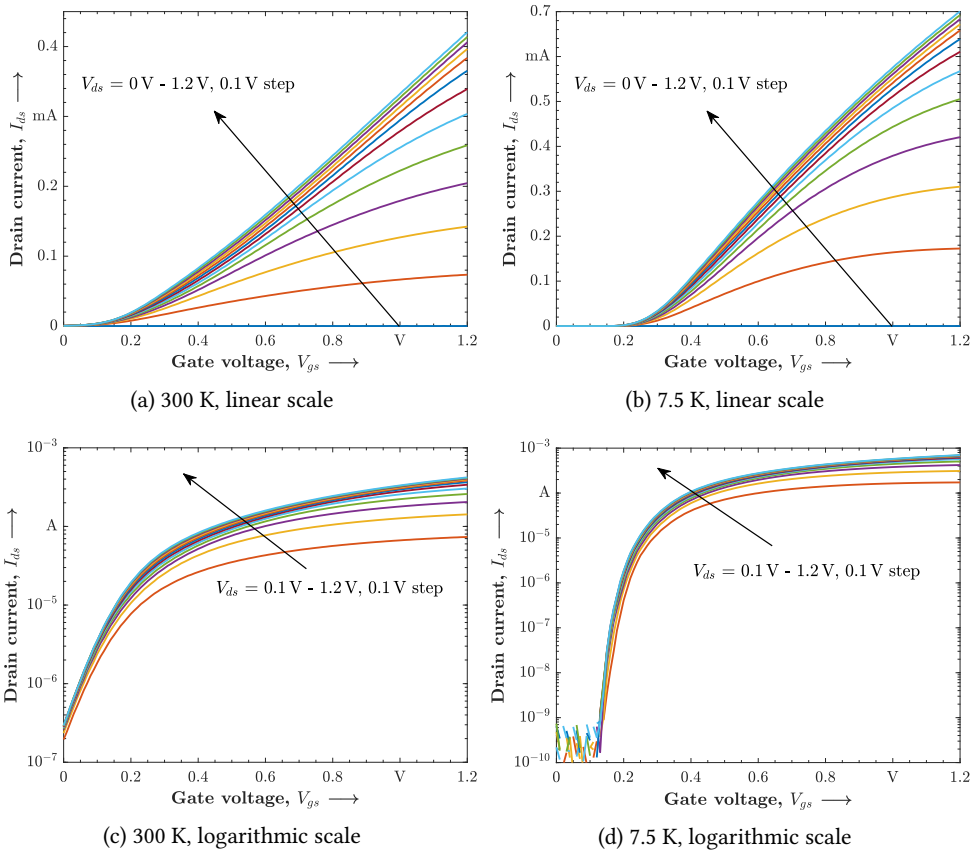
(b) P-type device

Figure 5.7: Cryogenic effect in a short-channel P-type transistor.

The dependence of transconductance on gate voltage is demonstrated in Fig. 5.6. The transconductance shows a significant increase due to increased electron mobility. The maximum value for this transistor increased from 300 μS up to 460 μS.

Nevertheless, some devices show undesired kinks (Fig. 5.7). Similar effects have been reported in [79], p. 37. The possible explanation for that is the impact ionization, happening when the gate voltage reaches around the threshold voltage, causing the increase in drain current.

Fig. 5.7 shows the $I_{ds} - V_{gs}$ curves of two short-channel devices with the same dimensions, but different types. It has been noticed, that the p-type devices are more often prone to this subthreshold cryogenic effect than the n-type ones. This effect is reproducible for the same sample, however, it might be different or absent at all for the same devices on different dies. This unpredictability might also be a challenge for IC designers or could have a yield impact on production.



(a) 300 K, linear scale

(b) 7.5 K, linear scale

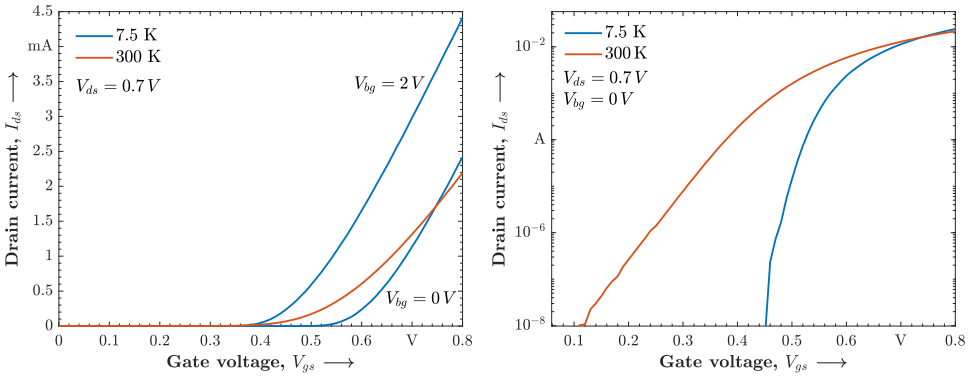
(c) 300 K, logarithmic scale

(d) 7.5 K, logarithmic scale

Figure 5.8: Comparison of the measured $I_{ds} - V_{gs}$ characteristics of a native transistor at room temperature and 7.5 K.

The cryogenic behavior of native devices was not reported before. This type of transistor is fabricated directly on a p-type wafer, without additional doping. That forms a transistor with "zero" threshold voltage, which in reality conducts some current even with zero gate voltage (Fig. 5.8c). As shown in previous research (section 2.2) and measurements in this section, the threshold voltage of CMOS devices increases at cryogenic temperatures. That makes the use of native devices promising: increased threshold voltage in this case might lead to normal low-V_{th} transistor behavior.

The results of the $I_{ds} - V_{gs}$ measurements at 300 K and 7.5 K are presented in Fig. 5.8 and they confirm this hypothesis. Although, fractions of μA flow through the native device at 300 K even at $V_{gs} = 0\ V$, at 7.5 K the device behaves like a normal transistor with a low threshold voltage of ca. 0.2 V. This feature of native devices can help to decrease the power dissipation in comparison to normal transistors. The main drawback is that the devices are only available in n-type versions, and that significantly complicates the IC design.



(a) linear scale (b) logarithmic scale

Figure 5.9: $I_{ds} - V_{gs}$ characteristics of low V_{th} FD-SOI transistor.

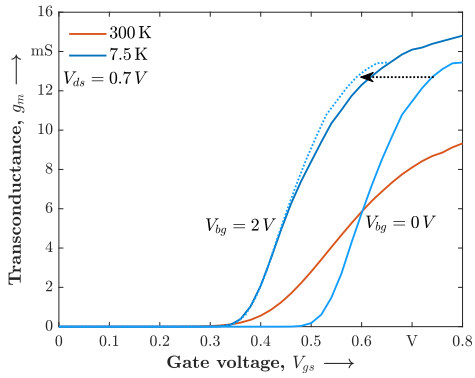


Figure 5.10: Transconductance g_m of low V_{th} FD-SOI transistor.

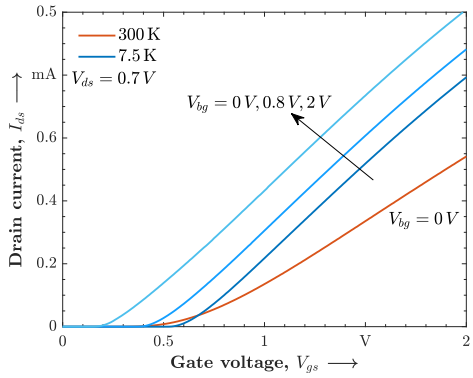


Figure 5.11: $I_{ds} - V_{gs}$ characteristics of super-low V_{th} FD-SOI transistor.

5.5 22 nm FD-SOI technologies CMOS transistors

There are several variants of transistors available for 22 nm FD-SOI technology. In SQuBiC5 there are RF structures that contain arrays of a low threshold version of core transistors. In the DC part of the chip so called "super-low" threshold voltage thick oxide devices have been placed. Both of these versions have been measured within the framework of the project.

The cryogenic effects in FD-SOI devices are similar to bulk ones, as they still represent CMOS transistor structures. They show a decrease of subthreshold swing with temperature decrease from ca. 70 mV/dec down to ca. 20 mV/dec (Fig. 5.9) and threshold voltage shift of ca. 0.1 V (Fig. 5.9a), as seen from the $I_{ds} - V_{gs}$ measurement results (Fig. 5.9). The transconductance also increases significantly (Fig. 5.10). The reasons for these changes are the same as described in the previous section.

However, for this technology, there is the ability to apply a back-gate voltage, that allows decreasing the V_{th}, and that feature can be very profitable for IC design.

In Fig. 5.9a it is shown, that for low-V_{th} devices it is possible to change the cryogenic V_{th} value back to the RT value by applying 2 V to the back gate terminal. Fig. 5.11 demonstrates the super-low-V_{th} $I_{ds} - V_{gs}$ characteristics. It is shown, that for these devices the V_{th} can be shifted in a wider range, and it can go from 0.6 V down to 0.2 V at 7.5 K.

In order to find out, whether V_{th} shift by the back gate changes the transconductance of the $I_{ds} - V_{gs}$ curve, the g_m curve at $V_{bg} = 0\ V$ (Fig. 5.10, light blue solid line) has been mathematically moved by 0.15 mV (light blue dotted line) in order to compare it with $V_{bg} = 2\ V$ g_m curve (dark blue line). It is observed, that the g_m decreases slightly by less than 10% at high V_{gs}.

5.6 Conclusions

Devices, fabricated in 65 nm bulk CMOS technology, behave similarly to other modern bulk CMOS technologies, described in recent publications (section 4.2). MIM capacitors keep their performances over the whole temperature range, while diodes show an increased threshold voltage, an increased steepness of the curve and demonstrate some undesirable cryogenic effects. Transistors show mostly improved behavior - lower subthreshold swing and increased transconductance, but increased threshold voltage, that need to be taken into account in future cryogenic PDKs.

In addition to previous publications, native transistors have been measured in cryogenic temperatures for the first time. The results show normal transistor behavior with all the cryogenic improvements and very low subthreshold voltage. That can be useful for future cryogenic IC design. However, more investigation should be done in this field and valid cryogenic PDKs should be developed. Another difficulty is that only native devices of n-type are available, while p-type devices are also very essential for advanced IC design.

22 nm FD-SOI transistors provide the ability to shift threshold voltage by active use of the back gate. That is very profitable for cryogenic applications, as V_{th} can be shifted to the same value as at room temperature, or even lower, helping the IC designers in a certain way. However, this is also generating additional effort and complexity. Nevertheless, cryogenic PDKs should be developed in order to take into account the improving parameters, like subthreshold swing or transconductance.

Personal contribution includes performing all the measurements shown, organizing the data processing, and extracting key results.

Chapter 6

High-frequency characterization of single 22 nm FD-SOI CMOS devices

Some qubit implementations, like SiGe spin qubits, require high-frequency pulses for control [80]. Hence, valid cryogenic RF models are needed in order to develop low-temperature control electronics. This, in turn, requires a reliable RF needle probing procedure, performed at cryogenic temperatures.

This chapter is aimed at the valid high-frequency characterization of MOSFET devices, fabricated in commercial 22 nm FD-SOI technology, at cryogenic temperatures and frequencies up to 20 GHz.

The work, described in the chapter, was performed together with Leander Willeke, a Master's student supervised by the author. He was involved in conducting the measurements and data analysis. Some of the results are also published in his Master's thesis [81].

6.1 Small-signal equivalent circuit parameter extraction

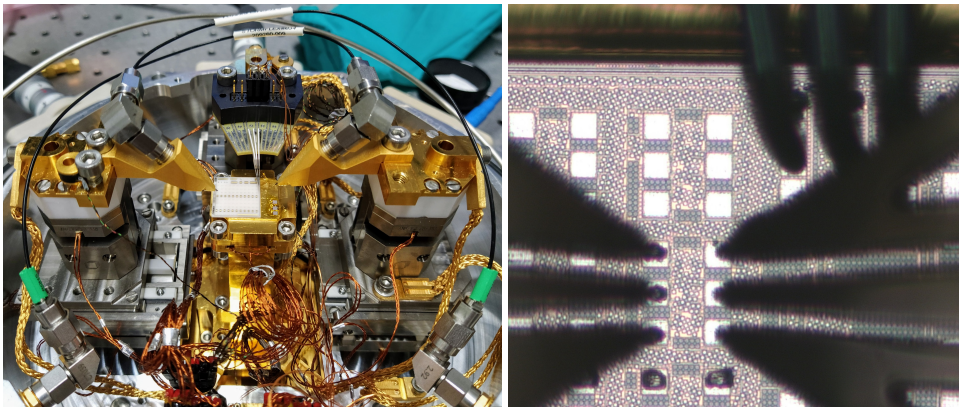
6.1.1 Experiment description

The RF needle probe setup, described in section 3.3, is used (Fig. 6.1). RF DUTs were fabricated on the SQuBiC5 chip (see section 4.3).

For RF probing two ground-signal-ground probes Z40-XF with a 75 µm pitch by Cascade Microtech were used (Fig. 6.1). In order to move the measurement plane to the tips of the probes, a calibration substrate CSR-9 by FormFactor was used. Both RF probes and calibration substrate are specified down to cryogenic temperatures. CSR-9 keeps its parameters over the whole temperature range, so the calibration procedure remains the same. However, it should be performed at every temperature before the measurement.

DC connections, needed for substrate, n-well, and back gate contacts, are established with a DC multi-contact wedge by GGB, which has 3 needles with a 100 μm pitch.

A Vector Network Analyzer N5242A from Keysight's PNA-X series [82] is used. It supplies a frequency range from 10 MHz to 26.5 GHz and various features for easier calibration procedure and noise measurements. In this case, the measurements were performed from 10 MHz up to 20 GHz in steps of 10 MHz. The SOLT (Short-Open-Load-Thru) calibration is performed



(a) photo of the setup (b) microscopic photo

Figure 6.1: Photos of the high-frequency probing configuration.

with the probing needles on a calibration substrate using an averaging factor of 100 and a transmitted RF power equal to that of the measurement (-21 dBm).

The power supply Keysight N6705C has been used to control the back gate and n-well potentials.

Preliminary DC measurements of the DUTs have been done with Keysight B1500A Semiconductor Analyzer. Gate-source voltage and drain-source voltage are swept from 0 V to 0.8 V, according to the device specification.

For noise measurements, Ecal Kit Agilent N4691-60006 and a noise source Keysight 346C were used in addition to the mentioned above equipment.

6.1.2 Calibration and de-embedding

As the measured devices are small – physically and in terms of their electrical behavior – it is not trivial to connect them and find out about their behavior without the need to take into account the influence of cables, needles, and contact pads. For RF characterization impedance matching needs to be considered as well. The DUTs on the chip include the pads and feed lines that embed a transistor array between them. In order to subtract the influence of the RF chain, two procedures are applied: calibration and de-embedding.

Calibration is performed with the use of the vector network analyzer (VNA). By connecting the RF probes to well-characterized standards and using the determined S-parameters, the VNA is able to perform 12-term error correction and shift the reference plane towards the needle tips.

De-embedding is made using corresponding structures integrated on the die. By measuring an OPEN and SHORT structure, the influences of the contact pads and of the feed lines on a chip can be removed mathematically, remaining the characteristics of the transistor array itself.

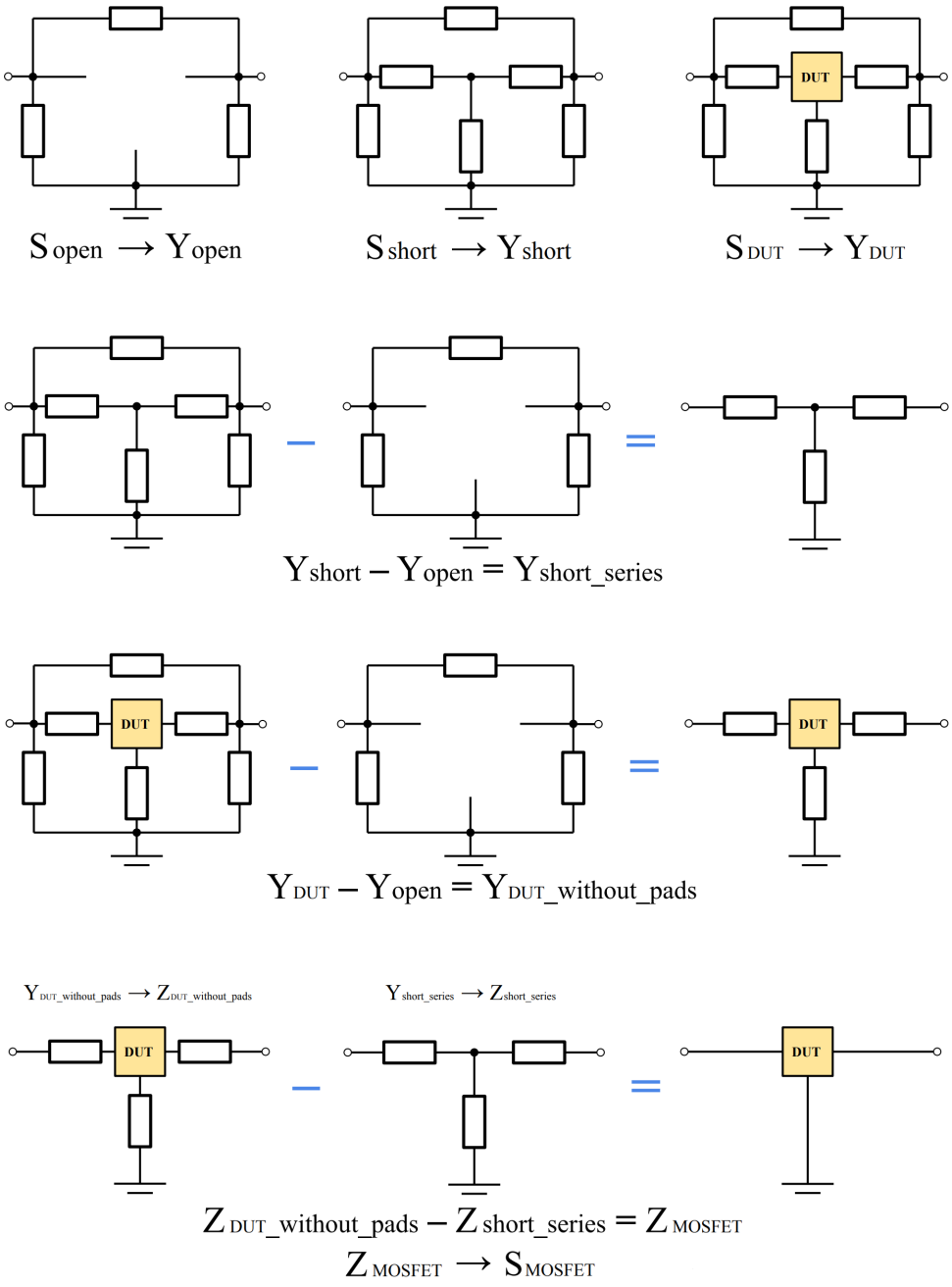
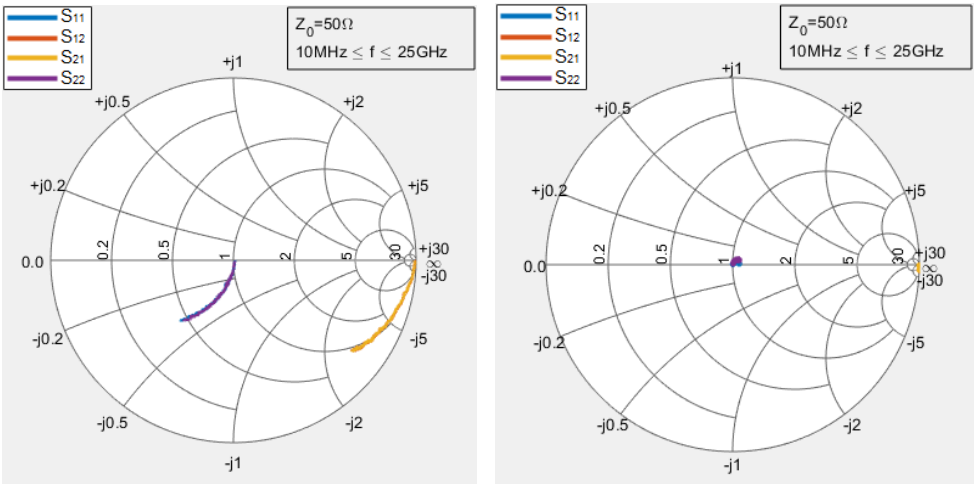


Figure 6.2: De-embedding procedure scheme and formulae. S, Y, and Z are scattering, admittance, and impedance matrices respectively.

Utilizing more de-embedding structures can increase the accuracy of the measurement [83]. However, these two are reported to provide enough accuracy for frequencies up to 20 GHz.

Briefly speaking, the OPEN structure represents the capacitive behavior of the embedding, while the SHORT structure includes in addition the resistive and inductive characteristics of the metal lines leading up to the transistors. The procedure including transformations should be performed in order to remove embedding parasitic parameters. This procedure is shown in Fig. 6.2.

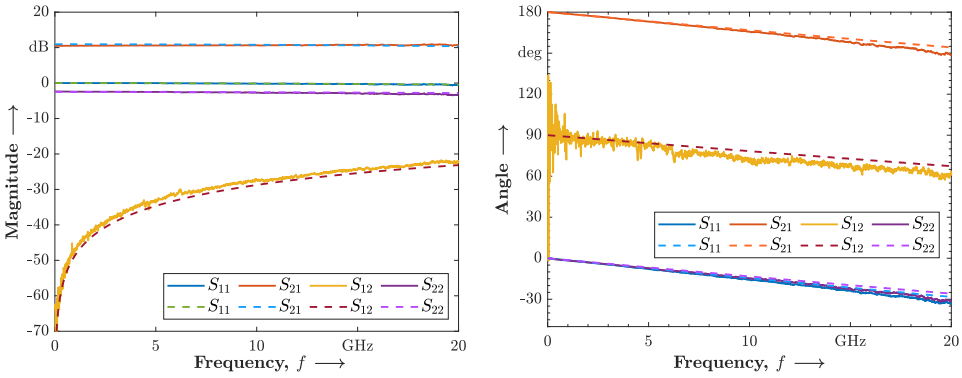
In order to check the quality of calibration and de-embedding procedures, the THRU structure on a SQuBiC5 chip is measured. It repeats DUT embedding as accurately as possible, but



(a) before de-embedding

(b) after de-embedding

Figure 6.3: S-parameter data of the THRU structure before and after de-embedding [81].



(a) magnitude data

(b) angle data

Figure 6.4: Comparison of the simulated (dashed lines) and measured (solid lines) scattering parameters data of the transistor array [81].

the gate and the drain terminals are connected with a short line. As seen from the results in Fig. 6.3, all the parasitic elements are basically removed for the whole frequency range.

Additional proof of the validity of the de-embedding is the comparison of the simulated by PDK RF-structure S-parameters and the measured ones (Fig. 6.4). Process variations can contribute to the result of the measurements and explain minor incompatibility, however, the results are extremely well matched.

6.1.3 Input and output impedance

As seen in Fig. 6.4, S_{11} at 20 GHz is -0.4 dB. That means, that more than 90 % of the input signal power is reflected back to the port of the VNA, and less than 10 % is actually amplified by the transistor. This happens due to the fact, that the line and the input transistor impedances are not matched.

As all the RF lines and sources have a standard impedance of $50+j0\,\Omega$, in order to achieve perfect matching the DUT input and output impedance should have the same value, but in the case of a transistor array, it is not possible without additional matching structures. Transistor input shows mostly capacitive behavior due to the geometry of the device with the gate. Due to the channel connection, the output of the transistor is also not matched with the line, as can be seen from the S_{22} measurements.

The input Z_{in} and Z_{out} impedance values can be extracted from the scattering parameter measurements [84]:

$$Z_{in} = Z_{11} - \frac{Z_{12}Z_{21}}{Z_{22} + Z_L} \tag{6.1}$$

$$Z_{out} = Z_{22} - \frac{Z_{12}Z_{21}}{Z_1 + Z_S}, \tag{6.2}$$

where Z_L and Z_S are the load and source impedances respectively. As in this case source and load are the lines and ports of the VNA, they both are equal to 50 Ω.

The full Z_{in} and Z_{out} analysis is performed in [81], p. 34-37, and the figures for the two devices are shown in Appendix A. It was shown, that these values stay the same or change insignificantly for both 300 K and 6 K. In table 6.1 impedances of the RF structures for two frequencies are presented.

T_A=300 K,V_{bg}=0	nMOS W=2.4 μm	nMOS W=4.8 μm	nMOS W=9.6 μm
Z_{in}, 8 GHz	(74-4298j) Ω	(76-1663j) Ω	(51-623j) Ω
Z_{in}, 15 GHz	(79-1945j) Ω	(87-741j) Ω	(57-272j) Ω
Z_{out}, 8 GHz	(1718-1187j) Ω	(814-1103j) Ω	(417-619j) Ω
Z_{out}, 15 GHz	(922-1070j) Ω	(397-657j) Ω	(319-315j) Ω

Table 6.1: Input and output impedance of transistor array structures values at 8 and 15 GHz.

As the impedance for a single transistor in each case should be 10 times larger, these results prove the advantage of transistor array measurements in terms of 50 Ω matching. Transistors of larger size show relatively better matching, however, the imaginary part is still several hundred Ω. An increase in frequency also improves the matching due to a decrease in gate capacitor impedance.

6.1.4 MOSFET small-signal parameter extraction

After calibration and de-embedding, S-parameters of the transistor structure itself are achieved. In order to describe and model its RF behavior, a small-signal equivalent circuit (SSEC) should be extracted. A common model, which validity has been shown for SOI MOSFETs up to frequencies above 30 GHz [85], can be seen in Fig. 6.5. The subscripts "e" and "i" in the figure mean the extrinsic or intrinsic components respectively. The intrinsic elements are usually assumed to be bias-point-dependent as they represent the channel characteristics, while the extrinsic parts are bias-independent [86]. R_{gs} can be neglected if the operation can be seen as quasi-static, meaning that the input signal changes slowly enough that the charge carriers are able to follow the applied field instantaneously [87]. If the change of the gate potential happens too fast, a non-quasi-static model needs to be used with additional R_{gs} and C_{gsi} elements.

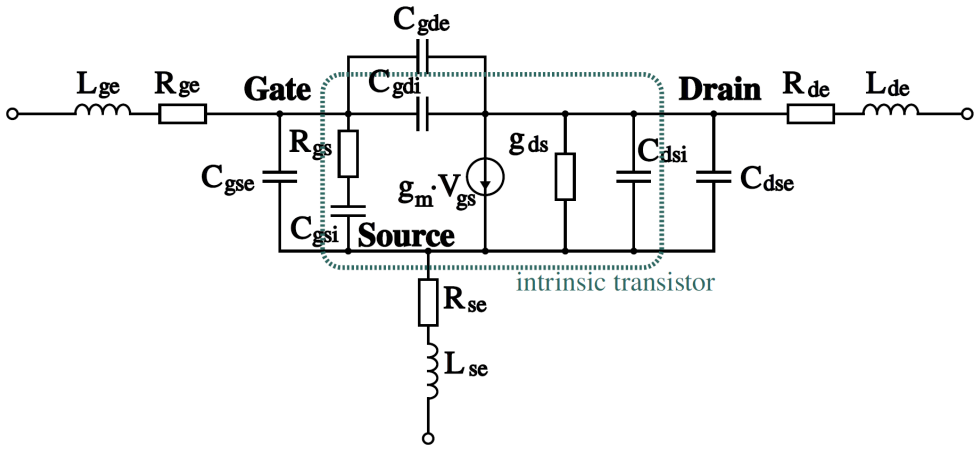
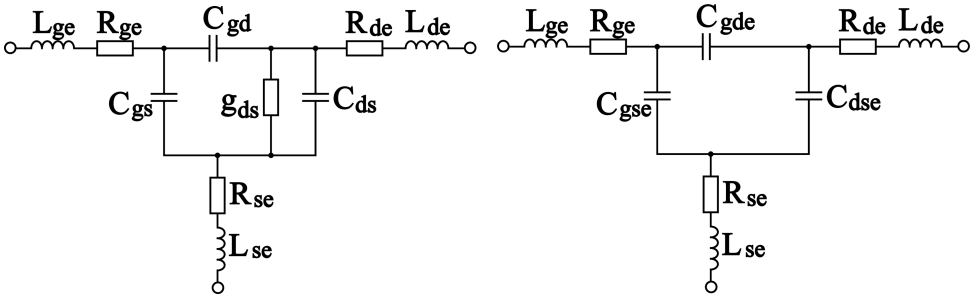


Figure 6.5: Small-signal equivalent circuit of a de-embedded single FDSOI MOSFET device (adopted from [88]).

In Fig. 6.6a the SSEC for cold bias and strong inversion case is given, when the bias voltages $V_{ds} = 0\,V$ and $V_{gs} > V_{th}$ are applied. In that case, the controlled source can be neglected. No drain-source current will be caused by a changing gate potential and g_m will be equal to zero.

Fig. 6.6b shows cold-bias ($V_{ds} = 0\,\mathrm{V}$) and deep depletion ($V_{gs} < 0\,\mathrm{V}$) case. The inversion layer in the channel disappears, and the intrinsic capacitances are neglected together with channel conductance. The extrinsic capacitances and the access impedances can be extracted.



(a) cold bias and strong inversion regime (b) cold bias and deep depletion regime

Figure 6.6: Small-signal equivalent circuits in quasi-static operation (adopted from [88]).

The access impedances ($R_{ge} + j\omega L_{ge}$, $R_{se} + j\omega L_{se}$, and $R_{de} + j\omega L_{de}$) depend on the chosen extraction method determined by considering their dependence on bias voltage and frequency. There are several possible approaches, described in [89, 90, 91]. All three of them were thoroughly compared in [92] and investigated in [81] in order to make a choice for that case.

The approach in [91] has been chosen as the most accurate for these measurements. Following it, cold bias and strong inversion are used to suppress the influence of transconductance. The equivalent circuit in this case drain, channel, and source resistances (R_{de}, R_{ch} and R_{se}) are connected in series, with R_{ch} shunted by capacitance C_x. The necessary resistances can be calculated using the following equations:

$$R_{se} = Re\{Z_{12}\} - A/2 \tag{6.3}$$

$$R_{de} = Re\{Z_{22}\} - R_{se} - A \tag{6.4}$$

$$R_{ge} = Re\{Z_{11}\} - R_{se} - A/4, \tag{6.5}$$

where the frequency-dependent A describes the impedance of the intrinsic device and is defined as

$$A = \frac{R_{ch}}{(1 + \omega^2 C_x R_{ch}^2)}, \tag{6.6}$$

where

$$C_x = C_{ds} + \frac{C_{gs}C_{gd}}{C_{gs} + C_{gd}}; \qquad R_{ch} = \frac{1}{g_{ds}}. \tag{6.7}$$

Linear regression is used towards $\omega^2 = 0$ for

$$-\frac{\omega}{Im\{Z_{22}\}} = C_x\omega^2 + \frac{1}{R_{ch}^2 C_x}. \tag{6.8}$$

This gives C_x as the slope over ω^2 and the second term is given as the intercept of the line of best fit with the y-axis. As a result, A and the series resistances can be extracted.

The series parasitic impedances can be removed by subtraction of Z matrices. Then Y-parameters of the structures in Fig. 6.6 can be obtained and the intrinsic transistor in Fig. 6.5,

and using them, the values of the transistor parameters can be extracted [89]:

$$Z_{intr\_trans} = Z_{trans} - Z_{series\_elements} \tag{6.9}$$

$$Z_{series\_elements} = \begin{bmatrix} R_{ge} + R_{se} & R_{se} \\ R_{se} & R_{de} + R_{se} \end{bmatrix} + j\omega \begin{bmatrix} L_{ge} + L_{se} & L_{se} \\ L_{se} & L_{de} + L_{se} \end{bmatrix} \tag{6.10}$$

$$Y_{intr\_trans} = Y = \begin{bmatrix} j\omega(C_{gd} + C_{gs}) & -j\omega C_{gd} \\ g_m - j\omega C_{gd} & g_{ds} + j\omega(C_{ds} + C_{gd}) \end{bmatrix} \tag{6.11}$$

$$Y_{deep\_depletion} = \begin{bmatrix} j\omega(C_{gde} + C_{gse}) & -j\omega C_{gde} \\ -j\omega C_{gde} & j\omega(C_{dse} + C_{gde}) \end{bmatrix} \tag{6.12}$$

$$C_{gd} = Im\{Y_{12}\}/\omega; \qquad C_{gs} = Im\{Y_{11} + Y_{12}\}/\omega; \qquad C_{ds} = Im\{Y_{22} + Y_{12}\}/\omega \tag{6.13}$$

$$C_{gde} = Im\{Y_{deep\_depletion,12}\}/\omega \tag{6.14}$$

$$C_{gse} = Im\{Y_{deep\_depletion,11} + Y_{deep\_depletion,12}\}/\omega \tag{6.15}$$

$$C_{dse} = Im\{Y_{deep\_depletion,22} + Y_{deep\_depletion,12}\}/\omega \tag{6.16}$$

$$g_{ds} = Re\{Y_{22}\} \tag{6.17}$$

$$g_m = |Y_{21} - Y_{12}| \tag{6.18}$$

The intrinsic and extrinsic capacitances together sum up to the full capacitances. The intrinsic capacitances are calculated by subtraction [88]:

$$C_{gdi} = C_{gd} - C_{gde}; \qquad C_{gsi} = C_{gs} - C_{gse}; \qquad C_{dsi} = C_{ds} - C_{dse} \tag{6.19}$$

In order to extract R_{gs} the charge-rearrangement constant τ and the determined intrinsic gate-source-capacitance are used [88]:

$$\tau = -\frac{arctan(\frac{Im\{Y_{21}-Y_{12}\}}{Re\{Y_{21}-Y_{12}\}})}{\omega} \tag{6.20}$$

$$R_{gs} \approx \tau/(2C_{gsi}) \tag{6.21}$$

The above-described procedure provides the desired internal parameters of the DUT, excluding all the present parasitic elements. As described in section 4.3, DUTs in this case are the arrays of 10 identical transistors, connected in parallel. That makes all of the capacitances and resistances connected in parallel. Therefore, in order to extract the parameters of a single transistor, all the capacitances and (trans)conductances should be divided by 10 as well as all the series resistances should be multiplied by 10.

6.1.5 Measurement results

All the following results are presented at $V_{gs} = V_{ds} = 0.7$ V. This bias point selection is useful due to the fact, that at this bias point RF structures, measured during the experiment, showed the same current densities at 300 K and 6 K (Fig. 5.9a).

After implementing all the procedures, described in the previous subsections, the curves of the small-signal equivalent circuit elements are obtained (Fig. 6.7, 6.8, 6.9, and 6.10). In some cases, slight frequency dependencies or artifacts can be observed. This behavior happens usually due to inaccuracies during the needle probe contact procedure. In total, 8 needle applications to calibration, de-embedding structures, and the sample itself are needed in order to obtain the data for one sample. Some error appears as well during multiple needle applications to the same structures, as the probes damage the pads a little every time they are applied, hence, slightly change their parameters.

Nevertheless, this experiment allows the extraction of overall capacitances, intrinsic gate-source capacitance, and transconductance with deviation from the mean value of not more than 10%. Intrinsic capacitances C_{gdi} and C_{dsi} are not possible to be extracted due to extremely small values of less than 1 fF: the resulting curves sometimes go below 0.

Drain-source conductance g_{ds} measurement also shows low accuracy of up to 100%. The result of g_{ds} measurement depends a lot on the needle contact quality, which differs from measurement to measurement. The average of 0.4 mS, which is the same for all the transistor sizes (due to the same width-length ratio) and does not change with temperature, can be observed. The increase of intrinsic gate capacitance is consistent with gate area increase – by 4 and 16, compared to the smallest one.

As seen from the extracted small-signal circuit parameters at 300 K and 6 K, almost all of them remain stable with temperature decrease. The only noticeable change shows the transconductance g_m (Fig. 6.10). This result is also consistent with g_m values, extracted from the DC data (Fig. 5.10).

The extracted values for all the available structures are published in [81] and added in Appendix B.

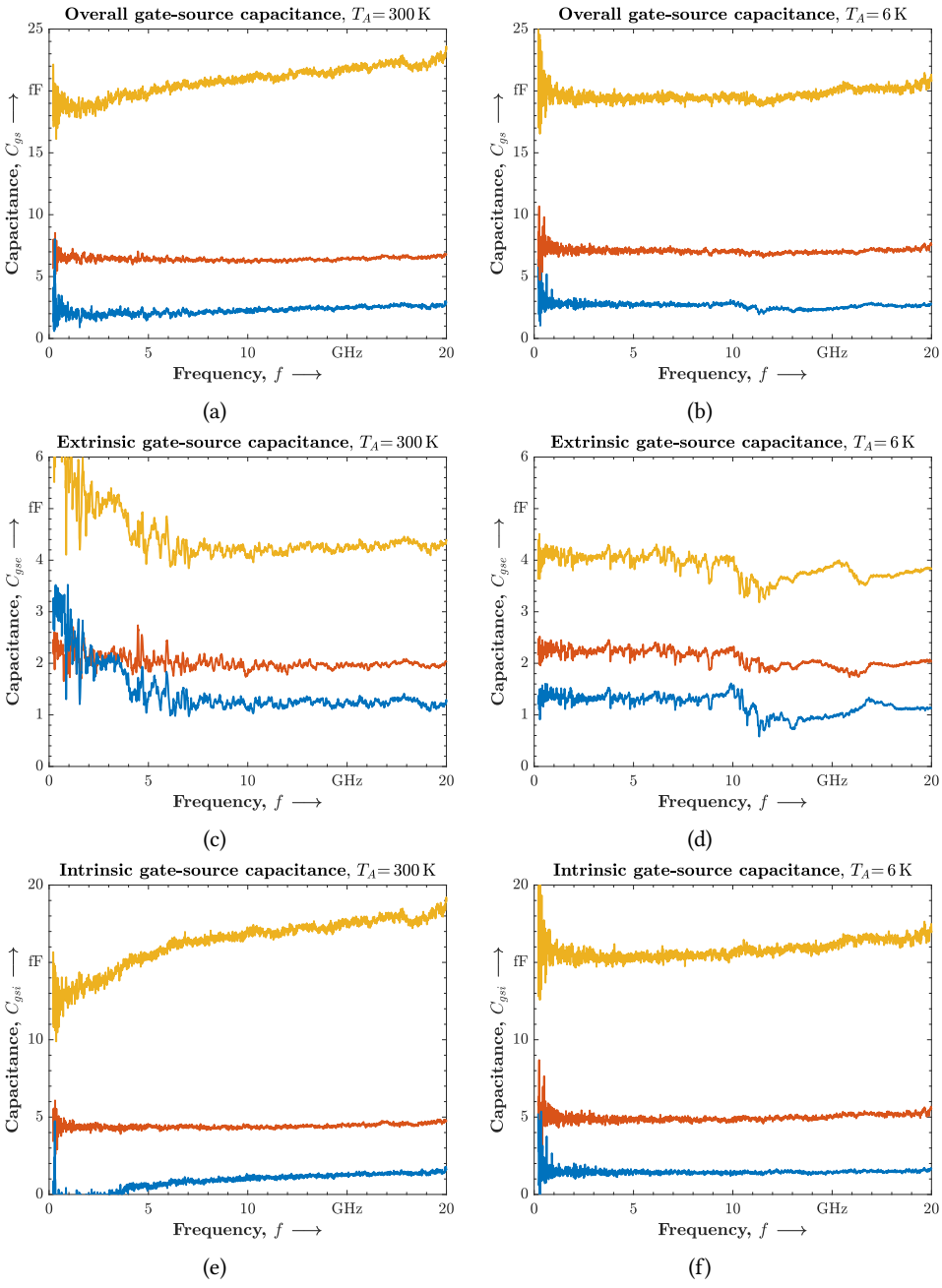


Figure 6.7: Gate-source capacitance extraction: blue - W = 2.4 μm, red - W = 4.8 μm, yellow - W = 9.6 μm.

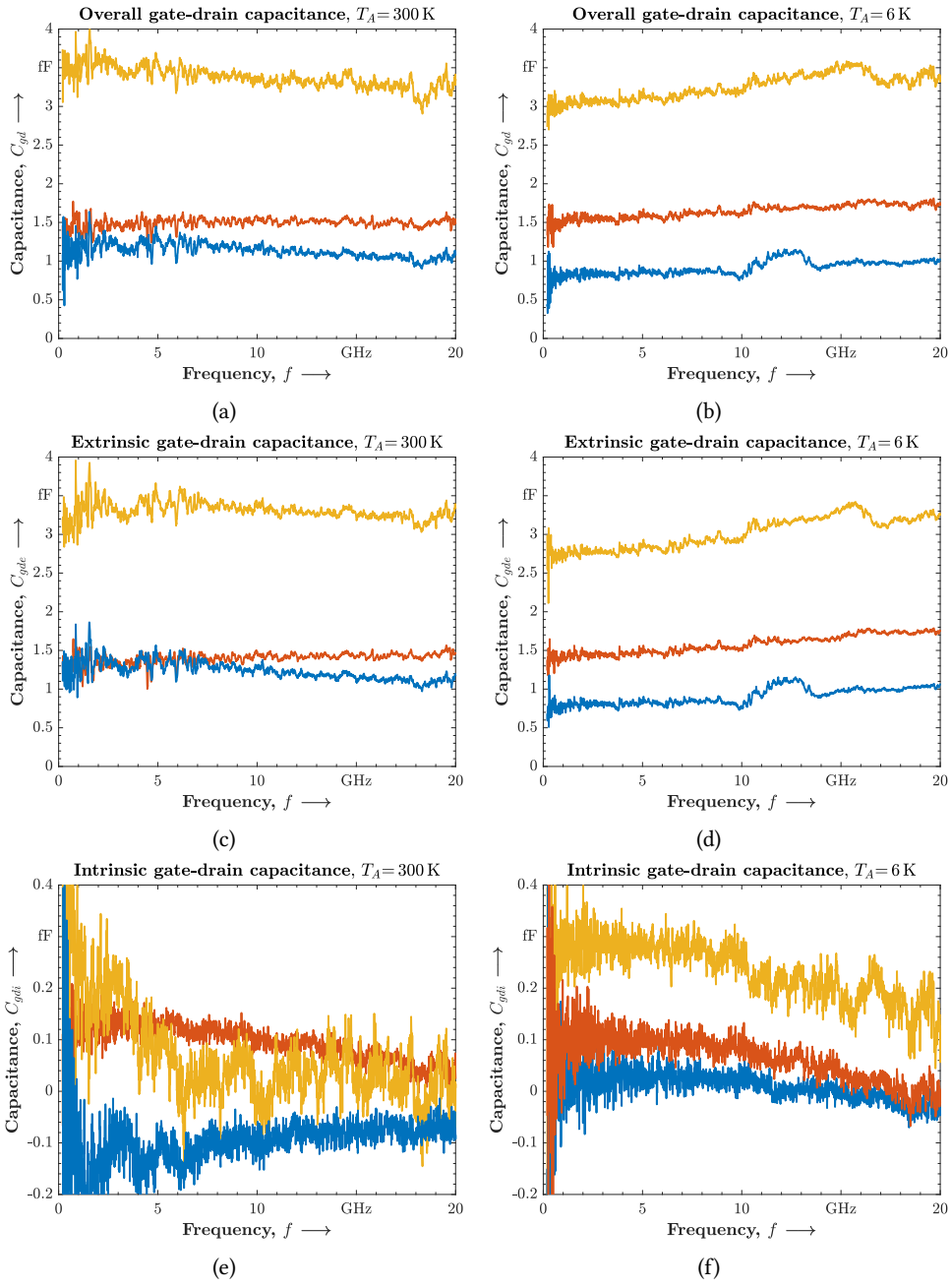


Figure 6.8: Gate-drain capacitance extraction: blue - W = 2.4 μm, red - W = 4.8 μm, yellow - W = 9.6 μm.

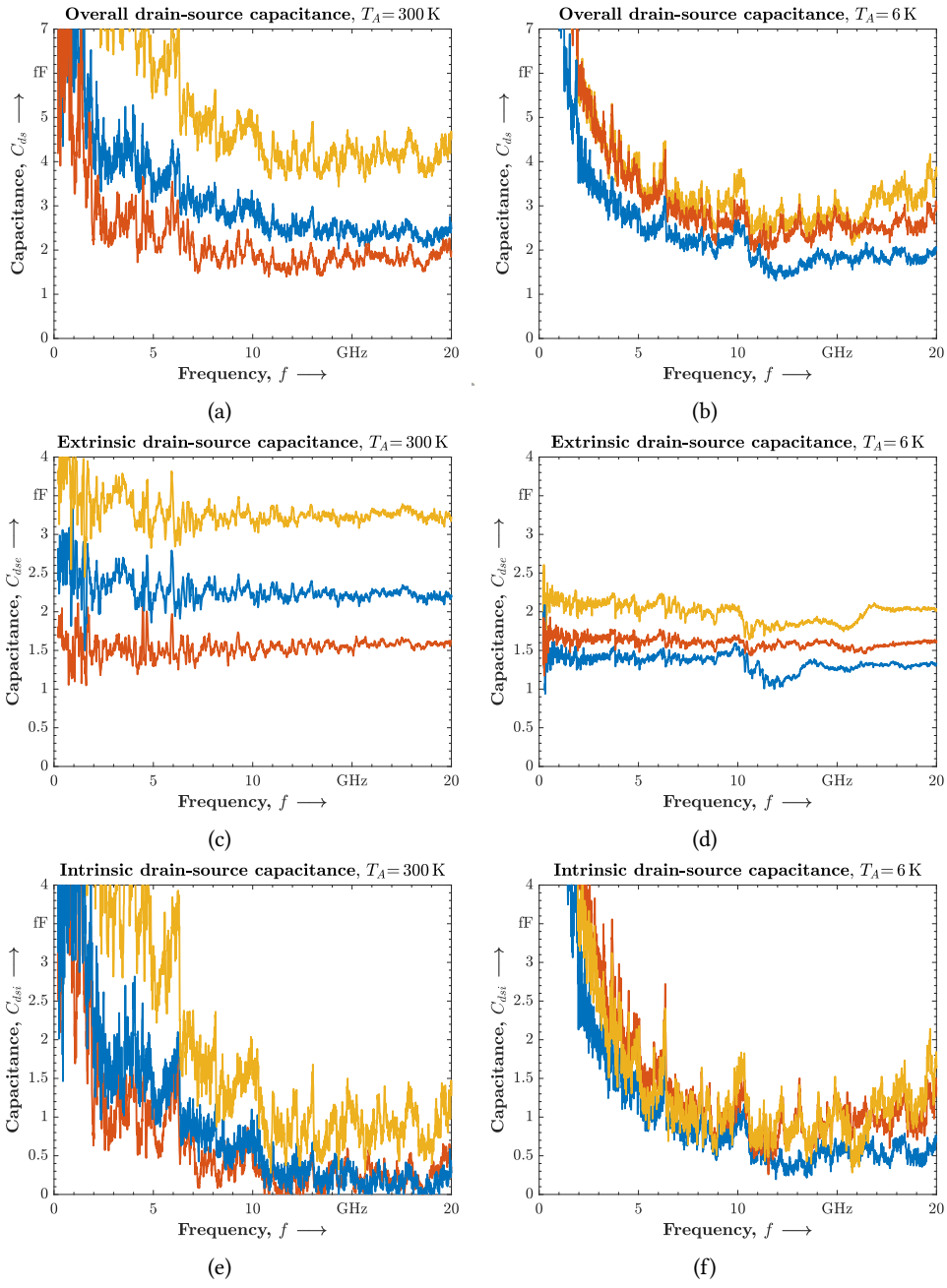


Figure 6.9: Drain-source capacitance extraction: blue - W = 2.4 μm, red - W = 4.8 μm, yellow - W = 9.6 μm.

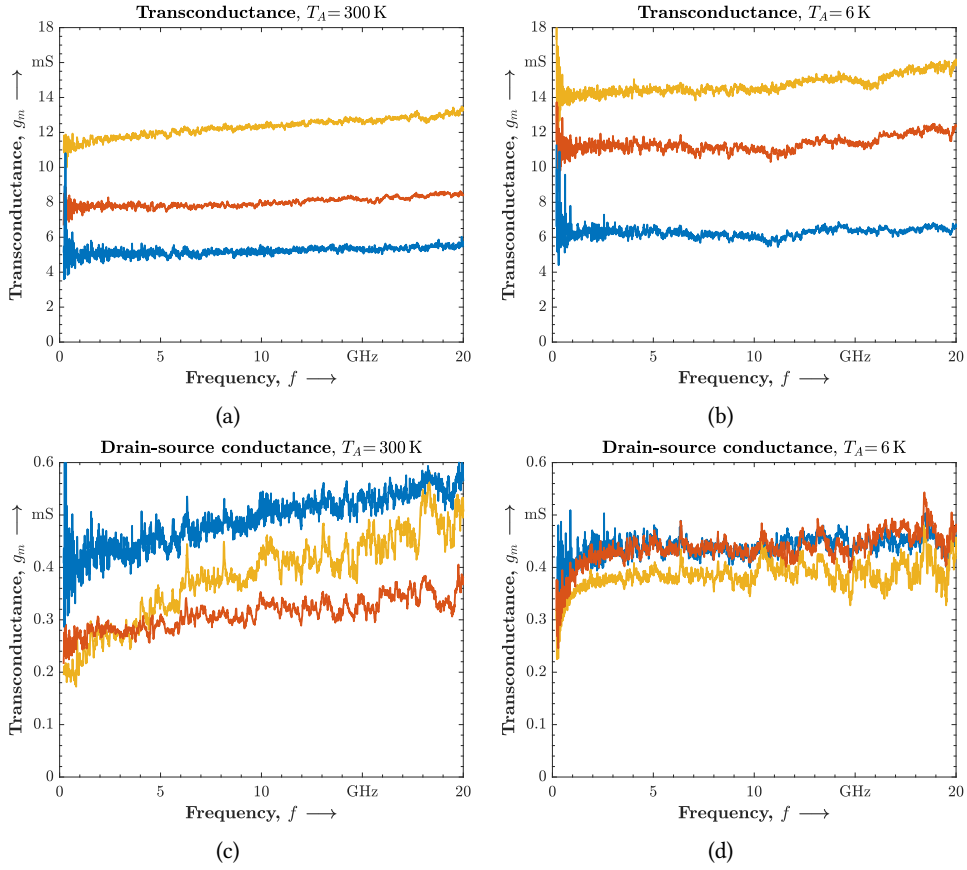
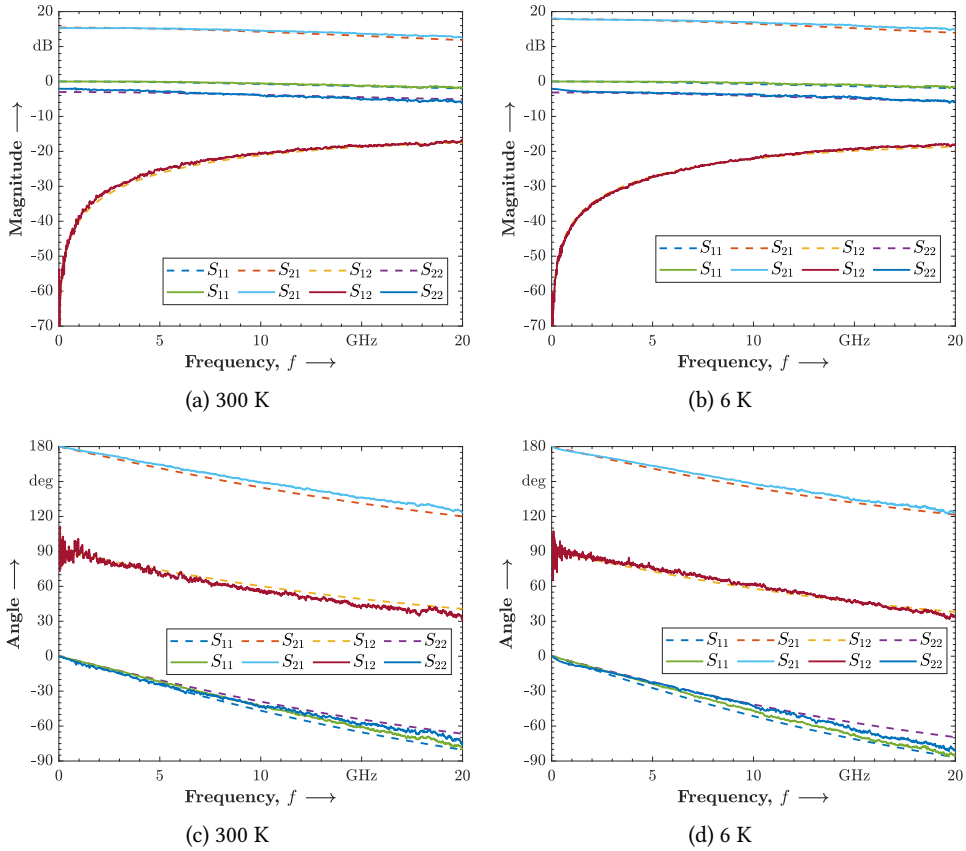


Figure 6.10: Transconductance g_m and drain-source conductance g_{ds} extraction: blue - W = 2.4 μm, red - W = 4.8 μm, yellow - W = 9.6 μm.

In order to validate the extracted SSEC parameters, the simulations using the obtained parameters using LTSpice software and the comparison with the measured S-parameter data are performed. The results are presented in Fig. 6.11. The deviations are less than 1 dB for magnitude and 10 degrees for angle over the whole frequency range. That shows the fair quality of these measurements, as well as the validity of the chosen small-signal equivalent circuit in application to this case.

6.1.6 Transition and maximum oscillation frequencies extraction

Transition frequency f_t and maximum oscillation frequency f_{max} are important figures of merit of MOSFETs in high-frequency applications. f_t determines the frequency at which the current gain goes down to 0 dB. f_{max} determines the maximum frequency at which amplification of power takes place under perfect matching conditions with S_{12} = 0 (unilateral power gain [93] higher than 0 dB). It is usually difficult to achieve f_t and f_{max} in a measurement environment,



(a) 300 K (b) 6 K

(c) 300 K (d) 6 K

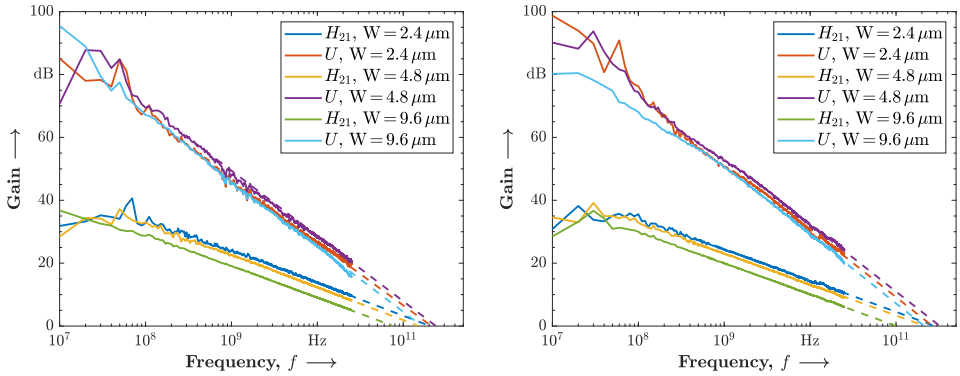
Figure 6.11: The comparison of the simulated with extracted SSEC (dashed lines) and measured (solid lines) scattering parameters data of the nMOS-FET array, W = 4.8 μm.

but they can be extrapolated from the measured high-frequency data or calculated from SSEC parameters [88]:

$$f_t \approx \frac{g_m}{2\pi C_{gs}(1+\frac{C_{gd}}{C_{gs}}) + (R_s+R_d)(C_{gd}/C_{gs}(g_m+g_{ds})+g_{ds})} \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{6.22}$$

$$f_{max} \approx \frac{f_t}{2\sqrt{g_{ds}(R_g+R_s)+2\pi f_t R_g C_{gd}}} \approx \sqrt{f_t/(8\pi R_g C_{gd})} \tag{6.23}$$

The extrapolation is performed by plotting values of the current gain H_{21} and the unilateral power gain U over frequency and extending the resulting lines until they reach 0 dB [94, 93]:



(a) 300 K (b) 6 K

Figure 6.12: The extrapolations of H_{21} and U for three nMOS devices at 300 K and 6 K [81].

$$H_{21} = \frac{-2S_{21}(R_{01}R_{02})^{0.5}}{(1-S_{11})(Z_{02}+S_{22}Z_{02})+S_{12}S_{21}Z_{02}} \tag{6.24}$$

$$U = \frac{|S_{21}/S_{12}-1|^2}{2K\cdot|S_{21}/S_{12}|-2Re\{S_{21}/S_{12}\}}, \tag{6.25}$$

where

$$K = \frac{1+|S_{11}S_{22}-S_{12}S_{21}|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}||S_{21}|}$$

and $Z_{01} = R_{01} = Z_{02} = R_{02} = Z_0 = 50\,\Omega$.

The extrapolations of H_{21} and U for all three nFET devices at 300 K and 6 K are presented in Fig. 6.12. The comparison of extrapolated and calculated values is demonstrated in tables 6.2 and 6.3.

It can be observed, that both f_t and f_{max} increase with temperature decrease. It can be explained by the increase of transconductance g_m, which contributes to both of the parameters and was shown as the only significantly changing parameter in the previous subsection.

While the results for the methods are consistent with each other, both of them have limitations and provide only approximate results. The extrapolation method produces an error due to the logarithmic scale of the frequency axis and noise in the measured data. The calculation uses SSEC parameters, which are valid only up to 20 GHz, while at higher frequencies the SSEC could become more detailed and complicated. Thus, while this measurement is still useful for a rough estimation of transistor capabilities, higher frequency measurements are needed in order to provide more accurate results.

	nFET, $W = 2.4\,\mu$m		nFET, $W = 4.8\,\mu$m		nFET, $W = 9.6\,\mu$m	
	f_t	f_{max}	f_t	f_{max}	f_t	f_{max}
300 K (extrapolated)	220 GHz	230 GHz	160 GHz	240 GHz	75 GHz	170 GHz
300 K (calculated)	225 GHz	222 GHz	166 GHz	257 GHz	81 GHz	251 GHz
6 K (extrapolated)	300 GHz	270 GHz	210 GHz	330 GHz	100 GHz	220 GHz
6 K (calculated)	283 GHz	380 GHz	209 GHz	317 GHz	104 GHz	359 GHz

Table 6.2: f_t and f_{max}, extracted by extrapolation and calculation methods for three nFETs [81].

Medium-sized nFET	f_t	f_{max}
300 K (extrapolated)	160 GHz	240 GHz
300 K (calculated)	166 GHz	257 GHz
200 K (extrapolated)	180 GHz	260 GHz
200 K (calculated)	183 GHz	296 GHz
100 K (extrapolated)	190 GHz	300 GHz
100 K (calculated)	195 GHz	311 GHz
6 K (extrapolated)	210 GHz	330 GHz
6 K (calculated)	209 GHz	317 GHz

Table 6.3: f_t and f_{max}, extracted by extrapolation and calculation methods, for several temperatures and nFET W = 4.8 μm [81].

6.2 High-frequency noise measurements

Noise, as a term in electronics, is an undesired disturbance in an electrical signal. There could be several sources of noise, caused by different physical phenomena [84].

Thermal noise, also called Johnson-Nyquist noise, is caused by the random thermal motion of charge carriers inside the conductive material. It is unavoidable due to its thermal nature, and independent from applied voltages. Available thermal noise power N is determined with the equation:

$$N = k_B T B, \tag{6.26}$$

where k_B is the Boltzmann constant, T is the physical temperature, and B is the frequency bandwidth.

Shot noise, or Poisson noise, appears due to the discrete nature of the electric current, caused by carriers with fixed charge values. It appears in such devices as diodes or vacuum tubes, where the charge carriers flow across a barrier, where they have discrete arrival times. Shot noise results in current fluctuations, the root mean square of which is determined by:

$$\sigma_i = \sqrt{2qIB}, \tag{6.27}$$

where q is the elementary charge of a carrier, I is the DC current, and B is the frequency bandwidth. In the case of a matched load R, the noise power provided is:

$$P = \frac{1}{2} qIBR, \tag{6.28}$$

Flicker noise, also called $1/f$ noise because of $1/f$ power spectral density, is caused by a variety of phenomena, like the generation and recombination of carriers in semiconductor devices or impurities in a conductive channel.

Noise characteristics of single devices or complete circuits are important for IC design, and therefore should be properly extracted and included in the corresponding PDKs.

6.2.1 Noise characterization fundamentals

Every active two-port device has a gain G, which determines the ratio between the input and output signal, and the noise power N_{add}, that it adds to the output signal. In order to characterize the noise behavior of a two-port system, some figures of merit are used, which can be recalculated into each other.

Noise temperature T_{eq} is the hypothetical temperature of the load on the input of a "noiseless" two-port device, that would create the same amount of noise, created by the "noisy" device:

$$T_{eq} = \frac{N_{add}}{k_B B}, \tag{6.29}$$

Noise factor F determines the ratio between signal-to-noise ratios (SNR) on the input and output of the DUT:

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} = \frac{S_{in}/N_{in}}{G \cdot S_{in}/(G \cdot N_{in} + N_{add})} = 1 + \frac{N_{add}}{G \cdot N_{in}} \tag{6.30}$$

$$T_{eq} = \frac{N_{add}}{k_B B}, \tag{6.31}$$

N_{in} here is the noise power, generated by an input termination at standard temperature $T_0 = 290\,\mathrm{K}$, hence $N_{in} = k_B B T_0$, and

$$F = 1 + \frac{T_{eq}}{T_0} \qquad T_{eq} = (F-1)T_0 \tag{6.32}$$

It is also common to use noise figure NF, which is defined as noise factor in dB:

$$NF = 10 \cdot log_{10}(F) \tag{6.33}$$

T_{eq} is usually more convenient than F or NF for use in cryogenic environments, as it is not normalized on standard room-temperature value N_{in}, and therefore easier to understand and operate with, nevertheless, all these values can be used for noise behavior description.

Moreover, the noise figure can be expressed in dependence on the complex source admittance. There are four classical noise parameters: equivalent noise resistance R_n, minimum noise figure F_{min}, complex optimum noise reflection coefficient Γ_{opt}, and characteristic impedance Z_0. The knowledge of all four gives information about the SNR degradation for any matching scenario:

$$F = F_{min} + \frac{4R_n \cdot |\Gamma_S - \Gamma_{opt}|^2}{Z_0 \cdot (1 - |\Gamma_S|^2) \cdot |1 + \Gamma_{opt}|^2} \tag{6.34}$$

Here, F is the noise factor, expected for the source admittance defined through the complex reflection coefficient Γ_S, while the smallest possible noise factor is F_{min} and it occurs for $\Gamma_S = \Gamma_{opt}$. R_n describes how big the change of the noise factor is with the difference between Γ_S and Γ_{opt}.

The four noise parameters are required for some test cases, one of which is noise de-embedding. Noise de-embedding is performed when the DUT is surrounded by embedding with considerable transmission and noise characteristics.

In the case of a cascade of two-port devices, when each of them has available gain $G_1, G_2 \ldots G_n$ and noise factor $F_1, F_2 \ldots F_n$, a Friis formula is used in order to determine the total noise factor or noise temperature of the system:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \tag{6.35}$$

$$T_{eq} = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \cdots + \frac{T_n}{G_1 G_2 \cdots G_{n-1}} \tag{6.36}$$

In the case of noise measurement, when the measurement chain in addition to DUT contains lossy lines and amplifiers with known characteristics, the Friis formula helps to extract the noise factor of the DUT itself.

Another important issue is the DUT mismatch. As shown in the previous section, the transistor arrays are poorly matched with the line, and that also influences the result of the noise measurement. A simple correction is proposed in [84], p. 511:

$$F_m = 1 + \frac{F - 1}{1 - |\Gamma_{in}|^2} \Leftrightarrow F = (F_m - 1) \cdot (1 - |\Gamma_{in}|^2) + 1, \tag{6.37}$$

where F_m is the measured noise factor of the mismatched device, Γ_{in} is the input reflection coefficient, and F is the noise factor that is achievable with perfect noise matching. For a matched load Γ_{in} can be calculated from the input impedance or from S-parameters $\Gamma_{in} = S_{11}$ [84], p. 560.

6.2.2 Noise measurement methods

The Y-factor method is a common and reliable way to measure noise temperature. It is useful when two well-characterized noise sources are available, for example, a calibrated diode in an on (T_{hot}) and off (T_{cold}) state. They are applied in turn to the DUT's input, and by comparison of the two output noise powers $N_{out,hot}$ and $N_{out,cold}$, the noise added by the device is calculated [84]:

$$Y = \frac{N_{out,hot}}{N_{out,cold}} \tag{6.38}$$

$$T_{eq} = \frac{T_{hot} - Y T_{cold}}{Y - 1} \tag{6.39}$$

Another method called the Cold Source method (also referred to as the "direct noise measurement method" [95]) is more complicated, but widely used due to its implementation in the VNA instruments [96], together with some useful features like input impedance tuning. This option speeds up the measurement procedure and helps to improve the measurements in some test cases.

Two measurements are done during the Cold Source method procedure: one is standard S-parameter measurement in order to determine the available gain G of the DUT. During the second one, the input port is turned off (equivalent to 50 Ω load at room temperature, producing $N_{in} = k_B B T_{room}$) and the output noise power N_{out} of the transistor is measured with a low-noise power receiver. Using the obtained data, added noise power N_{add}, noise temperature T_{eq}, and noise factor F can be calculated:

$$N_{out} = (N_{in} + N_{added}) \cdot G \Leftrightarrow \tag{6.40}$$

$$N_{added} = \frac{N_{out}}{G} - N_{in} \Rightarrow T_{eq} = \frac{N_{added}}{k_B T} \tag{6.41}$$

$$F = \frac{N_{out}}{G N_{in}} \tag{6.42}$$

Both methods have been tried out during the experiments, however, more attention was paid to the Cold Source method due to its availability in the VNA. Some adjustments have been done due to the cryogenic application.

6.2.3 Noise measurements in the cryosetup

In order to successfully implement the Cold Source method for noise measurement, some conditions should be fulfilled. The first one - the input noise power should be well-defined. In the case of room temperature measurements, the current temperature in the room, hence, the temperature of the load on the input will determine the input power, and this value should be entered in the VNA. In the case of a lossy line between the load and DUT, like a coaxial cable or the RF probe, this value will stay the same, as the line has the same room temperature, and is seen by DUT as a matched load directly at the input.

The available gain of the device itself is measured during S-parameter measurement. In the case of RF probing, SOLT calibration with a specified calibration substrate should be done.

The output line should have as low attenuation as possible, as it should be de-embedded from the measured output power. At room temperature that is also not a complicated procedure, as the lossy line with loss L and temperature T_L has T_{eq} and F of [84], p. 504:

$$T_{eq} = (L-1)T_L \qquad F = 1 + (L-1)\frac{T_L}{T_0}. \tag{6.43}$$

For $T_L = T_0$ that means, that $F = L$. By measuring the L during calibration, it is possible to remove its influence.

Unfortunately, due to the necessity of cooling down the DUT, the RF wires have to be long in order to keep thermal isolation between the thermal stages, causing the presence of lossy lines in the input and output of the DUT (Fig. 6.13). Due to the fact, that each stage, the probes, and the DUT have different physical temperatures, for each part of the chain $T_L \neq T_0$. In turn, the ends of the RF cables are thermalized at different temperatures, which leads to a temperature gradient over each cable, that is difficult to calculate, hence, accurately determine the noise properties of the cables.

In order to estimate the input power in this configuration, formulae 6.36 and 6.43 should be applied:

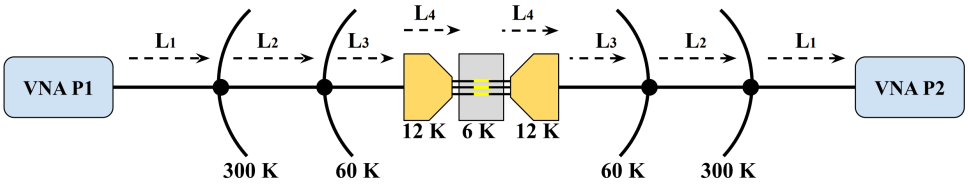


Figure 6.13: Schematic representation of the cryogenic noise measurement chain.

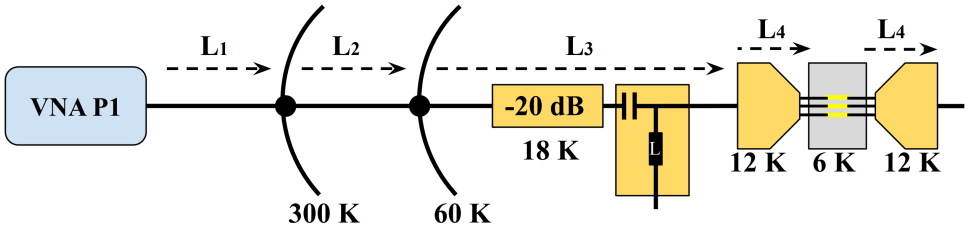


Figure 6.14: Schematic representation of the input chain with cryogenic attenuator.

$$T_{in} = \frac{T_{RT}}{L_2 L_3 L_4} + T_{cables} = \frac{T_{RT}}{L_2 L_3 L_4} + \frac{T_2(L_2 - 1)}{L_3 L_4} + \frac{T_3(L_3 - 1)}{L4} + T_4(L_4 - 1) \tag{6.44}$$

Here T_2, T_3, and T_4 are the temperatures of the cables. In case of the assumption, that the real temperature of the cable is somewhere between the temperatures of its ends and the separately measured losses of each cable in the chain are taken, an error of $\pm 33\,K$ for T_{eq} or around $\pm 0.25\,dB$ for NF at 20 GHz is present for the setup and the test case.

In order to improve the cryogenic noise measurements, it is common to add a cryogenic attenuator close to the DUT [97]. In this case, a bias-tee is also required, as the signal line for gate bias is being used (Fig. 6.14).

In this case, the attenuator with a well-defined temperature (measured by an additional temperature sensor) attenuates most of the noise power, coming from the room temperature load, and adds N_{add}, which is well-defined. This approach in this case reduces the N_{in} down to approx. 20 K, and its error down to $\pm 0.7\,K$ for T_{eq} or $\pm 0.005\,dB$ for NF at 20 GHz. This approach is also very useful for low-noise applications, as it reduces N_{in}, making the N_{add} easier to distinguish.

In turn, the output chain attenuates the output signal and adds noise power N_{add}, which can be estimated in a similar way as the input chain, but can be also calibrated by the connection of a well-defined matched load to the output RF probe. The attenuation is also determined during SOLT calibration, and the output power of the DUT can be determined. However, the total attenuation can be up to -4 dB at cryo and up to -5 dB at room temperature (Fig. 3.9), which is a big value for RF noise measurements. If the DUT output power level is too low, the measurement will be not valid or even not possible.

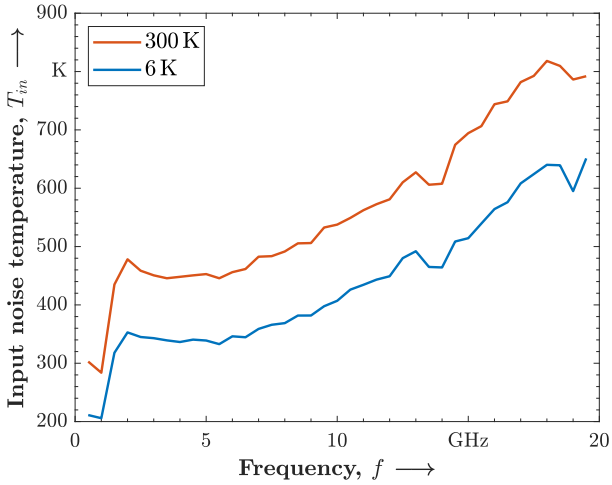


Figure 6.15: Minimum DUT input noise temperature required for the condition of DUT output power to be above the receiver noise level, for the nFET with W = 2.4 μm [81].

The S-parameters of the DUTs in section 6.1 have been measured, and the RF chain and VNA with certain specifications have been operated, so the only way to increase the receiver input power is a higher input load noise temperature. In the following analysis, the minimum T_{in} needed to be above the receiver noise level is determined.

In the case of noiseless DUT, the following condition should be fulfilled:

$$T_{in} \cdot G_{DUT}/L_{chain} > T_{receiver} \tag{6.45}$$

Then with known device available gain, cable losses, chain equivalent noise temperature, and receiver noise, this can be rewritten as:

$$T_{in} > \frac{L_{chain} T_{receiver}}{G_{DUT}}, \tag{6.46}$$

where $T_{receiver} = 290\,K \cdot (10^{NF/10} - 1)$. NF can be taken from the VNA manual [98].

The result is presented in Fig. 6.15. Unfortunately, even room temperature termination on the input is not enough for reliable noise measurements in this setup. An additional calibrated noise source can be used instead, however, with higher temperatures the problem of accurate calibration of the noise source appears. E.g., Keysight 345C calibrated noise source can provide T_{eq} of more than 7000 K, but the provided calibrated value has an error of 0.01 dB, which means T_{eq} error of more than 16 K.

The required DUT amplification G_{DUT} at 20 K input noise temperature has been calculated using the same approach. It turned out to be 30 dB at 20 GHz. That value is 15-20 dB higher than the measured available gain of the DUTs.

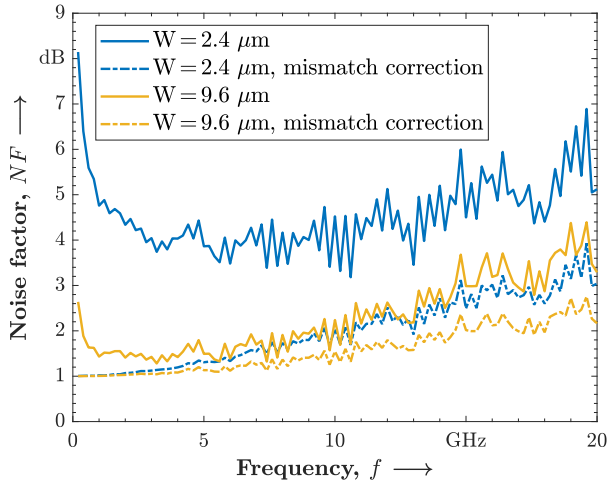


Figure 6.16: Noise measurements of two transistor arrays at room temperature. [81].

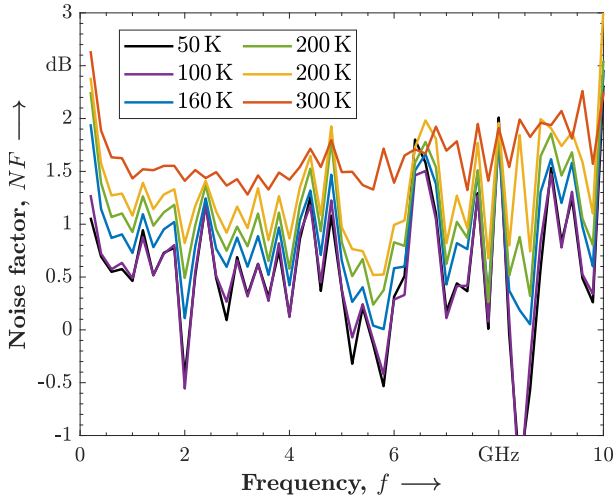


Figure 6.17: Noise measurement at different temperatures for W = 9.6 μm transistor array [81].

6.2.4 Measurement results

The noise measurements at room and cryogenic temperatures using the Cold Source method have been conducted. Room temperature results for transistor arrays with W of 2.4 μm and 9.6 μm are presented in Fig. 6.16. As expected, the measurements are not reliable: large deviations in the curve and large inaccuracies do not allow us to make certain conclusions regarding the noise behavior. Implementation of the noise correction (equation 6.37) makes the curves smoother at frequencies below 4 GHz, however, the mismatch is large in this region, so the reliability of this method is questionable.

The attempt to perform low-temperature measurements is presented in Fig. 6.17. As the temperature control is performed with the local sample heater, and the attenuator is placed on a probe holder with a long thermal braid (Fig. 3.8), its temperature is always much lower than RT and gets lower with the decrease of the sample temperature. That results in a decreased N_{in} to the DUT, hence, smaller DUT output power and larger noise in the measurement curve.

With the decrease in temperature, a decrease in thermal noise is expected. The tendency of the noise measurement curve to go down with temperature in Fig. 6.17 can be observed. That is consistent with the expectations, but, unfortunately, quantitative conclusions are not possible under these circumstances.

6.3 Conclusions

The high-frequency behavior up to 20 GHz of 22 nm FD-SOI technology transistor structures has been tested in the cryogenic environment. Small signal equivalent circuit parameters have been extracted at some temperatures from 300 K down to 6 K. It was shown, that the capacitances do not significantly change over temperature, while the main impact on cryogenic behavior is introduced by the change in transconductance g_m, which shows the same value as extracted from DC measurements. f_t and f_{max} have been also determined for the measured structures, both of these values are higher at 6 K, compared to RT.

Unfortunately, noise measurements with the fabricated DUTs are complicated and can't be done with the current setup configuration. There could be two possible solutions. The first is the improvement of the matching between the line and the DUT input, leading to an improved S_{21}-parameter. That would require the design of matching structures on the chip. Another possible solution is the use of an additional cryogenic amplifier with well-defined self-noise. Both of these solutions can increase the DUT output power, which should be significantly above the VNA receiver noise level.

Personal contribution includes development and verification of the measurement and initial data processing procedures, as well as scientific supervision of a master student and support in measurement performance and data processing.

Chapter 7

Self-heating effects in CMOS technologies

Highly integrated system-on-chip solutions can be used as control and read-out electronic systems for several types of qubits, providing the future opportunity to scale up the number of qubits in quantum information processors [36]. Some of the design concepts even propose the placement of control electronics together with the qubit array on the same die [99].

However, semiconductor-based integrated circuits produce a relatively large amount of Joule heat. As already reported by several authors [100, 101, 102, 103, 104, 105], the presence of various scattering processes self-heats the transistor and increases its temperature compared to the cryogenic environment. That could influence the self-behavior of the single devices, as well as the devices placed on the same chip or the ones which are thermally connected to the circuit. That should be taken into account for the development of the proper cryogenic process design kit (PDK), IC, and system design. Moreover, self-heating is not taken into account in most of the literature on cryogenic effects research in CMOS devices. In the case of quantum computing, electro-thermal effects in the CMOS could severely degrade the performance of the qubits or even render them unusable.

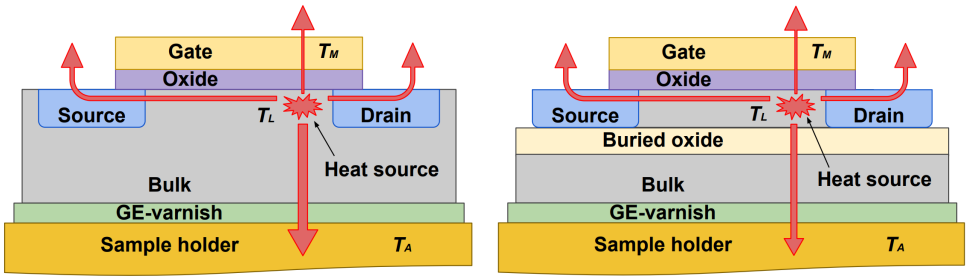
Therefore, understanding the way heat is generated in the active region of the transistor and how it diffuses away from the hot spot through the different thermal paths, becomes essential for the design of high-performance integrated circuits for cryogenic applications and the overall system design.

The purpose of this chapter is to investigate and compare self-heating effects (SHE) in 65 nm bulk CMOS and 22 nm FD-SOI technologies. The thermal properties of the transistor and its surroundings have been investigated using the gate resistance thermometer technique.

Part of the data, presented in this chapter, has been presented in IEEE 14th Workshop on Low Temperature Electronics [106] and published in IEEE Transactions on Electron Devices [107].

7.1 Approach

The thermal behavior of a MOSFET is explained by the interplay of electrical and thermal parameters, such as Joule power P dissipated by the device, thermal resistance R_{th} and thermal capacitance C_{th}, surrounding the active region of the transistor. In the case of a system in thermal equilibrium, where the transient thermal effects are neglected, then most of the carrier energy is transferred to the lattice because of carrier scattering [108] in the active channel,



(a) (b)

Figure 7.1: The principle schemes, showing four thermal paths of the n-type transistor, fabricated in 65 nm bulk CMOS (left) and 22 nm FD-SOI (right) technologies.

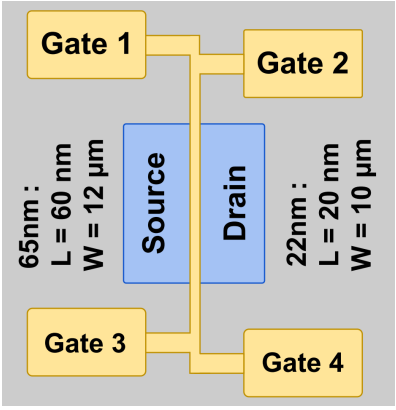


Figure 7.2: Layout scheme of the measured samples.

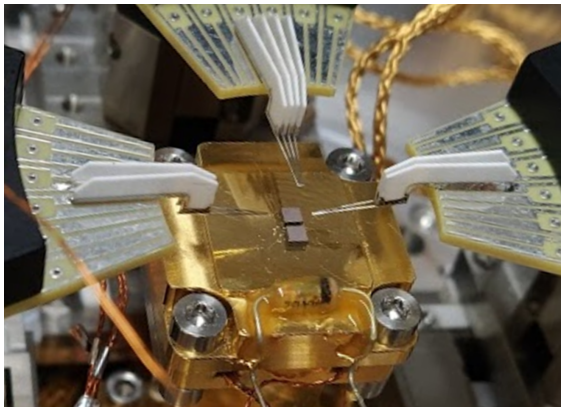


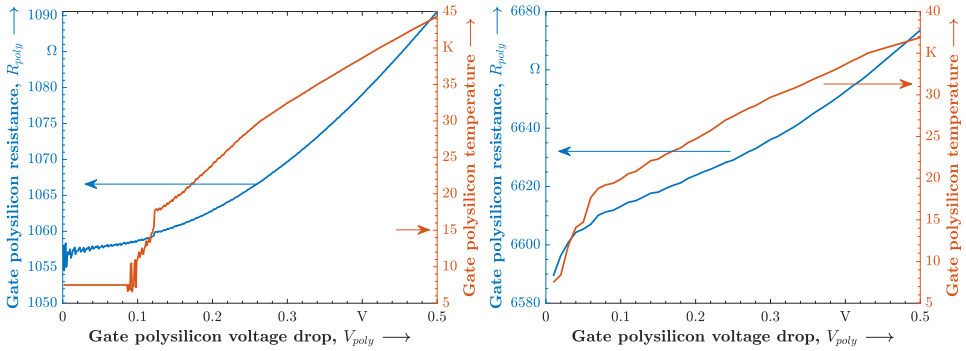
Figure 7.3: Photo of the working area of the setup.

which then translates into an increase in the local temperature T_L [109]. This is known as the self-heating effect [110]. As the Joule power is a function of the bias conditions, such as drain current I_{ds}, gate voltage V_{gs}, and drain voltage V_{ds}, then T_L also becomes a function of the bias conditions.

The thermal equilibrium of the transistor is reached when the cooling power, determined by temperature difference and thermal conductivity through the 4 different paths (as shown in Fig. 7.1), is equal to the self-heating power.

The main difference between the technologies will be the presence of the buried oxide (BOX) in FD-SOI technology, which introduces more thermal resistance to the thermal path, going into the substrate.

The differential temperature $\Delta T = (T_L - T_A)$ is defined by the temperature drop across the four thermal paths. Therefore, a way to indirectly measure T_L is by setting a thermometer as close as possible to the hot spot in the active channel. For that purpose, in this experiment structures with gate resistor thermometers [111], configured as a 4-terminal device as shown in Fig. 7.2,



(a) 65 nm bulk CMOS

(b) 22 nm FD-SOI

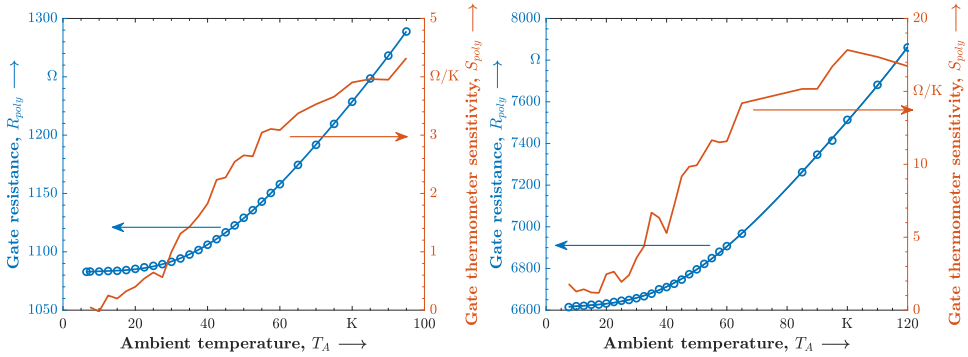
Figure 7.4: Dependence of gate polysilicon resistance and temperature on voltage drop.

have been designed. The self-heating structures were designed and fabricated in 65 nm CMOS and 22 nm FD-SOI technologies. The poly-silicon gate is used as a thermometer which is as close as possible to the source of heat produced in the active channel of the transistor. The self-heating test structure, fabricated in 65 nm technology has (W/L) = 12 µm / 60 nm geometry, in case of 22 nm - (W/L) = 10 µm / 20 nm.

The gate of the test transistor with its four contacts (Fig. 7.2) is used to calibrate the gate resistance as a function of the temperature, which is measured with the transistor in off mode. The DC probing configuration of the cryogenic setup (section 3.3) has been used for the measurements. The sample was glued to the sample holder with thermally conductive GE-varnish. The Keysight B1500A Semiconductor Device Analyzer was used for all the DC measurements.

In order to determine the reasonable bias voltage for the gate poly resistance measurement, the IV curves for both structures have been measured and recalculated to gate polysilicon resistance curves (Fig. 7.4). The base temperature for 65 nm and 22 nm samples are 6.5 K and 7.5 K respectively, due to different behavior of the cryosetup during these experiments. It is important to provide high accuracy of the measurement and avoid significant self-heating of the gate material. As a result, the bias voltage of 20 mV is chosen, as it provides Joule power of less than 400 nW for the 65 nm sample and less than 60 nW for the 22 nm one. This causes a slight increase in temperature for both of the structures, but it can be neglected even at the lowest possible heating power of a biased transistor.

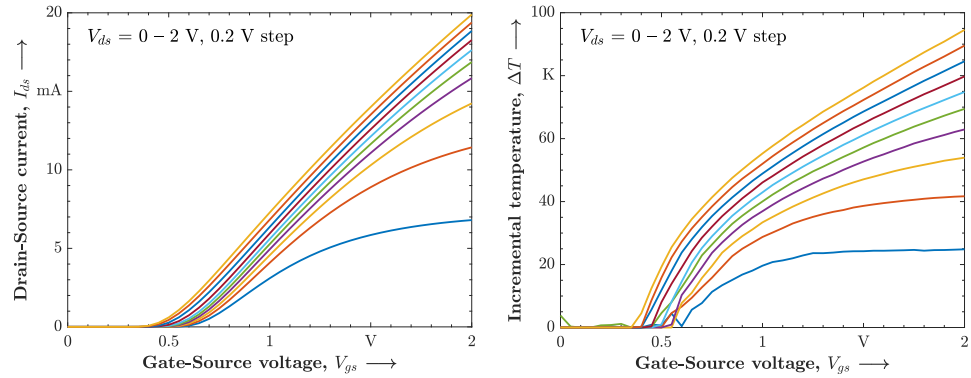
A temperature-controlled measurement of the gate resistance dependence with respect to the base temperature (see Fig. 7.5) has been performed. The results show that the polysilicon resistance R_g is almost constant for temperatures below about 15 K, which is a result of residual impurity scattering, due to the metallic behavior of polysilicon versus temperature [112]. As the resistance measurement accuracy in this range is around 0.3 Ω, data for 65 nm sample channel temperatures lower than 15 K is not reliable. A time of 1 s is set before each measurement point in order to achieve a state close to thermal equilibrium over the whole chip.



(a) 65 nm bulk CMOS [107]

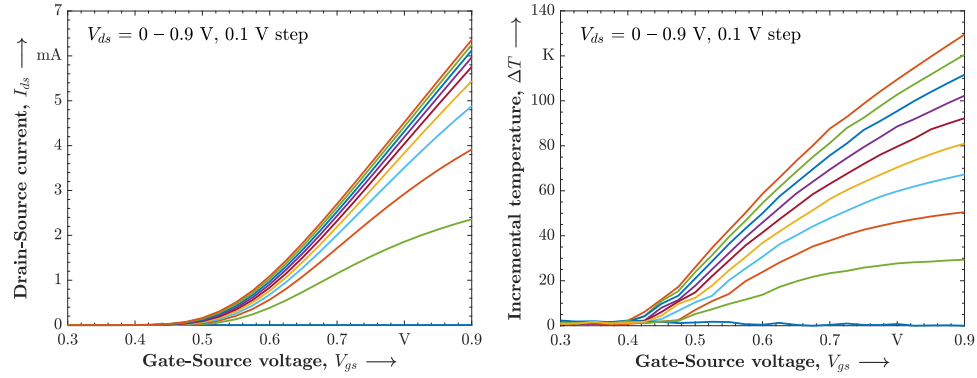
(b) 22 nm FD-SOI

Figure 7.5: Dependence of gate polysilicon resistance and temperature measurement sensitivity on ambient temperature.



(a) I_{ds} vs V_{gs}, 65 nm bulk CMOS [107]

(b) ΔT vs V_{gs}, 65 nm bulk CMOS [107]



(c) I_{ds} vs V_{gs}, 22 nm FD-SOI

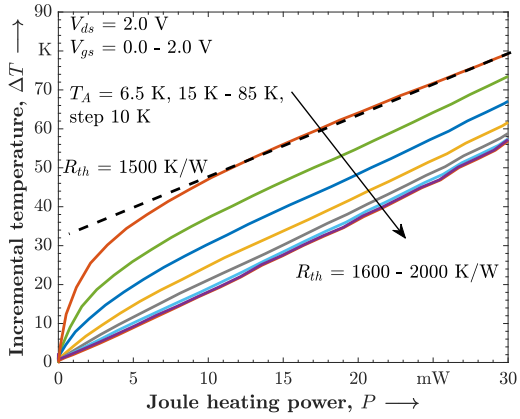
(d) ΔT vs V_{gs}, 22 nm FD-SOI

Figure 7.6: Measured $I_{ds} - V_{gs}$ characteristics and incremental temperature ΔT versus V_{gs} for samples in both fabrication technologies.

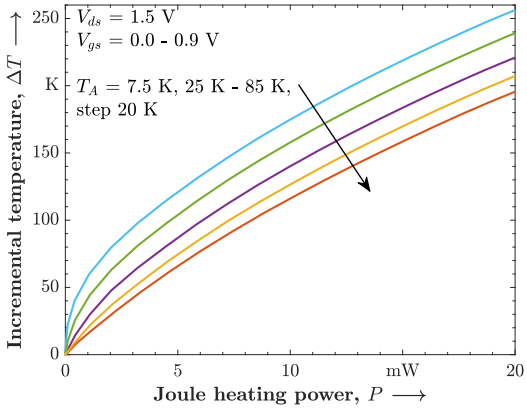
7.2 Results and analysis

The gate temperature data in Fig. 7.4, as well as $I_{ds} - V_{gs}$ characteristics with V_{ds} as a parameter in Fig. 7.6 have been plotted using the data in Fig. 7.5.

The 65 nm structure handles I_{ds} up to 20 mA, which is equivalent to a heating power P of 40 mW, at $V_{gs} = V_{ds} = 2.0\ V$. The 22 nm structure was biased up to $V_{gs} = V_{ds} = 0.9\ V$, which results in I_{ds} of 6.4 mA and P of 5.7 mW. Further increase of V_{gs} leads to gate leakage current up to 100 nA, which makes the gate resistance measurement unreliable. Nevertheless, V_{ds} can be increased up to 1.5 V, which increases the P up to 20 mW.



(a) 65 nm bulk CMOS [107]



(b) 22 nm FD-SOI

Figure 7.7: Measured incremental temperatures ΔT versus Joule power P at several ambient temperature values T_A for samples in both fabrication technologies.

As seen from Fig. 7.6, ΔT is a function of I_{ds}, V_{gs}, and V_{ds}. For the 65 nm sample at $V_{gs} = V_{ds} = 2.0\ V$ condition, ΔT raises up to 94 K. For the FD-SOI sample ΔT goes up to 130 K, although the Joule power is 7 times lower. This is partly the result of the smaller size of the 22 nm structure, but the main reason is the presence of BOX, which will be proven below.

Plotting the incremental temperature ΔT versus the Joule power (I_{ds} times V_{ds}) gives a better perspective, as it is related to the thermal properties, like the thermal resistance R_{th} (Fig. 7.7).

Since bulk CMOS and FD-SOI structures show different thermal behavior, both cases will be considered separately.

7.2.1 65 nm bulk CMOS SHE structure

The $\Delta T - P$ curve for $V_{ds} = 2.0\ V$ with V_{gs} sweeping from 0.0 to 2.0 V in Fig. 7.7a shows two regions: a nonlinear region for low Joule power magnitudes, and a linear region for high Joule power. Incremental temperature ΔT is related to the Joule power through the thermal resistance R_{th} as described by the equation:

$$\Delta T = R_{th} \cdot P \tag{7.1}$$

Fig. 7.8 allows for a better understanding of the thermal performance, which is based on the temperature dependence of the thermal resistance. The data shown in Fig. 7.8 have been replotted and fitted from various references [113, 114, 115, 116, 117, 118]. Because of the presence of SiO_2, the heat flow sees a higher thermal resistance when flowing from the hot spot towards the SiO_2. GE-varnish, which was used to glue the Si die to the cold plate, has higher thermal resistivity than Si, but the large thermal contact area and small thickness of the varnish layer make this path relatively high thermally conductive: estimation of conductivity is more than 10 W/K for a varnish layer versus less than 1 W/K for a tungsten needle. The

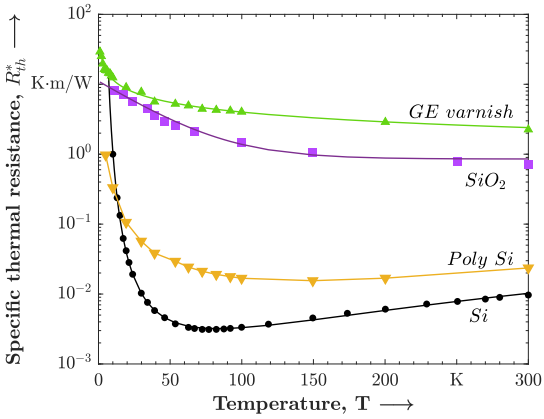


Figure 7.8: Specific thermal resistance R^*_{th} versus temperature for different materials [113, 114, 115, 116, 117, 118].

heat, generated at the active region of the channel, flows through the bulk and lateral paths of the drain and source, then through the vias and metal interconnects (Fig. 7.1). Under this thermal scenario, the thermal resistance of Si dominates the heat flow. In turn, any increase in temperature in the transistor will dramatically reduce the thermal resistance of Si by several orders of magnitude. The experimental data in Fig. 7.7a show the temperature raise from the 6.5 K cold-plate value up to about 100 K. Thus, the Si specific thermal resistance R^*_{th} swings from about 30 K·m/W down to 0.004 K·m/W (Fig. 7.8). This enables heat flow from the transistor channel through the Si out through the source/drain contacts and varnish layer, leading to thermalization of the transistor.

The profile of the $R^*_{th} - T$ curve for Si, SiO_2, and poly-Si (Fig. 7.8) is a function of the doping profile and sample thickness [113, 116, 119, 120, 121]. Therefore, the magnitude varies according to thickness and doping or composition in the case of poly-Si and SiO_2. In the case of Si, the minimum value R^*_{th} happens at about T = 75 K and moves to a lower or higher temperature, depending on the doping concentration. The higher Si doping concentration, the higher the magnitude of the thermal resistance and the higher the temperature at which it reaches its minimum value or inflection point [122].

In order to prove the Si thermal resistance domination over the other thermal components, the experiment was repeated for several higher temperatures, including T_A = 75 K, which is the temperature at which R^*_{th} gets its minimum value and has an inflection point. The incremental temperature ΔT versus the Joule power for V_{ds} = 2.0 V and V_{gs} swept from 0.0 to 2.0 V is shown in Fig. 7.7a. Starting from T_A = 60 K the $\Delta T - P$ relationship is almost linear with a slight second-order polynomial behavior. The derivatives ($d\Delta T/dP$) of lines for T_A higher than 60 K give a thermal resistance R_{th} of 1600-2000 K/W. This result indicates that R_{th}, measured at the gate at temperatures close to 75 K, changes slightly, which is consistent with Fig. 7.8. Because of the increased thermal resistance of silicon, the SHE effect is more pronounced at T_A lower than 60 K, remaining almost constant as the T_A rises.

The plot of the derivative ($d\Delta T/dP$) versus the measured temperature at the gate for both T_A = 6.5 K and 75 K, is shown in Fig. 7.9. The data at T_A = 6.5 K are given for V_{gs} sweep and V_{ds} equal 0.5, 1.0, 1.5 and 2.0 V; the data at T_A = 75 K are given for V_{ds} = 1.0. The R_{th} data, extracted at 6.5 K, nicely fits with that of 75 K, giving continuity to the R_{th} curve. The solid line is calculated from the specific thermal resistance R^*_{th} curve for Si (Fig. 7.8), with the assumption that the effective length versus effective area ratio is $7{\cdot}10^5$ m^{-1} as a fitting parameter. The thermal resistance curves, that are seen from the gate side, have the same shape as the thermal resistivity curve of Si. That confirms the hypothesis, that Si thermal resistance dominates over the other thermal components.

In addition to that, the modeling of the $\Delta T - P$ behavior has been performed, based on the approach, proposed in [103]:

$$\delta\Delta T = R_{th}(T_A + \Delta T) \cdot \delta P, \tag{7.2}$$

$$P = \int_0^{\Delta T} \frac{\delta\Delta T'}{R_{th}(T_A + \Delta T')}. \tag{7.3}$$

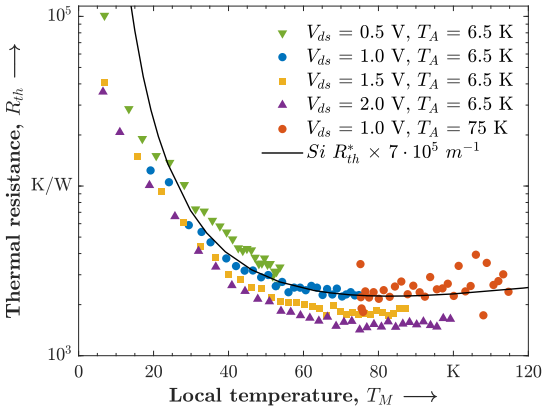


Figure 7.9: Extracted thermal resistance R_{th} seen from the gate as a function of the temperature T_M measured at the gate, 65 nm bulk CMOS [107].

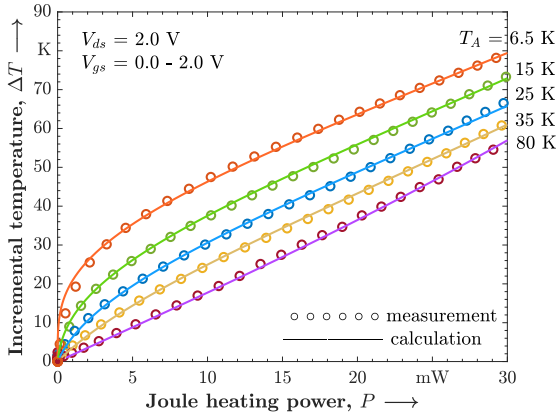
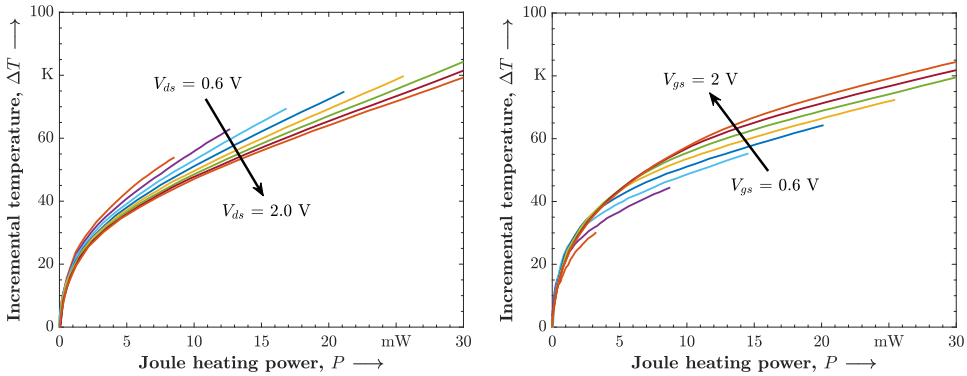


Figure 7.10: Calculated and measured channel temperature increase as a function of the dissipated power for several T_A, 65 nm bulk CMOS [107].

Silicon-specific resistance dependency over temperature multiplied by effective length versus area ratio, which serves as a fitting parameter, was taken as $R_{th}(T)$ function in (7.3). The result is shown in Fig. 7.10. The measured and calculated data agree with each other, and that additionally confirms the analysis above.

This approach allows for quite accurate thermal behavior modeling, especially for temperatures higher than 20 K. The only fitting parameter is the effective length versus area ratio. It is complicated to get it from the structure dimensions, but it can be extracted from one of the thermal curve measurements. The inaccuracy of this method at low temperatures can be connected to different doping profiles, changes in thermal conductance due to material thickness, and thermal interfaces between different materials.



(a) V_{gs} primary sweep and 0.1 V step V_{ds} secondary sweep

(b) V_{ds} primary sweep and 0.1 V step V_{gs} secondary sweep

Figure 7.11: Calculated and measured channel temperature increase as a function of the dissipated power at different bias conditions, 65 nm bulk CMOS [107].

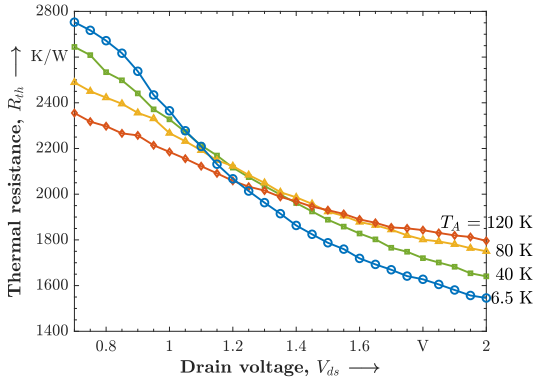


Figure 7.12: Dependency of the thermal resistance R_{th} (linear regime), seen from the gate side, on drain-source voltage V_{ds} for several ambient temperatures T_A [107].

The thermal resistance, extracted at the gate side, shows noticeable dependence on bias voltages. As V_{ds} increases from 0.5 to 2.0 V the $R_{th} - T$ curve shows a reduction in magnitude. It is especially clearly visible in Fig. 7.11. The dependency on bias voltages most likely is a result of the influence of bias voltages on the thermal embedding resistance of the transistor. Linear parts of the curves are parallel to each other in Fig. 7.11b and have decreasing slopes in Fig. 7.11a. That means, that V_{ds} increase causes a decrease in thermal resistance. The dependence of the thermal resistance R_{th} on the linear parts of the curves in Fig. 7.11a on V_{ds} for several T_A is shown in Fig. 7.12. The slope of this dependency decreases with temperature. Several approaches have been taken in an attempt to explain this effect, however, the reason for this thermal resistance decrease remains unclear. Moreover, this effect has not been observed in similar 40 nm bulk CMOS technology [105]. It should be a subject of further study.

7.2.2 22 nm FD-SOI SHE structure

A similar procedure to the one described in section 7.2.1 has been performed.

Unlike the bulk CMOS structure, the curves in Fig. 7.7b show different behavior. The thermal resistance of the thermal path also reduces with temperature, but no linear regime can be observed. This indicates that the thermal path from the hot spot to the coldplate is different from silicon thermal behavior.

The main difference in the described 22 nm technology is the presence of the buried oxide, as shown in Fig. 7.1. It is a layer of SiO_2 that separates the active channel of the transistor and the substrate. In case of the assumption, that most part of the heat flows through the bulk, the

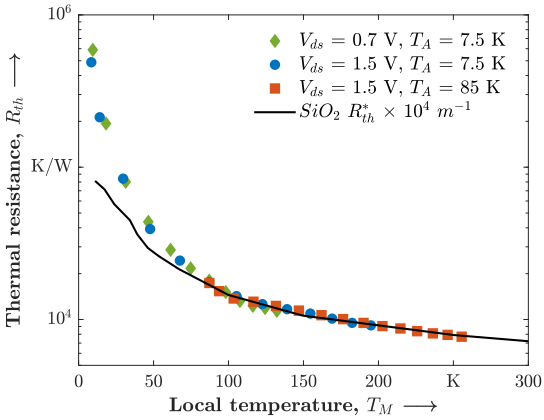


Figure 7.13: Extracted thermal resistance R_{th} seen from the gate as a function of the temperature T_M measured at the gate, 22 nm FD-SOI.

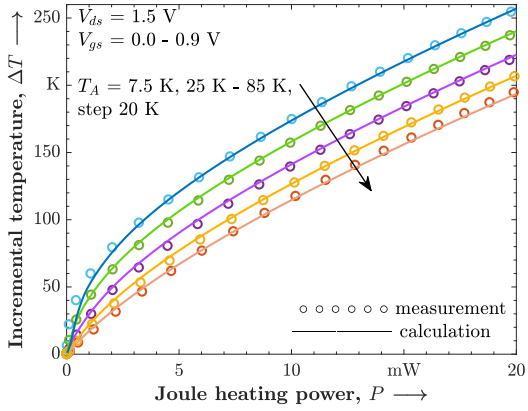


Figure 7.14: Calculated and measured channel temperature increase as a function of the dissipated power for several T_A, 22 nm FD-SOI.

thermal resistance seen from the gate side would behave similarly to SiO_2 specific thermal resistance.

The plot of the derivative ($d\Delta T/dP$) versus the measured temperature at the gate is shown in Fig. 7.13. Unlike the 65 nm sample, thermal resistance here does not depend on the bias conditions, and all the R_{th} vs T_L dependence curves are overlapping. By introducing again the effective length versus area ratio, the SiO_2 specific thermal resistance R^*_{th} curve is added to this graph. Similar to the previous case, this curve nicely fits the measured data at temperatures higher than 85 K. Qualitatively both curves show an increase in R_{th} at lower temperatures; the quantitative difference could be again explained by the different thermal behavior of a thin SiO_2 layer [123], as well as the influence of the material interfaces.

Using formula 7.3 and the fit for SiO_2 R^*_{th} the ΔT vs P behavior for a wide range of temperatures can be modeled with a quite high accuracy.

All this confirms that the SiO_2 thermal resistance dominates over other thermal components in the 22 nm FD-SOI structure. Although the R^*_{th} of SiO_2 is relatively high, compared to Si or metals, most part of the heat flows through BOX, as the cross-section area of this channel is much larger than those of drain and source contacts.

This also indirectly proves, that the main thermal path in the 65 nm bulk CMOS structure is the one through the substrate, as the absence of the BOX even more reduces the thermal resistance of the substrate thermal channel.

Both of these cases show, that the most important role plays the material, which is the closest to the hot spot of the structure. This happens due to the fact, that the highest thermal resistance on the way from the hot spot to the cold plate of the cryostat is provided by the material, surrounding the hot spot, due to the small cross section, which increases in proportion to squared distance.

7.3 Distribution of the temperature

In sections 7.2.1 and 7.2.2 the thermal behavior of single structures is described. Nevertheless, that analysis does not explain, how big is the influence of one device on the other, placed near on the same chip. In order to get a hint of how far is the influence of local heating, a simplified temperature distribution model is built.

The assumption that the dimensions of the chip are much bigger than the thermal influence of the single device is made. That allows to consider the hot spot as a point on a substrate surface, and the substrate as a silicon box with infinite surface area and thickness (Fig. 7.15).

The Joule heat flow density at the distance x to the heat source is determined by the ratio of Joule heating power to the area of the hemisphere with radius x:

$$\delta = \frac{P}{2\pi x^2}, \tag{7.4}$$

where δ is the Joule power density on the distance x from the heat source.

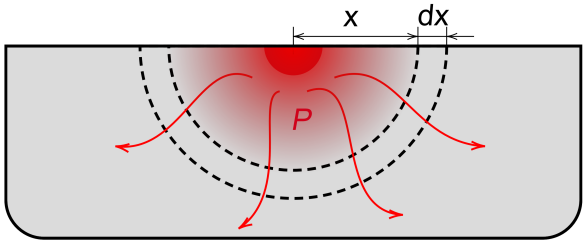


Figure 7.15: Simplified temperature distribution scheme.

In order to determine the temperature T in coordinate x, a layer dx is selected in the Joule heat spreading field. The temperature drop in this layer is:

$$dT = \delta \cdot R^*_{th}(T) \cdot dx. \tag{7.5}$$

After moving $R^*_{th}(T)$ to the left part of the equation, both sides can be integrated, assuming that the temperature far away from the hot spot equals T_A:

$$\int_T^{T_A} \frac{dT}{R^*_{th}(T)} = \int_a^{\infty} \frac{P}{2\pi x^2} dx, \tag{7.6}$$

$$\frac{P}{2\pi a} = \int_{T_A}^{T} \frac{dT}{R^*_{th}(T)}, \tag{7.7}$$

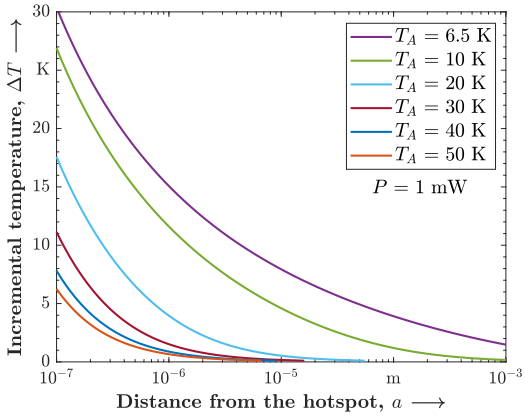
$$a = \frac{P}{2\pi \int_{T_A}^{T} \frac{dT}{R^*_{th}(T)}}, \tag{7.8}$$

where a is the distance from the hot spot, T_A is the ambient temperature, T is the temperature at the distance a, P is the Joule heating power and $R^*_{th}(T)$ is the specific thermal resistance of the material.

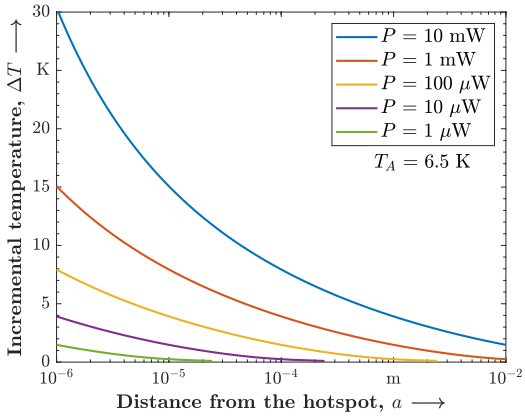
The case close to the measurement conditions is considered: T_A is 6.5 K, $R^*_{th}(T)$ of silicon is taken from Fig. 7.8. The results of equation 7.8 for different P and T_A are presented in Fig. 7.16.

Due to the steep increase of Si $R^*_{th}(T)$ at temperatures lower than 50 K, the temperature drops very fast from any temperature to 50 K, and then the decrease becomes flatter. For the same reason, the temperature spreads farther with the decrease of T_A (Fig. 7.16a). This distribution stays almost constant at T_A higher than 50 K.

It is also predictable, that the increase of Joule power P leads to an increase in distance, where the increased local temperature will be observed (Fig. 7.16b). It is seen, that even for 1 μW of power, the ΔT of 0.3 K will be detected at a 10 μm distance. For 1 mW of power, which is the first estimate of the power budget for a qubit control chip in [75], the increase of 1 K is predicted for a 2 mm distance, which exceeds the chip dimensions.



(a) different ambient temperatures T_A



(b) different Joule powers P

Figure 7.16: Modeled dependence of temperature versus distance from the hotspot.

Of course, this model is very simplified, but it should give a hint on temperature distribution at low Joule heating powers. Unlike the model, in reality, a chip has a thickness of less than 1 mm, and it is mounted on a cold plate with glue with a thermal conductivity lower, than silicon one. That means, that the increase of the substrate temperature would be even higher.

This effect will be even more pronounced at lower temperatures, at which the qubit is operated, due to a high decrease in specific thermal resistance with the decrease of temperature (Fig. 7.8). It would be also more difficult to model thermal behavior at temperatures lower than 1 K, as R_{th} will highly depend not only on temperature, but also on the purity and doping of the materials, as well as the quality of thermal contacts.

In order to achieve experimental results on the temperature distribution over the chip, an additional measurement is performed. The chip has other similar structures, placed at different distances from the measured one. These structures are activated one by one and while using

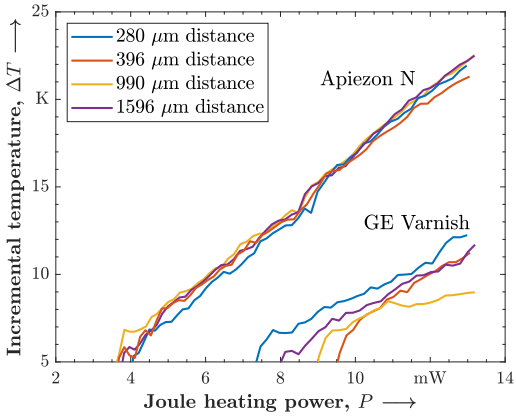


Figure 7.17: Measured incremental temperatures ΔT of one structure versus Joule power P, produced by other structures on the chip.

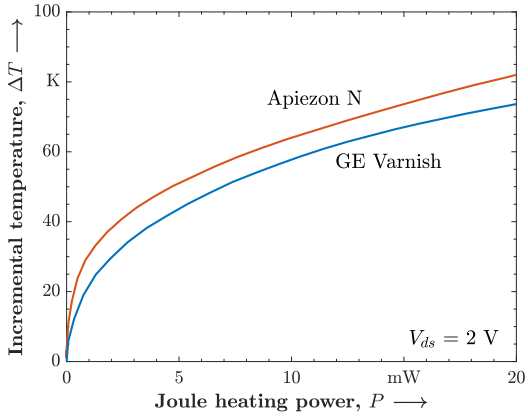


Figure 7.18: Measured incremental temperatures ΔT versus Joule power P for the same 65 nm structure, mounted by two types of glue.

them as heat sources the temperature at the first SHE structure is measured. This measurement is repeated for two different types of glue for sample mounting: Apiezon N and GE varnish, which have a thermal conductivity of 0.005 W/(K·m) and 0.062 W/(K·m) respectively at 4.2 K. The results of this measurement are presented in Fig. 7.17.

Predictably, the result depends on the thermal conductivity of the used glue. The measurement is performed in the region of low-temperature measurement accuracy (Fig. 7.5a), and therefore the result is noisy, especially in the case of GE varnish.

It is observed that the result of the measurement does not depend on the distance of the heat source from the measurement place, unlike the result of the model. That happens due to two reasons. First of all, the thermal conductivity of the glue is quite high, which leads to an increase in the temperature of the whole substrate material. The second reason is that even

the closest heating device is too far away to be able to detect the temperature distribution: due to the increased chip temperature, the temperature decreases faster with the distance.

In order to see the influence of glue on the thermal behavior of the structure, the procedure is performed for the same sample, mounted with two different types of glue, as described in sec. 7.2 (see Fig. 7.18). It is seen, that the increase in chip temperature, caused by low thermal connection to the coldplate, provided by glue, influences the local temperature rise.

7.4 Conclusions

Experimental results from self-heating structures, fabricated using commercial 65 nm CMOS and 22 nm FD-SOI technologies, have been introduced. In these cases, the measurements were performed on a bare die attached with thermally conductive glue to the cold plate of the cryostat. The thermal paths determined by the bulk, source, drain, and gate have been considered.

The thermal behavior of the structures is mostly determined by the material, surrounding the structures. In accordance with this, the FD-SOI structure shows more pronounced SHE and can heat up locally to more than 200 K. That from one point of view helps to avoid some cryogenic effects, from another - reduces the cryogenic benefits, like lower noise, leakages, etc.

The distribution of temperature in silicon substrate has been modeled. That showed a noticeable temperature increase around the hot spot. Apart from that, the way how the sample is mounted on a cold plate plays a significant role in local device temperature, as well as the temperature of the whole substrate. That leads to the conclusion, that implementing temperature-sensitive devices, e.g. qubits, on the same silicon die with control electronics, is not reasonable. As semiconductor qubits operate at mK temperatures, where this effect is even more pronounced, such integration would lead to severely degraded qubit performance. Therefore, the qubit should be as good as possible thermally decoupled from the control electronics.

Another consequence of far temperature propagation is the thermal interaction of the transistors in highly integrated circuits, causing the change in each other's electrical behavior. That means, that even if the single device is characterized at a certain temperature, its characteristics will not stay the same during IC operation. This change will be quite difficult to predict due to frequent changes of dissipated power by each device.

This work also prompts the development of a thermal de-embedding technique that enables the creation of dynamic thermal models for CMOS technologies. These electro-thermal models should serve the purpose to reduce the thermal load, either by modifying the technology for specific cryogenic applications, such as bulk thinning or metal pillars in the bulk as heat exchangers, among other alternative approaches. Having a bias- and technology-dependent electro-thermal model should serve for the proper design of integrated circuits for cryogenic applications.

Personal contribution includes verification and performing all the measurements shown, data processing, extraction of key results, and publishing.

Chapter 8

Summary, conclusions, and outlook

8.1 Summary

Quantum computing is expected to provide solutions for certain tasks exponentially faster than any modern high-performance computer system. In order to operate millions of qubits, required for universal QC realization, it was proposed to use local classical circuitry, that brings control and read-out to the lowest temperature stage, next to the qubits themselves [9]. In turn, the design of such circuitry is complicated by the absence of cryogenic models and lack of knowledge in the cryogenic operation of CMOS technologies.

In the framework of this project, DC and RF characterization up to 20 GHz of single devices fabricated in 65 nm bulk CMOS and 22 nm FD-SOI technologies has been performed in a cryogenic environment down to 6 K. For this purpose a cryogenic setup including the configuration for needle probing has been implemented and characterized. The chips with single-device test structures in both technologies have been designed and measured.

DC research of 65 nm bulk CMOS samples reproduced and confirmed the results of other scientific groups for the same or similar technologies. The cryogenic effects of threshold voltage, subthreshold slope and transconductance increase have been observed, as well as stable behavior of MIM-capacitors at frequencies up to 1 MHz.

For the first time, the possible profit of native transistors usage in cryogenic behavior has been demonstrated. Due to the threshold voltage shift at 6 K compared to room temperature, these devices behave like classical n-type transistors with a low threshold voltage of ca. 0.2 V.

The transistor structures fabricated in 22 nm FD-SOI technology have been characterized at frequencies up to 20 GHz and cryogenic temperatures down to 6 K. Small signal equivalent circuit parameters have been extracted, demonstrating the transconductance g_m improvement with temperature decrease. f_t and f_{max} improvement with temperature decrease have been demonstrated. High-frequency noise measurements have been evaluated, however, they turned out to be extremely challenging for this setup configuration.

For the first time, self-heating effects in 65 nm bulk CMOS and 22 nm FD-SOI technologies at cryogenic temperatures have been investigated. Electro-thermal behavior of two transistor-like structures, fabricated in 65 nm bulk CMOS and 22 nm FD-SOI technologies have been investigated and compared. The dependence of electro-thermal behavior on the embedding material of the transistor has been demonstrated and the modeling of such behavior based on the specific thermal resistance of Si and SiO_2 dependence on temperature has been performed.

8.2 Conclusions and outlook

The demonstrated work contributes to the field of modern cryogenic CMOS research. The results showed the feasibility of small-node CMOS technologies for cryogenic applications, especially for quantum computing. The behavior and effects of MOSFETs in 65 nm bulk CMOS and 22 nm FD-SOI technologies at 6 K have been investigated and compared to room temperature ones.

The presented results prompt the development of cryogenic process design kits in order to help IC designers in QC and other cryogenic topics. Electro-thermal research showed also the necessity of dynamic thermal models, as the nearby devices can influence each other's behavior.

Self-heating effect measurements in 65 nm bulk CMOS technology showed the dependency of the transistor thermal behavior on drain-source voltage, which will be a subject of future studies.

Various DC devices, not mentioned in this thesis but still present on the SQuBiC2 and SQuBiC5 chips, will be investigated in the nearest future.

In the framework of upcoming projects, it is planned to develop PDKs for FD-SOI technology. However, some measurement results are gathered during this work, it is not enough for a complete PDK development. That activity requires the design and test of new chips with a variety of CMOS structures with different sizes and flavors, as well as the same devices fabricated in different areas of the substrate in order to characterize process variations and mismatch.

Using the experience gained during this research, new chips with more various test structures will be designed and measured using the verified test methods.

Bibliography

[1] P. Benioff. "The computer as a physical system: A microscopic quantum mechanical Hamiltonian model of computers as represented by Turing machines". In: *Journal of Statistical Physics* 22 (May 1980), pp. 563–591. DOI: 10.1007/BF01011339.

[2] Y. I. Manin. "Vychislimoe i nevychislimoe [Computable and Noncomputable]". In: Moscow, USSR: Soviet Radio, 1980.

[3] R. P. Feynman. "Simulating physics with computers". In: *International Journal of Theoretical Physics* 21 (1981), pp. 467–488. DOI: 10.1007/BF02650179.

[4] A. Montanaro. "Quantum algorithms: An overview". In: *npj Quantum Information* 2 (Jan. 2016). DOI: 10.1038/npjqi.2015.23.

[5] F. Arute et al. "Quantum supremacy using a programmable superconducting processor". In: *Nature* 574.7779 (2019), pp. 505–510.

[6] A. Karamlou et al. "Analyzing the performance of variational quantum factoring on a superconducting quantum processor". In: *npj Quantum Information* 7 (Dec. 2021). DOI: 10.1038/s41534-021-00478-z.

[7] H.-S. Zhong et al. "Quantum computational advantage using photons". In: *Science* 370.6523 (2020), pp. 1460–1463.

[8] L. M. K. Vandersypen et al. "Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent". English. In: *NPJ Quantum Information* 3.1 (Sept. 2017), p. 34. ISSN: 2056-6387. DOI: 10.1038/s41534-017-0038-y.

[9] L. Geck et al. "Control electronics for semiconductor spin qubits". In: *Quantum Science and Technology* 5.1 (Dec. 2019), p. 015004. DOI: 10.1088/2058-9565/ab5e07.

[10] R. R. Green. "MOSFET operation at 4.2 K." In: *Review of Scientific Instruments* 39 (1968), pp. 1495–1497. DOI: 10.1063/1.1683144.

[11] C. G. Rogers. "MOST's at cryogenic temperatures". In: *Solid State Electronics* 11.11 (Nov. 1968), pp. 1079–1091. DOI: 10.1016/0038-1101(68)90130-5.

[12] A. Caglar and M. B. Yelten. "Design of Cryogenic LNAs for High Linearity in Space Applications". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 66.12 (2019), pp. 4619–4627. DOI: 10.1109/TCSI.2019.2936506.

[13] M. Mudavath et al. "Design of Cryogenic CMOS LNAs for Space Communications". In: *Journal of Physics: Conference Series* 1817.1 (Mar. 2021), p. 012005. DOI: 10.1088/1742-6596/1817/1/012005.

[14] E. Gutierrez-D, J. Deen, and C. Claeys. *Low Temperature Electronics*. New York: Academic Press, 2000. ISBN: 9780080510507.

[15] C. G. Almudever et al. "The engineering challenges in quantum computing". In: *Design, Automation Test in Europe Conference Exhibition (DATE), 2017*. 2017, pp. 836–845. DOI: 10.23919/DATE.2017.7927104.

[16] B. Patra et al. "Cryo-CMOS Circuits and Systems for Quantum Computing Applications". In: *IEEE Journal of Solid-State Circuits* 53.1 (2018), pp. 309–321. DOI: 10.1109/JSSC.2017.2737549.

[17] L. K. Grover. "A Fast Quantum Mechanical Algorithm for Database Search". In: *Proceedings of the Twenty-Eighth Annual ACM Symposium on Theory of Computing*. STOC '96. Philadelphia, Pennsylvania, USA: Association for Computing Machinery, 1996, pp. 212–219. ISBN: 0897917855. DOI: 10.1145/237814.237866.

[18] P. W. Shor. "Algorithms for quantum computation: discrete logarithms and factoring". In: *Proceedings 35th Annual Symposium on Foundations of Computer Science*. 1994, pp. 124–134. DOI: 10.1109/SFCS.1994.365700.

[19] A. T. Bell and M. Head-Gordon. "Quantum Mechanical Modeling of Catalytic Processes". In: *Annual Review of Chemical and Biomolecular Engineering* 2.1 (2011), pp. 453–477. DOI: 10.1146/annurev-chembioeng-061010-114108.

[20] A. Robert et al. "Resource-efficient quantum algorithm for protein folding". In: *npj Quantum Information* 7 (Dec. 2021). DOI: 10.1038/s41534-021-00368-4.

[21] R. Shankar. *Low Temperature Electronics*. New York: Springer, 1994. ISBN: 978-0-306-44790-7.

[22] R. Waser. *Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices*. Berlin, Germany: Wiley-VCH, 2012. ISBN: 978-3-527-40927-3.

[23] M. A. Nielsen and I. L. Chuang. *Quantum Computation and Quantum Information: 10th Anniversary Edition*. Cambridge University Press, 2010. DOI: 10.1017/CBO9780511976667.

[24] D. P. DiVincenzo. "The Physical Implementation of Quantum Computation". In: *Fortschritte der Physik* 48.9-11 (2000), pp. 771–783. DOI: 10.1002/1521-3978(200009)48:9/11<771::AID-PROP771>3.0.CO;2-E.

[25] C. D. Bruzewicz et al. "Trapped-ion quantum computing: Progress and challenges". In: *Applied Physics Reviews* 6.2 (2019), p. 021314. DOI: 10.1063/1.5088164.

[26] W. Neuhauser et al. "Localized visible Ba^+ mono-ion oscillator". In: *Phys. Rev. A* 22 (3 Sept. 1980), pp. 1137–1140. DOI: 10.1103/PhysRevA.22.1137.

[27] T. P. Harty et al. "High-Fidelity Trapped-Ion Quantum Logic Using Near-Field Microwaves". In: *Phys. Rev. Lett.* 117 (14 Sept. 2016), p. 140501. DOI: 10.1103/PhysRevLett.117.140501.

[28] C. J. Ballance et al. "High-Fidelity Quantum Logic Gates Using Trapped-Ion Hyperfine Qubits". In: *Phys. Rev. Lett.* 117 (6 Aug. 2016), p. 060504. DOI: 10.1103/PhysRevLett.117.060504.

[29] L. Schreiber and H. Bluhm. "Quantum computation: Silicon comes back". In: *Nature nanotechnology* 9 (Oct. 2014). DOI: 10.1038/nnano.2014.249.

[30] J. P. Dehollain et al. "Optimization of a solid-state electron spin qubit using Gate Set Tomography". In: *New Journal of Physics* 18 (Oct. 2016), p. 103018. DOI: 10.1088/1367-2630/18/10/103018.

[31] H. Yang et al. "Silicon qubit fidelities approaching incoherent noise limits via pulse engineering". In: *Nature Electronics* 2 (Apr. 2019), p. 1. DOI: 10.1038/s41928-019-0234-1.

[32] J. Yoneda et al. "A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%". In: *Nature Nanotechnology* 13 (Feb. 2018), p. 102. DOI: 10.1038/s41565-017-0014-x.

[33] F. Arute et al. "Quantum supremacy using a programmable superconducting processor". In: *Nature* 574 (Oct. 2019), pp. 505–510. DOI: 10.1038/s41586-019-1666-5.

[34] P. Krantz et al. "A quantum engineer's guide to superconducting qubits". In: *Applied Physics Reviews* 6.2 (2019), p. 021318. DOI: 10.1063/1.5089550.

[35] M. Kjaergaard et al. "Superconducting Qubits: Current State of Play". In: *Annual Review of Condensed Matter Physics* 11.1 (2020), pp. 369–395. DOI: 10.1146/annurev-conmatphys-031119-050605.

[36] C. Degenhardt et al. "Systems Engineering of Cryogenic CMOS Electronics for Scalable Quantum Computers". In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2019, pp. 1–5. DOI: 10.1109/ISCAS.2019.8702442.

[37] R. M. Incandela et al. "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures". In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 996–1006. DOI: 10.1109/JEDS.2018.2821763.

[38] A. Beckers, F. Jazaeri, and C. Enz. "Cryogenic MOSFET Threshold Voltage Model". In: *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*. 2019, pp. 94–97. DOI: 10.1109/ESSDERC.2019.8901806.

[39] Y. Creten et al. "An 8-Bit Flash Analog-to-Digital Converter in Standard CMOS Technology Functional From 4.2 K to 300 K". In: *IEEE Journal of Solid-State Circuits* 44.7 (2009), pp. 2019–2025. DOI: 10.1109/JSSC.2009.2021918.

[40] G. Ghibaudo and F. Balestra. "Low temperature characterization of silicon CMOS devices". In: *Proceedings of International Conference on Microelectronics*. Vol. 2. 1995, 613–622 vol.2. DOI: 10.1109/ICMEL.1995.500938.

[41] F. Balestra and G. Ghibaudo. "Brief review of the MOS device physics for low temperature electronics". In: *Solid-State Electronics* 37.12 (1994), pp. 1967–1975. DOI: 10.1016/0038-1101(94)90064-7.

[42] A. Beckers et al. "Physical Model of Low-Temperature to Cryogenic Threshold Voltage in MOSFETs". In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 780–788. DOI: 10.1109/JEDS.2020.2989629.

[43] T.-Y. Yang et al. "Quantum Transport in 40-nm MOSFETs at Deep-Cryogenic Temperatures". In: *IEEE Electron Device Letters* 41.7 (2020), pp. 981–984. DOI: 10.1109/LED.2020.2995645.

[44] B. Cretu et al. "Assessment of DC and low-frequency noise performances of triple-gate FinFETs at cryogenic temperatures". In: *Semiconductor Science and Technology* 31 (Dec. 2016), p. 124006. DOI: 10.1088/0268-1242/31/12/124006.

[45] P. Galy et al. “Cryogenic Temperature Characterization of a 28-nm FD-SOI Dedicated Structure for Advanced CMOS and Quantum Technologies Co-Integration”. In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 594–600. DOI: 10.1109/JEDS.2018.2828465.

[46] A. Beckers et al. “Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures”. In: *Solid-State Electronics* 159 (2019). SI: EUROSOI 2018, pp. 106–115. ISSN: 0038-1101. DOI: 10.1016/j.sse.2019.03.033.

[47] B. C. Paz et al. “Integrated Variability Measurements of 28 nm FDSOI MOSFETs down to 4.2 K for Cryogenic CMOS Applications”. In: *2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS)*. 2020, pp. 1–5. DOI: 10.1109/ICMTS48187.2020.9107906.

[48] S. Bonen et al. “Cryogenic Characterization of 22-nm FDSOI CMOS Technology for Quantum Computing ICs”. In: *IEEE Electron Device Letters* 40.1 (2019), pp. 127–130. DOI: 10.1109/LED.2018.2880303.

[49] O. Lopez-L et al. “Electrical and Thermal Characterization for SOI p-type FinFET down to Sub-Kelvin Temperatures”. In: *2020 IEEE Latin America Electron Devices Conference (LAEDC)*. 2020, pp. 1–3. DOI: 10.1109/LAEDC49063.2020.9072950.

[50] D. Boudier et al. “On quantum effects and low frequency noise spectroscopy in Si Gate-All-Around Nanowire MOSFETs at cryogenic temperatures”. In: *2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*. 2017, pp. 5–8. DOI: 10.1109/ULIS.2017.7962578.

[51] H. Bohuslavskyi et al. “28nm Fully-depleted SOI technology: Cryogenic control electronics for quantum computing”. In: *2017 Silicon Nanoelectronics Workshop (SNW)*. 2017, pp. 143–144. DOI: 10.23919/SNW.2017.8242338.

[52] B. Patra et al. “Characterization and Analysis of On-Chip Microwave Passive Components at Cryogenic Temperatures”. In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 448–456. DOI: 10.1109/JEDS.2020.2986722.

[53] T. Lehmann. “Cryogenic Support Circuits and Systems for Silicon Quantum Computers”. In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2019, pp. 1–5. DOI: 10.1109/ISCAS.2019.8702413.

[54] P. A. ’T Hart et al. “Characterization and Modeling of Mismatch in Cryo-CMOS”. In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 263–273. DOI: 10.1109/JEDS.2020.2976546.

[55] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers. “Matching properties of MOS transistors”. In: *IEEE Journal of Solid-State Circuits* 24.5 (1989), pp. 1433–1439. DOI: 10.1109/JSSC.1989.572629.

[56] F. Jazaeri et al. “A Review on Quantum Computing: From Qubits to Front-end Electronics and Cryogenic MOSFET Physics”. In: *2019 MIXDES - 26th International Conference "Mixed Design of Integrated Circuits and Systems"*. 2019, pp. 15–25. DOI: 10.23919/MIXDES.2019.8787164.

[57] J. van Dijk et al. “Cryo-CMOS for Analog/Mixed-Signal Circuits and Systems”. In: *2020 IEEE Custom Integrated Circuits Conference (CICC)*. 2020, pp. 1–8. DOI: 10.1109/CICC48029.2020.9075882.

[58] D. van Delft and P. Kes. "The discovery of superconductivity". In: *Physics Today* 63.9 (2020), p. 38. DOI: 10.1063/1.3490499.

[59] R. A. Ackermann. "Regenerative Cryogenic Refrigerators". In: *Cryogenic Regenerative Heat Exchangers*. Boston, MA: Springer US, 1997, pp. 193–221. ISBN: 978-1-4757-9891-3. DOI: 10.1007/978-1-4757-9891-3_6.

[60] W. E. Gifford. "The Gifford-McMahon Cycle". In: *Advances in Cryogenic Engineering*. Ed. by K. D. Timmerhaus. Boston, MA: Springer US, 1966, pp. 152–159. ISBN: 978-1-4757-0522-5.

[61] E. I. Mikulin, A. A. Tarasov, and M. P. Shkrebyonock. "Low-Temperature Expansion Pulse Tubes". In: *Advances in Cryogenic Engineering: Volume 29*. Ed. by R. W. Fast. Boston, MA: Springer US, 1984, pp. 629–637. ISBN: 978-1-4613-9865-3. DOI: 10.1007/978-1-4613-9865-3_72.

[62] H. Bohuslavskyi et al. "Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs Described With Band Broadening". In: *IEEE Electron Device Letters* 40.5 (2019), pp. 784–787. DOI: 10.1109/LED.2019.2903111.

[63] A. Beckers, F. Jazaeri, and C. Enz. "Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors". In: *IEEE Electron Device Letters* 41.2 (2020), pp. 276–279. DOI: 10.1109/LED.2019.2963379.

[64] *Wide-field microscopy with the attoDRY800 optical cryostat*. https://www.attocube.com/en/products/cryostats/closed-cycle-cryostats/attodry800-optical-cryostat/white-paper. Accessed: 2022-02-23. attocube systems AG, 2018.

[65] L. Howald, H. Rudin, and H.-J. Güntherodt. "Piezoelectric inertial stepping motor with spherical rotor". In: *Review of Scientific Instruments* 63.8 (1992), pp. 3909–3912. DOI: 10.1063/1.1143290.

[66] *Multi-Contact Wedges*. https://ggb.com/home/multi-contact-wedges/. Accessed: 2022-02-24. GGB Inductries Inc.

[67] *STORM FLEX 034 SERIES*. https://delft-circuits.com/product-overview/cf2/. Accessed: 2022-02-24. Teledyne Storm Microwave.

[68] https://www.teledynedefenseelectronics.com/stormmicrowave/products/flexibleassemblies/cableselectionchart/Pages/StormFlex.aspx. Accessed: 2022-02-24. Teledyne Storm Microwave.

[69] *STORM FLEX 034 SERIES*. https://www.teledynedefenseelectronics.com/stormmicrowave/resources/Documents/StormFlex_034_SS_2020_web_r1.pdf. Accessed: 2022-02-24. Teledyne Storm Microwave.

[70] *|Z| Probe*. https://www.formfactor.com/product/probes/z-probe/z-probe-coaxial/. Accessed: 2022-02-24. Cascade Microtech.

[71] M. M. Atalla, E. Tannenbaum, and E. J. Scheibner. "Stabilization of silicon surfaces by thermally grown oxides". In: *The Bell System Technical Journal* 38.3 (1959), pp. 749–783. DOI: 10.1002/j.1538-7305.1959.tb03907.x.

[72] D. Kahng. *Electric Field Controlled Semiconductor Device*. U. S. Patent No. 3102230, May. 1960.

[73] F. Wanlass and C. Sah. "Nanowatt logic using field-effect metal-oxide semiconductor triodes". In: *1963 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*. Vol. VI. 1963, pp. 32–33. DOI: 10.1109/ISSCC.1963.1157450.

[74] R. H. Norman and H. E. Stephenson. *Shift Register Employing Insulated Gate Field Effect Transistors*. U. S. Patent No. 3454785 , July 1964.

[75] P. Vliex et al. "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications". In: *IEEE Solid-State Circuits Letters* 3 (2020), pp. 218–221. DOI: 10.1109/LSSC.2020.3011576.

[76] K. G. Lyon et al. "Linear thermal expansion measurements on silicon from 6 to 340 K". In: *Journal of Applied Physics* 48.3 (1977), pp. 865–868. DOI: 10.1063/1.323747.

[77] J. Ekin and G. Zimmerman. "Experimental Techniques for Low-Temperature Measurements: Cryostat Design, Material Properties, and Superconductor Critical-Current Testing". In: *Physics Today - PHYS TODAY* 60 (May 2007). DOI: 10.1063/1.2743130.

[78] F. A. Miranda et al. "Measurements of Complex Permittivity of Microwave Substrates in the 20 to 300 K Temperature Range From 26.5 to 40.0 GHz". In: *NASA Technical Memorandum 102123*. Los Angeles, California: University of California, 1989.

[79] L. Song. "Cryogenic characterization and modeling of nanometer cmos transistors for quantum computing applications". PhD thesis. Delft University of Technology, 2016.

[80] T. Struck et al. "Low-frequency spin qubit energy splitting noise in highly purified 28Si/SiGe". In: *npj Quantum Information* 6 (Dec. 2020). DOI: 10.1038/s41534-020-0276-2.

[81] L. Willeke. "Characterization of 22 nm FD-SOI MOSFET devices at cryogenic temperatures". MA thesis. Forschungzentrum Jülich GmbH, ZEA-2, 52428 Jülich and Ruhr-Universität Bochum, Chair for integrated systems, 447880 Bochum, 2021.

[82] *N5242A PNA-X Microwave Network Analyzer*. keysight.com/de/de/product/N5242A/pnax-microwave-network-analyzer-265-ghz.html. Accessed: 2022-03-01. Keysight.

[83] S. Lee et al. "Comparison of On-chip De-embedding Methods with 28-nm FDSOI MOSFETs up to 110-GHz". In: *2019 IEEE Asia-Pacific Microwave Conference (APMC)*. 2019, pp. 1241–1243. DOI: 10.1109/APMC46564.2019.9038233.

[84] D. M. Pozar. *Microwave Engineering, 4th Edition*. Wiley, 2011. ISBN: 9781118213636.

[85] J.-P. Raskin et al. "Accurate SOI MOSFET characterization at microwave frequencies for device performance optimization and analog modeling". In: *IEEE Transactions on Electron Devices* 45.5 (1998), pp. 1017–1025. DOI: 10.1109/16.669514.

[86] G. Crupi et al. "The large world of FET small-signal equivalent circuits". In: *International Journal of RF and Microwave Computer-Aided Engineering* 26.9 (2016), pp. 749–762. DOI: 10.1002/mmce.21028.

[87] J. C. Tinoco and J.-P. Raskin. "Advanced RF MOSFET´s for Microwave and Millimeter Wave Applications: RF Characterization Issues". In: *Microwave and Millimeter Wave Technologies*. Rijeka: IntechOpen, 2010. Chap. 9. DOI: 10.5772/9053.

[88] B. Kazemi Esfeh et al. "Assessment of 28nm UTBB FD-SOI technology platform for RF applications: Figures of merit and effect of parasitic elements". In: *Solid-State Electronics* 117 (2016), pp. 130–137. ISSN: 0038-1101. DOI: 10.1016/j.sse.2015.11.020.

[89] D. Lovelace, J. Costa, and N. Camilleri. "Extracting small-signal model parameters of silicon MOSFET transistors". In: *1994 IEEE MTT-S International Microwave Symposium Digest (Cat. No.94CH3389-4)*. 1994, 865–868 vol.2. DOI: 10.1109/MWSYM.1994.335220.

[90] A. Bracale et al. "A New Approach for SOI Devices Small-Signal Parameters Extraction". In: *Analog Integrated Circuits and Signal Processing* 25 (Nov. 2000), pp. 157–169. DOI: 10.1023/A:1008332732738.

[91] R. Torres-Torres, R. Murphy Arteaga, and S. Decoutere. "MOSFET bias dependent series resitance extraction from RF measurements". In: *Electronics Letters* 39 (Nov. 2003), pp. 1476–1478. DOI: 10.1049/el:20030936.

[92] J. C. Tinoco and J.-P. Raskin. "RF-extraction methods for MOSFET series resistances: A fair comparison". In: *2008 7th International Caribbean Conference on Devices, Circuits and Systems*. 2008, pp. 1–6. DOI: 10.1109/ICCDCS.2008.4542657.

[93] S. Mason. "Power Gain in Feedback Amplifier". In: *Transactions of the IRE Professional Group on Circuit Theory* CT-1.2 (1954), pp. 20–25. DOI: 10.1109/TCT.1954.1083579.

[94] D. A. Frickey. "Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances". In: *IEEE Transactions on Microwave Theory and Techniques* 42.2 (1994), pp. 205–211. DOI: 10.1109/22.275248.

[95] Keysight Application Note 5990-8255. "Fundamentals of RF and Microwave Noise Figure Measurements". In: USA: Keysight Technologies, 2019.

[96] Keysight Application Note 5990-5800. "High-Accuracy Noise Figure Measurements Using the PNA-X Series Network Analyzer". In: USA: Keysight Technologies, 2014.

[97] J. E. Fernandez. "A Noise-Temperature Measurement System Using a Cryogenic Attenuator". In: *TMO Progress Report 42-135*. 1998.

[98] Data Sheet and Technical Specifications. "Keysight 2-Port and 4-Port PNA-X Network Analyzer". In: USA: Keysight Technologies, 2018.

[99] J. M. Boter et al. "A sparse spin qubit array with integrated control electronics". In: *2019 IEEE International Electron Devices Meeting (IEDM)*. 2019, pp. 31.4.1–31.4.4. DOI: 10.1109/IEDM19573.2019.8993570.

[100] E. A. Gutierrez-D., L. Deferm, and G. Declerck. "Experimental determination of self-heating in submicrometer MOS transistors operated in a liquid-helium ambient". In: *IEEE Electron Device Letters* 14.3 (1993), pp. 152–154. DOI: 10.1109/55.215141.

[101] B. M. Tenbroek et al. "Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques". In: *IEEE Transactions on Electron Devices* 43.12 (1996), pp. 2240–2248. DOI: 10.1109/16.544417.

[102] K. Raleva et al. "Study of self-heating effects in SOI and conventional MOSFETs with electro-thermal particle-based device simulator". English (US). In: *Journal of Computational Electronics* 11.1 (Mar. 2012), pp. 106–117. ISSN: 1569-8025. DOI: 10.1007/s10825-012-0384-0.

[103] K. Triantopoulos et al. "Self-Heating Effect in FDSOI Transistors Down to Cryogenic Operation at 4.2 K". In: *IEEE Transactions on Electron Devices* 66.8 (2019), pp. 3498–3505. DOI: 10.1109/TED.2019.2919924.

[104] Xiong Zhang et al. "Measurements and Simulation of Self-Heating in 40 nm SOI MOSFETs". In: *2021 5th IEEE Electron Devices Technology Manufacturing Conference (EDTM)*. 2021, pp. 1–3. DOI: 10.1109/EDTM50988.2021.9421023.

[105] P. A. 't Hart et al. "Characterization and Modeling of Self-Heating in Nanometer Bulk-CMOS at Cryogenic Temperatures". In: *IEEE Journal of the Electron Devices Society* 9 (2021), pp. 891–901. DOI: 10.1109/JEDS.2021.3116975.

[106] A. Artanov et al. "Self-heating effect in 65nm CMOS technology (poster)". In: *Proc. 14th WOLTE*. 2021, pp. 20–21.

[107] A. A. Artanov et al. "Self-Heating Effect in a 65 nm MOSFET at Cryogenic Temperatures". In: *IEEE Transactions on Electron Devices* 69.3 (2022), pp. 900–904. DOI: 10.1109/TED.2021.3139563.

[108] L. Wang et al. "Investigation of scattering mechanisms for scaled mosfets". In: *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*. 2014, pp. 1–3. DOI: 10.1109/ICSICT.2014.7021279.

[109] R. Kibushi et al. "Comparison of hot spot temperature between Si and SiC power MOSFET using electro-thermal analysis". In: *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*. 2017, pp. 921–925. DOI: 10.1109/ITHERM.2017.7992584.

[110] F. J. De la Hidalga, M. J. Deen, and E. A. Gutierrez. "Theoretical and experimental characterization of self-heating in silicon integrated devices operating at low temperatures". In: *IEEE Transactions on Electron Devices* 47.5 (2000), pp. 1098–1106. DOI: 10.1109/16.841246.

[111] P. G. Mautry and J. Trager. "Self-heating and Temperature Measurement in Sub-µm-MOSFETs". In: *ESSDERC '89: 19th European Solid State Device Research Conference*. 1989, pp. 675–678. DOI: 10.1007/978-3-642-52314-4_141.

[112] Z. Boekelheide et al. "Resonant impurity scattering and electron-phonon scattering in the electrical resistivity of Cr thin films". In: *Phys. Rev. B* 80 (13 Oct. 2009), p. 134426. DOI: 10.1103/PhysRevB.80.134426.

[113] A. D. McConnell, S. Uma, and K. E. Goodson. "Thermal conductivity of doped polysilicon layers". In: *Journal of Microelectromechanical Systems* 10.3 (2001), pp. 360–369. DOI: 10.1109/84.946782.

[114] V. J. Johnson. "A Compendium of the Properties of Materials at Low Temperature (Phase l), Part II: Properties of Solids". In: *Wadd Technical Report*. Boulder, CO, USA: National Bureau of Standards, 1960, pp. 56–60.

[115] J. G. Hust and A. B. Lankford. "Thermal conductivity of aluminum, copper, iron, and tungsten for temperatures from 1 K to the melting point". In: *Wadd Technical Report*. Boulder, CO, USA: National Bureau of Standards, 1984.

[116] M. Asheghi et al. "Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates". In: *Journal of Heat Transfer* 120.1 (Feb. 1998), pp. 30–36. ISSN: 0022-1481. DOI: 10.1115/1.2830059.

[117] D. de Faoite et al. "A review of the processing, composition, and temperature-dependent mechanical and thermal properties of dielectric technical ceramics". In: *Journal of Materials Science* 47 (May 2012), pp. 4211–4235. DOI: 10.1007/s10853-011-6140-1.

[118] "Temperature Measurement and Control Catalog". In: Westerville, OH, USA: Lake Shore Cryotronics, Inc., 2016.

[119] J. Jaramillo Fernandez et al. "Thermal Conductivity of Polycrystalline Aluminum Nitride Films: Effects of the Microstructure, Interfacial Thermal Resistance and Local Oxidation". In: Sept. 2015. DOI: 10.1109/THERMINIC.2015.7389602.

[120] A. M. Darwish, A. J. Bayba, and H. A. Hung. "Accurate determination of thermal resistance of FETs". In: *IEEE Transactions on Microwave Theory and Techniques* 53.1 (2005), pp. 306–313. DOI: 10.1109/TMTT.2004.839916.

[121] P. Hopkins and L. Phinney. "Thermal Conductivity Measurements on Polycrystalline Silicon Microbridges Using the 3 ωTechnique". In: *Journal of Heat Transfer-transactions of The Asme* 131 (Apr. 2009). DOI: 10.1115/1.3072907.

[122] S. Kasap, J. Málek, and R. Svoboda. "Thermal Properties and Thermal Analysis: Fundamentals, Experimental Techniques and Applications". In: Jan. 2017. ISBN: 978-3-319-48931-5. DOI: 10.1007/978-3-319-48933-9_19.

[123] S.-M. Lee and D. G. Cahill. "Heat transport in thin dielectric films". In: *Journal of Applied Physics* 81.6 (1997), pp. 2590–2595. DOI: 10.1063/1.363923.

Curriculum vitae

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Professional experience

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01.2013 – 01.2018	Engineer at Laboratory of Superconducting Devices for Signal Detection and Processing, Kotel'nikov IREE RAS, Moscow, Russia
09.2016 – 01.2018	Teaching assistant at Dept. of General Physics, Moscow Institute of Physics and Technology (MIPT), Moscow, Russia
07.2017 – 08.2017	Internship at Kavli Institute of Nanoscience, Delft University of Technology, Delft, The Netherlands
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Education

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Publications and conferences

Journal publications

A. A. Artanov, E. A. Gutierrez-D., A. R. Cabrera-Galicia, A. Kruth, C. Degenhardt, D. Durini, J. Mendez-V., S. van Waasen "Self-Heating Effect in a 65 nm MOSFET at Cryogenic Temperatures" in *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 900-904, March 2022, doi: 10.1109/TED.2021.3139563

O. López-López, I. Martínez, A. Cabrera, E. A. Gutiérrez-D, D. Ferrusca, D. Durini, F. J. De la Hidalga-Wade, M. Velazquez, O. Huerta, A. Kruth, C. Degenhardt, A. Artanov, S. van Waasen, "Energy Consumption, Conversion, and Transfer in Nanometric Field-Effect Transistors (FET) Used in Readout Electronics at Cryogenic Temperatures" in *Journal of Low Temperature Physics*, vol. 199, pp. 171–181, January 2022, doi: 10.1007/s10909-020-02340-6

Conferences and workshops

A. Artanov et al., "Self-Heating Effect in 65 nm CMOS Technology" at *14th IEEE Workshop on Low Temperature Electronics*, Matera, Italy, May 2021

P. Vliex, D. Nielinger, A. Artanov et al., "Scalable Quantum Bit Control (SQuBiC1) Cryogenic CMOS IC for Spin Qubit Control" at *14th IEEE Workshop on Low Temperature Electronics*, Matera, Italy, May 2021

C. Degenhardt, A. Artanov, L. Geck, C. Grewing, A. Kruth, D. Nielinger, P. Vliex, A. Zambanini, S. van Waasen, "Systems Engineering of Cryogenic CMOS Electronics for Scalable Quantum Computers" at *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1-5, doi: 10.1109/ISCAS.2019.8702442

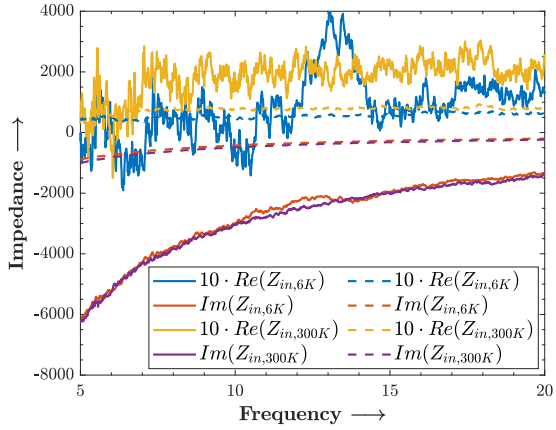
A. Artanov et al., "Scalable Cryogenic CMOS Electronics for Spin Qubit Control" at *WE-Heraeus-Seminar "Engineering a Scalable Quantum Information Processor"*, Bad Honnef, Germany, April 2019

Master thesis supervision

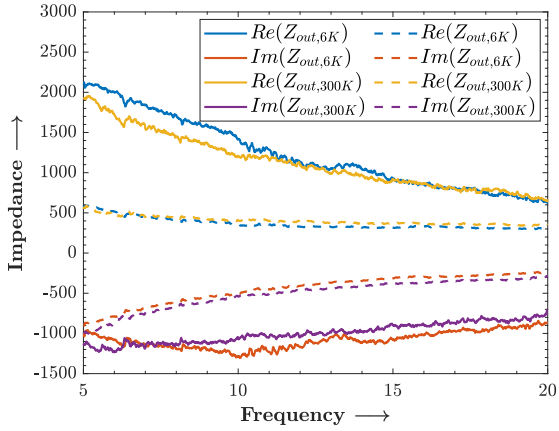
L. Willeke, "Characterization of 22 nm FD-SOI MOSFET devices at cryogenic temperatures and frequencies up to 20 GHz". Master thesis, Chair for Integrated Systems, Ruhr-Universität Bochum, Bochum, Germany, December 2021

Appendix A

Input and output impedances of the RF structures



(a) Input impedances



(b) Output impedances

Figure A.1: Input and output impedances of the transistor arrays with W = 2.4 μm (solid lines) and W = 9.6 μm (dashed lines)

Appendix B

Results of the SSEC elements extraction

The following data were published in [81]. It has been extracted from the measurement of S-parameters via a cryogenic probing station. An open-short deembedding technique was used. Access resistances were obtained as described by Torres-Torres [91], other values as shown in [88] and [89]. The values are the result of calculating the arithmetic mean value between 5 GHz and 20 GHz, the errors are determined by the values of one standard deviation. The data were then adjusted to describe single devices instead of transistor arrays. Some of the values contradict common sense, like negative resistances. They are caused by not sufficient measurement accuracy.

B.1 nMOS

300 K

$300K, V_{bg} = 0V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	194.1 ± 71.1	60.6 ± 13.1	16.7 ± 1.9
R_{de} in Ω	85.9 ± 4.2	55.4 ± 1.8	45.0 ± 1.0
R_{se} in Ω	86.2 ± 4.2	58.9 ± 2.3	49.8 ± 1.3
R_{gs} in Ω	48.2 ± 12.7	5.4 ± 4.9	−10.8 ± 2.1
C_{ds} in fF	3.5 ± 0.7	4.4 ± 0.9	5.5 ± 1.1
C_{gd} in fF	1.0 ± 0.1	1.7 ± 0.1	3.1 ± 0.1
C_{gse} in fF	1.5 ± 0.1	2.5 ± 0.1	4.5 ± 0.1
C_{gsi} in fF	2.6 ± 0.3	7.7 ± 0.6	27.1 ± 1.0
g_m in mS	3.5 ± 0.3	6.2 ± 0.4	8.8 ± 0.5
g_{ds} in mS	0.68 ± 0.04	0.62 ± 0.05	0.55 ± 0.05
$g_{m,DC}$ in mS	3.9	6.2	8.0
$g_{ds,DC}$ in mS	0.3	0.2	0.1
V_{th} in mV	428.2	503.7	554.1
j_{ds} in $mA/\mu m$	4.37	2.62	1.34
Z_{in} @5GHz in Ω	30.1-6195.1j	79.6-2589.5j	65.3-993.1j
Z_{in} @10GHz in Ω	173.4-3047.1j	110.9-1266.5j	75.5-488.8j
Z_{in} @15GHz in Ω	229.8-2013.8j	144.3-841.0j	87.9-322.0j
Z_{in} @20GHz in Ω	259.0-1374.1j	136.4-585.6j	82.8-230.2j
Z_{out} @5GHz in Ω	1927.6-1148.4j	1178.5-1433.2j	551.7-996.3j
Z_{out} @10GHz in Ω	1209.8-1056.2j	635.4-912.5j	408.6-541.9j
Z_{out} @15GHz in Ω	912.5-900.3j	490.3-657.4j	378.2-379.5j
Z_{out} @20GHz in Ω	669.0-717.3j	395.0-480.8j	353.0-286.2j
f_t in GHz	225 ± 7	166 ± 4	81 ± 1
f_{max} in GHz	222 ± 37	257 ± 27	251 ± 15

$300K, V_{bg} = 1V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	200.7 ± 69.6	65.0 ± 12.8	20.7 ± 1.9
R_{de} in Ω	75.3 ± 4.1	46.0 ± 1.8	35.2 ± 1.0
R_{se} in Ω	74.7 ± 4.1	49.0 ± 2.1	39.6 ± 1.1
R_{gs} in Ω	70.0 ± 12.5	17.6 ± 4.9	−1.7 ± 2.2
C_{ds} in fF	3.2 ± 0.6	4.1 ± 0.9	5.4 ± 1.1
C_{gd} in fF	1.0 ± 0.1	1.8 ± 0.1	3.2 ± 0.1
C_{gse} in fF	1.5 ± 0.1	2.5 ± 0.1	4.5 ± 0.1
C_{gsi} in fF	2.3 ± 0.3	6.9 ± 0.5	25.5 ± 1.0
g_m in mS	3.3 ± 0.2	6.0 ± 0.4	9.3 ± 0.5
g_{ds} in mS	0.78 ± 0.04	0.74 ± 0.04	0.70 ± 0.05
$g_{m,DC}$ in mS	3.9	6.5	9.0
$g_{ds,DC}$ in mS	0.3	0.3	0.2
V_{th} in mV	351.2	436.7	499.1
j_{ds} in $mA/\mu m$	5.55	3.59	2.00
Z_{in} @5GHz in Ω	94.2-6161.2j	76.6-2500.7j	61.9-921.7j
Z_{in} @10GHz in Ω	163.7-3026.7j	110.4-1231.5j	72.5-453.6j
Z_{in} @15GHz in Ω	208.5-2022.3j	137.9-814.4j	83.8-298.8j
Z_{in} @20GHz in Ω	251.6-1366.6j	131.5-566.9j	77.8-214.6j
Z_{out} @5GHz in Ω	1705.2-823.4j	1135.5-1103.2j	525.5-807.3j
Z_{out} @10GHz in Ω	1160.7-841.3j	635.1-768.3j	374.8-446.0j
Z_{out} @15GHz in Ω	900.4-753.8j	482.0-567.5j	344.1-309.9j
Z_{out} @20GHz in Ω	664.8-629.2j	388.2-420.8j	319.9-232.5j
f_t in GHz	224 ± 7	171 ± 4	89 ± 1
f_{max} in GHz	215 ± 34	248 ± 24	231 ± 12

$300K, V_{bg} = 2V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	206.1 ± 70.7	68.0 ± 12.6	23.1 ± 1.9
R_{de} in Ω	68.1 ± 3.9	40.1 ± 1.7	29.4 ± 1.0
R_{se} in Ω	67.1 ± 3.9	42.9 ± 2.0	33.5 ± 1.0
R_{gs} in Ω	88.9 ± 12.2	26.9 ± 5.2	4.2 ± 2.3
C_{ds} in fF	3.0 ± 0.6	3.8 ± 0.8	5.1 ± 1.1
C_{gd} in fF	1.0 ± 0.1	1.8 ± 0.1	3.4 ± 0.1
C_{gse} in fF	1.5 ± 0.1	2.5 ± 0.1	4.5 ± 0.1
C_{gsi} in fF	2.1 ± 0.3	6.4 ± 0.5	23.9 ± 1.0
g_m in mS	3.1 ± 0.2	5.7 ± 0.3	9.2 ± 0.5
g_{ds} in mS	0.90 ± 0.04	0.90 ± 0.04	0.88 ± 0.05
$g_{m,DC}$ in mS	3.8	6.5	9.6
$g_{ds,DC}$ in mS	0.4	0.3	0.3
V_{th} in mV	269.2	365.0	437.3
j_{ds} in $mA/\mu m$	6.66	4.53	2.69
Z_{in} @5GHz in Ω	61.5-6173.1j	82.3-2481.0j	61.5-884.7j
Z_{in} @10GHz in Ω	176.1-3031.2j	108.7-1218.8j	69.9-434.4j
Z_{in} @15GHz in Ω	213.5-2019.4j	132.9-805.7j	81.5-285.8j
Z_{in} @20GHz in Ω	242.7-1372.4j	127.2-565.4j	74.3-205.2j
Z_{out} @5GHz in Ω	1479.3-580.5j	1064.1-821.2j	506.9-656.2j
Z_{out} @10GHz in Ω	1084.7-663.9j	627.5-635.9j	351.1-373.2j
Z_{out} @15GHz in Ω	866.4-615.8j	475.3-490.1j	318.2-257.3j
Z_{out} @20GHz in Ω	656.7-537.2j	377.8-368.7j	294.5-193.7j
f_t in GHz	220 ± 6	171 ± 4	93 ± 1
f_{max} in GHz	209 ± 32	238 ± 22	218 ± 10

200 K

$200K, V_{bg} = 0V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	176.6 ± 52.9	54.4 ± 8.6	12.6 ± 1.7
R_{de} in Ω	98.4 ± 4.2	62.0 ± 2.1	47.5 ± 1.4
R_{se} in Ω	72.1 ± 4.2	51.3 ± 1.9	45.8 ± 1.1
R_{gs} in Ω	30.0 ± 9.1	−3.9 ± 3.0	−16.4 ± 1.1
C_{ds} in fF	2.1 ± 0.4	2.8 ± 0.5	3.7 ± 0.7
C_{gd} in fF	0.8 ± 0.0	1.5 ± 0.0	3.0 ± 0.1
C_{gse} in fF	1.3 ± 0.0	2.3 ± 0.1	4.3 ± 0.1
C_{gsi} in fF	2.7 ± 0.1	8.2 ± 0.3	29.7 ± 0.9
g_m in mS	3.8 ± 0.3	7.9 ± 0.6	10.4 ± 0.9
g_{ds} in mS	0.54 ± 0.03	0.46 ± 0.03	0.37 ± 0.04
$g_{m,DC}$ in mS	4.5	7.3	9.4
$g_{ds,DC}$ in mS	0.3	0.2	0.1
V_{th} in mV	466.7	539.4	587.2
j_{ds} in $mA/\mu m$	4.34	2.53	1.24
Z_{in} @5GHz in Ω	-52.4-6513.5j	58.9-2539.9j	56.8-947.8j
Z_{in} @10GHz in Ω	146.2-3186.0j	106.4-1237.4j	68.3-463.6j
Z_{in} @15GHz in Ω	157.3-2079.9j	112.5-807.0j	72.4-298.1j
Z_{in} @20GHz in Ω	166.0-1459.4j	116.4-572.2j	74.1-212.2j
Z_{out} @5GHz in Ω	2500.5-1233.8j	1476.3-1852.7j	559.2-1210.0j
Z_{out} @10GHz in Ω	1523.3-1359.1j	647.2-1106.2j	389.2-595.7j
Z_{out} @15GHz in Ω	1052.6-1169.5j	463.2-768.8j	356.8-401.7j
Z_{out} @20GHz in Ω	713.6-973.0j	372.7-560.7j	338.2-303.8j
f_t in GHz	254 ± 8	183 ± 4	89 ± 2
f_{max} in GHz	268 ± 33	296 ± 22	307 ± 23

$200K, V_{bg} = 1V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	183.2 ± 53.1	59.1 ± 8.3	17.3 ± 1.6
R_{de} in Ω	85.5 ± 4.0	51.1 ± 1.8	36.3 ± 1.1
R_{se} in Ω	60.6 ± 4.0	40.9 ± 1.8	34.5 ± 0.9
R_{gs} in Ω	48.5 ± 9.0	8.2 ± 2.8	−6.5 ± 1.1
C_{ds} in fF	2.0 ± 0.4	2.7 ± 0.5	3.7 ± 0.8
C_{gd} in fF	0.9 ± 0.0	1.6 ± 0.0	3.2 ± 0.1
C_{gse} in fF	1.3 ± 0.0	2.3 ± 0.1	4.3 ± 0.1
C_{gsi} in fF	2.4 ± 0.1	7.3 ± 0.3	27.1 ± 1.0
g_m in mS	3.6 ± 0.3	6.6 ± 0.5	10.8 ± 0.9
g_{ds} in mS	0.62 ± 0.03	0.57 ± 0.03	0.51 ± 0.04
$g_{m,DC}$ in mS	4.5	7.6	10.9
$g_{ds,DC}$ in mS	0.4	0.3	0.2
V_{th} in mV	389.6	471.3	531.5
j_{ds} in $mA/\mu m$	5.70	3.67	2.02
Z_{in} @5GHz in Ω	-12.4-6445.1j	57.8-2452.1j	54.0-868.3j
Z_{in} @10GHz in Ω	134.2-3160.5j	98.8-1195.6j	66.5-426.3j
Z_{in} @15GHz in Ω	154.4-2058.6j	109.9-779.6j	68.8-273.8j
Z_{in} @20GHz in Ω	171.9-1446.1j	110.5-553.6j	70.1-196.5j
Z_{out} @5GHz in Ω	2120.4-844.8j	1416.6-1372.6j	539.9-960.6j
Z_{out} @10GHz in Ω	1435.2-1040.6j	658.8-926.3j	357.0-477.9j
Z_{out} @15GHz in Ω	1037.3-966.4j	469.6-663.4j	322.9-321.8j
Z_{out} @20GHz in Ω	728.8-841.5j	369.1-492.5j	305.3-243.5j
f_t in GHz	252 ± 8	188 ± 4	100 ± 1
f_{max} in GHz	259 ± 30	284 ± 19	271 ± 15

$200K, V_{bg} = 2V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	186.4 ± 51.0	62.0 ± 8.2	19.8 ± 1.7
R_{de} in Ω	77.3 ± 3.7	44.6 ± 1.7	30.1 ± 0.9
R_{se} in Ω	53.2 ± 3.7	34.8 ± 1.8	28.4 ± 0.9
R_{gs} in Ω	63.9 ± 9.3	16.4 ± 2.9	−0.6 ± 1.1
C_{ds} in fF	1.9 ± 0.4	2.6 ± 0.5	3.7 ± 0.8
C_{gd} in fF	0.9 ± 0.0	1.6 ± 0.0	3.3 ± 0.1
C_{gse} in fF	1.3 ± 0.0	2.3 ± 0.0	4.3 ± 0.1
C_{gsi} in fF	2.2 ± 0.1	6.7 ± 0.2	24.8 ± 0.9
g_m in mS	3.4 ± 0.3	6.2 ± 0.5	10.6 ± 0.8
g_{ds} in mS	0.72 ± 0.03	0.71 ± 0.03	0.68 ± 0.04
$g_{m,DC}$ in mS	4.4	7.6	11.5
$g_{ds,DC}$ in mS	0.4	0.4	0.2
V_{th} in mV	306.2	396.1	469.9
j_{ds} in $mA/\mu m$	7.00	4.79	2.85
Z_{in} @5GHz in Ω	-28.5-6500.9j	52.8-2430.4j	53.2-832.4j
Z_{in} @10GHz in Ω	143.7-3158.1j	102.6-1188.5j	65.6-408.2j
Z_{in} @15GHz in Ω	149.7-2069.3j	107.1-775.8j	66.7-262.6j
Z_{in} @20GHz in Ω	167.0-1462.1j	109.2-550.1j	66.0-187.7j
Z_{out} @5GHz in Ω	1797.2-589.8j	1313.8-990.1j	537.0-783.0j
Z_{out} @10GHz in Ω	1329.6-800.6j	674.9-775.5j	340.9-405.6j
Z_{out} @15GHz in Ω	1013.1-790.8j	475.2-576.4j	301.4-271.8j
Z_{out} @20GHz in Ω	745.3-723.5j	371.4-433.8j	281.8-203.1j
f_t in GHz	247 ± 8	187 ± 4	104 ± 2
f_{max} in GHz	252 ± 28	272 ± 17	252 ± 12

100 K

$100K, V_{bg} = 0V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	195.9 ± 69.8	52.1 ± 9.8	10.5 ± 2.0
R_{de} in Ω	96.3 ± 4.5	58.4 ± 2.1	43.5 ± 1.4
R_{se} in Ω	59.8 ± 4.5	43.8 ± 2.2	39.9 ± 1.3
R_{gs} in Ω	24.5 ± 7.1	−3.2 ± 2.7	−15.0 ± 1.1
C_{ds} in fF	2.3 ± 0.4	3.2 ± 0.7	4.5 ± 1.0
C_{gd} in fF	0.9 ± 0.0	1.6 ± 0.1	3.1 ± 0.1
C_{gse} in fF	1.3 ± 0.1	2.3 ± 0.1	4.4 ± 0.1
C_{gsi} in fF	2.8 ± 0.1	8.5 ± 0.4	30.9 ± 1.0
g_m in mS	4.1 ± 0.4	7.6 ± 0.7	11.8 ± 1.0
g_{ds} in mS	0.52 ± 0.03	0.45 ± 0.04	0.37 ± 0.06
$g_{m,DC}$ in mS	4.9	8.2	10.8
$g_{ds,DC}$ in mS	0.3	0.2	0.2
V_{th} in mV	488.3	558.7	606.1
j_{ds} in $mA/\mu m$	4.36	2.51	1.19
Z_{in} @$5GHz$ in Ω	-86.5-6217.7j	29.6-2406.6j	45.6-889.5j
Z_{in} @$10GHz$ in Ω	41.6-2937.3j	78.7-1151.6j	60.8-431.3j
Z_{in} @$15GHz$ in Ω	110.3-1870.0j	99.2-733.5j	67.0-272.7j
Z_{in} @$20GHz$ in Ω	140.5-1308.2j	105.7-516.7j	67.5-195.6j
Z_{out} @$5GHz$ in Ω	2434.6-1257.6j	1330.3-1813.2j	489.4-1117.6j
Z_{out} @$10GHz$ in Ω	1359.1-1336.0j	545.1-1009.5j	342.5-526.0j
Z_{out} @$15GHz$ in Ω	918.7-1115.8j	407.1-688.4j	328.0-352.1j
Z_{out} @$20GHz$ in Ω	634.2-897.9j	336.4-496.8j	315.0-262.8j
f_t in GHz	262 ± 8	195 ± 4	98 ± 2
f_{max} in GHz	258 ± 34	311 ± 25	351 ± 37

$100K, V_{bg} = 1V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	202.1 ± 68.4	57.1 ± 9.7	15.6 ± 1.9
R_{de} in Ω	83.5 ± 4.2	47.2 ± 1.8	31.7 ± 1.0
R_{se} in Ω	48.8 ± 4.2	33.3 ± 2.1	28.2 ± 1.1
R_{gs} in Ω	42.6 ± 7.2	8.7 ± 2.7	−4.3 ± 1.1
C_{ds} in fF	2.2 ± 0.4	3.1 ± 0.7	4.5 ± 1.0
C_{gd} in fF	0.9 ± 0.0	1.6 ± 0.1	3.2 ± 0.1
C_{gse} in fF	1.3 ± 0.1	2.3 ± 0.1	4.4 ± 0.1
C_{gsi} in fF	2.5 ± 0.1	7.4 ± 0.3	26.9 ± 1.1
g_m in mS	3.8 ± 0.3	7.1 ± 0.6	11.8 ± 1.0
g_{ds} in mS	0.60 ± 0.03	0.55 ± 0.04	0.50 ± 0.06
$g_{m,DC}$ in mS	4.9	8.6	12.5
$g_{ds,DC}$ in mS	0.4	0.3	0.2
V_{th} in mV	411.0	490.4	549.6
j_{ds} in $mA/\mu m$	5.87	3.78	2.07
Z_{in} @5GHz in Ω	-58.6-6178.5j	33.0-2319.6j	45.6-812.0j
Z_{in} @10GHz in Ω	45.9-2919.9j	73.8-1113.7j	60.9-395.6j
Z_{in} @15GHz in Ω	111.4-1874.3j	97.5-709.5j	64.4-249.9j
Z_{in} @20GHz in Ω	139.5-1306.3j	101.7-501.2j	63.6-177.8j
Z_{out} @5GHz in Ω	2074.4-874.4j	1301.8-1363.9j	478.9-887.0j
Z_{out} @10GHz in Ω	1307.7-1050.5j	563.6-861.8j	315.9-426.0j
Z_{out} @15GHz in Ω	929.8-939.0j	415.0-599.4j	295.6-283.0j
Z_{out} @20GHz in Ω	652.2-784.1j	336.3-436.6j	282.7-209.4j
f_t in GHz	260 ± 8	200 ± 5	109 ± 2
f_{max} in GHz	250 ± 32	296 ± 22	296 ± 21

$100K, V_{bg} = 2V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	206.9 ± 69.6	60.1 ± 9.7	18.0 ± 1.9
R_{de} in Ω	75.8 ± 4.1	41.3 ± 1.7	26.1 ± 0.8
R_{se} in Ω	41.9 ± 4.1	27.7 ± 2.1	22.6 ± 1.0
R_{gs} in Ω	56.9 ± 7.7	16.7 ± 2.8	1.2 ± 1.2
C_{ds} in fF	2.1 ± 0.4	3.0 ± 0.6	4.4 ± 1.0
C_{gd} in fF	0.9 ± 0.0	1.7 ± 0.1	3.4 ± 0.1
C_{gse} in fF	1.3 ± 0.1	2.3 ± 0.1	4.4 ± 0.1
C_{gsi} in fF	2.3 ± 0.1	6.7 ± 0.3	24.5 ± 1.0
g_m in mS	3.6 ± 0.3	6.6 ± 0.5	11.5 ± 1.0
g_{ds} in mS	0.70 ± 0.03	0.68 ± 0.04	0.65 ± 0.06
$g_{m,DC}$ in mS	4.8	8.6	13.3
$g_{ds,DC}$ in mS	0.4	0.4	0.3
V_{th} in mV	327.2	415.2	485.9
j_{ds} in $mA/\mu m$	7.29	5.04	3.02
Z_{in} @5GHz in Ω	-43.9-6192.0j	35.7-2305.1j	44.7-778.9j
Z_{in} @10GHz in Ω	62.5-2947.5j	76.3-1106.1j	58.5-379.1j
Z_{in} @15GHz in Ω	104.6-1890.8j	93.4-707.0j	61.7-240.0j
Z_{in} @20GHz in Ω	133.1-1315.6j	99.5-497.7j	61.3-171.5j
Z_{out} @5GHz in Ω	1773.1-612.9j	1236.0-1003.1j	480.3-732.1j
Z_{out} @10GHz in Ω	1239.4-826.1j	585.1-736.3j	302.8-361.9j
Z_{out} @15GHz in Ω	919.2-781.5j	422.4-528.1j	276.6-239.9j
Z_{out} @20GHz in Ω	663.5-679.2j	338.3-388.5j	263.4-176.7j
f_t in GHz	254 ± 8	198 ± 5	113 ± 2
f_{max} in GHz	242 ± 31	283 ± 20	274 ± 17

6 K

$6K, V_{bg} = 0V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	192.4 ± 122.4	55.9 ± 15.6	11.4 ± 2.9
R_{de} in Ω	85.5 ± 6.6	51.6 ± 2.8	39.1 ± 1.5
R_{se} in Ω	57.2 ± 6.6	40.0 ± 2.0	36.3 ± 1.0
R_{gs} in Ω	19.1 ± 6.8	2.5 ± 2.6	−11.4 ± 1.2
C_{ds} in fF	2.4 ± 0.4	3.0 ± 0.4	3.3 ± 0.6
C_{gd} in fF	0.9 ± 0.1	1.6 ± 0.1	3.0 ± 0.1
C_{gse} in fF	1.2 ± 0.2	2.1 ± 0.1	3.8 ± 0.2
C_{gsi} in fF	2.8 ± 0.2	8.1 ± 0.4	29.6 ± 0.9
g_m in mS	4.2 ± 0.5	7.7 ± 0.8	11.9 ± 1.0
g_{ds} in mS	0.60 ± 0.03	0.60 ± 0.03	0.61 ± 0.04
$g_{m,DC}$ in mS	5.1	8.5	11.4
$g_{ds,DC}$ in mS	0.3	0.2	0.2
V_{th} in mV	494.0	564.4	611.2
j_{ds} in $mA/\mu m$	4.41	2.52	1.18
Z_{in} @5GHz in Ω	-30.2-6199.9j	44.4-2385.6j	45.4-885.9j
Z_{in} @10GHz in Ω	-62.7-3018.5j	59.8-1152.8j	45.5-429.0j
Z_{in} @15GHz in Ω	78.9-1944.9j	87.2-740.6j	57.2-272.2j
Z_{in} @20GHz in Ω	133.7-1336.2j	96.5-535.2j	61.9-202.8j
Z_{out} @5GHz in Ω	2124.2-997.8j	1295.2-1315.7j	589.2-904.9j
Z_{out} @10GHz in Ω	1419.4-1280.4j	607.1-950.8j	353.8-500.1j
Z_{out} @15GHz in Ω	922.1-1069.5j	397.0-656.9j	319.4-315.1j
Z_{out} @20GHz in Ω	628.3-861.9j	330.5-461.8j	301.8-240.9j
f_t in GHz	283 ± 17	209 ± 6	104 ± 2
f_{max} in GHz	380 ± 899	317 ± 43	359 ± 50

$6K, V_{bg} = 1V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	197.6 ± 121.4	60.6 ± 15.6	16.3 ± 2.9
R_{de} in Ω	75.8 ± 6.1	42.0 ± 2.5	27.5 ± 1.1
R_{se} in Ω	48.2 ± 6.1	30.8 ± 2.1	24.7 ± 0.9
R_{gs} in Ω	32.8 ± 7.3	12.1 ± 2.7	−1.5 ± 1.3
C_{ds} in fF	2.3 ± 0.4	3.0 ± 0.5	3.1 ± 0.6
C_{gd} in fF	0.9 ± 0.1	1.6 ± 0.1	3.2 ± 0.1
C_{gse} in fF	1.2 ± 0.2	2.1 ± 0.1	3.8 ± 0.2
C_{gsi} in fF	2.5 ± 0.1	7.2 ± 0.3	25.4 ± 0.8
g_m in mS	4.0 ± 0.5	7.4 ± 0.7	11.9 ± 0.9
g_{ds} in mS	0.68 ± 0.03	0.69 ± 0.03	0.70 ± 0.04
$g_{m,DC}$ in mS	5.1	9.0	13.2
$g_{ds,DC}$ in mS	0.4	0.4	0.2
V_{th} in mV	416.0	497.0	555.5
j_{ds} in $mA/\mu m$	5.97	3.83	2.10
Z_{in} @5GHz in Ω	-41.0-6169.5j	51.2-2294.3j	42.7-811.6j
Z_{in} @10GHz in Ω	-52.5-2991.0j	61.5-1113.2j	43.2-394.5j
Z_{in} @15GHz in Ω	78.9-1946.1j	84.1-715.6j	53.7-248.1j
Z_{in} @20GHz in Ω	126.5-1330.4j	94.5-516.3j	57.5-185.6j
Z_{out} @5GHz in Ω	1850.2-745.3j	1187.6-1030.7j	527.3-717.0j
Z_{out} @10GHz in Ω	1336.4-1023.4j	602.5-807.2j	320.3-407.9j
Z_{out} @15GHz in Ω	922.6-912.0j	396.4-575.3j	287.5-253.5j
Z_{out} @20GHz in Ω	642.1-759.3j	324.4-407.3j	271.6-194.4j
f_t in GHz	281 ± 17	214 ± 6	116 ± 3
f_{max} in GHz	335 ± 458	302 ± 38	303 ± 29

$6K, V_{bg} = 2V$	Small nFET	Medium nFET	Large nFET
R_{ge} in Ω	198.4 ± 120.4	62.7 ± 15.4	18.4 ± 2.9
R_{de} in Ω	69.5 ± 5.9	37.1 ± 2.3	22.7 ± 1.0
R_{se} in Ω	42.5 ± 5.9	26.1 ± 2.1	19.9 ± 0.9
R_{gs} in Ω	42.8 ± 7.3	18.3 ± 2.7	3.0 ± 1.4
C_{ds} in fF	2.3 ± 0.4	3.1 ± 0.5	3.7 ± 0.8
C_{gd} in fF	0.9 ± 0.1	1.7 ± 0.1	3.3 ± 0.1
C_{gse} in fF	1.2 ± 0.2	2.1 ± 0.1	3.9 ± 0.2
C_{gsi} in fF	2.3 ± 0.1	6.7 ± 0.3	23.6 ± 0.8
g_m in mS	3.8 ± 0.4	6.9 ± 0.6	11.6 ± 0.9
g_{ds} in mS	0.76 ± 0.03	0.80 ± 0.04	0.85 ± 0.04
$g_{m,DC}$ in mS	5.0	8.9	14.0
$g_{ds,DC}$ in mS	0.4	0.4	0.4
V_{th} in mV	332.4	421.6	492.0
j_{ds} in $mA/\mu m$	7.45	5.15	3.10
Z_{in} @5GHz in Ω	-9.9-6159.6j	54.9-2277.5j	46.9-778.0j
Z_{in} @10GHz in Ω	-27.9-2999.0j	61.9-1106.7j	45.3-379.7j
Z_{in} @15GHz in Ω	77.2-1953.3j	84.8-714.2j	52.9-239.9j
Z_{in} @20GHz in Ω	129.7-1338.5j	92.1-515.3j	55.8-179.8j
Z_{out} @5GHz in Ω	1621.5-565.3j	1095.6-818.4j	479.1-597.4j
Z_{out} @10GHz in Ω	1256.3-817.1j	597.0-698.0j	299.0-344.6j
Z_{out} @15GHz in Ω	907.1-771.9j	401.1-515.0j	266.3-217.2j
Z_{out} @20GHz in Ω	647.3-673.0j	322.1-366.9j	249.3-165.2j
f_t in GHz	273 ± 16	211 ± 6	120 ± 3
f_{max} in GHz	323 ± 334	290 ± 35	283 ± 24

B.2 pMOS

300 K

$300K, V_{bg} = -0.8V$	Small pFET	Medium pFET	Large pFET
R_{ge} in Ω	160.1 ± 34.9	49.1 ± 9.7	15.1 ± 2.5
R_{de} in Ω	102.3 ± 4.2	62.9 ± 1.9	51.7 ± 1.0
R_{se} in Ω	74.8 ± 4.2	65.2 ± 2.5	57.2 ± 1.3
R_{gs} in Ω	42.3 ± 13.1	−8.2 ± 3.7	−15.7 ± 1.6
C_{ds} in fF	2.3 ± 0.5	4.4 ± 0.7	4.7 ± 0.9
C_{gd} in fF	1.1 ± 0.0	2.0 ± 0.1	3.8 ± 0.1
C_{gse} in fF	1.4 ± 0.1	2.7 ± 0.1	4.8 ± 0.1
C_{gsi} in fF	2.3 ± 0.2	7.0 ± 0.4	24.8 ± 0.7
g_m in mS	2.6 ± 0.2	4.3 ± 0.3	6.4 ± 0.5
g_{ds} in mS	0.58 ± 0.03	0.56 ± 0.04	0.54 ± 0.04
$g_{m,DC}$ in mS	3.3	4.7	6.1
$g_{ds,DC}$ in mS	0.3	0.3	0.2
V_{th} in mV	442.2	522.0	552.6
j_{ds} in $mA/\mu m$	-3.59	-1.83	-1.01
Z_{in} @5GHz in Ω	159.1-6143.5j	89.9-2571.0j	74.8-984.7j
Z_{in} @10GHz in Ω	138.0-3018.3j	105.6-1252.4j	81.8-482.2j
Z_{in} @15GHz in Ω	182.0-1910.1j	125.5-826.3j	89.9-320.0j
Z_{in} @20GHz in Ω	234.5-1396.2j	138.1-579.4j	89.5-227.9j
Z_{out} @5GHz in Ω	2069.1-1043.9j	1219.2-1434.6j	574.4-985.6j
Z_{out} @10GHz in Ω	1352.4-1040.7j	634.6-933.6j	413.8-536.6j
Z_{out} @15GHz in Ω	1006.8-925.1j	468.4-674.9j	375.3-381.5j
Z_{out} @20GHz in Ω	790.0-762.0j	387.6-488.9j	347.0-291.4j
f_t in GHz	167 ± 4	116 ± 2	62 ± 1
f_{max} in GHz	196 ± 21	217 ± 21	208 ± 18

$300K, V_{bg} = -2.8V$	Small pFET	Medium pFET	Large pFET
R_{ge} in Ω	-64.8 ± 81.5	50.4 ± 9.7	20.2 ± 2.1
R_{de} in Ω	95.6 ± 4.1	59.7 ± 1.8	35.6 ± 0.9
R_{se} in Ω	61.0 ± 4.1	61.9 ± 2.4	39.9 ± 1.0
R_{gs} in Ω	40.6 ± 12.5	-4.3 ± 3.7	-0.7 ± 1.6
C_{ds} in fF	2.9 ± 0.4	4.3 ± 0.6	4.7 ± 0.9
C_{gd} in fF	1.2 ± 0.0	2.1 ± 0.1	4.1 ± 0.1
C_{gse} in fF	1.7 ± 0.1	2.7 ± 0.1	4.9 ± 0.2
C_{gsi} in fF	2.2 ± 0.2	6.9 ± 0.4	22.1 ± 0.9
g_m in mS	2.4 ± 0.2	4.3 ± 0.3	6.6 ± 0.5
g_{ds} in mS	0.58 ± 0.04	0.57 ± 0.04	0.71 ± 0.04
$g_{m,DC}$ in mS	3.3	4.8	6.2
$g_{ds,DC}$ in mS	0.4	0.3	0.2
V_{th} in mV	389.2	504.9	545.0
j_{ds} in $mA/\mu m$	-4.31	-2.04	-1.10
Z_{in} @5GHz in Ω	-248.5-5861.5j	85.4-2549.7j	64.5-910.9j
Z_{in} @10GHz in Ω	-94.9-2709.7j	105.1-1243.0j	73.5-444.5j
Z_{in} @15GHz in Ω	74.5-1679.8j	123.7-818.1j	83.2-295.3j
Z_{in} @20GHz in Ω	162.9-1219.0j	135.6-575.8j	83.2-210.5j
Z_{out} @5GHz in Ω	1947.5-993.2j	1216.8-1384.8j	549.6-763.1j
Z_{out} @10GHz in Ω	1174.4-1048.9j	637.4-910.4j	374.3-423.6j
Z_{out} @15GHz in Ω	817.3-895.3j	470.3-656.4j	337.2-298.2j
Z_{out} @20GHz in Ω	636.8-703.7j	384.6-480.2j	312.2-228.2j
f_t in GHz	151 ± 7	117 ± 2	68 ± 1
f_{max} in GHz	409 ± 538	215 ± 20	182 ± 10

200 K

$200K, V_{bg} = -0.8V$	Small pFET	Medium pFET	Large pFET
R_{ge} in Ω	156.1 ± 71.7	46.2 ± 7.9	10.3 ± 2.3
R_{de} in Ω	104.3 ± 6.1	73.1 ± 2.7	55.1 ± 1.9
R_{se} in Ω	73.6 ± 6.1	60.3 ± 2.0	53.7 ± 1.1
R_{gs} in Ω	19.4 ± 13.4	−17.2 ± 3.8	−21.6 ± 1.1
C_{ds} in fF	1.4 ± 0.3	2.7 ± 0.4	2.4 ± 0.5
C_{gd} in fF	0.9 ± 0.0	1.9 ± 0.1	3.8 ± 0.2
C_{gse} in fF	1.2 ± 0.1	2.6 ± 0.1	4.8 ± 0.1
C_{gsi} in fF	2.4 ± 0.1	7.4 ± 0.3	26.2 ± 0.8
g_m in mS	2.9 ± 0.2	4.7 ± 0.4	7.3 ± 0.7
g_{ds} in mS	0.49 ± 0.02	0.42 ± 0.02	0.35 ± 0.03
$g_{m,DC}$ in mS	3.7	5.4	7.2
$g_{ds,DC}$ in mS	0.3	0.2	0.1
V_{th} in mV	493.1	549.4	575.7
j_{ds} in $mA/\mu m$	-3.29	-1.81	-1.03
Z_{in} @$5GHz$ in Ω	39.8-6673.9j	84.9-2575.2j	65.1-955.9j
Z_{in} @$10GHz$ in Ω	120.8-3294.7j	99.2-1255.5j	75.1-465.1j
Z_{in} @$15GHz$ in Ω	107.2-2122.0j	105.7-805.6j	80.5-300.6j
Z_{in} @$20GHz$ in Ω	187.6-1525.4j	119.4-569.4j	80.3-210.7j
Z_{out} @$5GHz$ in Ω	2577.0-1087.8j	1547.5-1822.6j	605.0-1201.3j
Z_{out} @$10GHz$ in Ω	1765.1-1416.2j	675.4-1159.0j	410.9-606.2j
Z_{out} @$15GHz$ in Ω	1224.2-1274.8j	466.0-796.0j	374.3-411.8j
Z_{out} @$20GHz$ in Ω	929.6-1078.9j	374.7-579.9j	339.6-313.0j
f_t in GHz	204 ± 6	126 ± 3	67 ± 2
f_{max} in GHz	264 ± 125	243 ± 19	264 ± 27

$200K, V_{bg} = -2.8V$	Small pFET	Medium pFET	Large pFET
R_{ge} in Ω	23.4 ± 81.1	6.9 ± 11.9	19.2 ± 2.2
R_{de} in Ω	78.0 ± 5.6	60.4 ± 2.4	33.6 ± 1.2
R_{se} in Ω	48.4 ± 5.6	46.9 ± 1.9	32.3 ± 0.8
R_{gs} in Ω	52.1 ± 14.8	−5.1 ± 3.8	−1.7 ± 1.0
C_{ds} in fF	1.7 ± 0.3	3.2 ± 0.4	2.8 ± 0.5
C_{gd} in fF	1.0 ± 0.1	2.0 ± 0.1	4.0 ± 0.1
C_{gse} in fF	1.4 ± 0.1	2.9 ± 0.1	4.8 ± 0.1
C_{gsi} in fF	1.9 ± 0.1	6.6 ± 0.3	21.7 ± 0.9
g_m in mS	2.6 ± 0.2	4.5 ± 0.4	7.8 ± 0.7
g_{ds} in mS	0.52 ± 0.02	0.42 ± 0.02	0.51 ± 0.03
$g_{m,DC}$ in mS	3.8	5.6	8.7
$g_{ds,DC}$ in mS	0.4	0.2	0.2
V_{th} in mV	393.7	521.1	478.5
j_{ds} in $mA/\mu m$	-4.84	-2.16	-2.07
Z_{in} @5GHz in Ω	-95.9-6527.0j	23.4-2484.2j	59.5-867.7j
Z_{in} @10GHz in Ω	-43.4-3121.5j	45.7-1188.4j	69.0-422.5j
Z_{in} @15GHz in Ω	27.7-1980.7j	76.9-753.2j	73.7-273.3j
Z_{in} @20GHz in Ω	153.1-1408.9j	107.0-525.6j	74.0-191.0j
Z_{out} @5GHz in Ω	2186.3-807.2j	1454.6-1629.6j	582.3-890.9j
Z_{out} @10GHz in Ω	1547.0-1172.9j	594.3-1066.7j	371.6-463.5j
Z_{out} @15GHz in Ω	1067.8-1092.1j	406.3-711.1j	333.1-315.1j
Z_{out} @20GHz in Ω	801.6-911.8j	330.2-509.9j	301.9-237.4j
f_t in GHz	196 ± 6	125 ± 2	76 ± 1
f_{max} in GHz	555 ± 1000	728 ± 882	198 ± 11

100 K

$100K, V_{bg} = -0.8V$	Small pFET	Medium pFET	Large pFET
R_{ge} in Ω	113.5 ± 91.7	36.2 ± 7.5	6.9 ± 2.4
R_{de} in Ω	108.2 ± 7.2	74.3 ± 3.4	56.7 ± 2.1
R_{se} in Ω	76.1 ± 7.2	60.6 ± 2.3	53.0 ± 1.3
R_{gs} in Ω	17.0 ± 10.8	−18.8 ± 3.4	−23.5 ± 1.1
C_{ds} in fF	1.5 ± 0.3	3.1 ± 0.4	2.6 ± 0.6
C_{gd} in fF	0.9 ± 0.1	1.9 ± 0.1	3.8 ± 0.2
C_{gse} in fF	1.2 ± 0.1	2.6 ± 0.1	4.8 ± 0.1
C_{gsi} in fF	2.8 ± 0.2	8.5 ± 0.5	28.6 ± 0.7
g_m in mS	3.5 ± 0.4	5.5 ± 0.6	8.3 ± 0.8
g_{ds} in mS	0.54 ± 0.03	0.44 ± 0.03	0.38 ± 0.04
$g_{m,DC}$ in mS	4.1	5.9	7.7
$g_{ds,DC}$ in mS	0.3	0.2	0.1
V_{th} in mV	524.9	576.9	603.1
j_{ds} in $mA/\mu m$	-3.06	-1.62	-0.88
Z_{in} @$5GHz$ in Ω	-89.5-6517.1j	39.9-2492.6j	59.8-927.7j
Z_{in} @$10GHz$ in Ω	5.5-3112.3j	70.2-1192.2j	67.9-446.7j
Z_{in} @$15GHz$ in Ω	30.6-1997.9j	98.5-755.0j	74.7-285.8j
Z_{in} @$20GHz$ in Ω	128.3-1396.1j	115.1-520.9j	77.0-200.3j
Z_{out} @$5GHz$ in Ω	2509.6-1020.8j	1495.5-1766.0j	585.4-1148.9j
Z_{out} @$10GHz$ in Ω	1629.7-1370.8j	612.9-1074.2j	387.6-565.8j
Z_{out} @$15GHz$ in Ω	1095.3-1187.7j	417.7-712.2j	355.1-381.5j
Z_{out} @$20GHz$ in Ω	793.6-955.3j	345.6-499.7j	327.8-284.4j
f_t in GHz	220 ± 7	135 ± 3	71 ± 2
f_{max} in GHz	338 ± 245	285 ± 46	346 ± 82

$100K, V_{bg} = -2.8V$	Small pFET	Medium pFET	Large pFET
R_{ge} in Ω	126.9 ± 90.7	49.2 ± 7.5	17.2 ± 2.4
R_{de} in Ω	81.2 ± 6.2	43.9 ± 2.1	31.8 ± 1.2
R_{se} in Ω	50.6 ± 6.2	32.2 ± 2.1	28.4 ± 0.9
R_{gs} in Ω	53.9 ± 11.9	14.4 ± 3.4	0.2 ± 1.1
C_{ds} in fF	1.4 ± 0.3	2.9 ± 0.4	3.0 ± 0.5
C_{gd} in fF	1.0 ± 0.1	2.0 ± 0.1	4.0 ± 0.2
C_{gse} in fF	1.2 ± 0.1	2.6 ± 0.1	4.8 ± 0.1
C_{gsi} in fF	2.2 ± 0.1	6.1 ± 0.3	22.1 ± 1.0
g_m in mS	3.1 ± 0.3	4.8 ± 0.4	8.0 ± 0.8
g_{ds} in mS	0.54 ± 0.02	0.50 ± 0.02	0.49 ± 0.03
$g_{m,DC}$ in mS	4.2	4.2	9.5
$g_{ds,DC}$ in mS	0.4	0.1	0.2
V_{th} in mV	459.7	651.0	517.2
j_{ds} in $mA/\mu m$	-4.22	-0.56	-1.87
Z_{in} @5GHz in Ω	-112.6-6419.8j	37.2-2357.0j	53.5-832.0j
Z_{in} @10GHz in Ω	-5.3-3077.7j	67.5-1127.9j	64.3-401.3j
Z_{in} @15GHz in Ω	21.9-1957.3j	96.2-715.0j	69.0-256.1j
Z_{in} @20GHz in Ω	125.5-1378.2j	106.4-492.4j	70.6-178.7j
Z_{out} @5GHz in Ω	2220.4-796.5j	1381.3-1248.6j	553.5-852.6j
Z_{out} @10GHz in Ω	1555.4-1147.2j	616.3-871.4j	349.1-431.9j
Z_{out} @15GHz in Ω	1072.0-1035.7j	420.0-592.9j	315.8-289.2j
Z_{out} @20GHz in Ω	790.1-851.1j	336.6-423.6j	288.5-215.3j
f_t in GHz	223 ± 7	143 ± 3	81 ± 1
f_{max} in GHz	312 ± 217	242 ± 23	218 ± 14

6 K

$6K, V_{bg} = -0.8V$	Small pFET	Medium pFET	Large pFET
R_{ge} in Ω	151.6 ± 77.8	21.8 ± 10.6	7.5 ± 4.3
R_{de} in Ω	115.7 ± 6.6	83.9 ± 2.8	61.0 ± 2.9
R_{se} in Ω	83.3 ± 6.6	70.3 ± 2.2	60.5 ± 1.3
R_{gs} in Ω	0.4 ± 10.4	−36.9 ± 3.1	−33.5 ± 1.2
C_{ds} in fF	1.6 ± 0.2	3.1 ± 0.3	2.4 ± 0.6
C_{gd} in fF	0.9 ± 0.1	1.7 ± 0.1	3.4 ± 0.2
C_{gse} in fF	1.4 ± 0.1	2.5 ± 0.1	4.4 ± 0.3
C_{gsi} in fF	3.3 ± 0.2	10.2 ± 0.4	34.0 ± 1.1
g_m in mS	3.8 ± 0.4	6.4 ± 0.6	9.9 ± 1.0
g_{ds} in mS	0.64 ± 0.03	0.61 ± 0.02	0.60 ± 0.05
$g_{m,DC}$ in mS	4.2	6.0	7.9
$g_{ds,DC}$ in mS	0.3	0.2	0.1
V_{th} in mV	532.1	584.0	609.3
j_{ds} in $mA/\mu m$	-3.02	-1.58	-0.86
Z_{in} @5GHz in Ω	-110.6-6273.3j	57.3-2482.1j	57.6-922.2j
Z_{in} @10GHz in Ω	49.9-3069.1j	61.5-1224.9j	50.5-452.7j
Z_{in} @15GHz in Ω	80.6-1849.1j	75.5-770.2j	72.7-288.6j
Z_{in} @20GHz in Ω	152.0-1327.6j	99.5-550.9j	71.0-208.3j
Z_{out} @5GHz in Ω	2273.2-854.7j	1483.2-1445.0j	645.1-1032.0j
Z_{out} @10GHz in Ω	1609.6-1190.2j	678.2-1065.6j	377.2-575.0j
Z_{out} @15GHz in Ω	1028.5-1109.9j	430.0-718.4j	356.5-369.0j
Z_{out} @20GHz in Ω	742.8-869.2j	352.5-518.8j	325.5-281.2j
f_t in GHz	218 ± 7	141 ± 3	76 ± 3
f_{max} in GHz	285 ± 162	474 ± 440	397 ± 174

$6K, V_{bg} = -2.8V$	Small pFET	Medium pFET	Large pFET
R_{ge} in Ω	178.2 ± 76.7	40.6 ± 10.6	19.4 ± 4.2
R_{de} in Ω	66.9 ± 5.4	43.0 ± 1.9	28.7 ± 2.0
R_{se} in Ω	39.9 ± 5.4	32.0 ± 2.2	27.4 ± 1.1
R_{gs} in Ω	69.7 ± 13.1	6.3 ± 3.4	−0.8 ± 1.0
C_{ds} in fF	1.5 ± 0.2	2.7 ± 0.2	2.7 ± 0.5
C_{gd} in fF	1.0 ± 0.1	1.9 ± 0.1	3.9 ± 0.2
C_{gse} in fF	1.4 ± 0.1	2.5 ± 0.1	4.5 ± 0.3
C_{gsi} in fF	2.0 ± 0.1	6.1 ± 0.2	22.3 ± 0.8
g_m in mS	3.0 ± 0.2	5.0 ± 0.3	8.3 ± 0.7
g_{ds} in mS	0.61 ± 0.02	0.60 ± 0.02	0.63 ± 0.03
$g_{m,DC}$ in mS	4.4	6.8	10.1
$g_{ds,DC}$ in mS	0.4	0.4	0.3
V_{th} in mV	416.2	476.4	514.4
j_{ds} in $mA/\mu m$	-5.14	-3.19	-2.00
Z_{in} @5GHz in Ω	-44.2-6142.8j	77.1-2345.7j	53.3-820.9j
Z_{in} @10GHz in Ω	51.6-3019.9j	65.4-1157.4j	46.9-403.4j
Z_{in} @15GHz in Ω	78.7-1812.5j	77.1-730.1j	66.3-257.0j
Z_{in} @20GHz in Ω	153.7-1307.3j	94.2-523.4j	63.7-185.5j
Z_{out} @5GHz in Ω	1873.0-601.4j	1299.0-1017.0j	563.5-744.4j
Z_{out} @10GHz in Ω	1440.8-882.2j	659.2-852.2j	336.4-431.7j
Z_{out} @15GHz in Ω	991.6-888.0j	425.0-596.7j	307.7-274.4j
Z_{out} @20GHz in Ω	730.7-726.8j	340.5-436.9j	279.6-208.0j
f_t in GHz	218 ± 8	151 ± 3	86 ± 2
f_{max} in GHz	247 ± 178	284 ± 46	216 ± 22

B.3 Deembedding structure

Deembedding Structure	6 K	100 K	200 K	300 K
R_{gc}	0.373 Ω	0.354 Ω	0.443 Ω	0.558 Ω
R_{dc}	0.376 Ω	0.351 Ω	0.466 Ω	0.508 Ω
R_{sc}	0.168 Ω	0.274 Ω	0.410 Ω	0.568 Ω
L_{gc}	23.1 pH	26.4 pH	23.8 pH	25.3 pH
L_{dc}	23.6 pH	25.8 pH	22.8 pH	15.8 pH
L_{sc}	7.8 pH	7.7 pH	8.1 pH	9.0 pH
C_{gc}	72 fF	85 fF	82 fF	81 fF
C_{dc}	80 fF	97 fF	94 fF	90 fF

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