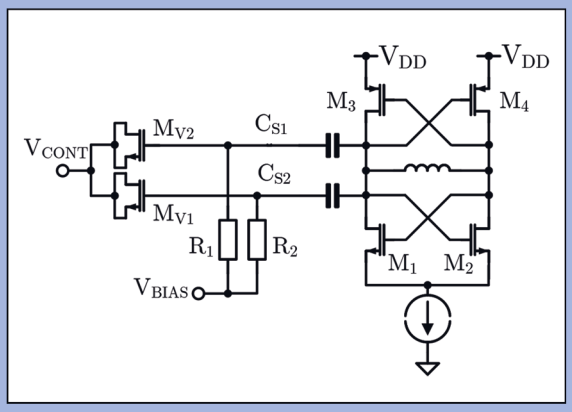

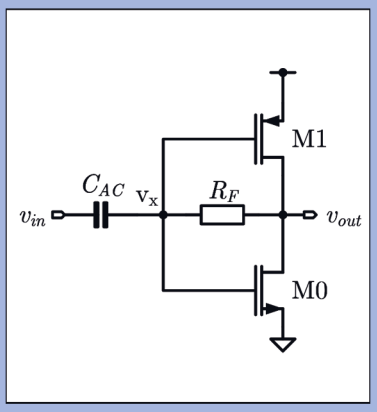

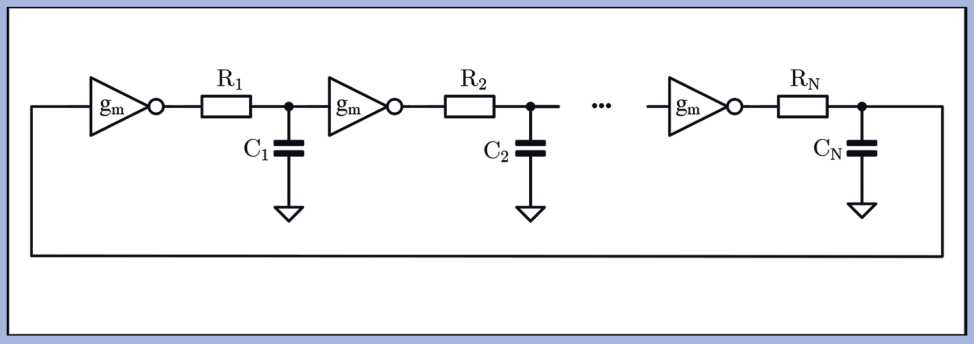

Integrated Control Electronics for Qubits at Ultra Low Temperature

Dennis Nielinger

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We are not lost. We're locationally challenged.

John M. Ford

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Abstract

Quantum computing has shown an increased interest in recent years. The basis of a quantum computer is a qubit, which is the quantum equivalent of a classical bit. Common qubit are only viable in a cryogenic environment and need electrical connections to operate. For this, it is needed to solve the problem to bringing more qubits into the cryostat and connecting the quantum and the macroscopic world. The number of qubits per cryostat is limited just by the amount of interconnects and cooling power of the cryostat even if one neglect the other challenges which come with the increasing number of qubits integrated on one chip.

This work investigates the performance of different integrated circuit architectures for operating at low temperature. The goal is to place the control electronics in close vicinity of the qubit itself and replace parts of the classical control electronics which by now are located at room temperature. The particular circuits investigated and implemented focus on the needs for operating a GaAs singlet triplet qubit. These qubits need frequency synthesis, biasing and readout circuitry to operate.

This work includes the implementation of a digital controlled oscillator operating at a frequency of 500 MHz, a voltage controlled oscillator operating at 20 GHz and a 8-bit digital to analog converter with a sample rate of 250 MHz. The circuitry was fabricated on a 2 x 2 mm^2 65 nm chip. The performance of the circuitry is evaluated at room temperature and in a closed-cycle Gifford-McMahon cryostat down to temperatures as low as 6 K. The results are compared and cryogenic effects are discussed.

Zusammenfassung

Das Interesse an Quantumcomputing ist in den letzten Jahren sehr gestiegen. Das Grundelement des Quantencomputers ist das Qubit, das Äquivalent zu dem klassischen binären Bit. Ein Qubit kann nur bei kryogenen Temperaturen betrieben werden und benötigt klassische Kontrollelektronik. Dazu ist es notwendig, mehr Qubits in den Kryostaten zu bringen und die Quanten- und die makroskopische Welt zu verbinden. Selbst wenn man die anderen Herausforderungen vernachlässigt, die aus der steigenden Anzahl von Qubitspro Chip resultieren, ist die Anzahl der Qubits pro Kryostaten allein durch die Anzahl der Verbindungsleitungen und die Kühlleistung des Kryostaten begrenzt.

Diese Arbeit untersucht die Leistungsfähigkeit verschiedener integrierter Schaltkreisarchitekturen für den Betrieb bei niedrigen Temperaturen. Ziel ist es, die Kontrollelektronik in unmittelbarer Nähe des Qubits zu platzieren und Teile der klassischen Kontrollelektronik, die sich jetzt bei Raumtemperatur befinden, zu ersetzen. Die untersuchten und implementierten Schaltungen konzentrieren sich auf die Anforderungen für den Betrieb von GaAs-Singlet-Triplett-Qubits. Diese Qubits benötigen Frequenzsynthese-, Bias- und Ausleseschaltungen zum Betrieb.

Diese Arbeit umfasst die Implementierung eines digital gesteuerten Oszillators, mit einer Frequenz von 500 MHz, eines spannungsgesteuerten Oszillators mit 20 GHz und eines 8-Bit Digital-Analog-Wandler mit einer Abtastrate von 250 MHz. Die Schaltung wurde hergestellt auf einem 2 x 2 mm^2 großen 65-nm-Chip gefertigt

Die Performance der Schaltungen wurde bei Raumtemperatur und in einem Gifford-McMahon-Kryostaten bei Temperaturen um 6K evaluiert. Die Ergebnisse werden miteinander verglichen und die kryogenen Effekte diskutiert.

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Acronyms

2DEG	Two-dimensional electron gas
AC	Alternating current
ADC	Analog to digital converter
ASIC	Application-specific integrated circuit
BiCMOS	Bipolar Complementary metal–oxide–semiconductor
CM	Common-mode
CMOS	Complementary metal–oxide–semiconductor
D flip-flop	delay flip-flop D
DAC	Digital to analog converter
DC	Direct current
DCO	Digital Controlled Oscillator
DNL	Differential non-linearity
DUT	Device under test
ESD	Electrostatic discharge
FF	Flip-flop
GaAlAs	Aluminium gallium arsenide
GaAs	Galium arsenid
GM	Gifford-McMahon
I^2C	Inter-Integrated Circuit
I/O	Input/output
IC	Integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral non-linearity
MOSFET	metal–oxide–semiconductor field-effect transistor
NMOS	n-channel MOSFET
PCB	Printed circuit board
PEX	Parasitic exctracted
PMOS	p-channel MOSFET
QC	Quantum Computing
qubit	Quantum bit
RF	Radio frequency
scl	Serial clock line
sda	Serial data line
SOC	System on a chip
SOI	Silicon on insulator

SOS	Silicon on Saphire
SQuBiC	Scalable quantum bit control
SRAM	Static random acces memory
SSA	Signal Source Analyzer
TSV	Through silicon via

Chapter 1

Introduction

1.1 Motivation

Quantum computing is a topic that has received increasing attention over the recent years. One reason are the opportunities arising from a universal quantum computer. Quantum computers are believed to speed up the solution of specific tasks such as drug development, traffic optimization or prime number segmentation. In the IVF proposal [1] inside the Helmholtz Association 'Scalable solid state quantum computing' it is stated:

> "It has been argued that we are on the threshold of a second quantum revolution based on utilizing essential aspects of quantum mechanics such as superpositions and entanglement on macroscopic scales. Among the shorter-term promises of this revolution are improved sensors and a better understanding of complex quantum systems via dedicated analogue quantum simulators. The vision that probably lies furthest in the future, but may eventually also have the largest impact, is to put large-scale information processing on a quantum-mechanical footing. This change of paradigm is expected to enable an exponential speed-up of certain computational tasks, and arm physical basis for the security and privacy of data. It is arguably more fundamental than the 5000 year-long evolution from the abacus to today's semiconductor circuits."

This is underlined by recently published results from Googles Sycamore qubit chip [2], with 53 qubits, which shows that even this low number of qubits can perform operations which conventional computers would need several thousands of years to solve.

Many challenges have to be solved to enable a universal quantum computer of any kind. One of the very first challenge is the number of qubits needed for the operation of any "useful" quantum algorithm. It is easily in the range of millions to billions depending on estimations and algorithms. Another challenge is that the qubits which make up the quantum computer are typically at temperatures as low as 100 mK which brings the challenge of operating electrical circuits at such low temperatures. Even more elementary

problems such as the sheer number of interconnects which have to be connected to some kind of room temperatures electronics occur.

To overcome the challenges associated with extending the currently used room temperature based control electronics to millions of qubits, it is very attractive to relocate as much of the control circuitry as useful to the immediate vicinity of the qubits. One central element of our envisioned system architecture is the use of integrated, cryogenic qubit control electronics. Very few activities so far address this challenge, since it lies outside recent experimental quantum information research. Clock and bias generation is one of the preconditions for electronic circuity of any substantial complexity.

This work aims to design and implement circuitry that can be investigated for the usage in the generation of controlled voltages and frequency signals for the use of very low temperature circuits based on standard-CMOS processes as vehicle for assessing the principal concepts.

1.2 Organization of this thesis

This work is divided into six chapters. The first is the introduction chapter, followed by a chapter on fundamentals, which covers the basic knowledge needed in order to understand quantum computing and discusses some of its different implementations and the basic of cryogenic CMOS operation. Based on the chosen implementation, the third chapter derives the required electrical signals and architectures needed to operate a qubit. Following the requirement description, different architecture choices are discussed. The implementation of the architecture is shown in the fourth chapter. The fabricated chip is measured at both cryogenic as well as room temperature and the following chapter discusses the results. The final chapter concludes this work with a summary and an outlook towards future research.

Chapter 2

Fundamentals of Quantum Computing

In this chapter the requirements for quantum computers and the definitions for basic qubit operations are derived. A brief introduction into quantum gates is given and the different types of qubit implementations are quickly summarized and compared.

2.1 Requirements for Quantum Computing

DiVincenzo proposed five conditions which have to be fulfilled for the construction of an universal quantum computer [3]:

1. The available qubits must be well characterized, it must be possible to place them in a scaleable way. This means a sufficiently large number of qubits must be contained within the computer.
2. It must be possible to initialize the qubit into an initial quantum state.
3. Qubits should exhibit a long relevant decoherence time. During the operation the actual and ideal qubit state should not be distinguishable.
4. It must be possible to implement a set of basic logical gates with a high fidelity.
5. It must be possible to measure the 0 and 1 state of any individual qubit.

In the following chapters the five conditions are analyzed. In chapter 2.2 the basic definitions for the quantum computing are given with respect to condition 5. Condition 3 is related to chapter 2.3 , were the qubits are explained in detail and typical error and their timescales are described. In the chapters 2.5.1 to 2.5.3 different qubits are explained and compared in chapter 2.5.5, which relates to condition 1. The implications of condition 4 are discussed in chapter 2.4, were basic qubit logic gates are discussed. Condition 2 is the scope of the further work of this thesis and will be discussed in more detail in the chapters 3 to 5.

2.2 Quantum Mechanics

The Dirac or bra-ket notation is commonly used to simplify the notation of quantum mechanical states. In quantum mechanics a physical state is represented as state vector in a complex vector space. The Dirac notation calls such a vector a ket and can be written as $|a\rangle$. The ket contains complete information about the physical state [4]. Similar to the ket space there exists a vector space called bra space which is dual to the ket space and represented by $\langle a|$. For every bra there exists a ket. The ket can be constructed by transposing and conjugating the bra and vice versa. This can be summarized as:

$$|V\rangle \doteq \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ \\ v_n \end{bmatrix} \leftrightarrow \begin{bmatrix} v_1^*, & v_2^*, & \dots & v_n^* \end{bmatrix} \doteq \langle V| \,. \tag{2.1}$$

To understand the discussion and requirements of different qubit implementations the bra-ket notation and some basics on quantum mechanics are needed. The main idea behind quantum mechanics is that matter has a particle and wave characteristic. In a quantum mechanical description a particle can no longer described by a a classical trajectory but rather by a wave:

$$\psi(r,t) = ce^{j(kr-\omega t)}. \tag{2.2}$$

The interpretation of this wave function 2.2 in conjunction with the particle behavior has to be done in terms of a probability, where $|\psi(r,t)|^2 = \psi^*\psi$ is the probability to find a particle at r at the time t [5]. The propagation of a particle has to be described by a superposition of plane waves. To determine the dynamic of a quantum state $|\psi\rangle$ at a given time t the Schroedinger equation 2.3 has to be solved:

$$j\hbar\frac{d}{dt}|\psi(t)\rangle = H|\psi(t)\rangle, \tag{2.3}$$

with j being the imaginary unit, and H the hamilton operator:

$$H = \frac{p^2}{2m} + V(r), \tag{2.4}$$

with m being the mass of the particle, the impulse operator $p = -i\hbar\nabla$ and a potential $V(r)$ [6]. In classical mechanics a particle is associated with well defined values for its location and momentum. However, in contrast in quantum theory only a probability for a given state can be given for the possible outcomes of a measurement. This probabilities

have to obey the Heisenberg uncertainty relation:

$$\sigma_x \sigma_p \geqslant \frac{\hbar}{2}, \tag{2.5}$$

where σ_x and σ_p are the standard deviations of position and momentum from the expected value. Equation 2.5 shows that a well defined location x relates to a highly unknown momentum p, which means none of these variables can be simultaneously determined as sharp values [5][7].

The Schroedinger equation 2.3 is a linear differential equation, which means that a linear combination of solutions is a general solution of the problem. Because the amplitudes $\psi(r)$ are complex this solutions are superimposed which gives rise to interference effects [5]. This is called entanglement and is one of the key prerequisites for quantum computing. In a group of entangled particles the state of one particle cannot be described independent of the state of other particles. The loss of the quantum mechanical properties is called decoherence and can be interpreted as loss of information due to interaction with the environment [5].

2.3 What is a qubit?

A quantum computer is not a new generation of universal super computer. It is a new kind of computer [8]. Computations are carried out by the transformation of quantum mechanical states. The basic cell of a quantum computer is a qubit. A qubit is an abstract information-theoretic concept independent of the actual physical implementation of any kind of qubit [5].

The classical computer has two distinct states 0 and 1. At each given time the bit is either 1 or 0 never both. In contrast a qubit will be in a superposition of both states at any time. This is visualized in figure 2.1 where the state of a classical bit can only be one of 2 colors on the other hand the state of a qubit can be any combination of these two colors. Due to the quantum mechanical nature of a qubit the description of its state must be described by a wave function :

$$|\psi\rangle = c_0 |0\rangle + c_1 |1\rangle, \tag{2.6}$$

where $|0\rangle$ and $|1\rangle$ are two orthogonal states. c_0 and c_1 are complex coefficients which fulfill the normalization condition:

$$|c_0|^2 + |c_1|^2 = 1. \tag{2.7}$$

Because of this normalization condition $|c_0|^2$ can be interpreted as the probability of the qubit to be in state $|0\rangle$ and $|c_1|^2$ as the probability to be in state $|1\rangle$ [5]. The state of a

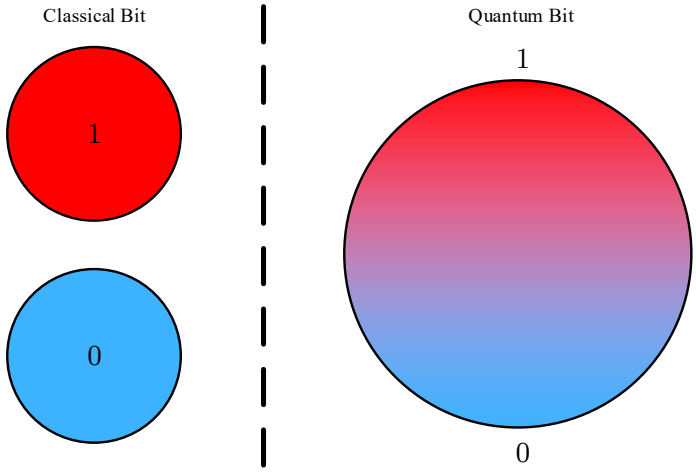


Figure 2.1: Comparison between a classical bit and a qubit.

qubit can be represented on the surface of a sphere. This so called Bloch sphere is shown in Figure 2.2, where $|0\rangle$ and $|1\rangle$ are the orthogonal base of the sub space.

Due to the normalization the wave function $|\psi\rangle$ of a qubit can be written as:

$$|\psi\rangle = \cos\left(\frac{\Theta}{2}\right)|0\rangle + e^{j\Phi}\sin\left(\frac{\Theta}{2}\right)|1\rangle. \tag{2.8}$$

Qubits are much more prone to errors then classical bits because the qubit is not only susceptible to bit flip (classical 0 to 1 flip or vice versa) but also to phase errors. In general, these errors are distinguished between either energy relaxation causing bit flip errors or decoherence causing the loss of the phase information. Those errors are usually related to a timescale on which they occur. The following sources of errors commonly used [9]:

Energy Relaxation
The qubit exchanges energy with the environment. This can be caused by e.g. phonon interaction. This process occurs on a timescale called T_1.

Decoherence
Is the loss of phase information of an qubit. This happens on a timescale T_2.

Inhomogeneous broadening
Is phase noise caused by inhomogenities in the environment of an ensemble of

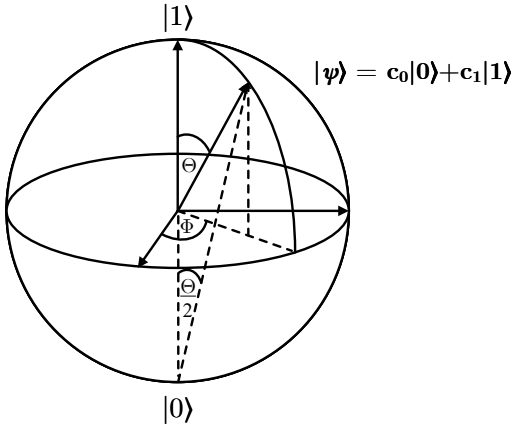


Figure 2.2: Bloch sphere representation of a 2 state quantum system.

qubits on a timescale T_2^*.

For the quality of a qubit fidelity is often referred to as the figure of merit. The fidelity is a way of measuring the distance between statistical states of a qubit. This can be used to define a metric. If the fidelity is used as a distance measure between two pure states it is called the transition probability. The fidelity of two states described by the unit vectors Φ and Ψ is $|\langle\Phi,\Psi\rangle|^2$. For two density matrices p, σ this can be generalized as the largest fidelity between any purification of given states. According to Uhlmann's theorem [10] this can be written as:

$$F(p,\sigma) = \left(tr\sqrt{\sqrt{p}\sigma\sqrt{p}}\right)^2, \tag{2.9}$$

where p, σ are pure quantum states and tr is the trace of the matrix. A different way for expressing the fidelity is derived from $|\langle\Phi,\Psi\rangle|$ and leads to:

$$F'(p,\sigma) = \left(tr\sqrt{\sqrt{p}\sigma\sqrt{p}}\right). \tag{2.10}$$

This is the so called square root fidelity.

The fidelity can be used to define a metric on a set of quantum states:

$$\begin{aligned} D_B(p,\sigma) &= \sqrt{2-2\sqrt{F(p,\sigma)}} \\ D_A(p,\sigma) &= \arccos\sqrt{F(p,\sigma)}. \end{aligned} \tag{2.11}$$

With D_B being the so called Bures distance and D_A the angle. D_B is the minimal distance between the purification of p and σ in a common environment [11].

2.4 Quantum Gates

Quantum gates are the quantum mechanical equivalent of the digital logic gate. One necessary condition for quantum computing is the implementation of quantum gates with high fidelity. A quantum gate is a standard operation on one or more qubit states. The most basic quantum gate is the "NOT-gate". Like a classical "NOT-gate" the operation is to invert the state of a qubit:

$$\begin{aligned} U_{NOT}\left|0\right\rangle &= \left|1\right\rangle \\ U_{NOT}\left|1\right\rangle &= \left|0\right\rangle \end{aligned} \tag{2.12}$$

If we expand this to a quantum state this means that the superposition of the states has be inverted as well [5]:

$$U_{NOT}(\alpha\left|0\right\rangle + \beta\left|1\right\rangle) = \alpha\left|1\right\rangle + \beta\left|0\right\rangle. \tag{2.13}$$

This operation can also be written as matrix:

$$U_{NOT}\begin{pmatrix}\alpha\\ \beta\end{pmatrix} = \begin{pmatrix}0 & 1\\ 1 & 0\end{pmatrix}\begin{pmatrix}\alpha\\ \beta\end{pmatrix} = \begin{pmatrix}\beta\\ \alpha\end{pmatrix}. \tag{2.14}$$

Another essential gate, which has no classical equivalent, is the "phase gate". The fundamental difference between this gate and classical gates is that it operates on the phase of a qubit [5]:

$$\begin{aligned} U_Z\left|0\right\rangle &= \left|0\right\rangle \\ U_Z\left|1\right\rangle &= -\left|1\right\rangle. \end{aligned} \tag{2.15}$$

$$U_Z = \begin{pmatrix}1 & 0\\ 0 & -1\end{pmatrix} \tag{2.16}$$

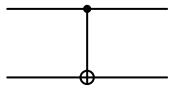


Figure 2.3: CNOT-Schematic.

Unlike classical operations also fractional values of operations are allowed. With this in mind one can construct a very important gate the "hadamard gate". It is capable of mapping an classical state into an equal superposition state [5]:

$$\begin{aligned} U_H |0\rangle &= \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle), \\ U_H |1\rangle &= \frac{1}{\sqrt{2}}(|0\rangle - |1\rangle). \end{aligned} \tag{2.17}$$

For a complete logic set of quantum computing only one additional gate is needed. The so called "controlled not gate" (CNOT). The CNOT gate is a two qubit gate, where the state of the first qubit controls if a not is performed on the second qubit:

$$\begin{aligned} U_{CNOT} |00\rangle &= |00\rangle \\ U_{CNOT} |01\rangle &= |01\rangle \\ U_{CNOT} |10\rangle &= |11\rangle \\ U_{CNOT} |11\rangle &= |10\rangle \end{aligned} \tag{2.18}$$

Figure 2.3 shows the notation for a logic CNOT gate. The controlled qubit is at the bottom and the control qubit on the top. The functionality of the CNOT can be seen as the logical XOR function and it is well known that AND gates cannot be created by any application of XOR's [5]. For the operation of elementary quantum algorithm operation AND gates are certainly needed for example even a simple addition needs the AND gate. In addition since all gates are unitary operation they have to revertable. Therefore it is impossible that any two qubit gate can represent the AND functionality. This problem can be circumvented by using a three qubit logic gate. For this a third fundamental qubit gate is introduced, the "Toffoli gate", which is shown in figure 2.4. It can be seen as a CNOT with two control qubits only when both qubits are 1 the controlled qubit will be inverted. The AND operation can now be implemented by setting the target qubit to $|0\rangle$ and supplying the two inputs of the addition to the control qubits [5].

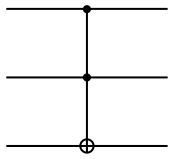


Figure 2.4: Toffoli Gate Schematic.

2.5 Qubit Implementations

There are several different types of qubit implementations, which can be further subdivided into sub categories. The fundamental principle of those will be explained in the following chapter.

2.5.1 Superconducting Qubits

The fundamental building block of superconducting qubits are Josephson junctions. A Josephson junction is formed by separating two superconducting electrodes with an insulator so that electrons can tunnel from one electrode to the other. The two Josephson relations are described by :

$$I = I_0 sin\delta \tag{2.19}$$

$$V = \frac{\Phi_0}{2\pi}\frac{d\delta}{dt}, \tag{2.20}$$

here is $\Phi_0 = \frac{h}{2e}$ the superconducting flux quantum, I_0 is the critical current of the junction, δ is the phase difference and V is the voltage across the junction [12]. Rewriting the Josephsons relations leads to :

$$\frac{dI}{d\delta} = I_0 cos\delta, \tag{2.21}$$

$$\frac{d\delta}{dt} = \frac{2\pi}{\Phi_0}V. \tag{2.22}$$

With those equations the time derivative of the current can be calculated:

$$\frac{dI}{dt} = \frac{dI}{d\delta}\frac{d\delta}{dt} = I_0 cos\delta\frac{2\pi}{\Phi_0}V. \tag{2.23}$$

Rearranging equation 2.23 leads to the current voltage relation of a indcutor:

$$V = \frac{\Phi_0}{2\pi I_0 cos\delta}\frac{dI}{dt}. \tag{2.24}$$

One can derive a Josephson inductance L_J which is:

$$L_J = \frac{\Phi_0}{2\pi I_0 cos\delta}. \tag{2.25}$$

From the denominator of this equation we can see the nonlinear behavior. A Josephson qubit can be viewed as a nonlinear resonator between the Josephson junction and a junction capacitor [12].

2.5.2 Trapped Ions

Ions are just atoms with additional electrons, therefore acquiring an electrical charge. Ions are created and then trapped in a ion trap by an electrical field. A simplified composition of an ion trap is shown in figure 2.5. A charged particle e.g. an Ion is trapped between electrodes. The potential on the opposite electrodes is shifted by 180 degree. It is not possible to contain a charged particle with a static field only. Therefore the trap operate by oscillating the potential on the electrodes with a frequency which is faster then the time fore the ion needed to escape from the trap.

The average potential over one oscillation period of the ion is zero [13]. Each ion is a qubit, with its two dimensional space spanned by two of the ions energy eigenstates [14]. The motion of the ion has to be reduced below a certain kinetic energy with:

$$k_B T << \hbar\omega. \tag{2.26}$$

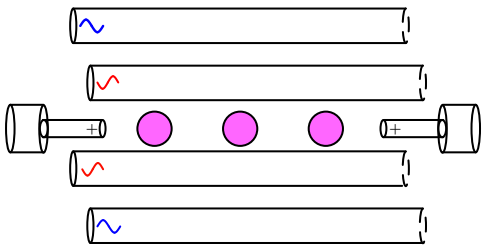


Figure 2.5: Simplified structure of an ion trap.

This can be achieved by cooling the ion with a laser. To process information in the ions it is needed to change any individual qubit [13].

2.5.3 Quantum Dots

Because electrons are intrinsically a two-level system they are an obvious choice for implementing qubits. The idea is to use the electron properties as quantum bits. One possible implementation employs an array of quantum dots and traps a single electron in it. Although quantum dots are similar in geometry and terms of fabrication they differ in the physical feature which is used to encode the information which is either the charge state or the spin of an electron. The spin category is further divided into multi and single electron spins. Each of the different spin implementations requires a different kind of control depending on the single qubit type. There are several ways to trap a single electron. For example a small bandgap semiconductor can be enclosed from all sides by a larger bandgap semiconductor to form a potential barriers[5]. One commonly used structure uses GaAs and AlGaAs with high doping on the interface leading to the formation of a two dimensional electron gas (2DEG). A single electron is confined in a dot within a diameter of a few tens of nm by a combination of an electrical field and band gap differences between different semiconductor borders. On the top of the stack metal contacts are placed and a control voltage is applied. The control voltages of the qubit is typically tuned so that a single electron is confined inside a single dot. Between neighboring dots an additional contact can be placed to control the tunneling between those dots and control the exchange. This type of qubits have the advantage of complete electronic control [5]. Another advantage of quantum dot architectures is the similarity to standard semiconductor processes and the advantages in process technology driven by a multi billion dollar industry.

Table 2.1: Summary of the differences between quantum dot implementations adopted from [15].

<table>
<tr><th colspan="2">Memory</th><th>Single-qubit control</th><th>Multiqubit control</th></tr>
<tr><td colspan="2">Charge</td><td>Direct</td><td rowspan="3">Capacitive</td></tr>
<tr><td rowspan="4">Spin</td><td rowspan="2">Multi</td><td>Exchange</td></tr>
<tr><td>Singlet-triple oscillations</td></tr>
<tr><td rowspan="2">Single</td><td>ESR with AC magnetic field</td><td rowspan="2">Magnetic dipole-dipole coupling</td></tr>
<tr><td>ESR with AC electric field</td></tr>
</table>

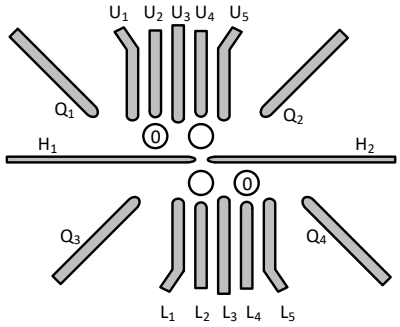


Figure 2.6: Layout of a charge qubit [16].

2.5.3.1 Charge Qubit

The qubit is formed by using the charge state of a double quantum dot. The qubit is defined by the electron occupation of the left or right dot. The base state where one electron is in the left dot and zero electrons in the right dot for the $\langle 0|$ state and the opposite occupation for the $\langle 1|$ state. Charge qubits have the benefit of speed which is determined by the inter-dot tunneling rate which can be extremely high [16]. Full electrical operation via electrodes with out external magnetic field is possible. On the other hand, they are more sensitive to electrical field fluctuations and have a limited coherence time which is usually below 1 ns [17]. The operation of two semiconductor charge qubit gates with comparable fidelity to that of spin-based semiconductor qubits has been shown by [16].

Figure 2.6 shows the two qubit system from [16]. The electrodes U1–U5 and H1 and H2 form the upper quantum dot, and L1-5 with H1 and H2 form the lower quantum dot. H1 and H2 also tune the coupling between the upper and lower quantum dot. Direct tunneling is suppressed by the negative bias voltages on H1 and H2. The four gates Q1–Q4 are used for read out and monitoring of the charge.

2.5.3.2 Spin qubits

In the simplest case the base states $|0\rangle$ and $|1\rangle$ can be encoded with the two opposite spin directions of an electron $|\uparrow\rangle$ and $|\downarrow\rangle$ since spin is mainly influenced by magnetic influence on the particle a spin qubit is less afflicted by charge noise compared to charge qubits and exhibits therefore longer coherence times. Single spin responds only to a magnetic fields rather than an electric field, therefore either electron spin resonance or electric dipole spin resonance is used to rotate the qubit around the x-axis of the bloch sphere.

A resonance mechanism that couples an electric field to spin is needed for an electric dipole spin. Examples for this are spin orbit coupling or the usage of micro magnets.

Singlet Triplet A singlet triplet qubit is based on the spin of two electrons in neighboring quantum dots. A triplet describes a quantum state where the overall spin quantum number s equals one of three different allowed values (1,0 and -1). If one does not consider the spin of one single electron, which is confined in one quantum dot but rather the spin configuration of two coupled electrons, which are confined in two quantum dots each particle can have one of two different spin states:$|1/2\ 1/2\rangle$ and $|1/2\ -1/2\rangle$, which leads to 4 different combined states.

$$\begin{aligned} |S\rangle &= \frac{1}{\sqrt{2}}|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle \\ |T_0\rangle &= \frac{1}{\sqrt{2}}|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle \\ |T_+\rangle &= |\uparrow\uparrow\rangle \\ |T_-\rangle &= |\downarrow\downarrow\rangle \end{aligned} \tag{2.27}$$

with the singlet state $|S\rangle$ and the triplet states $|T_0\rangle$, $|T_+\rangle$ and $|T_-\rangle$. The qubit is operated at the charge state transition from (2,0)-(1,1) where (n,m) denotes the number n of electrons in one or m electrons in the other quantum dot. Applying an external magnetic field splits the T_- and the T_+ apart and allows the formation of a two level system consisting of the singlet state S and the triplet state T_0. Figure 2.7 shows the energy diagram of two coupled electrons in a double quantum dot. The Hamiltonian can be written as:

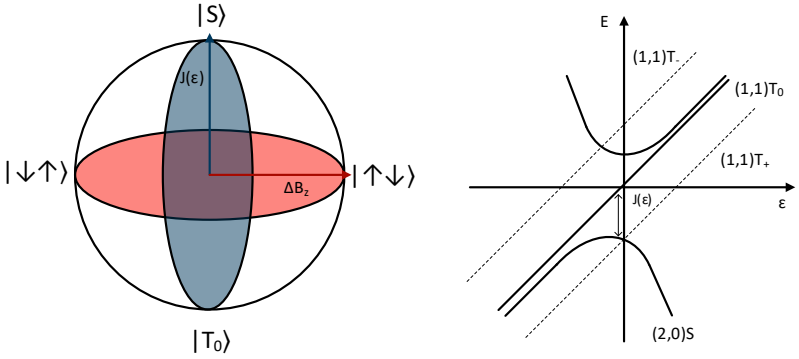
$$H = \frac{J(\epsilon)}{2}\sigma_z + \frac{\Delta B_z}{2}\sigma_x. \tag{2.28}$$

One can easily see two orthogonal control parameters of the qubit are the magnetic gradient ΔB_z and $J(e)$ the exchange splitting:

$$J(\epsilon) \approx J_0 exp(\epsilon/\epsilon_0). \tag{2.29}$$

The Bloch sphere representation in figure 2.7a shows the two orthogonal control axes for qubit manipulation, $J(\epsilon)$ and ΔB_z.

The GaAs Qubit The GaAs qubit is a singlet triplet semiconductor spin qubit based on the heterojunction formed within a GaAs stack. A usual implementation for a GaAs qubit is shown in figure 2.8. The confinement of the electrons in one direction is done by the formation of a heterostructure forming a 2 dimensional electron gas. The difference between the bandgap in GaAs and AlGaAs result in a discontinuity in the conduction



(a) (b)

Figure 2.7: Bloch sphere (a) and energy diagram (b) of a singlet triplet qubit adopted from [9].

band. In addition to that the other dimension is restricted by applying electrical potentials at electrodes on top of the stack.

The Si/SiGe Qubit Similar to GaAs a single electron is trapped in a quantum dot. The dot is formed by the Si/SiGe quantum well and the electrostatic potential of metallic contacts on top [18]. SiGe has a three times higher effective electron mass compared to GaAs which allows for smaller gate patterns and the 2DEG is closer to gates. The manipulation of individual spins is currently realized with either a local magnetic AC field, generated by a close by stripline or by spin orbit coupling via a co-integrated

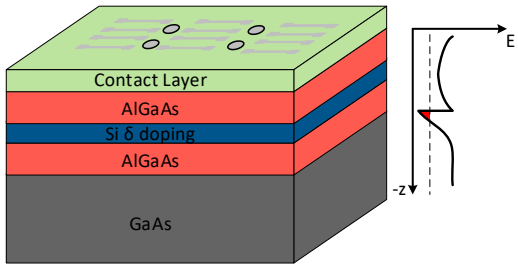


Figure 2.8: Conceptional layout of a GaAs singlet triplet qubit and simplified view on its energy diagram adopted from [9].

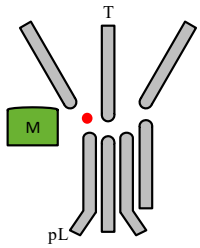


Figure 2.9: Conceptional layout of a SiGe qubit .

micromagnet [19]. The usage of Si and SiGe as the material for quantum dot qubit implementation has some advantages over GaAs. The magnetic noise is minimized and the lower hyperfine interaction in silicon. Nuclear spin free silicon allows for isotopic enrichment. An example structure from [19] is shown in figure 2.9. It employs a micro magnet and lines for the control of the qubit T and pL. This device was fabricated with an undoped Si/SiGe heterostructure which was grown on a Si-Wafer. On top depletion gates are fabricated by means of electron beam lithography. A micro magnet is placed in close vicinity to the gates in order to generate a local magnetic field for electric dipole spin resonance.

2.5.4 Quantum Annealing

Although quantum annealers are not a universal quantum computer they deserve a notion as an intermediate step, which show the power of quantum mechanics for computation and are used for powerful optimizations. Quantum annealing is a sub class of quantum processors, it is not a fully universal quantum computer but rather an application specific processor type for certain optimization problems. Quantum annealers are based on qubit implementations e.g. superconducting qubits. While being in a superposition state the probability the state is both 0 and 1 after a time the state of the qubit will either be 0 or 1. The probability into which state it evaluates can be manipulated. The real power of a quantum annealer comes with the entanglement of several qubits. When two qubits are entangled there are four different states. Each additional qubit doubles the number of possible states. During the annealing process the qubit states will evaluate to the most likely. The user of such a computer can formulate the coupling between the qubits and the probability between states [20].

Table 2.2: Comparison of key parameters of different qubit implementations.

Qubit Comparison			
Qubit Type	No. of Qubits	Fidelity	Footprint$[\frac{Qbit}{mm^2}]$
Superconducting	53	$> 99.9\%$	1.88[2]
Ion Trap	20	$> 99.9\%$	5.35612[22]
Spin	26	$\approx 99.9\%$	> 33[23]

2.5.5 Comparison

In addition to the knowledge of the basic principles of each qubit it is also important to understand the state of the development of each implementation as well as its benefits and drawbacks for future upscaling to millions of qubits. One of the most important feature for potential upscaling is the footprint of an individual qubit. In figure 2.10 the typical footprint of different qubit implementations is shown on a logarithmic scale. The superconducting transmon qubits are several decades larger in size compared to ion traps which are in turn several decades larger than the semiconductor based qubits. Among the semiconductor based qubits the finfet based have the smallest footprint.

Table 2.2 shows the maximum amount of qubits achieved in a technology, the best achieved fidelity for this type of qubit and a footprint estimation from different publications not necessarily from the record number itself. Although the superconducting qubits have achieved the highest number of qubits so far with a great fidelity the dimension of each individual qubit is far bigger then those of the spin qubit. Semiconductor spin qubits on the other side are not as far evolved in terms of number of qubits and fidelity but are excellent in size therefore offering the best perspective for future upscaling. Nevertheless the achievements and research in the fields of superconducting and ion traps should not be disregarded since they might be the first suitable vehicles for the application of real quantum algorithms.

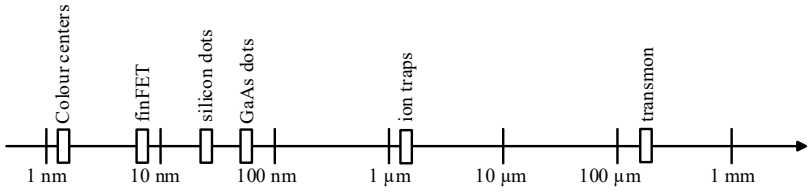


Figure 2.10: Footprints of different state of the art qubit implementations [21].

Chapter 3

Electronic Control of Qubits

In the following chapter the requirements for control signals used for quantum dots in general as well as GaAs and SiGe quantum dots qubits in particular are discussed. Not all requirements apply to each encoding and can be used as an assessment criterion to compare. Common to most qubit implementations are:

- DC Bias voltages that can be tuned and calibrated individually
- Gate voltages that can be individually tuned and calibrated
- Tuned microwave or static electric fields
- High precision of each control signal for high fidelity
- Initialization, operation and measurement finished within the coherence time of the quibt [24]

3.1 GaAs Control

The shortest path around the bloch sphere is not always the best solution for a given operation. Figure 3.1 shows a bloch sphere. The path is determined by 2 orthogonal rotation axis, one being the static magnetic field ΔB_z and the other one is the transient J. The pulse is used to get from the state Y to the state X. It is obvious that the path used is not the shortest but a non trivial path obtained by the optimizer.

The operation of GaAs qubits requires transient signals with timescales of different order of magnitudes. Slow voltage ramps and long idle times in the order of microseconds are needed to initiate and read out the qubit. Meanwhile operating the qubit requires fast pulses in the order of nanoseconds. A global optimizer acquires the pulse shapes used for the qubit operation. The optimizer assumes sources of noise and calculates the contribution on a pulse shape to find shapes insensitive to this noise. Figure 3.2 shows an example pulse shape resulting from the optimization. In the figure the signals ϵ, which is related to the voltage, and J, which is directly related to the change of the qubit state are

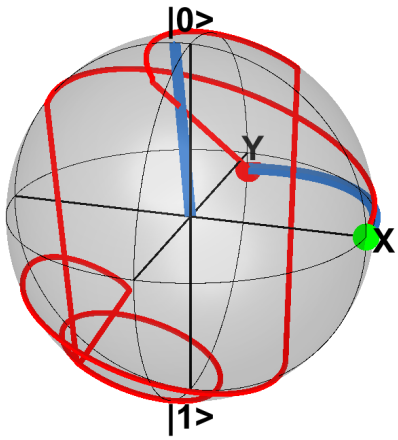


Figure 3.1: Corresponding Blochsphere representation of the pulse shape.

plotted over the time. ϵ_0 is a fitting parameter which is gained from experimental data. The width of one pulse segment is chosen to be 4 ns. The output of the DAC is shown in green and the waveform which is seen by the qubit is depicted in black. This waveform is generated by filtering the DAC output signal with a low pass filter representing the parasitic capacitance of the pads, wiring and the qubit chip. The resolution of the pulses directly impact the design of the DAC. The fidelity degradation due to quantization noise has to be evaluated. This is achieved by performing an pulse optimization for an ideal pulse to operate the qubit and apply different levels of quantization to this pulse. In Figure 3.3 the infidelity is plotted over the resolution of the applied quantization. Below a certain number of bits the fidelity is limited by the quantization. For higher number of

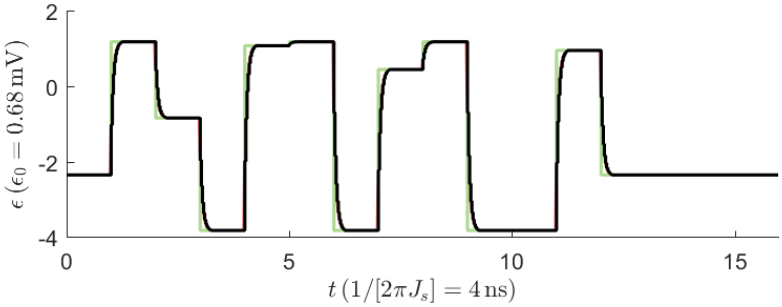


Figure 3.2: Example pulse shape for qubit gate operation.

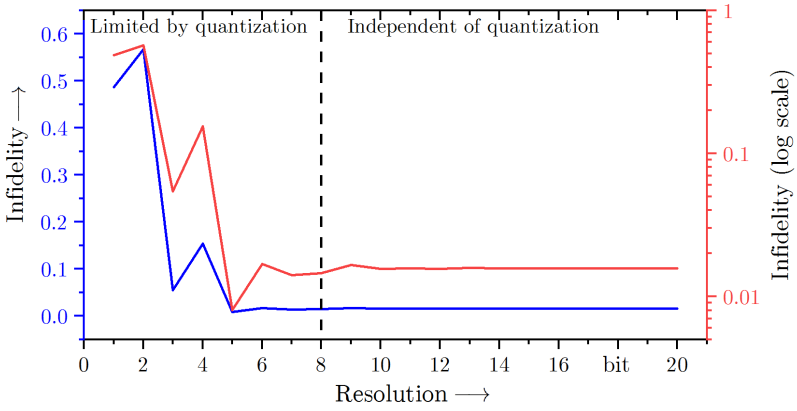
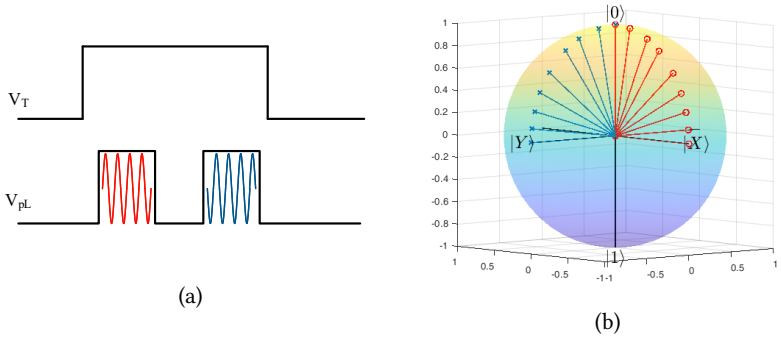


Figure 3.3: Influence of the quantization noise on the infidelity of the qubit.

bits the fidelity is limited by other sources of noise. In this way the optimum required number of bits is found to be 8 bit.

3.2 SiGe Control

The control of a SiGe qubit requires pulsed microwave signals. The carrier frequency of the microwave signal is around 20 GHz as shown in figure 3.4a. On the line V_{pL} a



(a) (b)

Figure 3.4: Example control pulses (a) from [19] and bloch sphere representation of two pulses with and without a phase shift (b).

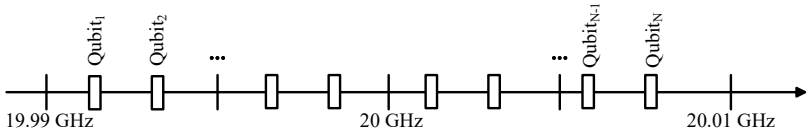


Figure 3.5: Example frequency plan for frequency multiplexed control of a qubit.

pulsed microwave signal is transmitted. The phase of the microwave package define the rotation axes around the bloch sphere. The area of the microwave pulse determines the length of the path moved around the sphere. The qubit itself has a very sharp resonance peak with a bandwidth <100 kHz which leads to the challenge of high quality frequency signals with very low shift but also offers the possibility to connect several qubits to the same line and address them via frequency multiplexing as shown in figure 3.5. Each qubit occupy a very small band at a certain frequency which can be influenced by the production process.

The control of a SiGe qubit can be done by a setup as depicted in figure 3.6. The envelope of the signal is controlled by a DAC which is mixed with a sample rate of approx. 500 MHz. The envelope signal is mixed with the carrier of the control signal. The exact frequencies of the signal are chosen to match the resonant frequency of the qubit. This signal is amplified by an amplifier to reach the required output amplitude. The phase of this signal can be changed between 0 and π with digital control. The mixer employed is a single-sideband mixers to avoid unnecassry mixing products which could excite other qubits. The output is used within regulation loop which controls and stores the frequency settings for each qubit and control the low frequency DAC and the 500 MHz source in order to stay at the resonant frequency.

The electrical key requirements for the frequency generation are shown in table 3.1. The carrier frequency is 20 GHz additional a offset frequency of $\pm$ 10 MHz is needed for the selection of the individual qubit. The phase has to be able to be shifted between at least two different values 0 and pi.

Table 3.1: Electrical requirements for the microwave control of a SiGe qubits.

Specification	Value
Carrier Frequency	20 GHz
Offset Frequency	10 MHz
Phase	0 & π
Amplitude	5 mV
Time Resolution	1..5 ns

3.3 Partitioning

3.3.1 State of the Art

Most of todays qubit experiments have qubit chips mounted on a interposer which is connected to a PCB and located on the lowest temperature stage of a cryostat around 20 mK. A simplified state of the setup is shown in figure 3.7. The only parts located at the lowest temperature in such a setup are the qubits itself and passive devices such as resonators and bias-Ts. The electrical connection between each stage can be done with attenuators. The attenuators suppress the thermal noise from the higher temperature stage and thermally anchor the lines to the temperature of the stage. Such a typically setup can supply up to almost 100 DC lines and several AC lines.

The setup is limited through the number of interconnects to room temperature. Assuming about 10 DC and 2 RF connections per qubit this approach will fail to address more than 10 qubits without any multiplexing strategies.

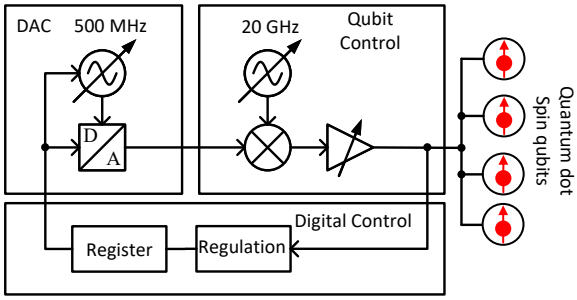


Figure 3.6: Example control system for SiGe microwave controlled spin qubits.

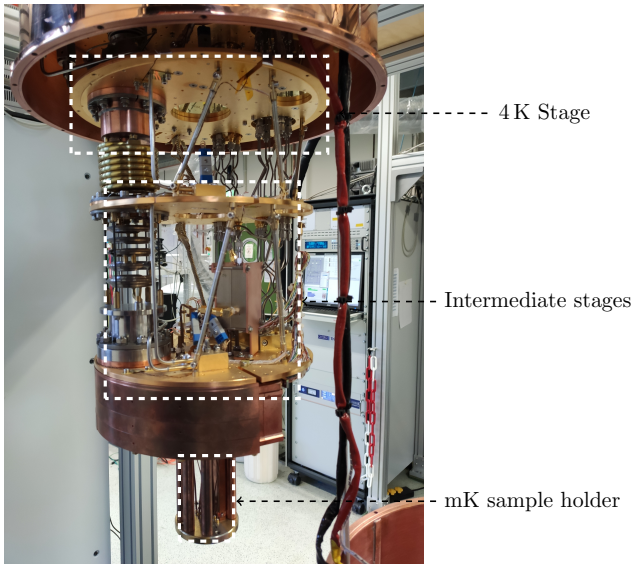


Figure 3.7: Simplified partitioning in a state of the art qubit cryostat setup.

3.3.2 Vision

Our aim is to move the integrated control electronics of a quantum computer solution as close to the qubit as possible. In an intermediate development step the corresponding System-on-Chip (SoC) can be located on a common interposer with the chip containing the qubit and connected via wire bonds to the qubit itself. Figure 3.8 depicts the lowest temperature stage of such an approach. The common interposer is placed in a cryogenic PCB and placed on the mK-stage. Only digital interface signals and supply lines are fed to the chip. In this approach the read out can be still done in the traditional way e.g. RF reflectometry [25]. With this approach the needed number of control signal does not directly decrease, but more importantly it is independent of the number of qubits and only limited by the number and the size of the bondpads on the SoC and the qubit chip.

Superconducting Trough-Silicon-Vias (TSVs) for the connection between control and read out electronic and silicon based spin qubits are used in [26]. The authors have demonstrated superconducting TSVs that connect from one side of an interposer to another and the operation of qubits while using such TSVs with a mean qubit coherence time of around 10 µs. It was shown that even with currents as high as 5 mA no heat was transferred to the dilution refrigerator which means that the superconducting behavior of the TSVs remained. If one takes this approach one step further it seems possible to

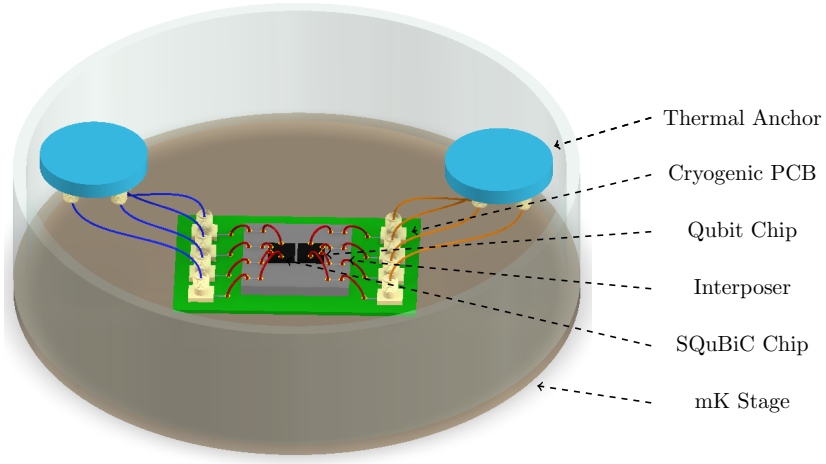


Figure 3.8: Conceptional drawing of an SoC on the same interposer with a qubit chip.

use 3D packaging techniques like TSVs to design and place a control chip in a way that the footprint of the qubit chip and control chip fit very well and can be connected by superconducting TSVs as shown in figure 3.9 which directly leads to increased qubit and electronics density.

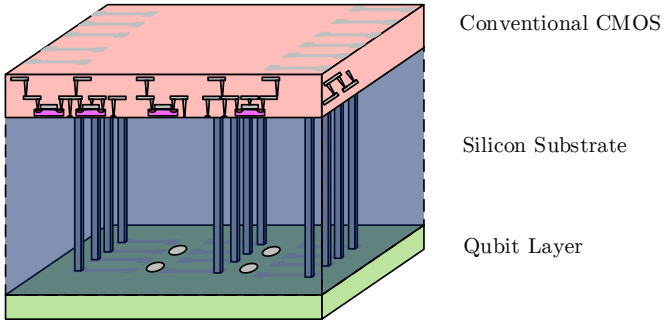


Figure 3.9: Conceptional drawing of an SoC connected with superconducting TSVs to a qubit.

3.4 Power Consumption

The cooling power of a dilution refrigerator on lowest temperature stage is today limited to a range of 1 mW [27]. A limited cooling power in turn leads to a limit on the power that can be used within the cryogenic electronics on the same temperature stage. Crossing this limit will heat up the stage and lead to a dephasing of the qubit. The available cooling power on a higher temperature stage is order of magnitudes higher [27]. With this setup up to 2 W are allowed at the second stage at 4 K.

No quantum computer can be operated by solely generating the required signals at room temperature due the massive problems with interconnects neither can all voltages be generated at cryogenic temperature due to the severe limits on the power consumption. It is a common view that in order to achieve successful quantum computing a combination of two things are needed: multiplexing strategies for the qubit signals and a first layer of electronics that is adequate for the qubit footprint size [24]. The very first layer of electronics has to be close to the qubit because at least some of the signals have to be independently calibrated and have to be supplied to every qubit [24]. Other layers of classical electronics may reside farther away from the qubit plane and at higher temperature. The data rates between the higher layers can be orders of magnitudes smaller compared to the inter qubit communication and the first control layer [24].

3.5 Interface

Any chip with some level of complexity needs a standardized digital interface to control the chip and read out data in order to communicate with the outside world. Especially at cryogenic temperatures a reliable communication with the chip is necessary to ensure that any unwanted effects are caused by the cryogenic effects in the circuits and not a faulty communication caused by the interface.

There are three dominant serial interface standards the Inter IC bus (I^2C), the Serial Peripheral Interface (SPI) and the Joint Test Action Group (JTAG). They differ in the number of wires needed to operate them as well as the complexity and features offered, which are summarized in table 3.2.

Table 3.2: Key parameters of different serial interfaces.

Interface	Wires	Acknowledgment	Data rate	Verfied @ CT
I^2C	2	yes	100 kbit/s	Yes
SPI	3	no	>4 MB/s	No
JTAG	4+1	yes	4 MB/s	No

The SPI interface needs 3 data lines: a clock signal, a data line from the master to the slave and a data line from the slave to the master. The interface definition does not define any maximum data rate and does not have an acknowledgment mechanism to confirm the data reception.

The JTAG interface consists of four data lines a test input, test output, test clock and a test mode select. It is a complex interface used for verification of digital systems after fabrication by means of accessing them via a debug port.

The Inter-IC bus or simply I^2C-bus is a simple bidirectional 2-wire interface which was developed by Philips Semiconductors. Only two bus lines are required for the operation: a serial data line (SDA) and a serial clock line (SCL). Both lines are bidirectional lines, connected to the positive supply with a pull-up resistor. When the bus is not driven the lines are pulled towards the high level [28].

3.6 Integrated Cryogenic CMOS

The usage of CMOS for cryogenic application has a lot of potential benefits and drawbacks, which have to be considered when designing circuits. The challenges are increased electron mobility, increased sub-threshold slope, increased threshold voltage, carrier freeze out and the so called kink-effect. At very low temperature the dopants in the substrate are fully frozen out. When a voltage is applied to a p-type substrate the majority carriers are emitted by the frozen dopants due to field effect [29]. A structure with a thin film of free carriers beneath the gate oxide is formed and allows the operation of a MOSFET device.

In semiconductors the electron mobility is determined by two kinds of scattering mechanism. The first is lattice scattering, where lattice vibrations cause the mobility to decrease with increasing temperature which is approximately proportional to $T^{-3/2}$. The second mechanism is scattering at charged impurities, this scattering is caused by crystal defects like dopants. This effect is proportional to $T^{3/2}$ therefore counter acting the temperature dependency of the lattice scattering. The authors of [30] have shown an overall increased mobility for temperatures as low as 8 K.

The region underneath the channel and the substrate in general is still frozen out. This leads to an drastically increased resistance into the substrate. For older technologies this region is believed to create the Kink effect. The substrate itself is basically on a floating potential, even though it is connected to a substrate contact. The substrate current cannot reach the substrate contact and therefore flows through the substrate into the source while increasing the substrate potential and thus reducing the threshold voltage. This current increases with the drain voltage which will increase the potential

within the depletion region and therefore decreases the threshold voltage once a certain drain voltage has been passed [29].

This kink effect is especially observed in mature process nodes with a geometries larger than 100nm due to less dopants in the channel and higher applied voltages. The benefit of freeze-out is dramatically reduced leakage current into the substrate.

The inverse subthreshold slope states how much gate voltage is needed in order to increase the current by one order of magnitude [5]:

$$S = (\frac{\partial log(I_d)}{\partial V_{GS}})^{-1} \leqslant \frac{k_B T}{\epsilon} ln(10). \tag{3.1}$$

The lower bound of the inverse sub-threshold S can be estimated by equation 3.1, which evaluates to $60\frac{\mathrm{mV}}{dec}$ at room temperature and roughly $200\frac{\mu\mathrm{V}}{dec}$ at 1 K.

For a Hitachi Hi-CMOSII 2µm process an increased threshold voltage has been reported down to a temperature of 4.2 K [31] and for a not clear specified "standard" CMOS technology down to a temperature of −180 °C [32].

One of the challenges when designing circuits for very low temperature is the absence of valid models. The operating temperature range for most circuits is specified up to temperatures as low as −55 °C which is known as military range. To investigate the effect of such low temperatures a chip containing single devices in a commercial 65 nm technology was measured at room temperature and at cryogenic temperature of approx. 6 K. The drain voltage of the transistor was swept from 0 V to 1.2 V and back to 0 V while the gate voltage was fixed to a potential. Figure 3.10 shows the output characteristics of a NMOS transistor for a gate voltage of 1.2 V and 0.6 V respectively. In addition to that simulation results for the same device at room temperature in different process corners are shown. The process corners represent the most extreme variation for a given process in which the circuit still has to be functional. The corners are named with a two letter representation which denote the electron mobility of the NMOS and PMOS transistor, which can be either slow, typical or fast

For both operating points the drain current of the transistors is close to the nominal value of the simulation. Normal transistor behavior can be observed. No kink effects or hysteresis is observable. For comparison the corner value of the technology show a behavior which is way different than the cryogenic effect. Which led to the assumption that a nominal design which fulfills specification in all corners should have sufficient margin to operate at cryogenic temperatures.

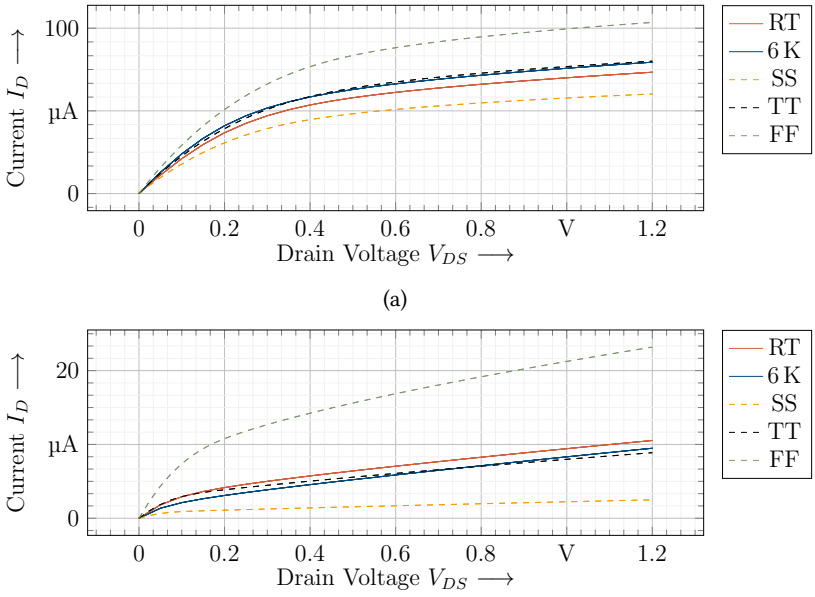


Figure 3.10: Output characteristic of a NMOS transistor at cryogenic and room temperature with a gate voltage of 1.2 V (a) and 0.6 V (b) .

Cryogenic CMOS is not a new topic with the earliest IEEE publications dated back to the early 1980's but rather an exciting growing field. The early publications were focused on single device characteristic at rather high and easy to reach temperatures like liquid nitrogen environments at 77 K. They try to benefit from the reduced thermal noise for the implementation of low noise amplifiers at reduced temperature. The field itself experienced very limited interest until the recent progress in quantum computing led to an increasing interest in cryogenic CMOS for scalable solutions for quantum computing control. Figure 3.11 shows the number of published articles in IEEE on the topic of cryogenic CMOS for each year. The number of publication per year remained well below 10 publications a year until the very first quantum computation applications reached the field in 2007. Although the publications with the main focus on the quantum computing remained low in comparison to the overall field until very recent the number of publications itself and the interest in the topic increased. From 2016 onward the number of IEEE publication increased drastically with a huge amount of publications focused on circuits specifically designed for qubit operation or read out (amplifiers, mixers, multiplexers) or more complex architectures like DAC's and System-on-Chip (SoC) solutions for qubit operation.

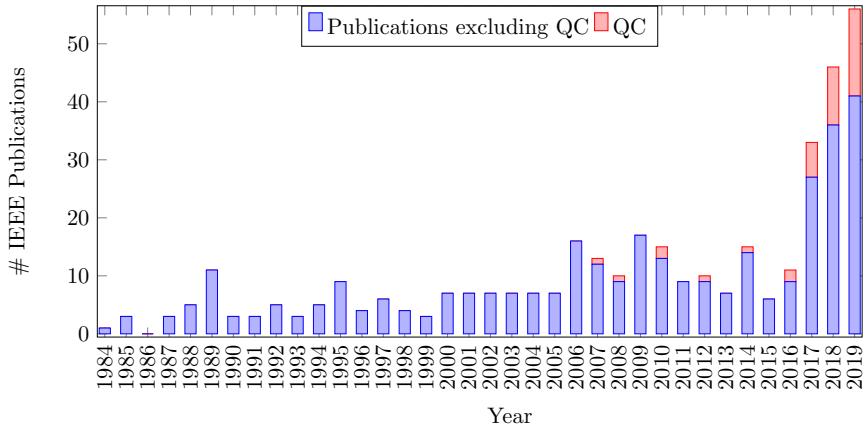


Figure 3.11: Number of cryogenic CMOS publication in IEEE.

Table 3.3 shows a selection of different recent publications on cryogenic CMOS and there application field as well as their respective operating temperature. Most cryogenic CMOS circuits which are used for sensor and detector applications are operated at 77 K due to the easy accessibility of this temperature with liquid nitrogen. A large portion of the publication focus on circuits for quantum computing which have to be operated at a temperature of 4.2 K and below. Another observation is that the need for scaleability encourages the circuits designed for quantum computing to use smaller process nodes. In addition more and more chips try to counteract the negative cryogenic effects by employing a silicon on insulator technology and adjusting the back gate voltage.

Table 3.3: Extract from recent publications on cryogenic CMOS.

Type	Technology	Temperature	Application	Source
LNA	65 nm	77 K	Square Kilometre Array	[33]
LNA	180 nm	77 K	X-band	[34]
Pre Amplifier	unknown	77 K	gamma spectroscopy	[35]
LNA	28 nm SOI	20 K	W-band	[36]
Circulator	40 nm	4.2 K	Quantum computing	[37]
VCO	180 nm	77 K	Quantum computing	[38]
VCO	40 nm	4.2 K	Quantum computing	[39]
Characterization	28 nm SOI	77 K	Modeling	[40]
Digital model	28 nm SOI	4.2 K	Quantum computing	[41]
Characterization	32 nm SOI	6 K	Modeling	[42]
Characterization	28 nm SOI	4.2 K	Quantum computing	[43]
Characterization	40 nm	4.2 K	Quantum computing	[44]
Voltage Reference	40 nm	4.2 K	Quantum computing	[45]
Voltage Reference	40 nm	4.2 K	Quantum computing	[46]
DAC	500 nm	4.2 K	-	[47]
ADC	700 nm	4.2 K	Quantum computing	[48]
DAC	500 nm	4.2 K	-	[49]

Chapter 4

Scalable Quantum Bit Control

A chip was designed in a commercial 65 nm CMOS process. It employs all the parts needed to operate a semiconductor spin qubit with the requirements stated in the previous chapter. The chip is called Scaleable Quantum Bit Control (SQuBiC). In addition to the circuitry needed for operation of a qubit there is additional circuitry to investigate the cryogenic effects on circuits and devices.

Interface
An I^2C interface was selected for the SQuBiC chip to control the chip and read out data.

Digital Clock
SQuBiC contains memory, custom made logic and standard cell based logic which need a clock signal. The clock signal of the chip can be supplied in two different ways. A clock buffer that can support frequencies up to 500 MHz was employed. As a second, more independent solution a digital controlled oscillator (DCO) is designed. The oscillator operates also at a frequency around 500 MHz.

Pulse DAC
For the generation of the control signals of a GaAs qubit a high speed DAC is needed. An 8 bit current DAC was designed. Two of these DACs were placed on the chip for qubit control. Additionally, a third DAC was employed on the chip for pure measurements.

Bias DAC
For the Bias voltage generation of the qubits a bias DAC is employed. It is not part of this thesis and details can be found in [50].

Voltage Controlled Oscillator
A voltage controlled oscillator (VCO) is implemented with a nominal frequency of around 20 GHz. The VCO can be used in the future for generating microwave signals for the operation of e.g. SiGe qubits.

Single Device Test Structures
Several single devices are included for measurements to characterize their behavior at cryogenic temperature ranges.

4.1 Clock Buffer

The input clock signal is amplified by the clock buffer to reach a full scale voltage. It is fed through several digital clock buffer cells and finally amplified by the same power amplifier structure that in turn is used for the voltage controlled oscillator (VCO) as well. The clock buffer is located within the same voltage domain as the Digital controlled oscillator (DCO). The top level schematic of the domain can be seen in figure 4.1. The DCO and the clock buffer share the same output circuitry to multiplex the output signal to the different parts of the chip and an optional frequency divider for clock rate reduction.

The first stage of the buffer is built with thick gate IO transistors which are more resilient to ESD. Applying a full scale 0 V to 1.2 V signal to the pad is not beneficial for many reason. The power consumption increases quadratic with the voltage. Additionally, most high quality signal generators generate a 0 V DC output signal which would force the usage of an additional bias T to operate the clock buffer. Therefore this stage is supplied with a supply voltage of 1.2 V. The clock buffer design is shown in figure 4.2.

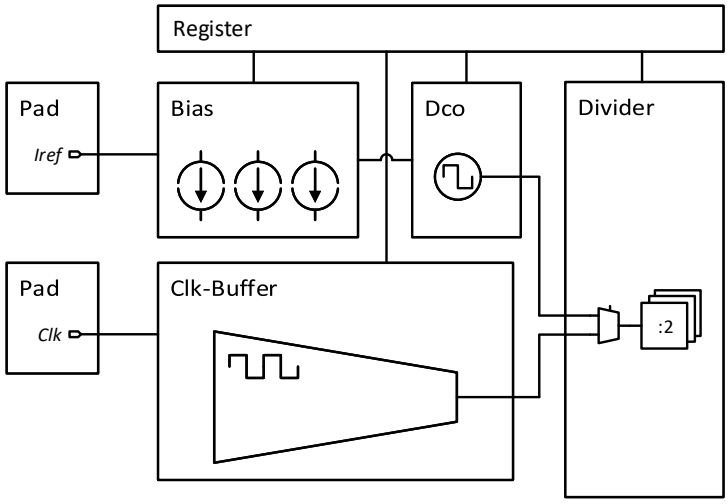


Figure 4.1: Simplified DCO domain top level schematic.

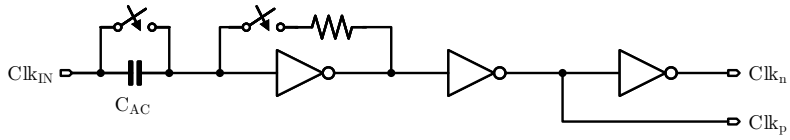


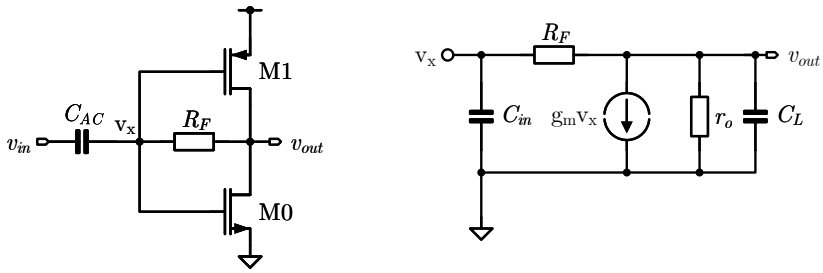
Figure 4.2: Schematic of the implemented clock buffer.

The clock signal CLK_{IN} is AC-coupled through the capacitance C_{AC} into an inverter with a resistive feedback which sets its DC operating point. The advantage of this structure is that it is independent of the DC operating point of the input signal and even small voltages can be easily amplified before the clock signal is distributed to the other parts of the chip. The feedback path can be disabled. The AC-coupling can be bypassed to set the input DC operating point independently of the input to different modes during the verification of the chip. The output of this buffer circuit is buffered with regular digital clock inverters from the standard cell library.

The core of the clock buffer is shown in figure 4.3a. For the purpose of a small signal analysis the transistors M0 and M1 can be combined into one transconductance $g_m \times C_{in}$ is the input capacitance of the transistors, r_o is the resistance formed by the parallel connection of the NMOS and PMOS transistor, C_L presents the capacitive input of the next stage and R_F is the feedback resistor.

The capacity C_{AC} is used to block the DC part of the clock signal. The resistor forms a DC voltage feedback and sets the operation point of the inverter, which will reduce duty cycle distortion.

From the derived equivalent circuit model shown in figure 4.3b the transfer function of



(a) (b)

Figure 4.3: Schematic of the clock buffer (a) and the small signal equivalent circuit (b).

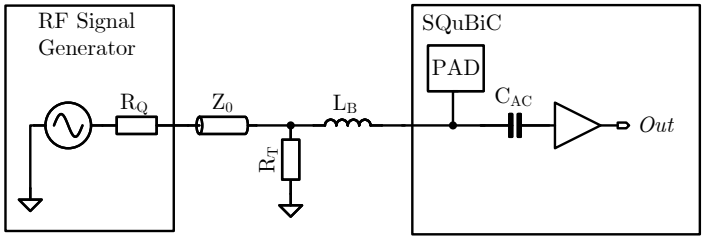


Figure 4.4: Schematic of the clock buffer testbench.

the amplifier can be calculated as:

$$\frac{v_x}{v_{out}} = \frac{1 - g_m R_F}{1 + \frac{R_F}{r_o} + j\omega R_F C_L}. \tag{4.1}$$

The amplifier was simulated using the testbench shown in figure 4.4. On the chip side the pad is included as well as a model of the bond wire and the amplifier itself. At the source a 300 mV peak-to-peak voltage is generated and fed through a transmission line with a characteristic impedance $Z_0 = 50\ \Omega$ to the SQuBiC chip. The transmission line has a length of approximately 3 m and represents the wiring from room temperature to the chip with an optional termination resistance R_T, which can be removed to reduce the power consumption. Assuming a power matched system the power consumption within the termination load is approximately 230 µW. The result of the simulation is shown in figure 4.5. The input signal (blue) to the buffer and the output signal (red) are plotted over time.

The delay caused by the transmission line is easy to observe. The input signal has an amplitude of about 300 mV and the output voltage reaches almost the nominal 1.2 V. The small input signal centered around 0 V is translated to a bigger signal centered around

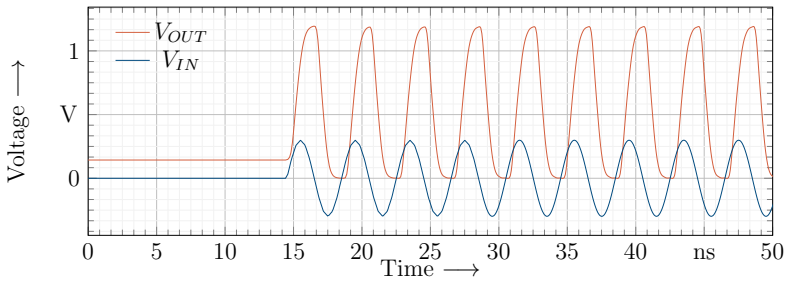


Figure 4.5: Transient simulation results of the implemented clock buffer.

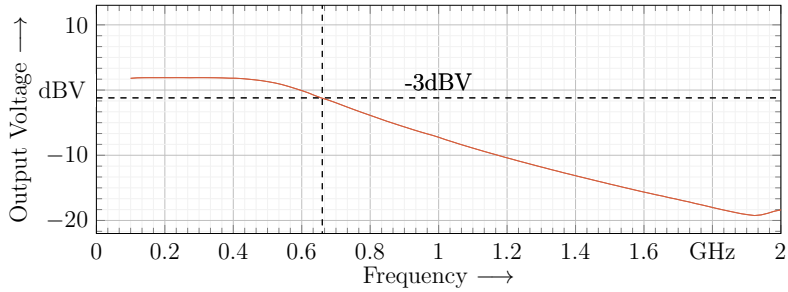


Figure 4.6: Simulated output voltage of the implemented clock buffer over input frequency.

0.6 V from 0 V to 1.2 V.

Figure 4.6 shows a simulation of the output voltage level of the clock buffer over the frequency of the input signal. For low frequencies the output level of the clock buffer is constant and starts to decrease after a certain point. The 3 dB corner frequency of the amplifier is marked in the plot at approx. 660 MHz.

Since not all circuits on the chip require the full frequency of 500 MHz or 250 MHz an additional frequency divider is implemented. Although this division could be done in each block it was implemented at the output of the DCO/clock buffer domain. The reason is to reduce the frequency to the desired frequency as early as possible in order to reduce losses due to parasitic capacitances and gate capacitance of the following buffer.

The divider circuit is constructed with D-flipflops in feedback configuration as shown in figure 4.7. The $\mathrm{CLK_{IN}}$ signal is connected to the clock input Φ of a D-flipflop and the inverted output $\overline{Q}$ is fed back to the input D.

To divide the frequency further it is sufficient to simply cascade multiple divide by 2 circuits as shown in figure 4.8. The 3-bit word T is a thermometer coded word which

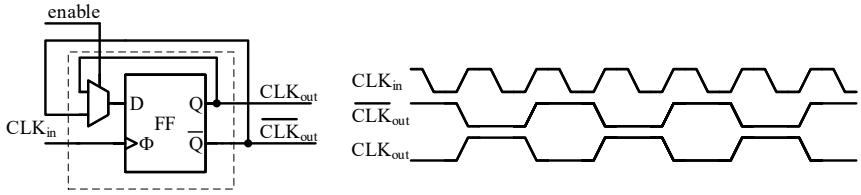


Figure 4.7: Circuit implementation of a frequency divider.

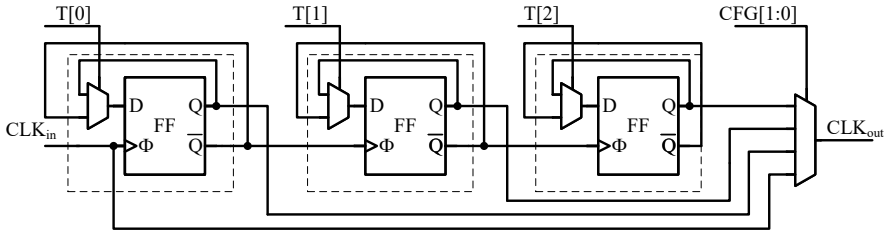


Figure 4.8: Circuit implementation of the divider.

controls the enable state of the individual flip flops.

4.2 Oscillators

4.2.1 Basic Feedback Theory

An oscillator has to satisfy two types of requirements first the system requirements which is the frequency of operation, phase noise and the interface requirements [51]. From the conceptual point of view one can see an oscillator as an amplifier with zero or negative phase margin. The formula for the transfer function in the Laplace domain of the simple feedback system from figure 4.9 can be derived to be:

$$Y(s)/X(s) = \frac{H(s)}{1 + H(s)}, \tag{4.2}$$

with the input $X(s)$, the output $Y(s)$ and the forward transfer function $H(s)$ with $s = j\omega$. If $H(s = j\omega) = -1$ the gain from input to output of the system points towards infinity, therefore an output at frequency ω_{out} can be sustained [51].

Figure 4.9: Feedback system.

Since $H(s)$ is a complex function, $H(s) = -1$ can be written as magnitude and phase:

$$\begin{aligned} |H(s = j\omega)| &= 1 \\ \underline{/H(s = j\omega)} &= 180^{\circ}. \end{aligned} \tag{4.3}$$

This representation 4.3 is called Barkhausens criteria for oscillation. It states that for an stable oscillation the loop gain has to be unity and the phase shift must be 180°. This will create a 360° overall phase shift and sustain a stable oscillation.

4.2.2 Digital Controlled Oscillator

In order to generate a clock signal with a controllable frequency a DCO is implemented on chip. The basic requirements for the oscillator are summarized in table 4.1. The 255 discrete values correspond to the configuration register bits, giving a sufficient accuracy for the digital clock. The tuning range is chosen to be 100 MHz. Twice the sampling frequency of the DAC was chosen to be able to operate on demand on both clock phases.

For a small foot print and low power consumption the implemented DCO is based on a ring oscillator topology. A ring oscillator is build by a number of delay stages with the output of the last stage being fed back to the first stage. To achieve a stable oscillation the overall phase shift must be 360 degree. Each stage provides a phase shift of π/N where N is the number of stages [52]. One possible implementation is based on simple inverters. An odd number of inverters can be combined to form a ring oscillator which is shown in figure 4.10. A closed series connection of an odd number of inverters theoretically has no defined or allowed state. However, if one considers the propagation time of the inverting components, an odd number results in an oscillating and self-exciting structure.

A way of determining the frequency of a ring oscillator is to use a linear model as shown in figure 4.10. If we assume that all stages are the same and the delay of a inverter is negligible the gain the transfer formula of a single inverting stage can be written as:

$$H_1(j\omega) = H_2(j\omega) = H_N(j\omega) = \frac{-g_m}{1 + j\omega RC}, \tag{4.4}$$

where C_x is the input capacitance of the next stage and R_x is the parasitic resistance of the connection between the inverter stages. According to equation 4.3 in order to achieve a stable oscillation the overall loop gain has to be:

$$N \cdot |H_1(j\omega)| \geqslant 1 \tag{4.5}$$

Table 4.1: Requirements of the DCO used as clock generator.

Requirement	Value
Discrete frequency values	255
Center frequency	500 MHz
Tuning range	±50 MHz

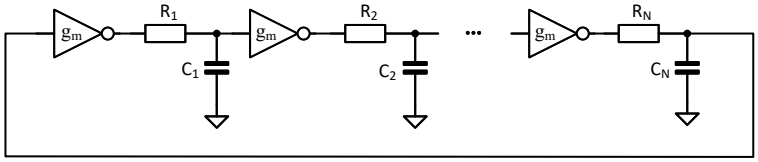


Figure 4.10: Linear model of the DCO.

and the phase has to satisfy:

$$\angle H(j\omega) = \theta = \arctan(\omega RC) = \frac{2k\pi}{N}. \tag{4.6}$$

The frequency of the oscillation can be derived by rewriting equation 4.6 as :

$$\omega = \frac{tan\theta}{RC}. \tag{4.7}$$

A different way to describe the oscillation frequency is in terms of the delay each stage provides. The signal passes N delay stages once to provide a phase shift of π in a time of t_d and the signal has to pass a second time to obtain the remaining phase shift. The frequency is then given by:

$$f = \frac{1}{2Nt_d}. \tag{4.8}$$

One way to control digitally the output frequency is to set the the capacity C_x. Accurately predicting the frequency of such an oscillator is a problem due to the strong non linearity in the used delay stages and the parasitic capacitance which is dependent on the layout and the interconnects of the design.

A different way of controlling the frequency of a ring oscillator is by limiting the current, which charges the next input node. The charging of the next stage is limited by a digital configurable current source array. In order to keep the rise and fall times equal both the NMOS and the PMOS side of the inverter will be starved. In order to extract the frequency of such a structure the delay of a transition has to be considered:

$$t_1 = C_x * \frac{V_{TH}}{I_D} \tag{4.9}$$

$$t_2 = C_x * \frac{V_{DD} - V_{TH}}{I_D}, \tag{4.10}$$

with V_{DD} being the supply voltage, V_{TH} the threshold voltage for the 0 and 1 transition,

C_x the capacitance of the next stage and I_D the limiting current. The overall delay is simply the sum of both, which simplifies to:

$$t_1 + t_2 = C_x * \frac{V_{DD}}{I_D}. \tag{4.11}$$

therefore the overall oscillation frequency can be described by the number of stages N and the delay of 2 transitions:

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{1}{N(C_{tot} * \frac{V_{DD}}{I_D})}. \tag{4.12}$$

The DCO itself, as depicted in figure 4.11, consists of a digital controlled current mirror bank to limit the current through the oscillator and a digital encoder that converts the binary 8 bit input word into a usable format word for the current mirror bank. The bias current I_I is supplied from outside the chip. The generation of the current can be done either in a unary way or a binary. Unary current steering DACs employ a single unit current source for each DAC step. This leads to a total of 255 identical current sources for a 8-bit DAC. In the binary fashion each current source is weighted by a power of two. The binary approach has the benefit of reduced digital overhead but suffers the most from mismatch due to the higher mirror factor which multiplies the current mismatch from the process variations. The unary approach requires a lot of area. The current bias generation is divided into 3 coarse regions each employing unary bias currents to reduce the area while maintaining reasonable matching.

The schematic for this circuit is shown in figure 4.12. A bias current I_{bias} is mirrored by the current mirror M_1 and M_2. The current from M_2 is the baseline output current which

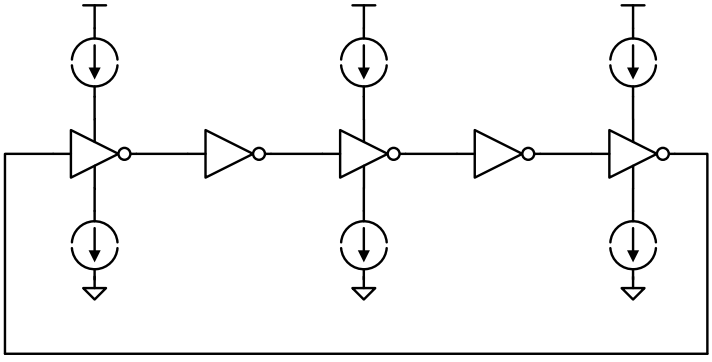


Figure 4.11: Current starving implementation of the digitally controlled oscillator.

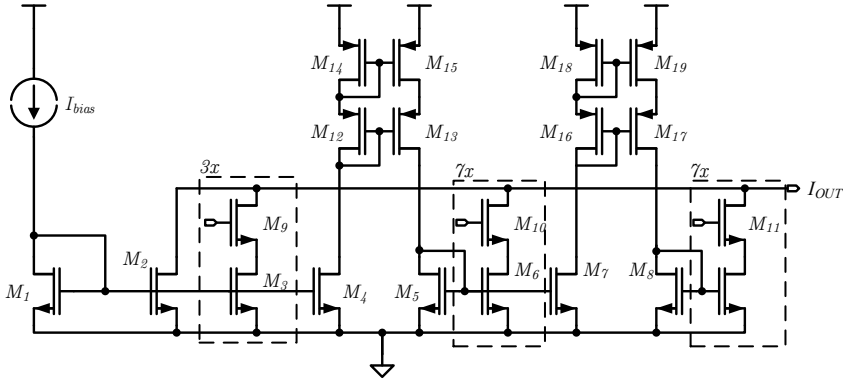


Figure 4.12: Current generation unit of the implemented DCO.

is always supplied to the DCO. M_9 is used to control the MSB part of the current and M_3 is used as mirror transistor. This structure is connected 3 times in parallel and each branch controlled by one word of the MSB subword. The transistor M_4 is used to mirror the current into the current mirror created by the transistors $M12$ to $M14$ which divide the current by a factor of 7 for the intermediate current stage. Similar to the previous stage, the transistor M_5 mirrors the current to the connection of M_6 and M_{10}. Here M_6 is the mirror transistor and M_{10} the switch. This is repeated for the lsb part.

The required digital word for this current sources is given by three separate binary to thermometer decoders. The signal is split into three separate words the least significant bits of the input word, the three following bits and the two most significant bits of the word. The three bits wide words are converted to 7 bits wide thermometer words and the two bits wide word in converted into a three bits wide thermometer word.

The DCO was simulated with a test bench using a netlist containing all circuits and their extracted parasitics (PEX). It is connected to the supplies via small inductances to emulate

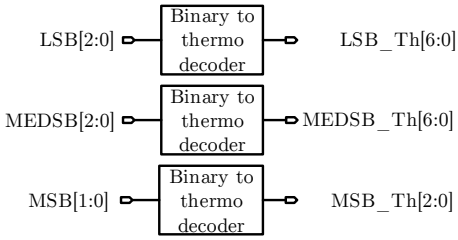


Figure 4.13: Digital decoder of the DCO.

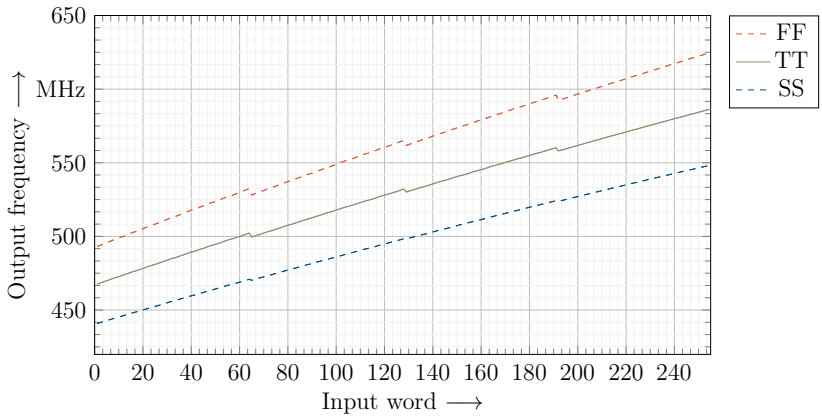


Figure 4.14: Simulation Results for the DCO at room temperature.

the effect of bond wires. The digital input configuration and the DCO input is controlled with verilog HDL code. The code creates the required bit values and configuration settings for the simulation. The outputs of the DCO are connected to a buffer chain that represents the load of the DCO when it has to drive either the digital parts of the chip or is rerouted to the output buffer. The testbench is used for simulations with complete parasitic extracted netlists and more simple connection and functionality tests. The simulation result is shown in figure 4.14 for the typical corner (TT), the slow corner (SS) and the fast corner (FF). The output frequency of the DCO is shown over the digital input word. The output frequency increases with an increasing input word. The output frequency is higher in the FF corner and lower if the devices are in the SS corner compared to nominal operation.

4.2.3 Voltage Controlled Oscillator

Some qubits, such as SiGe spin qubits, employ microwave signals to control the qubit. A Voltage Controlled Oscillator (VCO) was implemented on the chip to investigate the cryogenic effects on its characteristics. The most important requirements are summarized in table 4.2. The center frequency of the VCO shall be at 20 GHz with a linear tuning range of about 300 MHz which covers the frequency qubits with microwave control need for operation. It shall cover a greater frequency range with discrete tuning. The VCO is not intended for direct operation at same temperature stage as the qubit but rather at a higher temperature stage such as the 4 K, therefore lowering the constraints on power consumption. A LC oscillator design was chosen to get good phase noise performance and benefit from the increased quality factor of coils at cryogenic temperatures. Figure 4.15

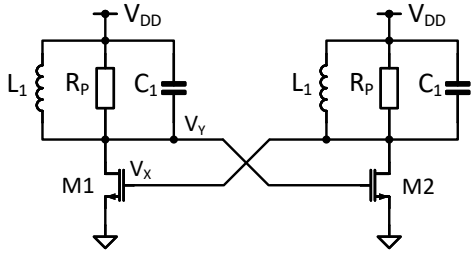


Figure 4.15: Cross-coupled oscillator formed by two LC-tuned amplifiers.

shows a feedback system consisting of two LC-tuned amplifiers to allow a simplified small signal analysis. The transfer function of one of those amplifiers can be separated into three transfer functions for different frequencies. For low frequencies the impedance of the coil is low compared to parallel resistance and capacitance. Therefore the amplification is determined by the inductive load and can be described by :

$$\frac{V_Y}{V_X} \approx -g_m L_1 s. \tag{4.13}$$

The amplification is very small and the phase is close to -90°. In case of resonance the LC tank reduces to the parallel resistance which leads to the amplification:

$$\frac{V_Y}{V_X} \approx -g_m R_p. \tag{4.14}$$

The amplification is at its peak and the phase shift equals -180°. At high frequencies the amplification is determined by the capacitance and can be described by:

$$\frac{V_Y}{V_X} \approx -g_m \frac{1}{C_1 s}. \tag{4.15}$$

The amplification drops and the phase goes to 90°. Since the total phase shift of this circuit fails to achieve a 360° phase shift for any given frequency it cannot sustain a

Table 4.2: Electrical requirements of the VCO.

Requirement	Value
Power consumption	5 mW
Center frequency	20 GHz
Linear tuning range	300 MHz
Discrete tuning range	2 GHz

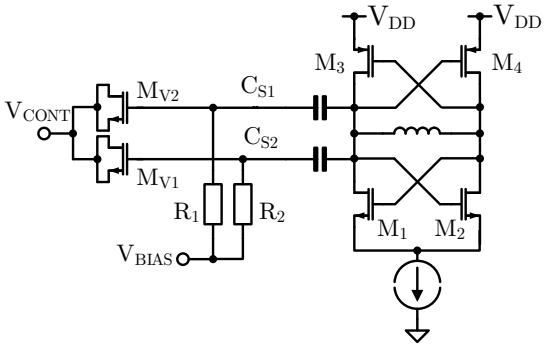


Figure 4.16: Frequency control of VCO.

stable oscillation. But it achieves a phase shift of 180° with a gain of $-g_m R_p$ for the resonance frequency w_0, therefore a cascade of two identical of these amplifiers will satisfy the Barkhausen criteria 4.3 as long as:

$$(g_m R_p)^2 \geqslant 1. \tag{4.16}$$

The oscillation frequency of such an oscillator is determined by C_1 the parasitic capacitance of the inductor L_1 and the input capacitance of the next stage. The capacitance at V_X consists of C_{GS2}, C_{DB1} and the effect of C_{GD1} and C_{GD2}, where C_{GD1} and C_{GD2} are in parallel and the voltage change across $C_{GD1} + C_{GD2}$ is twice the voltage change at V_X due to the differential nature of V_X and V_Y[51]. To control the frequency of the oscillator electrically the capacitance of the LC circuit is changed by using a varactor. The output frequency is determined by:

$$w_{osc} = \frac{1}{\sqrt{L_1(C_1 + C_{DB1} + 4C_{GD} + C_{GS2})}} \tag{4.17}$$

$$w_{osc} = \frac{1}{\sqrt{L_1(C_1 + C_{var})}}, \tag{4.18}$$

where C_1 now combines the different static capacitance and C_{var} is the voltage dependent capacitance value of the varactor.

To increase the usable tuning range of the VCO positive and negative voltages across the varactor are beneficial. This is achieved by AC-coupling between the varactors and the core of the oscillator as seen in figure 4.16. The control voltage V_{CONT} is connected to the varactors M_{V1} and M_{V2}. The other side of the varactor is connected with a resistance to a bias voltage V_{BIAS} and with coupling capacitances C_{S1} and C_{S2} to the core of the

oscillator. The bias voltage is set to a value close to $V_{DD}/2$. The frequency of the oscillator is independent of the common mode of the oscillator. Instead of applying a voltage from 0 to V_{DD} we now apply a voltage optimal for the the tuning range of the varactor. The drawback of this approach is the parasitic capacitance of the coupling capacitors. C_{S1} and C_{S2} have to be much bigger than the value of the varactor [51]. We assume that $C_{S1} = C_{S1} = C_S$ and C_{var1}, C_{var2} are connected in series with C_S inserting into equation 4.18 leads to an expression of the oscillation frequency:

$$w_{osc} \approx \frac{1}{\sqrt{L_1 C_1}} * \frac{1}{2C_1} * \frac{C_S^2(C_{var2} - C_{var1})}{(C_S + C_{var2}) + (C_S + C_{var1})}. \tag{4.19}$$

When C_S is chosen to be about 10 times bigger than C_{Var} the impact of the tuning capacitance is reduced by about 10% of the overall capacitance. Increasing the capacitance infinitely cannot solve this issue due to the parasitic capacitance of the coupling capacitor to the substrate. The current through the oscillator core is limited by a tail current source as can be seen in figure 4.16. In addition we use a second cross-coupled pair formed from the transistors M_3 and M_4. The previously used separate inductors are now combined into one differential inductor between the output node of the oscillator. The second cross-coupled pair reuses the current from the first and therefore doubling the gain for the same inductance and current. This is done to ensure operation even in the unknown cryogenic environment.

One issue with a VCO is the narrow tuning range. With an increase of the varactor range the oscillator gets sensible to control voltage V_{CONT} variations and noise. Instead for covering large frequency ranges one employs discrete tuning capacitances. This is achieved by placing a bank of unit capacitors C_u in parallel with the tank and digitally switch them in or out to change the frequency of the tank. The capacitors are chosen equal to minimize design effort and increase the matching between each other in the layout.

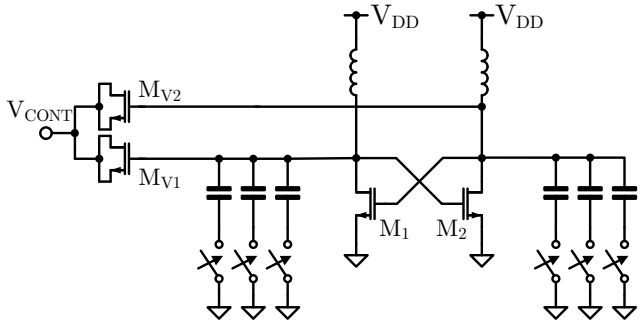
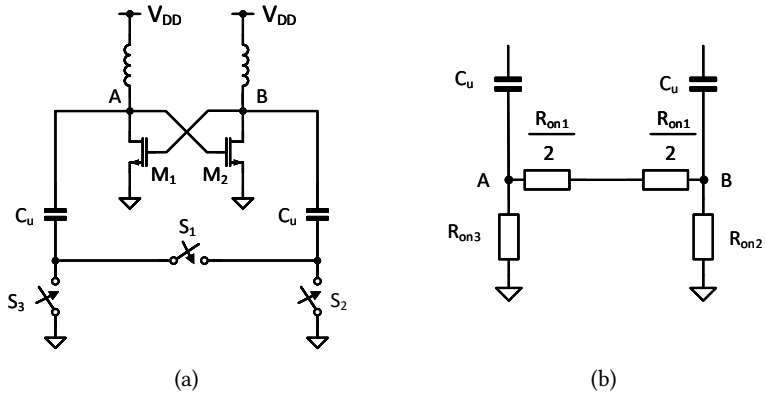


Figure 4.17: Discrete frequency control scheme of the VCO.



(a) (b)

Figure 4.18: Schematic (a) and small signal equivalent circuit (b) of the implemented discrete tuning scheme.

One of the problems of this discrete tuning scheme is that the on resistance of the switches degrades the Q of the tank. One cannot simply increase the width of the transistors to reduce the on resistance since larger switches produce greater parasitic capacitances. This problem can be reduced by exploiting the differential operation of the oscillator as shown in figure 4.18. By placing the main switch S_1 between the nodes A and B each capacitor C_u sees half of the resistance R_{on}. The switches S_2 and S_3 are minimal width switches and merely define the common mode [51]. This allows a reduction of the width of S_1 by a factor of two for a given R_{on}.

4.2.4 Output Amplifier

Since most measurement equipment employ a 50 Ω termination the output of the oscillators have to be able to drive an output load of 50 Ω. Neither the VCO nor the DCO can drive such low ohmic loads while sustaining a stable oscillation. To increase the driving strength an output amplifier must be used. A pseudo differential cascode amplifier with an off-chip balun as shown in figure 4.19 was designed for this reason.

The transistors M0 and M1 form the input stage and transistors M2 and M3 are the cascode transistors. The differential input signal is supplied to the input pair. Since the output oscillation is centered around the center tap voltage of the balun. The cascode transistors are used to shield the input transistors from the high voltage, avoid break down and in addition reducing the input capacitance. The drain source voltage of the input transistor M0 is always less than $V_B - V_{TH2}$. V_B has to be chosen in a way that V_{DS2} and V_{GS2} are always below VDD. Additionally, the cascode structure provides a

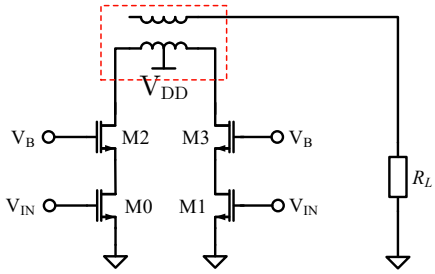


Figure 4.19: Simplified schematic of the output amplifier.

Table 4.3: Voltage requirements for GaAs-Qubit operation.

Characteristic	Specification
DC voltage range	1 V
DC voltage stability	20 µV
Number of DC Voltages	$\leqslant$ 8
Resolution	12 bit
Pulse voltage range	$\pm$4 mV
Number of pulse voltages	2
Pulse sampling rate	250 MHz
Pulse resolution	8 bit

higher reverse isolation and therefore less feedback and more stable operation than a normal common source stage [51]. The bias voltage V_B is a trade of between linearity and device stress. If V_B is to high the transistor M2 and M3 respectively can be driven out of saturation which leads to a change of the drain voltages of M0 and M1 respectively and therefore causing distortion. The voltage V_B can be set independently by a 8 bit on chip R-string DAC with a dynamic range of 2 V. The power consumption of the DAC can be neglected since the amplifier is just used for measurement.

4.3 Pulse Digital-to-Analog Converter

The requirements for the operation of GaAs qubits employing a singlet triplet encoding were explained in chapter 3.1 and are summarized in table 4.3. The derivation of the DC characteristics can be found in [50]. The transient signals require a sample rate of approx. 250 MHz and a resolution of 8 bit with a range of $\pm$4 mV. Although 8 bit seems not to be a challenging requirement, it means a step size of just 30 µV. The choice of a

pulse-DAC architecture is an optimization between the factors size, resolution and speed. There are several DAC architectures available with different benefits and drawbacks for the operation of a GaAs qubit. The key performance indicators of each architecture are the achievable resolution and the maximum speed of the architecture.

4.3.1 R-String

The simplest implementation of a DAC is a R-String or a Kelvin divider topology. A number of N equal resistors are connected in series to create N unique voltages. Figure 4.20 shows a divider made of 2^N resistors with $N = 3$ and generates 8 discrete voltages:

$$V_i = V_{DD}\frac{i}{8} \qquad , i = 0 \ldots 7. \tag{4.20}$$

The selection of each voltage is done with simple switches. Either the switches are connected in a tree like fashion, which allows the direct digital selection of the voltages without the need of an additional encoder. Or each output gets an individual switch, which requires more wiring and an additional encoder but has a significant lower on resistance. Such a DAC is inherently monotonic due to its design, it is simple to build, has a good DNL and very low glitch energy. On the other hand its resolution is limited

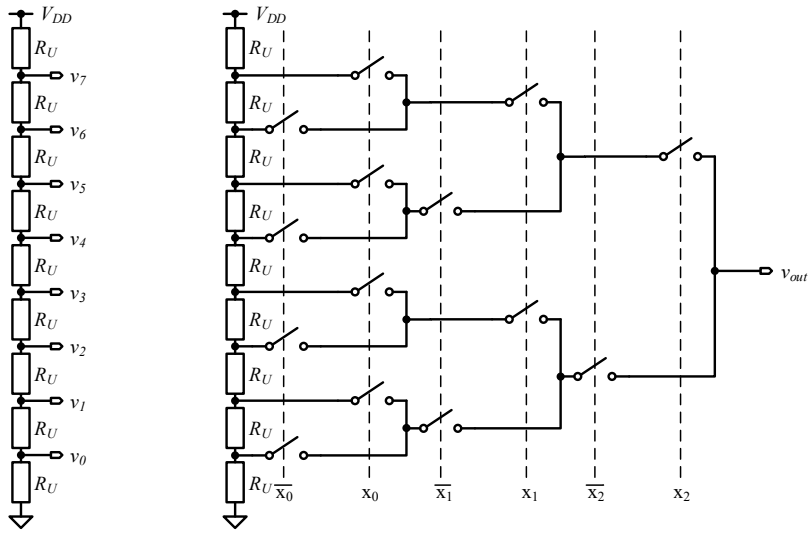


Figure 4.20: Simplified schematic of a Kelvin-DAC.

due to its size, which grows exponential with the resolution. The speed is limited by the decoding logic and the number of interconnects that lead to parasitic capacitances increasing recharging times.

4.3.2 R-2R

One of the main issues of an R-String DAC is that the number of resistors increases exponentially with the number of bits. Therefore resolutions of more than 8 bits occupy a large amount of active area. The R-2R ladder is constructed of a combination of resistance R and $2R$ in parallel forming a resistive divider to scale down the voltage V_{REF}. The resistance seen on the left of every node is 2R. The output of an R–2R ladder in the voltage mode is the superposition of terms that are a successive division of V_{REF} by 2 [53]:

$$V_{Out} = Vref(\frac{1}{2} * b_{n-1} + \frac{1}{4} * b_{n-2} + \cdots + \frac{1}{2^{n-1}} * b_1 + \frac{1}{2^n} * b_0). \tag{4.21}$$

The R-2R structure reduces the number of resistors needed from 2^n to $3n$. Thus decreasing the effort for interconnects and the number of switches and encoder logic. On the downside, the R-2R structure experience the most glitch energy while switching from one output level to another. Unless reference generators are used with an sufficient low impedance the output load of the voltage sources is code dependent, which in turn will lead to harmonic distortion. Another disadvantage is that an R-2R structure is not intrinsically monotonous with the worst nonlinearity in the middle of the characteristic.

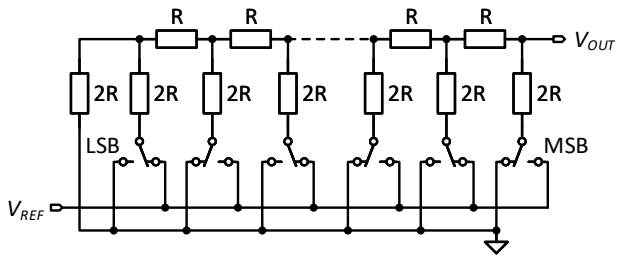


Figure 4.21: Simplified schematic of a R2R DAC.

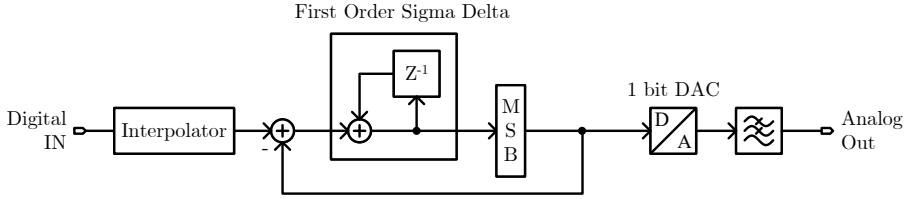


Figure 4.22: Simplified schematic of a ΣΔ DAC.

4.3.3 Sigma-Delta

Sigma-Delta (ΣΔ) converters are fundamental different to other types of converters. The ΣΔ converter achieves high resolution by combining many low resolution conversions into one. This is done in a way that the quantization noise is shifted to higher frequencies. Low pass filtering gets rid of the high frequency noise leads to the wanted output signal. The first block of a delta sigma DAC is usually an interpolator that increases the data-rate to a higher level: $2f_BOSR$, where f_B is the frequency at which the signal band ends and OSR is the oversampling ratio. Then the digital modulator reduces the number of bits to an intermediate signal is used to control a low resolution DAC which precedes an analog reconstruction filter [53]. Ideally, a 1 bit stage can be used as a DAC. A simple exemplary ΣΔ converter is shown in figure 4.22. The benefit of the ΔΣ DAC lies in the high resolution which can be achieved by massive oversampling. It does this while consuming very low power with a decent linearity. The drawback being the very limited sample rate due to the inherent need for oversampling and therefore an operating speed that is way higher then the signal bandwidth of the DAC itself.

4.3.4 Current Steering

The current steering (CS) topology operates by steering current into a load resistance. An example of a unitary weighted current steering DAC is shown in figure 4.23. The individual currents of each current source are summed up and form an overall current that represents the value of the digital input word b. One can derive the formula for the output current of such a current steering:

$$I_{OUT} = I_U(b_0 + 2b_1 + \cdots + 2^k b_k + \cdots + 2^{n-1}b_{n-1}), \tag{4.22}$$

where b_n is either 0 or 1 depending on the value of the digital word b at position n and I_U is the value of unit current. Each unit current source is connected to a switch that is controlled by a digital word b. The current sources are in binary, and all switch output nodes are connected in parallel thus summing up the current of each individual current

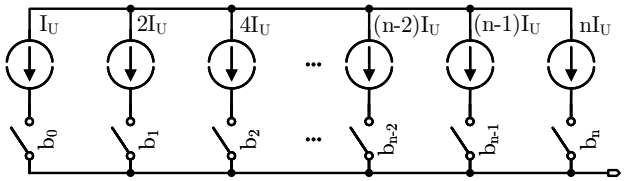


Figure 4.23: Simplified schematic of a current steering DAC.

source. One of the great benefits of a current steering topology is that it does not need an output buffer, because the output current can be directly converted to a voltage by the termination load. It is well suited for medium resolution and high frequency applications. The linearity of this topology is limited by the mismatch of the individual current sources to each other.

4.3.5 Comparison

The benefits and drawbacks of each DAC topology is summarized in table 4.4. Even though a Kelvin topology promises the best performance in terms of linearity the prospects for scaling are limited due to the size and number of elements. The R-2R architectures solves the size problem but loose considerable in terms of linearity and settling time and is therefore not a good candidate for operation at 250 MHz. ΣΔ perform very good in terms of linearity, size and resolution, but the need for oversampling permits the operation of such a DAC for high frequency operation. Finally the current steering topology offers a good trade off between size and resolution while maintaining excellent settling time, but suffers in linearity. Figure 4.24 shows the state of the art of different DAC architectures from Texas Instruments. The low frequency, high resolution side is

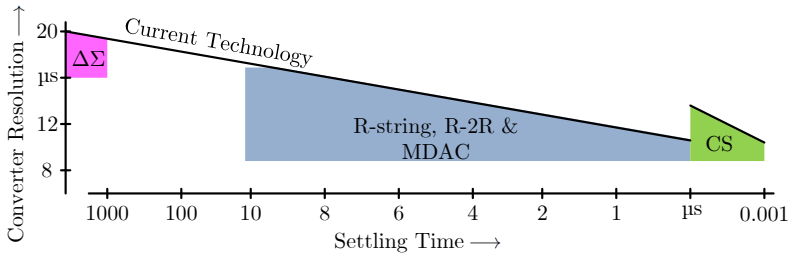


Figure 4.24: Resolution and settling time of state of the art DACs separated by architecture [54].

Table 4.4: Benefits and drawbacks of different DAC architectures.

Topology	Linearity	Settling Time	Size	Resolution
Kelvin	++	+	-	-
R-2R	+	o	+	+
ΣΔ	+	–	++	+
CS	o	++	+	+

predominantly filled with ΣΔ-DACs which benefit from oversampling and low operation speed to achieve a high resolution. In the medium frequency, medium resolution area one can find Kelvin, R-2R and MDAC architectures, which all have different benefits and drawbacks but all struggle to achieve a resolution of more than 8 bit while achieving a refresh rate beyond 250 MHz. A multiplying DAC (MDAC) generates an output signal which is the result of the multiplication of a reference signal and a digital word. The most common architecture achieving moderate resolutions with a refresh rate of 100 MHz or more is the current steering DAC topology.

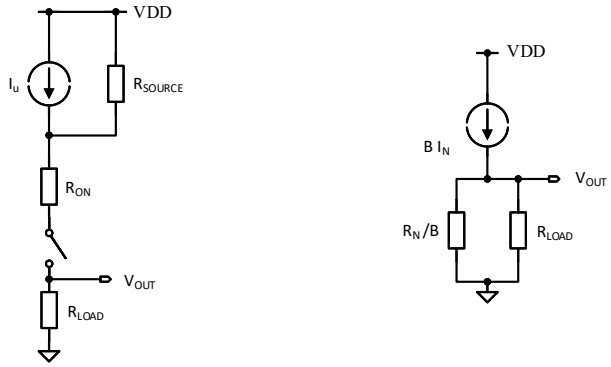
4.3.6 Implementation

For the pulse requirements gathered in figure 4.3 and with help of the overview of the DAC architectures given in figure 4.24 a current steering DAC has been chosen to be implemented for this chip. A number of current sources are connected to an output to sum up the individual current to one resulting current. The output current will be terminated at a load and converted into a voltage. To investigate the linearity of the DAC and to account for the resistance of the switches and the non infinite source resistance of the DAC, the Norton equivalent circuit of a unit current source is used [53]. The equivalent circuit is depicted in 4.25.

I_u is the current from a unit current cell, R_{SOURCE} is the source resistance of the cell, R_{ON} is the on-state resistance of the used switch and R_{Load} is the value of the resistance used to terminate the current. The Norton equivalent source contains a current I_N and a resistor R_N which can be derived by:

$$I_N = \frac{I_u R_{SOURCE} + VDD}{R_{SOURCE} + R_{ON}}$$
$$R_N = R_{SOURCE} + R_{ON}. \tag{4.23}$$

With an output load R_{LOAD} and a number k of connected switches together with the



(a) (b)

Figure 4.25: Schematic of a unit current cell (a) and its small signal equivalent circuit (b).

equations shown in 4.23 we can derive the equation for the output voltage:

$$V_{OUT} = kI_N \frac{R_{LOAD} \cdot R_N/k}{R_{LOAD} + R_N/k} = I_N R_{LOAD} \frac{k}{1 + \alpha k}, \tag{4.24}$$

where $\alpha = R_{LOAD}/R_N$.

One of the major characteristics of a DAC is the differential non-linearity (DNL) and the integral non-linearity (INL). The DNL describes the deviation of a single step size to the ideal step size. The INL expresses the overall deviation of the DAC characteristic to the ideal one [53].

Equation 4.24 shows a nonlinear relationship, which degrades the INL and causes distortion [53]. In order to minimize the INL error the output resistance of the current sources has to be maximized.

The INL can be described by:

$$INL(k) = \frac{k[1 + \alpha(2^n - 1)]}{1 + \alpha k} - k. \tag{4.25}$$

Equation 4.25 shows that in order to achieve an INL < 1LSB it is necessary that the source resistance $R_{SOURCE} > R_{LOAD} * 2^{2n-2}$. For ease of measurement and potential matching we assume a load of $R_{LOAD} = 50\Omega$ and a resolution $n = 8$ bit this means that source resistance R_{SOURCE} of the unit current cell must be bigger then 819kΩ.

A cascode current mirror is shown in figure 4.26 to investigate the output resistance. The transistors M1 and M2 form the current mirror and the transistors M3 and M4 act as

cascode. The output of the cascode current mirror is given by $rds4 * rds2 * gm4$, which

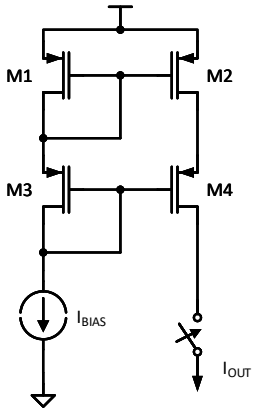


Figure 4.26: Unit current mirror with cascode transistor.

can be easily be in the range of several MΩ. In addition to systematic non linearity caused by the output resistance of the current sources systematic or random mismatch between the individual current sources due to process variations have to be considered. For a current mirror the error factor can be described by [55]:

$$EF = \frac{I_o}{I_i} - 1 = (1 + \frac{\Delta K_p}{K_p})(1 + \frac{\Delta W}{W})(1 + \frac{\Delta L}{L})^{-1}(1 - \frac{\Delta V_{th}}{V_{GS} - V_{th}}) - 1, \quad (4.26)$$

where K_p is a technology parameter, W is the width of the transistor and L is the length of a transistor. The error part due to ΔKp, ΔW and ΔL are only dependent on the manufacturing process, whereas the error part of the threshold variation ΔV_{th} is dependent on the effective gate overdrive voltage $V_{GS} - V_{th}$ [55].

A more in depth analysis reveals the Pelgrom-Law :

$$\frac{\sigma_P}{P} = \frac{A_P}{\sqrt{WL}}, \quad (4.27)$$

with σ_P/P being the relative standard deviation of a component parameter, A_P a mismatch technology parameter and W, L the component dimensions in the layout [55]. This means that the relative mismatch of a component can be reduced by increasing its area. However, it is not always feasible to arbitrarily increase the area and therefore for increased parasitic capacitance and thus reduced maximal operating frequency. Additionally, the use of binary weighted unit current sources lead to a worse matching behavior. Typically, it is beneficial to use unary weighted current sources due to the improved matching

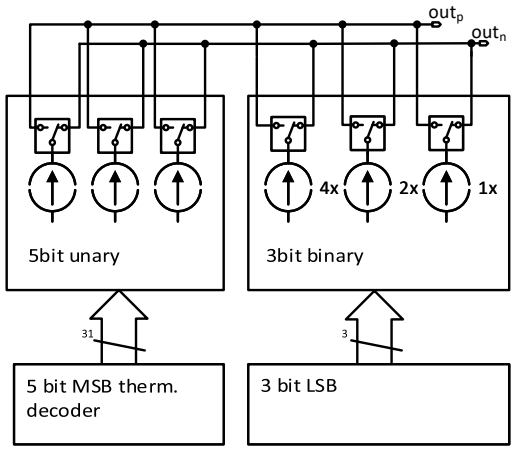


Figure 4.27: Functional diagram of the pulse DAC.

behavior and the inherent monotonic behavior. To counteract the mismatch, while still maintaining reasonable area the DAC is separated into 2 different parts as shown in 4.27.

The current sources responding to the three lsb of the DAC are weighted in a binary way. The remaining 5 bit MSB part is weighted in a unary fashion. For the LSB part binary weighted unit current sources are connected in parallel and switched together by the input bits. The digital encoder transform the 5 most significant bits of the binary input word into a thermometric signal which switches the unity current generators one by one.

Rather then switching the current sources on or off the current is switched between to outputs out_p and out_n. The switches in figure 4.27 are just conceptual switches, a more realistic implementation is shown in 4.28. If we would consider a single switch here instead of the complimentary controlled transistors M4 and M5, the current source would drop deep into the triode regime and the voltage on node A and B drift towards GND. When the current source would be switched back on a long recovery time is needed. This is avoided by not switching off the current but rather switching between a dummy output and the signal output. Correspondingly the current source formed by M6 and M7 is never turned off. The crossing point of the two signals controlling M4 and M5 has to be shifted towards the lower voltage so that both PMOS switches are turned on for a short duration. The control signal generator in 4.28 achieves this by first sampling the input signal with the clock of the DAC, then the signals of the flip-flop are delayed by two inverters, which achieve differential control with two complementary phases. Additionally, two inverters are used to control the delay. The voltage levels V_H, V_L can be

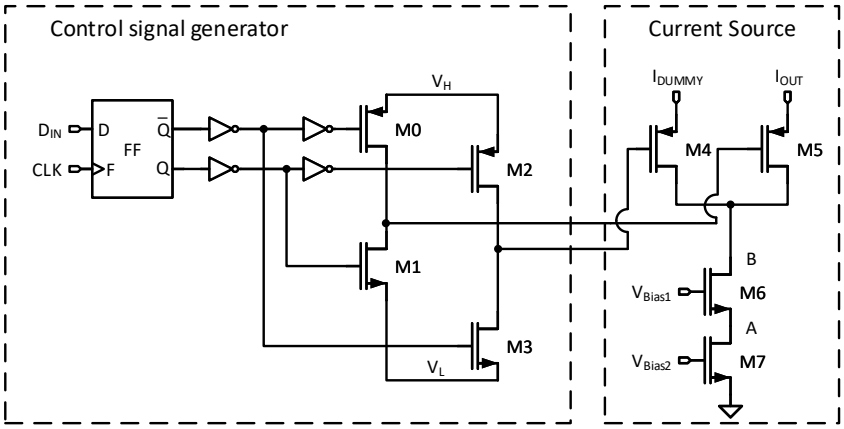


Figure 4.28: Implementation of a latch to shift the crossing point of the switching to avoid complete turn off.

adjusted to ensure the level to open and close the switches while having the possibility by reducing the level to circumvent charge injection [53].

At cryogenic temperatures, drastically worse current mismatch is expected. Therefore the Pulse-DAC employs the possibility for a manual calibration of each current source. Accordingly, each current cell employs a small calibration current DAC as depicted in Figure 4.29. This calibration DAC is connected between the cascode transistor of the

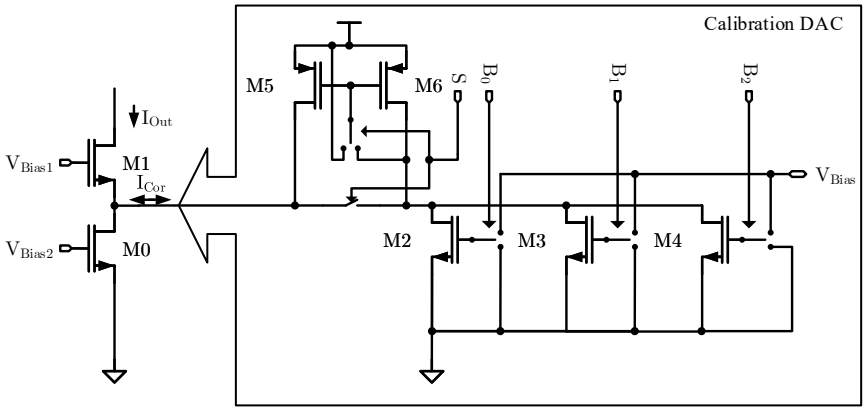


Figure 4.29: Unit current cell with calibration DAC cell.

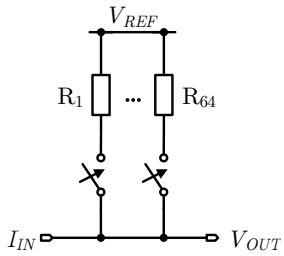


Figure 4.30: Simplified schematic of the implemented termination resistance array.

current source M1 and the current source transistor M0 to reduce the parasitic capacitance on the output of the DAC. The transistors M2, M3 and M4 are current sources with binary increasing W/L ratio with the gates switched by the digital word B to either 0 or the corresponding current mirror bias voltage V_{Bias}. The sign bit S controls the connection to the current cell of the DAC either adding the total current of M2-M4 to the output current of the cell or mirroring the current into a PMOS stage and then subtracting it from the output current.

The DAC is running at a frequency of 250 MHz. It is beneficial to terminate the current output of the DAC into a 50 Ω resistance for easier measurement at high frequencies. The output amplitude of the DAC is very small and for less than 10 mV the power consumption is still reasonable. As previously discussed, mismatch can lead to big deviations from the desired component value. Especially absolute values like 50 Ω resistors with good absolute matching are hard to achieve in CMOS processes.

The output termination of the DAC is not a single resistor but rather formed by 63 parallel resistors, as shown in figure 4.30. The middle value of 32 of such equivalent resistances in parallel equals 50 Ω in total. With this approach the variation of the resistances can be accounted for and the output resistance of the DAC can be configured. The current is drawn through the termination therefore an increasing digital word leads to an decreased analog output voltage.

Operation of a GaAs qubit requires signals with different timescales. The qubit needs fast pulses for operating and slow ramp like shapes for initialization and read out. A sample based approach leads to an enormous amount of memory used for storing ramps as well as the pulses.

Each pulse is encoded as a combination of a slope which is stored in a 9 bit register and a duration D which is an 8 bit word. The word D is given into a shift register, then a counter counts the duration of D clock cycles. Each clock cycle the digital input word to the DAC will be increased the value of S. When the counter reached the value of D

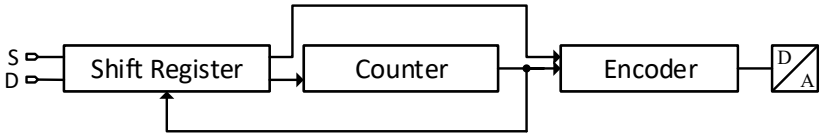


Figure 4.31: Control logic of the DAC.

the next value of the shift register is given into the counter and the slope value of the encoder is changed.

If we compare the required bits to save a ramp with duration n a traditional sample based encoding scheme would require $8n$ bits to save meanwhile the implemented encoding uses a constant 9 bit for the slope and a 8 bit for the step size. In the worst case this scheme needs twice the number of bits plus one, which is the case for pulses, but saves a lot of memory in the case of prolonged slopes.

The digital circuitry was simulated and evaluated in conjunction with an ideal DAC. A combination of rising and falling slopes, fast pulses and idle times were programmed and executed after a delay. Figure 4.32 shows the output voltage of the ideal DAC with a full scale range of 1 V over time.

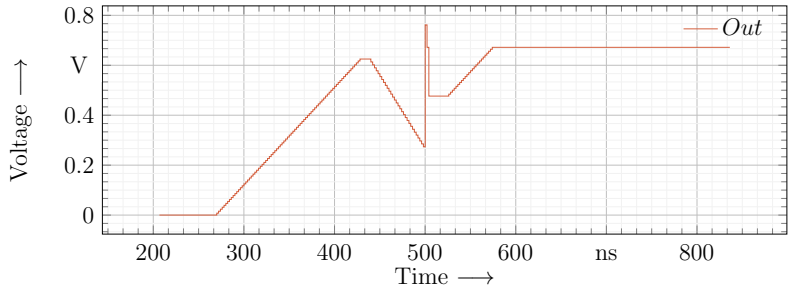


Figure 4.32: Transient simulation of the digital control of the DAC.

4.4 Toplevel

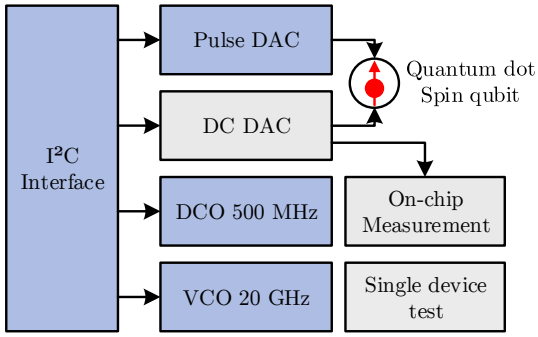


Figure 4.33: Simplified top level diagram of SQuBiC.

The sub blocks of the SQuBiC chip interact with each other. The connection between the individual sub blocks are shown in figure 4.33. The I^{2}C-Interface connects to and controls almost all parts of the chip. The DACs are meant to be connected to a GaAs spin qubit. The DCO and clock buffer connect indirectly to the other parts by a clock distribution network. The parts of the chip which are discussed in this thesis are denoted in blue the remaining parts are subject of a different thesis and can be found in [50].

4.4.1 Inter-IC Bus

The benefits of the I^{2}C bus for the application in the SQuBiC chips are the small number of wires that have to be used in implementation and the availability of a protocol for handling the acknowledgment of received and sent data. In addition, prior to the design of the SQuBiC chip an I^{2}C interface located on an ASIC for a different application was packaged and verified in a liquid helium environment down to temperatures as cool as 4.2 K prior to the design of the SQuBiC chip. Figure 4.34 shows the experimental setup in which the I^{2}C shall be operated in. The interface itself consists of two parts. A slave part on the IC and a master at room temperature. The control of the interface and the communication with a regular PC is done by a National Instruments Corp. "USB-8452". This is an off the shelf I^{2}C interface to connect and communicate via plug and play USB which acts as master device. The pull up resistances on the clock and data line are connected to a 2.5 V supply and thus can consume a considerable amount of current, creating a considerable amount of heat. Therefore, the pull-up resistances will be located at a higher temperature stage. In this case, the internal pull up resistor of the "USB-8452 are used.

The implemented I^2C on the SQuBiC chip contains 256 registers which are independently addressable by an eight bit word and are separated into configuration registers and status registers.

Configuration Register
The configuration registers are written by the I^2C master. The value is saved in the register of the on chip part of I^2C interface. 8 bits of data and a 1 bit indicator that shows if this data has been changed is combined to a 9 bit word.

Status Register
The remaining 64 registers are status registers whose values are written by the SQuBiC chip. Each status register consists of 8 bit of data and an update indicator that is supplied by the SQuBiC chip as well as an acknowledge signal that will show that the write process was successful.

In figure 4.35 the direction and arrangement of the I^2C configuration and status pins are shown.

4.4.2 Power Domains

Each individual part of the SQuBiC chip is located within its own power domain. Every power domain consists of a set of supply voltages for the 1.2 V core domain and if necessary for the 2.5 V input/output (I/O) domain as well as a ground, respectively. Every signal entering a domain from the outside of the chip has to pass through a set of ESD protection devices to ensure that the transistors on the chip survives production and handling.

When a signal enters from a lower voltage supply domain into a higher voltage supply domain the voltage can be so low that it is insufficient to fully turn off the PMOS transistor at the input of the following CMOS structures. This leads to significant static current

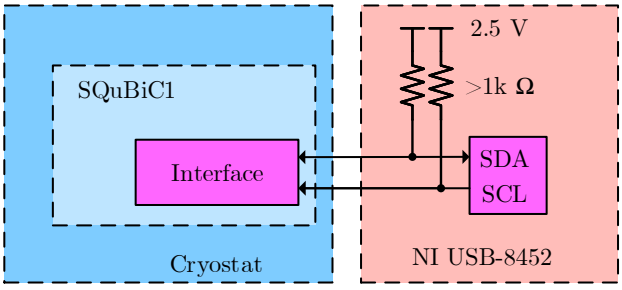
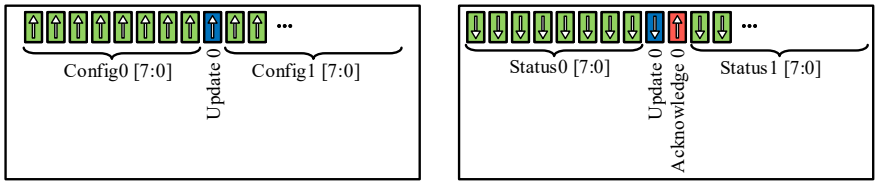


Figure 4.34: Experimental setup using the NI USB-8452 I2C-Interface.



(a) Config register lines (b) Status register lines

Figure 4.35: Direction and arrangement of the config and status registers on the SQuBiC chip.

consumption and decreased signal to noise ratio. The next stage does not see the full input level and has a lower input range to decide the next state. This is overcome by level-shifters. The employed level-shifter circuit is shown in figure 4.37.

All signals leaving the I^2C interface are level shifted to the local supply voltage and stored in local registers. These register are controlled by the level shifted update bit. This interface block is shown in figure 4.38 with three words (8 bit), three update bits and the levelshifters.

All the previously discussed circuits have been designed, layouted and fabricated in a TSMC 65 nm CMOS technology. A die photograph of this chip can be seen in figure 4.39. The overall die area is 4 mm^2.

The I^2C-Interface is located at the bottom chip edge of the die on an area of 0.092 mm^2. On the bottom right corner of the chip the DCO domain is located, containing the clock buffer as well as the DCO , frequency divider and distribution circuitry for the whole SQuBiC chip on an area of 0.007 mm^2. Above this area the VCO is located, which is

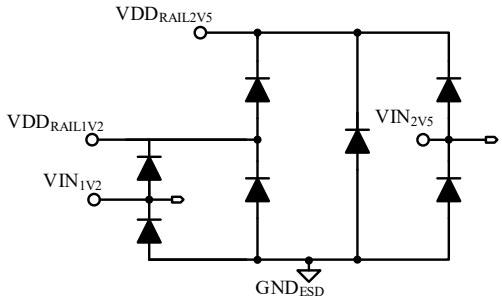


Figure 4.36: Functional schematic of the ESD protection structures.

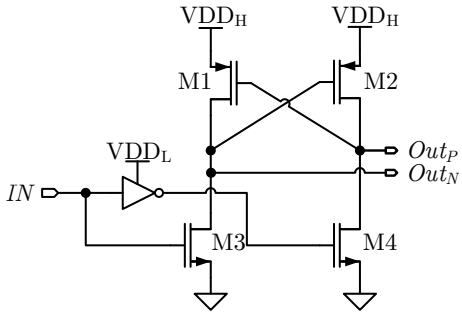


Figure 4.37: Schematic of the implemented level shifter.

easy to locate due the macroscopic coil that can be seen with bare eyes even without a microscope. The VCO contains the output amplifier as well as the VCO and its auxiliary circuitry within 0.12 mm^2. Finally the three different DACs (each 0.012 mm^2) are located in the top right part of the chip. They are placed together with a digital part (0.074 mm^2) common to all 3 DACs and the programmable termination (0.0592 mm^2) from figure 4.30 for two of the three DACs. The additional DAC is placed on the chip for measuring the DAC with external load. The remaining die area is used for single device test structures with GSG-probe pads and a qubit bias DAC and its auxiliary circuits, which are not within the scope of this thesis.

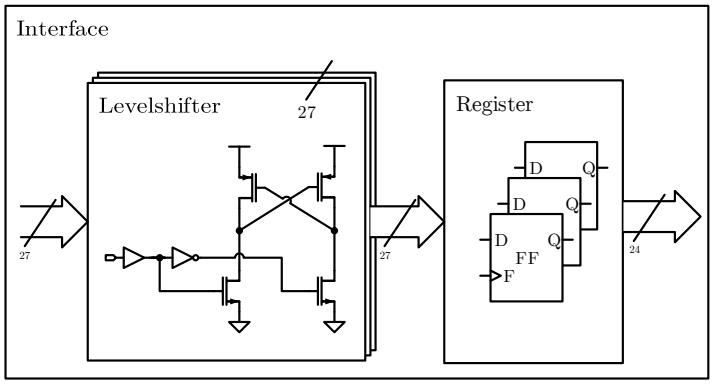


Figure 4.38: On-chip interface consisting of levelshifters and registers.

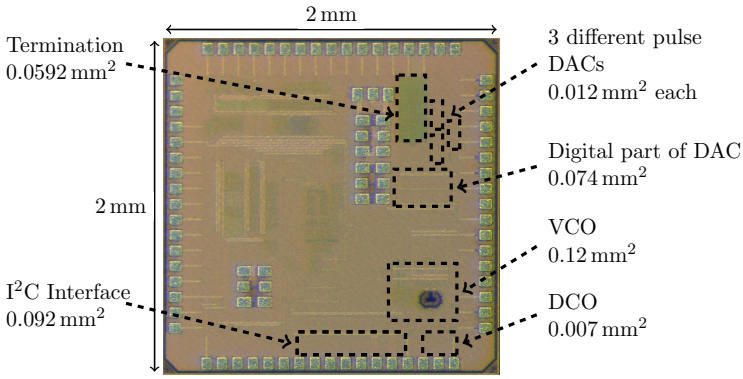


Figure 4.39: Die photograph of the fabricated control chip SQuBiC.

Chapter 5

Measurement Results

5.1 Measurement Setup

The performance of the circuitry must be verified not only at room temperature but also at a temperature close to absolute zero. The Central Institute of Engineering, Electronics and Analytics - Electronic Systems (ZEA-2), uses an Attocube attoDRY800 as shown in figure 5.1 for the low temperature verification of electronics. In the center of the attoDRY800 setup is a Gifford-McMahon (GM) cryo-cooler. On top of it is the cold sample

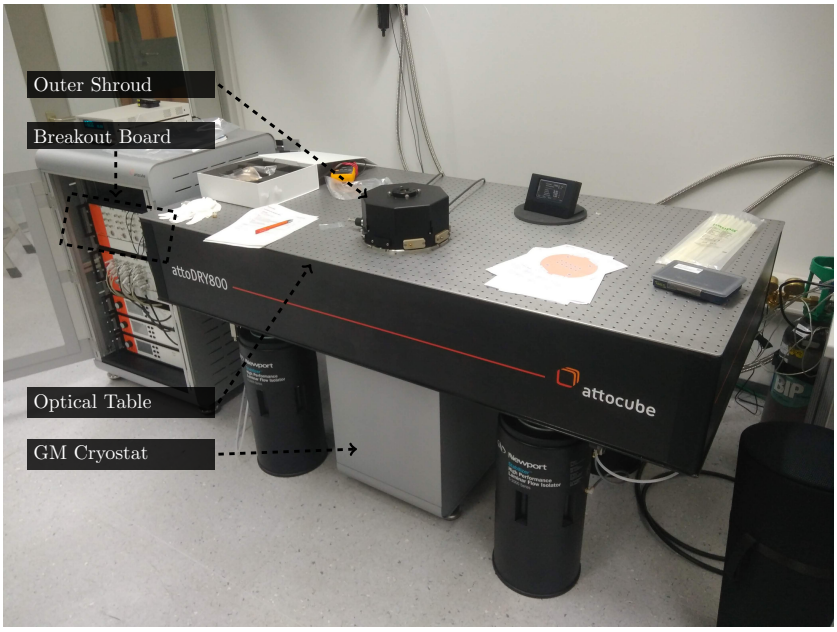
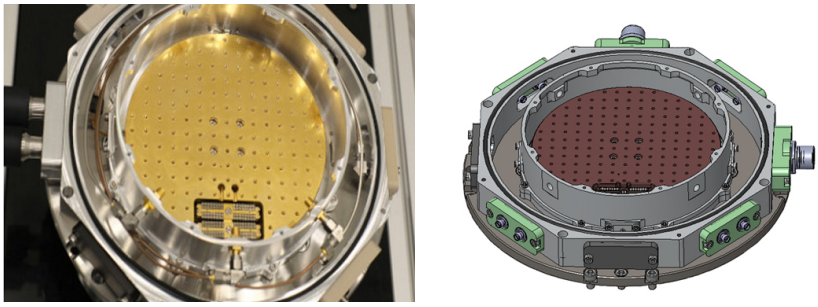


Figure 5.1: Photograph of the Attocube attoDRY800 cryostat.



(a) (b)

Figure 5.2: Photograph of the inside of the attocube setup (a) and CAD view of the shroud design (b) [56].

plate within the outer shroud. The cold plate and the shroud are mounted on an optical table to reduce vibrations. This allows for very accurate connection to the sample with needles. The GM cryo cooler is a closed loop system, which does not need any static helium supply or refill. The outer shroud isolates the interior from the outside and ensures a vacuum inside the cryostat.

Inside the outer shroud an intermediate shroud and temperature stage is located. This stage is cooled down to 40 K to reduce thermal leakage. The inner shroud can be seen in figure 5.2a. The golden metallic plate inside is the cold plate, which can be as cool as 4 K. Between the 40 K stage and the 4 K stage thermal anchors are employed that thermalize the cables down to 4 K. The setup allows the connection of up to 58 DC and 3 RF signals. The DC connection to room temperature is done by twisted pairs which are thermalized to the different temperature stages and connected to the breakout board at room temperature. The setup connects 3 semi-rigid coaxial lines. The coaxial lines loop around the shroud to reduce the thermal coupling to room temperature.

The measurement setup of circuits at cryogenic temperature contains parts inside and outside the cryostat. The DUT is placed inside the cryostat, while the signal sources and measurement equipment is typically located at room temperature with respect to the limited cooling power of the cryostat. In figure 5.3 the PCB mounted on the cold plate of the cryostat can be seen. The back plane of the PCB is a grounded plane using electroless nickel immersion gold to avoid oxidation. The back plane is connected with vias through out the whole PCB to increase the thermal conductivity. The PCB is mounted onto an copper plate inside the cryostat. The IC is mounted in the middle of the PCB and routed to DC connectors and RF SMP connectors. The RF signals are connected to the semi rigid coaxial cables. The DC connections of the chip are routed on the PCB to a DC connector. Additionally, capacitors are placed on the PCB to stabilize the supply voltages.

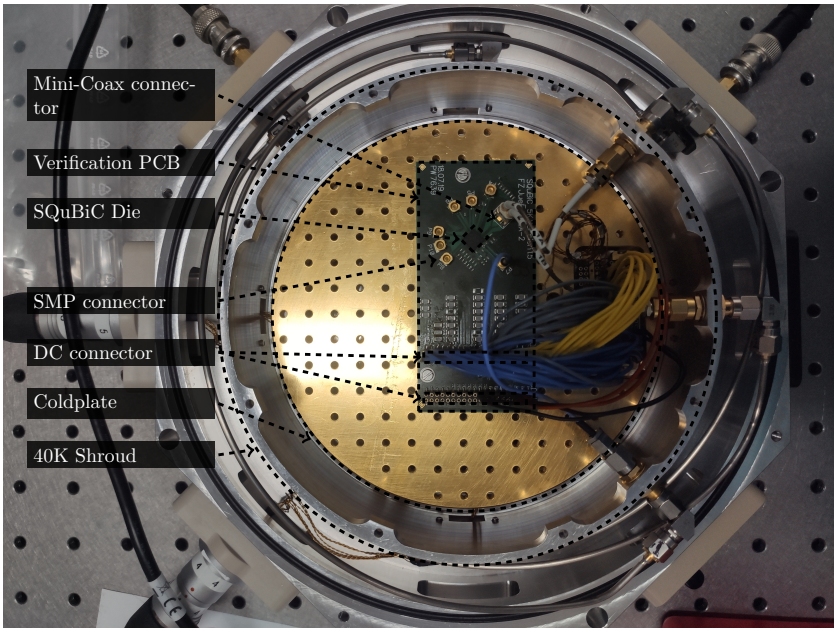


Figure 5.3: Top view into the shroud of the attocube cryostat.

5.2 Clock Buffer

The partitioning of the measurement setup for the clock buffer test case can be seen in figure 5.4. The input signal to the clock buffer is generated at room temperature by a Rohde & Schwarz SMC100A signal generator. This signal generator generates a high quality sine voltage which is connected via semi rigid coaxial cables to an SMP connector

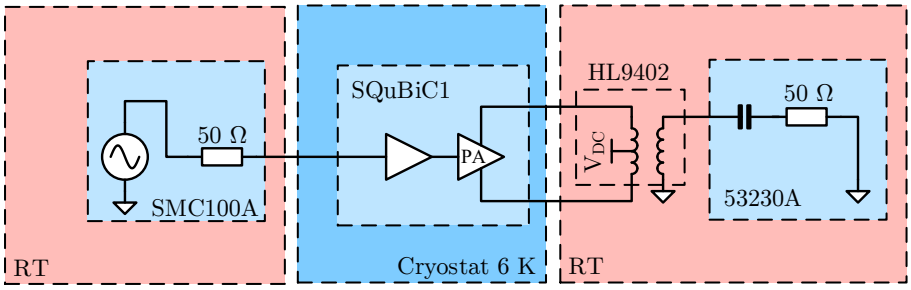


Figure 5.4: Partitioning of the measurement setup of the clock buffer.

Table 5.1: Typical parameters of the HL9402 Balun at 20 GHz.

Bandwidth	500 kHz - 20 GHz
Phase match	4-6°
Impedance	50 Ω, 2×50Ω

on the PCB.

The output of the power amplifier is connected to a mini-coax connector on the PCB which can be seen in figure 5.3. The balun of the amplifier is located at room temperature. The DC voltages are supplied by a Keysight N6705B DC power analyzer. The output is measured by a Keysight 53230A universal frequency counter. The output of the clock buffer is amplified by the pseudo differential amplifier discussed in figure 4.19. The Hyperlabs HL9402 Broadband balun acts as load. The key parameters of the balun are shown in table 5.1.

The amplitude of the input signal is set to a voltage of 100 mV. The frequency is swept between 100 MHz and 1.5 GHz. The signal is amplified by the clock buffer to a full scale voltage and fed through several digital clock buffer cells. Finally the signal is amplified by the same power amplifier structure which is also used for the measurement of the voltage controlled oscillator. In a first measurement the input of the clock buffer is not terminated to 50 Ω on the PCB or the IC.

In figure 5.5 the measured output frequency is plotted over the input frequency. The frequency of the output signal is shown for cryogenic and room temperature. Up to a

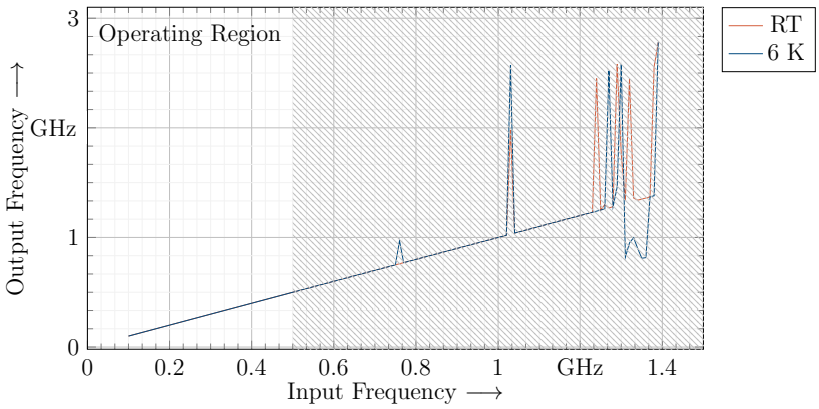


Figure 5.5: Measured output frequency of the clock buffer at room temperature and 6 K for a 100 mV input signal.

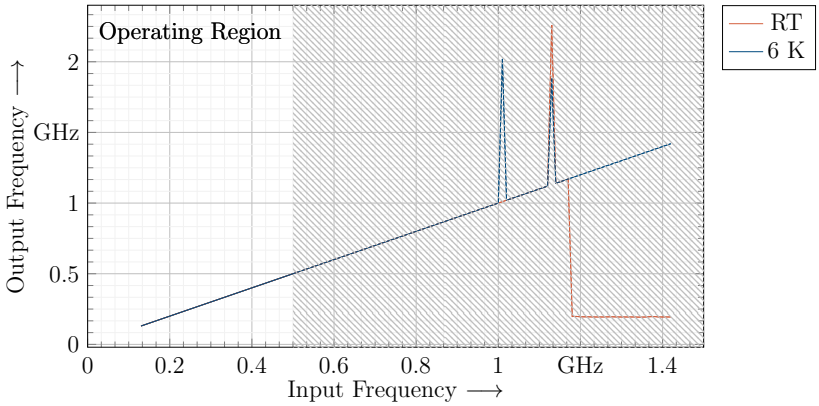


Figure 5.6: Measured frequency of the clock buffer terminated with 50 Ω.

frequency of 750 MHz the frequency of the output signal strictly follows the frequency of the input signal. For cryogenic temperature at around 760 MHz the frequency is not determined by the input signal but a disturbance can be observed. For an input frequency of 1.03 GHz and above 1.2 GHz, the measured output frequency does not follow the input neither at room temperature nor at cryogenic temperature. The disturbance in the characteristic are believed to be due to the bad input matching.

As next step the input to the clock buffer was terminated with a broadband 50 Ω termination resistance on the PCB to further investigate the clock buffer. The result of the measurement is shown in figure 5.6. The previously missing frequency point in the transfer characteristic shown in figure 5.5 at around 750 MHz at cryogenic temperature disappeared. The clock buffer is functional up to minimum frequencies as high as 1 GHz. The disturbance at 1 GHz disappears for room temperature measurements this increases the usable range of the buffer at room temperature but not at cryogenic temperature. Whether the functionality is limited by the output buffer or the clock buffer cannot certainly be determined.

Overall the buffer was intended for usage up to frequencies of 500 MHz, therefore the result shows the feasibility to operate the clock buffer in this frequency range in both cryogenic and at room temperature.

To examine the power consumption of the clock buffer the current into the DCO domain is measured with a Keysight 34465 digital multi-meter. Figure 5.7 shows the current consumption of the DCO domain over the frequency of the input signal. From 100 MHz to approximately 1 GHz the current consumption of the clock buffer increases linear with frequency for both cryogenic and room temperature. At around 1 GHz the room temperature curve starts to flatten until it drops for frequencies beyond 1.1 GHz. At

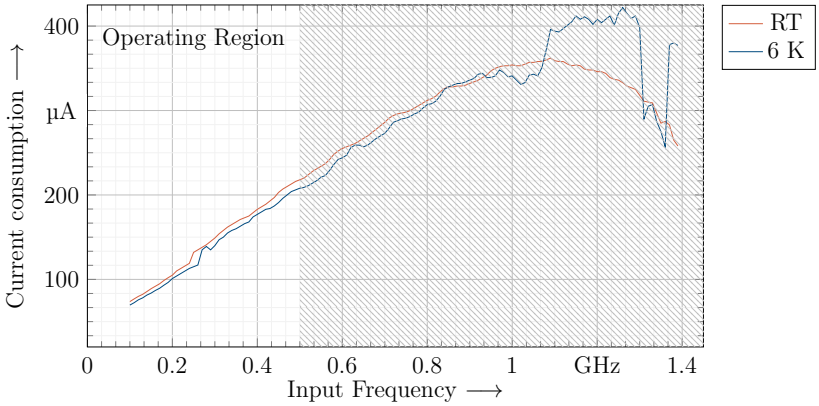


Figure 5.7: Current consumption of the clock buffer for different operating frequencies.

cryogenic temperature beyond 1 GHz the current consumption does not follow the input frequency in a predictable way. The current consumption lowers slightly at cryogenic temperature.

In the range from 100 MHz to approximately 1 GHz the curve follows the expected behavior of a linear relationship between current consumption and frequency. After that the curve flattens and even drops. This is due to the reduced gain of the clock buffer for high frequencies which is expected from the simulation shown in figure 4.6. Once a threshold has been exceeded the amplifier does not deliver a sufficient level for the next amplification stage to operate. After a certain point the output level is insufficient to exceed the threshold value of the following buffer stages. The amplifier itself is still consuming the considerable amount of power but the following stages do not operate anymore thus reducing the overall power consumption.

An important parameter for a clock signal is the duty cycle. An ideal clock buffer has a duty cycle of 50 % with corresponding input duty cycle. Due to mismatch between the NMOS and PMOS the switching point of the clock buffer is not centered in the middle of the supply. The measured clock buffer has shown a duty cycle of 43% at room temperature and 46% at cryogenic temperature respectively. The clock buffer implemented in the SQuBiC chip offers the possibility to bypass the AC coupling of the clock buffer and force the DC level of the clock buffer to a defined value. With this the dependency of the output duty cycle to the input common mode can be investigated. The DC common mode of a 250 MHz input signal is varied from 550 mV and the output duty cycle is measured. Figure 5.8 shows the duty cycle of the output signal over the input DC common mode. For an increasing DC level the duty cycle of the output signal decreases. The 50 % duty cycle should be reached at exactly 600 mV, but is in fact reached at approx. 650 mV.

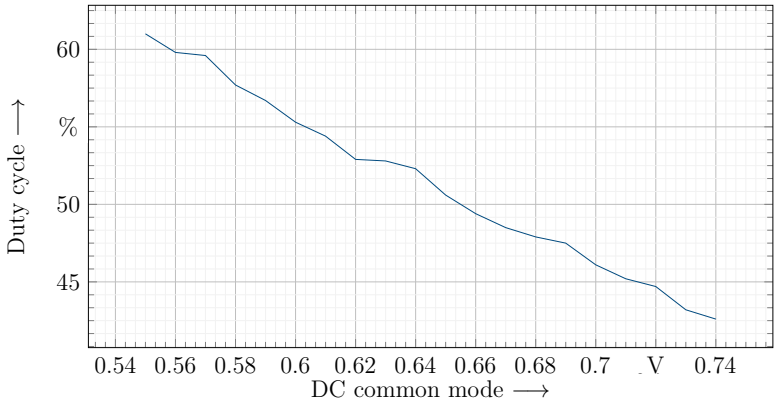


Figure 5.8: Measurement of the output duty cycle of the clock buffer for different input common mode.

Which means that the threshold of the clock buffer itself is not centered at 600 mV, but rather 650 mV, which is caused by the sizing of the NMOS and PMOS transistors.

5.3 Discussion of the Clockbuffer Measurement Results

The clock buffer is functional at cryogenic temperature. The buffer was designed for operation up to a frequency of 500 MHz but is still functional at frequencies as high as 700 MHz for both cryogenic and room temperature. A direct measurement of the gain of the clock buffer and characterization of the clock buffer itself was not possible since several digital buffer cells are used between the output of the clock buffer and the input of the output amplifier. The digital buffer cells function as very non linear high gain amplifier stages (limiter stages) which which will start clipping once a certain threshold is crossed. The low power consumption of approx. 200 µW at a frequency of 500 MHz allows for operation down to the lowest temperature stage without heating up the qubit. The used clock buffer has been demonstrated to be a suitable topology for operating at cryogenic temperature.

5.4 Voltage Controlled Oscillator

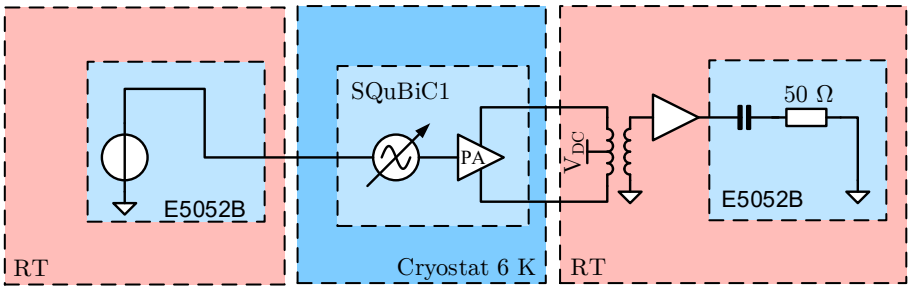


Figure 5.9: Partitioning of the VCO measurement setup.

The partitioning of the measurement setup for the VCO test case can be seen in figure 5.9. The output of the VCO is amplified by a single-ended Mini-Circuits ZX60-24-S+ amplifier which is used to amplify the unbalanced signal of the Balun. The parameters of this auxiliary measurement equipment are summarized in table 5.2.

The SQuBiC chip, containing the VCO and the first amplifier are located at cryogenic temperature. The balun, the Mini-Circuits amplifier and the signal source analyzer are at room temperature. The signal is analyzed by the Keysight E5052B signal source analyzer (SSA). In addition to the signal analysis the SSA provides low noise supply sources for the control voltage of the VCO on the chip. The control voltage of the VCO is swept while the other voltages are kept constant and the frequency and phase of the output signal are recorded and analyzed. Figure 5.10 shows the output frequency of the VCO over the applied control voltage from 0 V to 1.2 V. With increasing control voltage the output frequency of the VCO increases as expected from design.

The measured parameters are summarized in table 5.3. At cryogenic temperature the center frequency of the oscillator shifts from 18.12 GHz to 19.15 GHz, which is an increase of about 6%. The gain K_{VCO} of the VCO characteristic decreases from 425 MHz/V to 375 MHz/V at cryogenic temperature. For the calculation of the gain only the linear region of the characteristic was considered. The region in which the frequency of the

Table 5.2: Typical parameters of the used ZX 60-24-S+ amplifier at 20 GHz.

Gain	22.25 dB
Bandwidth	5 GHz - 20 GHz
NF	7 dB
Impedance	50 Ω, 50 Ω

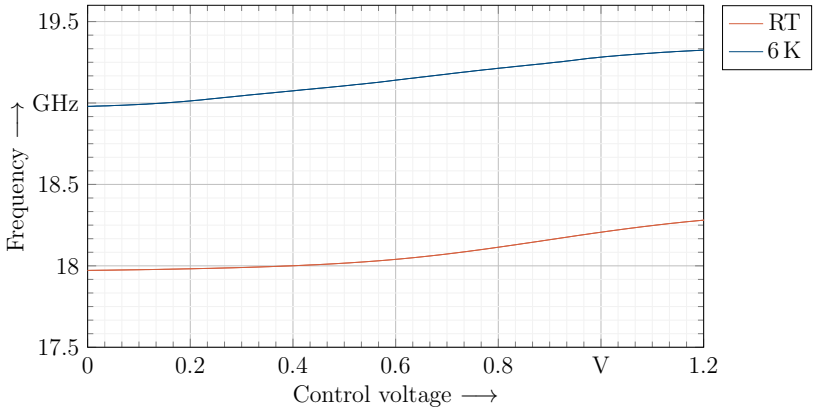


Figure 5.10: Output frequency of the VCO for cryogenic and room temperature.

VCO linearly follows the input voltage and the frequency span increases at cryogenic temperature although the gain decreases.

The current consumption of the VCO is measured over the control voltage of the VCO. Figure 5.11 shows the current consumption at the supply of the VCO over the input voltage of the oscillator. At room temperature the current consumption is about 7.7 mA, meanwhile the current consumption is about 5.8 mA at cryogenic temperature. The current consumption is independent of the control voltage since the operation point does not change for the relative small frequency shift.

In figure 5.12 the output power of the output amplifier is plotted over the control voltage.

At room temperature the curve is flat at a value of approximately -6 dBm until it reaches a cutoff point and drops off. For cryogenic temperature the output power is strongly depending on the output frequency. The fluctuating output level is caused by a mismatch between the output amplifier and the transmission line at cryogenic temperature. The overall baseline output power level at cryogenic temperature is around 0 dBm. The increased output level is caused by the increased g_m of the transistors of the output

Table 5.3: Summary of the measured parameters of the VCO.

Parameter	RT	6 K
K_{VCO}	425 MHz/V	375 MHz/V
Span	310 MHz	324 MHz
Center frequency	18.12 GHz	19.15 GHz

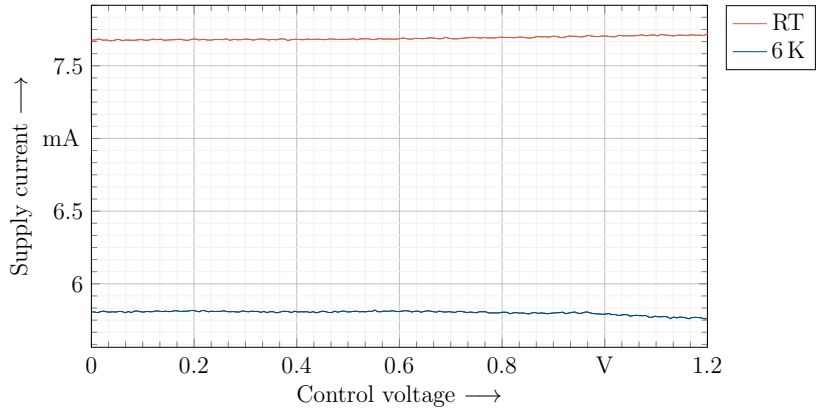


Figure 5.11: Current consumption of the VCO for different input voltage.

amplifier at cryogenic temperature [30]. Figure 5.13 shows the output power over the output frequency. The frequency shift for cryogenic temperature is clearly visible. The variation in the output power is periodic with frequency which results from varying reflection for different wavelength caused by the mismatched output driver.

The discrete frequency tuning of the VCO as described in figure 4.18 is verified by sweeping the control voltage and recording the output frequency for different configuration words. Increasing the values of the word D_{Tune} by one LSB increases the capacitance of the tank. The output frequency for each capacitance setting is shown in figure 5.14.

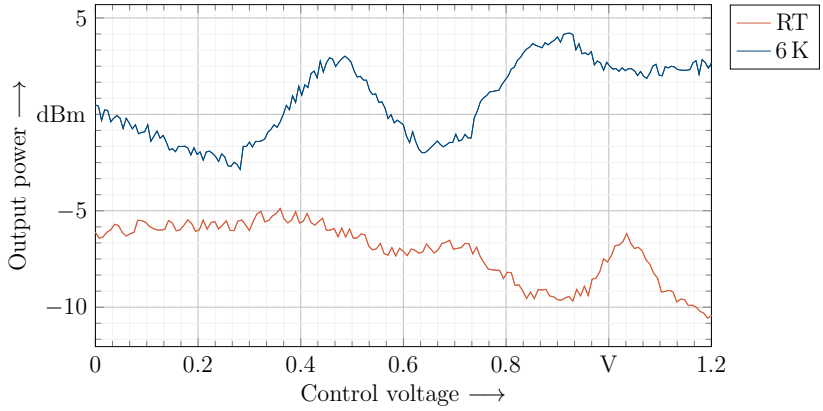


Figure 5.12: Output signal power of the VCO for different input voltage.

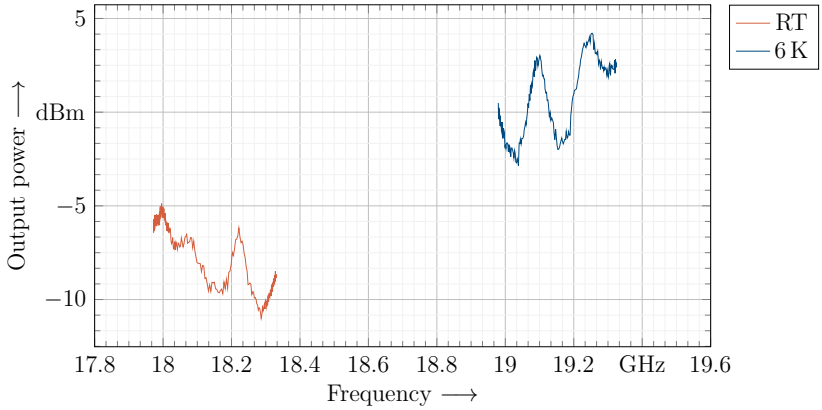


Figure 5.13: Output signal power of the VCO over the output frequency.

Increasing the word D_{Tune} leads to a shift of the overall characteristic to lower frequencies. For a D_{Tune} of 0 the frequency is the nominal as shown in figure 5.10. Each increase of the word shifts the characteristic down by approximately 500 MHz down to a frequency of 16 GHz. Ideally the different regions are overlapping in order to avoid zones in the characteristic in which the frequency cannot be controlled. However the regions are not overlapping which is caused by too small values in the extraction of the parasitic capacitance of the layout.

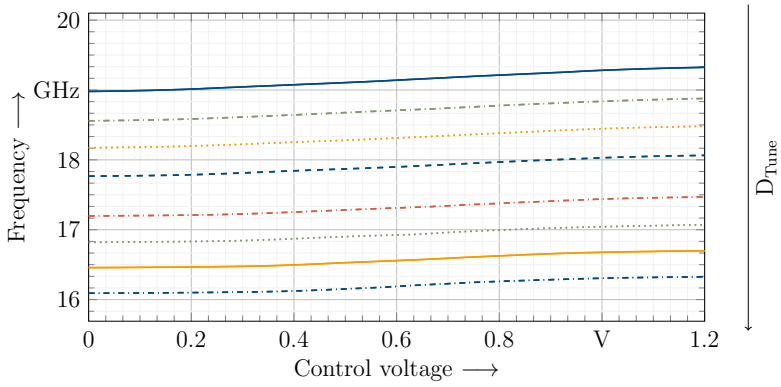


Figure 5.14: Frequency of the VCO for different digital setting of the tuning capacitance.

5.4.1 Phase Noise

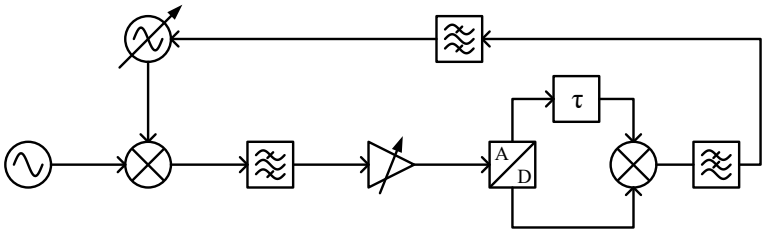


Figure 5.15: Schematic of phase noise measurement feedback loop used in the E5052B SSA signal Source Analyzer .

The phase noise measurement of a free running VCO is complicated. The VCO is very sensible to distortions on the control voltage. This does not allow directly measurement of the spectrum of the VCO and calculation of the power at given offset frequencies. Special equipment has to be employed that can supply very low noise voltages, very stable control voltage and is able to track frequency drifts of the carrier signal. The Keysight E5052B SSA Signal Source Analyzer accounts for the carrier frequency shift by actively regulating an intermediate frequency with a feedback configuration. Figure 5.15 shows the employed regulation scheme of the E5052B SSA signal Source Analyzer.

The carrier signal is mixed to a lower IF-frequency and band pass filtered fed it to an variable gain amplifier. It is converted to a digital signal which is mixed with a delayed

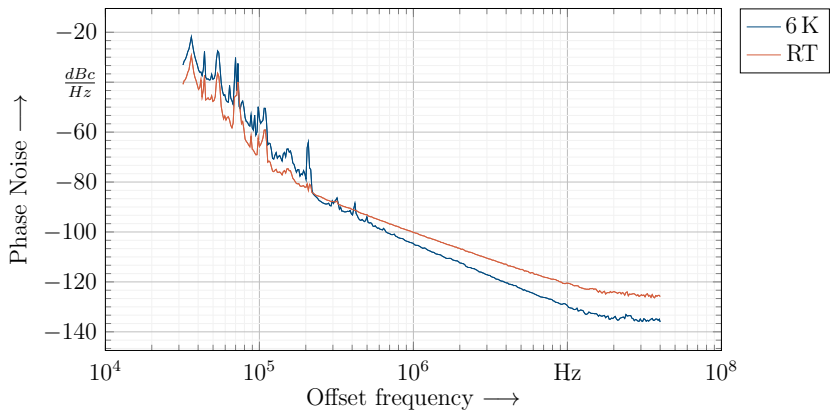


Figure 5.16: Phase noise measurement of the VCO at RT at a carrier frequency of 18.1 GHz and at 6 K at a carrier frequency of 19.2 GHz.

Table 5.4: Measured phase noise of the VCO at different offset frequencies and temperature.

Offset Frequency [kHz]	10	100	1000	10000	40000
Phase noise [dBc/Hz] @ 6 K	-37.74	-54.45	-104.63	-129.51	-136.05
Phase noise [dBc/Hz] @ 300 K	-43.80	-65.76	-100.17	-120.51	-125.88

version of the signal. The output of this mixer is zero when both signals are equal and phase shifted by exactly $\frac{\pi}{2}$. The output of the mixer is used to control the frequency of a voltage controlled oscillator which in turn provides the LO signal of the first mixer. This loop will regulate the frequency of the LO signal in such a way that the phase shift is always equal to $\frac{\pi}{2}$ and therefore will keep the IF frequency constant. In that way the power at an offset frequency can be calculated exactly even while the carrier frequency drifts. The change of the operation point of the VCO caused by the variation of the carrier frequency is very small. Therefore the influence of the operation point on the phase noise can be neglected.

With this measurement setup the phase noise of the implemented VCO was measured. In figure 5.16 the phase noise of the oscillator at room temperature at a carrier frequency of 18.1 GHz and at 6 K at a carrier frequency of 19.2 GHz is depicted.

The noise power relative to the power of the carrier is shown over the offset frequency of the carrier. The phase noise decreases with increasing offset frequency from the carrier. The observed phase noise can be separated into 2 distinct areas with different slopes. The far out phase noise follows a −20 dB/decade trajectory. The close in phase noise follows a decline of −30 dB/decade. For cryogenic temperature the far out phase noise is as low as -136 dBc/Hz decreases and is lower than its room temperature counter part at -125 dBc/Hz. The close in phase noise on the other hand increases at lower temperature as shown in table 5.4.

5.5 Discussion of the VCO Measurement Results

The voltage controlled oscillator is functional at cryogenic temperature. It was possible to generate a stable output at a center frequency of 18.12 GHz at room temperature and 19.16 GHz at cryogenic temperature, respectively. The center frequency of the oscillator shifted by around 6% to higher frequencies. The far out phase noise decreased due to the reduced thermal noise at lower temperature. Meanwhile the close in phase noise is increased, which is caused by the increased of $\frac{1}{f}$ in circuits at cryogenic temperature [57]. The output power level increased over the whole frequency range by about 6 dB but become less stable over frequency. The operation of a VCO is suitable at cryogenic temperature but its comparable high power consumption of approx. 6 mW prohibits an

implementation on the same temperature stage as the qubit itself. An implementation on a higher temperature stage like the 4 K stage can be still beneficial for the implementation of integrated qubit control with other partitioning and multiplexing schemes as discussed in chapter 2.5.5 .

5.6 Digitally Controlled Oscillator

The partitioning of the measurement setup for the DCO test case can be seen in figure 5.17. The digital input of the DCO is controlled by the National Instruments USB-8452 which is located at room temperature. The chip itself containing the DCO is located at cryogenic temperature. The output of the DCO can be redirected to the input of the amplifier which is also used for the measurement of the VCO. The balun of the amplifier is located at room temperature and the output signal is measured with an 50 Ω AC-coupled input of a Keysight 53230A frequency counter.

The oscillation frequency of the DCO was measured at room temperature. Different bias currents were configured and for each bias current the input word is swept from 0 to 255. The bias current is changed between 10 µA and 50 µA. Figure 5.18 shows the measured output frequency of the DCO over the digital input word of the oscillator. Increasing the value of the input word of the oscillator directly increases the output frequency of the oscillator. Increasing the bias current shift the frequency of the overall trajectory. Increasing the bias current beyond 50 µA the frequency settles at approximately 600 MHz. An increased bias current leads to reduced linearity in the characteristic.

At room temperature the DCO acts like expected. The upper limit of 600 MHz of the oscillator is set by the parasitics and the speed of the transistors instead of the current sources. The increased non-linearity is due to the bias current mirrors leaving the saturation regime.

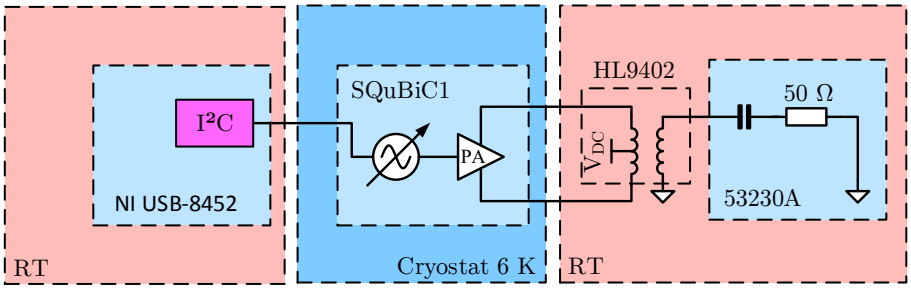


Figure 5.17: Partitioning of the DCO measurement setup.

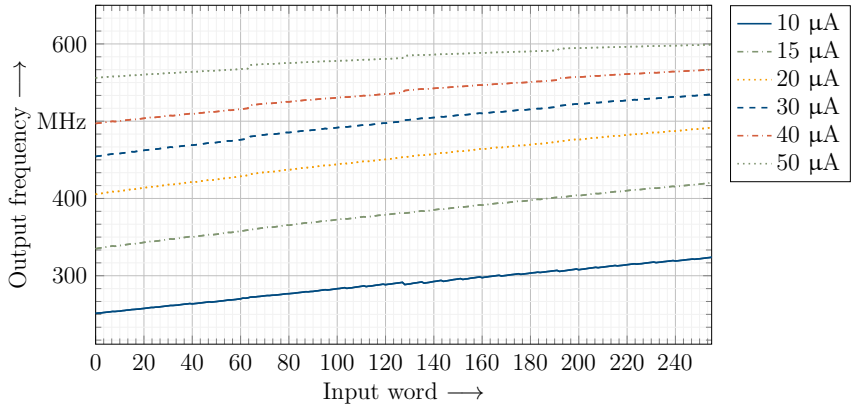


Figure 5.18: Measurement of the output frequency of the DCO for different bias currents at room temperature.

At cryogenic temperature the output frequency is increasing with the digital input word but no longer following it. It is separated into 4 different constant regimes. The reason for this behavior is in the bias circuitry of the DCO, which is discussed in chapter 4.2.2. The implemented biasing, shown in figure 4.12, employs cascodes for the generation of the bias current used to limit the current of the oscillator. The increased threshold at cryogenic temperature is believed to cause the transistors in the bias circuit leaving the desired operation point. The transistors drop into the sub-threshold regime due to the increased subthreshold slope at cryogenic temperature. This turns the transistor effectively off. Only the current controlled by the most significant bits are still working correctly. Because only these do not employ cascode transistors.

The supply voltage of the DCO is varied to investigate further the behavior and to confirm the suspicion that the reason for this behavior is the increased threshold voltage. The digital input word is swept from 0 to 255 for different supply voltage between 1 V and 1.5 V. The output frequency of the DCO for the different supply voltages is shown in figure 5.19. For low supply voltages the behavior of the curve is as previously discussed. An increase in the supply voltage shifts the center frequency of the oscillator. For higher supply voltages the input regains control over the behaviour of the oscillator and the steps of the characteristic start to bend towards the next level. Once the supply increases beyond approx. 1.4 V the behavior resembles to the previously observed behavior at room temperature. For the cryogenic measurement of the DCO with varying bias current the supply voltage is set to 1.4 V. The input words of the DCO are swept between 0 and 255 and the bias current is swept from 10 µA up to 60 µA. The measurement is depicted in figure 5.20.

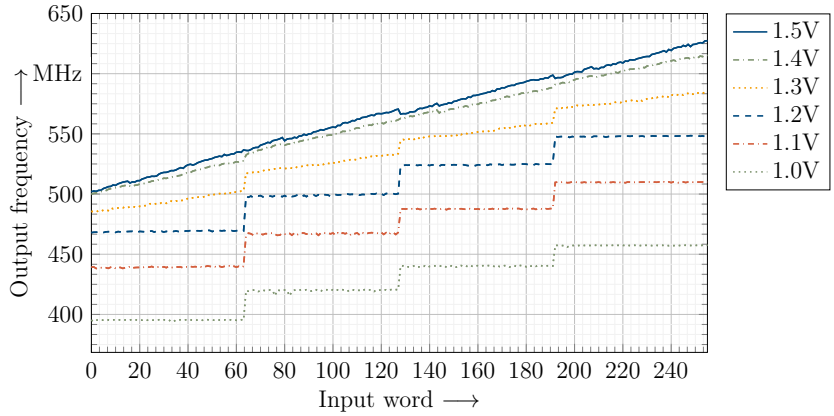


Figure 5.19: Measurement of the output frequency of the DCO for different supply voltages at cryogenic temperature for a bias current of 20 µA.

The oscillation frequency increases with increasing bias current. Similar to the room temperature result for high bias current the characteristic limits at a certain frequency.The maximum frequency of the oscillator is around 1 GHz at cryogenic temperature. For higher currents the discussed steps in the trajectory are visible again. For a bias current of 10 µA the oscillation frequency does not linearly increase with the input word. This region is already in the sub threshold regime which is much steeper at cryogenic temperatures and therefore more drastically limiting the current.

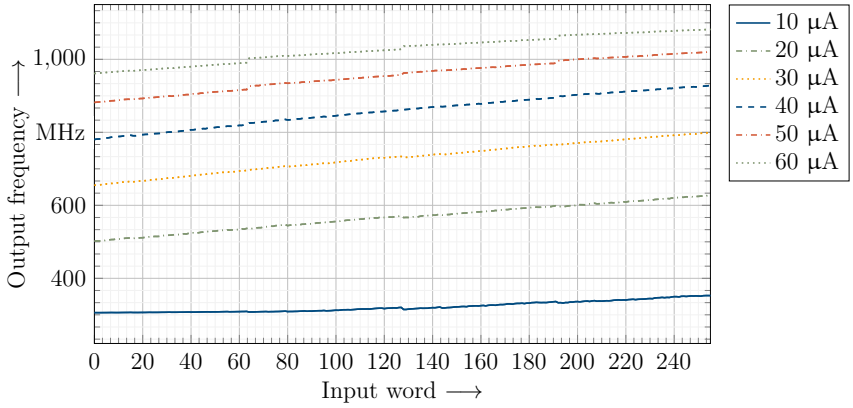


Figure 5.20: Measurement of the output frequency of the DCO for different bias currents at room temperature.

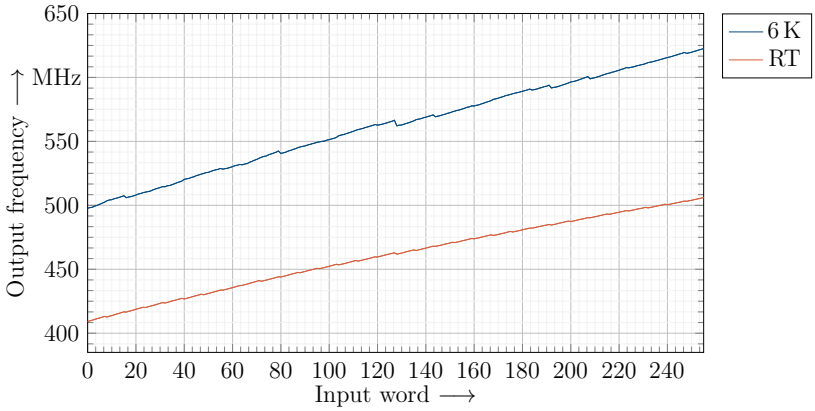


Figure 5.21: Measurement of the output frequency of the DCO with a bias current of 20 µA and a supply voltage of 1.4 V at cryogenic and room temperature.

In figure 5.21 the output frequency of the DCO over the input word is shown for a bias current of 20 µA and the same supply voltage. The supply voltage has been set to 1.4 V accordingly to allow for correct operation of the DCO at cryogenic temperature. The frequency of both the DCO at room temperature and cryogenic temperature increase with increasing input word. At room temperature is centered around approx. 450 MHz, while the frequency of the DCO at 6 K is shifted by approx. 100 MHz. In addition to that the characteristic of the DCO at 6 K shows increased non monotonic behavior and frequency jumps. These frequency jumps are caused by the increased mismatch of the bias current sources at cryogenic temperature [58].

5.7 Discussion of the DCO Measurement Results

The digital controlled oscillator is functional at cryogenic temperature but in order to fully operate the DCO at cryogenic temperature the supply voltage of the DCO domain has to be increased. The shift in threshold voltage made the bias circuit non functional by driving the cascode current mirrors out of saturation and into sub threshold regime. After increasing the supply voltage the full tuning range could be used again. The center frequency of the oscillator shifted to higher frequencies for lower temperature. The maximum oscillation frequency which can be achieved by an increased bias current shifted from 600 MHz at room temperature up to more than 1000 MHz. Although being fully functional an increased supply voltage leads to an increased power consumption. The frequency generation in the required region of 500 MHz can be achieved for both cryogenic and room temperature.

5.8 Pulse Digital-to-Analog Converter

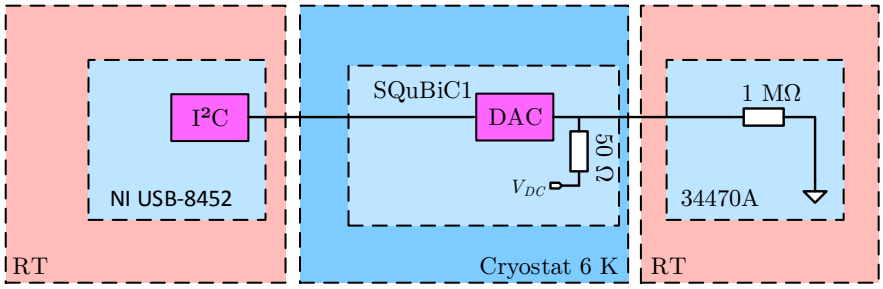


Figure 5.22: Partitioning of the DAC measurement setup.

The pulse DAC is measured at room temperature and at cryogenic temperature. The partitioning of the measurement setup for the DAC test case can be seen in figure 5.4. The DAC is terminated locally with a configurable termination load and measured by a Keysight 34470A high precision multimeter which employs an input resistance of more than 1MΩ.

Figure 5.23 shows the characteristic of the DAC at room temperature. The output voltage of the DAC is plotted over the control word. The output voltage starts at a voltage of 1.180 V and decreases with increasing input word until a value of 1.164 V spanning a range of 16 mV. The output follows the input linearly without noticeable non monotonic behavior.

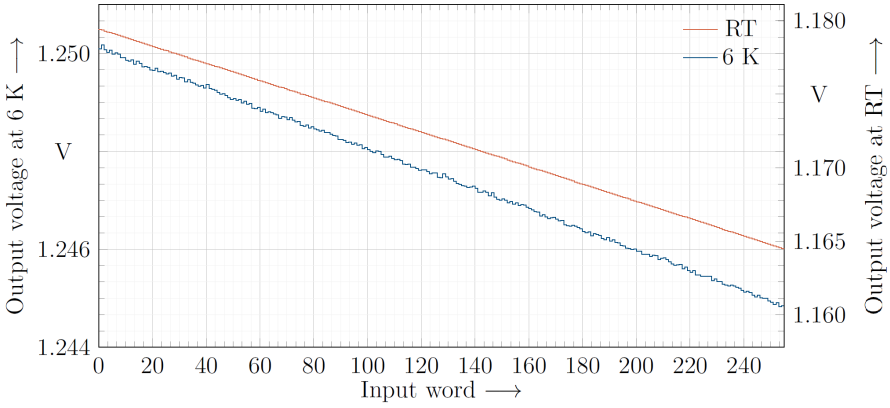
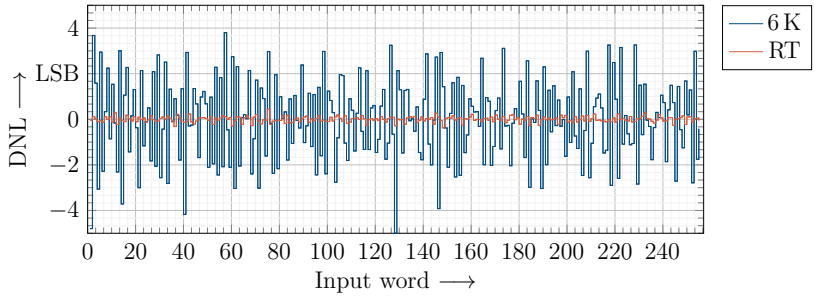
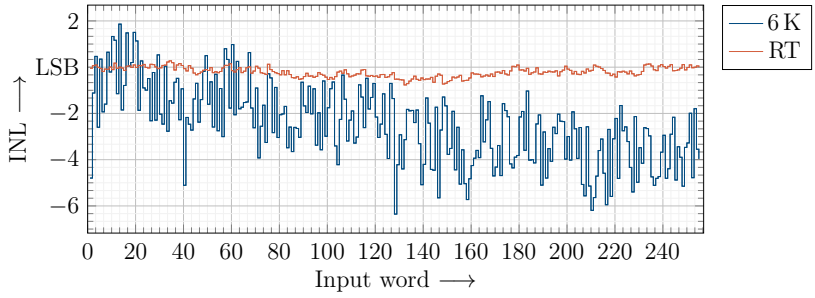


Figure 5.23: DC measurement of the DAC at room temperature and cryogenic temperature.



(a)



(b)

Figure 5.24: Measured DNL (a) and INL (b) of the DAC.

For comparison the DAC characteristic at cryogenic temperature is also shown in Figure 5.23. The output voltage starts at a voltage of 1.250 V and ends at a voltage of 1.245 V, resulting in a range of approx. 5 mV. The output of the DAC decreases with an increasing control word. At cryogenic temperature the DAC shows clearly visible non monotonic behavior in the characteristic.

Figure 5.24a shows the differential non linearity over the input word of the DAC. At room temperature small values well below 0.5 are observed. At cryogenic temperature the DNL increases drastically at up to values of 4. Figure 5.24b shows the integral non linearity over the DAC input word for cryogenic and room temperature. At room temperature the INL is very stable and close to zero. At cryogenic temperature the INL is heavily fluctuating and shows values up to 6. The reason behind the drastically increased INL and DNL is the worse matching behavior at cryogenic temperature. The mismatch of the current sources between each other leads to an increased deviation from the ideal value.

The problem of increased mismatch at cryogenic temperature is well known from litera-

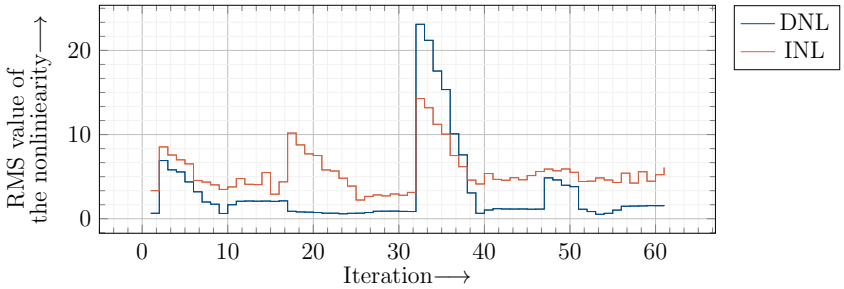


Figure 5.25: RMS value of the INL and DNL after each calibration step.

ture and was anticipated in the design of the chip. Each current source of the DAC has a smaller DAC which employs different configuration levels to counter the mismatch. Each measurement of the DNL takes roughly a time of 10 minutes, therefore severely limiting the number of measurements that can be done. Due to the high amount of possible calibration settings the binary part of the DAC was optimized first. The calibration is shown in figure 5.27. Starting with changing the MSB, the value of the calibration current is set and the whole DAC characteristic is measured. From the characteristic the INL is calculated. After that the next value for the calibration current is set until all possible values for the correction were set. The best root mean square value of the INL is extracted and the setting at which it was found is saved. With the calibration setting of the previous stage the procedure was repeated for the next stage until the LSB stage is reached.

Figure 5.25 shows the root mean square level of different DNL and INL curves for different calibration settings used in the binary part of DAC. A very low value responds to a very small overall absolute value of the linearity parameters.

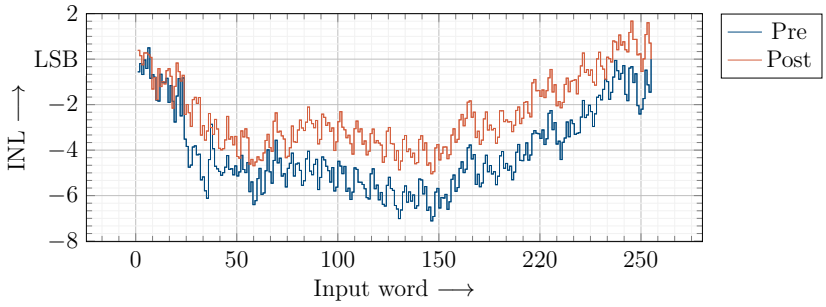


Figure 5.26: INL of the DAC before and after the calibration.

Changing the calibration DAC value directly affects the rms value of the DNL and INL, respectively. For each calibrated binary current source there is a local minimum and a local maximum leading to small repeating ripples in the root mean square values of the DNL and INL characteristic, with the maximum located at the LSB calibration DAC.

The measured INL of the DAC before and after the calibration procedure is shown in figure 5.26. The non calibrated INL characteristic reaches absolute values as bad as 6, whereas the calibrated INL characteristic is on average 1 LSB above the performance of the uncalibrated one.

The INL improves, but is in the end still worse than the previous discussed room temperature results. This is due to several issues. Firstly, the variation of the individual current sources at cryogenic temperature were unknown due to the absence of statistical

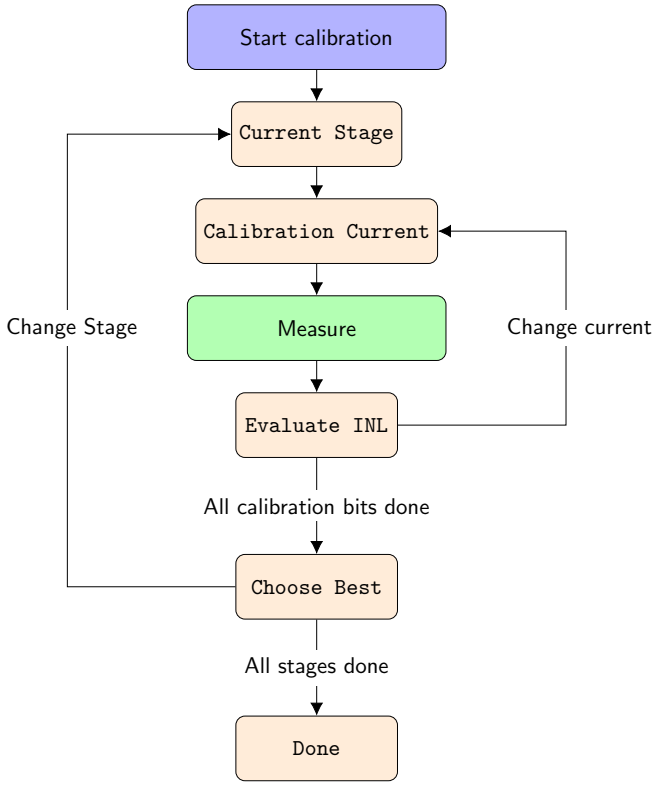


Figure 5.27: Flow chart of the pulse-DAC calibration process.

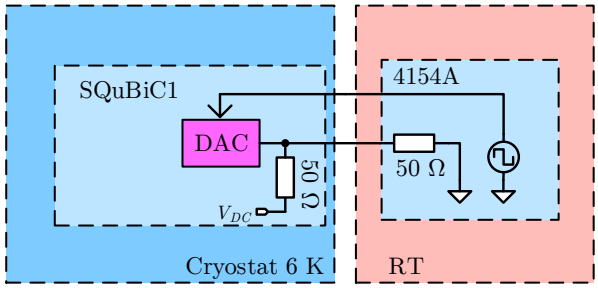


Figure 5.28: Measurement setup for transient measurement of the DAC.

cryogenic models. Therefore, they were assumed way worse, and the quantization levels of the individual DACs to calibrate the sources are chosen not small enough to reduces the error of the mismatch sufficiently.

Secondly, a rather simplistic calibration algorithm was used due to the limitation of the measurement and time constraints. Due to a missing on-chip calibration scheme the evaluation of the individual DACs values is very slow and single errors which occur over the course of one measurement, which is in the region of 10 minutes, can discard an otherwise optimal value for the calibration and a sub-optimal value is chosen for all following stages of the algorithm.

The transient measurement setup of the DAC is shown in figure 5.28. The measurement is done with a Keysight 4154A oscilloscope. The Keysight 4154A oscilloscope has a signal bandwidth of 1.5 GHz and 8 bit resolution. The internal wave generator of the oscilloscope is used to control the trigger input of the SQuBiC chip and the oscilloscope. The output of the DAC is measured by the oscilloscope.

A direct measurement of the transient response of the DAC is very hard to achieve due to two limitations on the measurement setup. The first is the very small full scale amplitude of approximately 10 mV and the very long cables that lead to high parasitic capacitance. The parasitic capacitance forms a low pass for the signal, therefore permitting measurement of fast signals from the DAC. To enable verification of the functionality of the digital control circuitry the frequency of the signal is reduced. The signal must be able to pass through the parasitic low pass formed by the capacitance of the wiring and the input capacitance of the oscilloscope. The output voltage range of the signal is increased in order to clearly differentiate it from the background noise and quantization of the oscilloscope.

For the transient measurement a predefined pattern is programmed in the memory shift register combination described in chapter 4.3.6. In figure 5.29 the result of a transient measurement with increased voltage amplitude and decreased operating frequency is

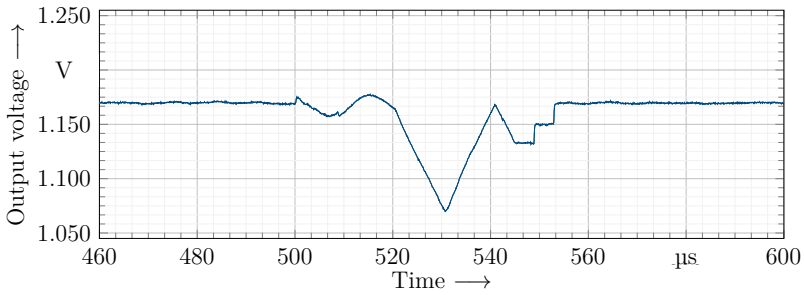


Figure 5.29: Transient DAC.

shown. The measurement shows the output voltage of the DAC over time. It starts with a idle part until the oscilloscope sends the trigger signal. A sinusoidal ringing is observable before the actual pulse sequence started. This is caused by the cross-talk of the lines when the full scale trigger signal is send to the input of the chip. The value of the DAC slowly decreases in a ramp from 1.17 V down to 1.08 V. The value increases back with a ramp up to the starting 1.17 V. This is followed by a smaller slope and afterwards some idle times and steps.

One of the key concerns when operating electronics in close vicinity of qubits is the power consumption. To ensure proper operation of the qubits the temperature of the qubit has to be as low as possible. The cooling power of modern dilution refrigerators are very limited strictly restricting allowed power consumption of the circuitry.

The power needed for operation of the DAC at room temperature and cryogenic temperature is shown in table 5.5. The power consumption of the digital part of the pulse DAC decreases by about 7 % and roughly 20 µW in total which is due to an increased threshold voltage and decreased sub-threshold currents which leads to drastically reduced leakage current. The power used within the clock buffer reduces from 244 µW to 195 µW. This is about 20 % decrease in power consumption. Finally the analog power consumption of the DAC is drastically reduced from 418 µW to 253 µW which is almost a reduction of 40 %. The analog power consumption consists of two parts. The first is the internal current drawn from the analog supply and used in generating the bias currents for the DAC as well as operating analog circuitry inside the DAC. The second part is the DAC current

Table 5.5: Power consumption of the different supplies operating the Pulse DAC.

Temperature	Digital	Clock Buffer	Analog
RT	287 µW	244 µW	418 µW
6 K	267 µW	195 µW	253 µW

Table 5.6: Comparison between different cryogenic DACs.

	[47]	[48]	[49]	This work
Temperature [K]	93.15	93.15	4.2K	6K
Technology	BiCMOS	BiCMOS	SOS-CMOS	CMOS
Feature size	0.5 µm	0.5 µm	0.5 µm	65 nm
Architecture	CS	R-2R	CS	CS
Resolution [bit]	12	8	10	8
Output range	520 mV	32 µA	520 mV	10 mV
Supply Voltage [V]	3.3	3.3	3	1.2
Area [mm^2]	6.3	0.2475	<1	0.1452
Sample Rate [MS/s]	80	10	100	250
Power [mW]	39.6	3	32.18	0.715

flowing from a reference voltage through a termination resistance to create a voltage output. Although the analog power seems to be drastically reduced this is conceiving since the output range of the DAC is drastically decreased. The decrease can be seen in figure **??** and a larger output range requires a larger power consumption.

A comparison of this DAC to other DACs used for cryogenic application is shown in 5.6. A direct comparison is complicated due to the limited amount of DACs for cryogenic operation. Many cryogenic DACs are used in various different application fields with different requirements. Not many DACs were published for the transient operation at temperature as low as 6 K.

Many of the published DACs are not done in modern state of the art CMOS technology but rather in a special technology such as BiCMOS or Silicon on Saphire (SOS) CMOS with drastically increased feature size. Many DACs used for transient cryogenic operation are based on a current steering topology. The DACs consume a considerable amount of power compared to the one in this work. This is due to several differences. Firstly, the reduced output range directly reduces the analog power consumption of the DAC. Secondly, the more mature technologies also employ a higher supply voltage which directly translates to an increased power consumption. The footprint of the compared DACs is bigger than the one in this work mainly because the increased feature size directly affects the size of the circuits especially for digital circuits.

5.9 Discussion of the DAC Measurement Results

The current steering DAC implemented is fully operational at both cryogenic and room temperature. Due to the increased mismatch between the transistors the DNL and the INL of the converter degrade. It was possible to partly restore the characteristic by means of a calibration. The calibration itself is very time consuming and insufficient to account for all the inaccuracies. The reasons for this are the absence of statistical cryogenic models during the design phase and the simple structure of the calibration algorithm used as well as the manual calibration outside of the ASIC. The power consumption of the DAC itself is higher than anticipated mainly due to underestimating the power consumption of the digital part and the clock buffer. The combined power consumption of one DAC, the clock buffer and the digital part is 715 µW which is still within the required value of 1 mW for the operation in a cryostat. The operation of multiple DACs will not require multiple clock buffer. On the other hand the additional power from each DAC and the digital part required will exceed the cooling budget of the lowest stage therefore limiting the operation together with qubits.

Chapter 6

Summary, Conclusion and Outlook

6.1 Summary

In this work, the basics of quantum mechanics and quantum computing have been explained on a level needed for engineering close to qubit circuit solutions considering the challenging cryogenic environment conditions. The requirements for an integrated control chip have been derived from theory, models and optimization. In particular the manipulation of the qubit information was in the focus of this work. The control for two different qubits was investigated. The GaAs quantum dot can be controlled by a DAC, which used a slope control suitable for scalable control electronics. The SiGe qubit requires a control by setting the phase of a characteristic microwave pulse at approximately 20GHz. Simulation, implementation and measurement of a pulse digital-to-analog converter for qubit operation, a digital controlled oscillator with clock buffers and a voltage controlled LC-oscillator for on chip frequency generation were shown at cryogenic and room temperatures.

The digital controlled oscillator is based on a current starving ring oscillator structure. It is functional at cryogenic temperatures although showing a drastically reduced tuning range. The increased transistor threshold voltage leads to unsaturated transistors in the bias current generator circuitry. The tuning range was restored to the desired tuning range by increasing the supply voltage. The changes in frequency and power consumption between room temperature and cryogenic temperature were discussed.

The voltage controlled oscillator was shown to be operational at temperatures as low as 6 K. The tuning range and frequency behavior are compared and the impact of the reduced temperature on the output power level and the current consumption were investigated.

The pulse-DAC is based on a current steering topology and its DC characteristics for both cryogenic operation and room temperature have been shown. At cryogenic temperatures INL and DNL show decreased performance which could partly restored by making use

of a calibration scheme. The power consumption of the DAC and the digital part were evaluated.

All circuits were verified to be functional at room temperature and cryogenic temperatures although with partly significantly changed characteristics.

6.2 Outlook

The increased threshold values in the transistors at cryogenic temperatures were known, but underestimated. The effect could be circumvented by increasing the supply voltage in certain parts of the circuitry such as the bias current generation of the DCO. Although working, this approach leads to increased power consumption. High output resistance, low head room current mirrors have to be investigated and evaluated for the operation in cryogenic environment.

The proposed voltage controlled oscillator is the foundation for the implementation of a cryogenic phase locked loop for frequency synthesis.

The power consumption of the digital part of the DAC is unsuitable for the operation of a high number of output channels or DACs in parallel, therefore limiting the possible number of qubits which can be operated. In order to overcome the increased mismatch, which leads to decreased DNL and INL performance at cryogenic temperatures an self-acting digital calibration scheme can be employed which improves the manual calibration to an automatic procedure.

For a final verification step the SQuBiC chip will be placed on a common interposer and wire bonded to an actual qubit chip. A setup planned to show the DC biasing of a GaAs qubit is shown in figure 6.1. It shows one SQuBiC chip which is placed on a interposer together with a chip containing 4 single qubits including sensing dots. The interposer is connected to PCB and mounted onto a sample holder which can be placed onto the lowest temperature stage of a dilution refrigerator.

The investigation of novel power saving digital circuitry and design methodology benefiting from the decreased leakage currents and increased sub-threshold slope is necessary. Shifting internal memory from register based memory architectures to static random-access memory (SRAM) would further decrease the power consumption of digital circuitry. Therefore, a SRAM array that was already designed and implemented for a different project will be tested at cryogenic temperature and its functionality will be evaluated.

The usage of modern state of the art special CMOS technologies such as Silicon on insulator (SOI) allows for the exploration of their unique features to counteract cryogenic effects. For example the variable back gate control of a SOI-CMOS process may allow circumventing the threshold shift of the transistors for cryogenic temperatures.

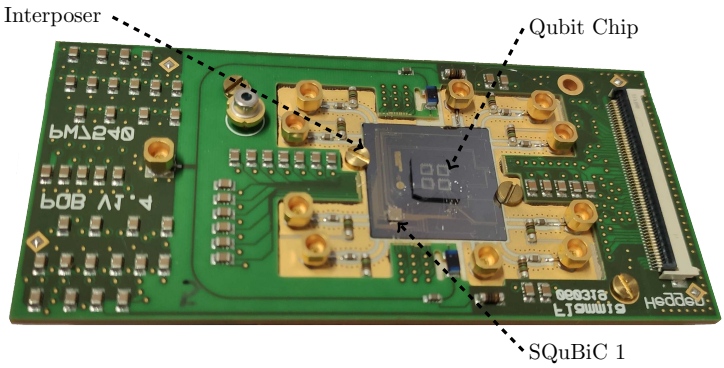


Figure 6.1: PCB with qubit chip and control chip on the same interposer.

6.3 Conclusion

This work has shown the basic operation of integrated CMOS circuitry at cryogenic temperatures. The feasibility of bulk CMOS circuits for qubit control has been shown. However, a lot investigations have still to be done to overcome the challenges when incorporating standard CMOS technology for qubit control.

The main challenges for the operation of CMOS at cryogenic temperatures are the absence of valid models, the increased mismatch of transistors and the increased 1/f noise. The operation of qubits in a cryostat further limit the available power for the circuitry as well setting requirements for the die size for future scaling.

Overall, this work shows the potential of cryogenic CMOS for operation in close vicinity to the qubit, although certain challenges still have to be solved. The circuits developed in this work can be the foundation of a cryogenic control system for qubit control which can be used for the implementation of more complex system that allows the system integration of qubits and electronics.

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