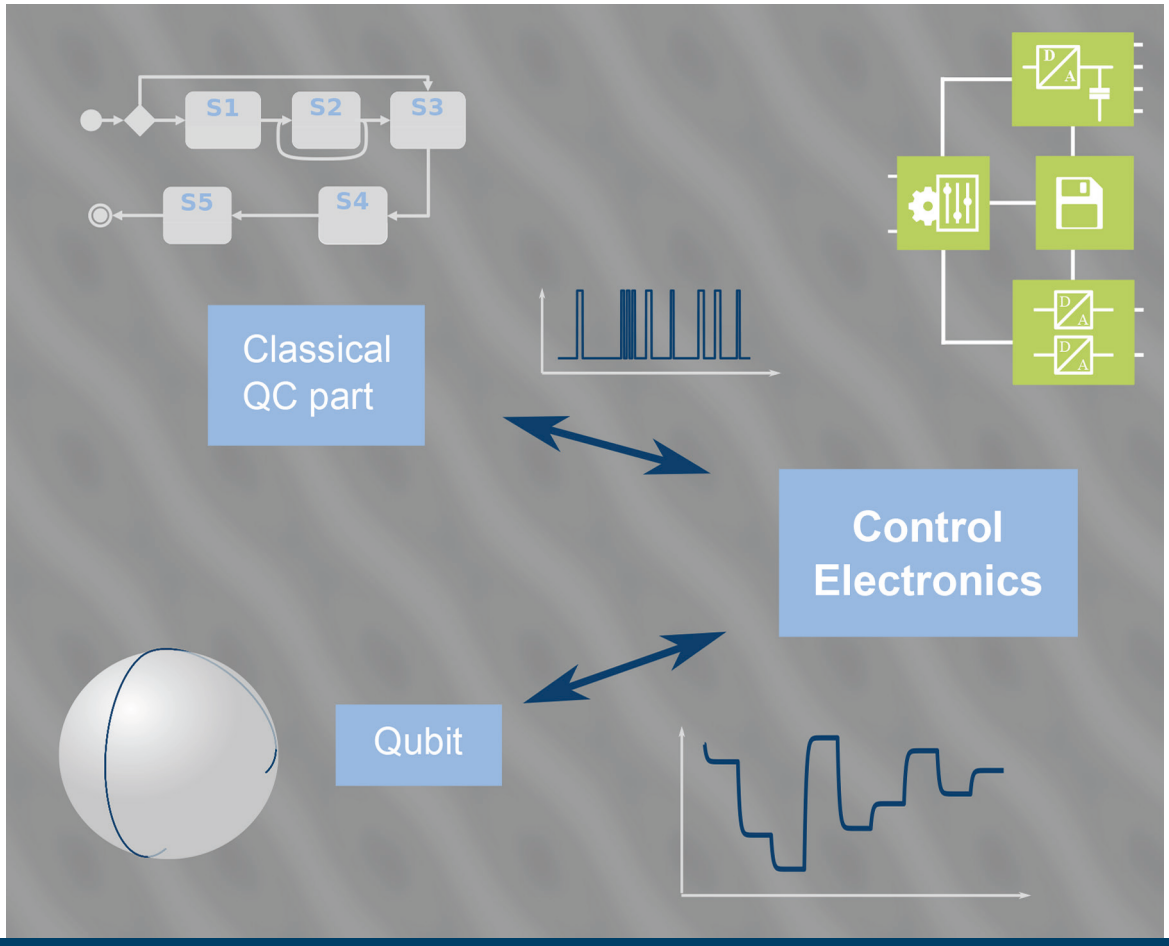


# Scalable Control Electronics for a Spin Based Quantum Computer

Lotte Geck

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# Abstract

In the last years, the topic of quantum computing has received increased attention and a rising number of universities, research institutes and companies are exploring it. One reason for that is the great potential to solve some of today's practically intractable mathematical problems. The superiority of quantum computers is based on quantum mechanical effects in the smallest computation unit, the quantum bit (qubit). The operation and readout of these qubits is complex and very sensitive to noise and other disturbances. For a universal, programmable quantum computer qubit numbers in the order of millions need to be operated together which is a great scale up from today's 53 qubits.

For a qubit several different implementations exist and one promising candidate type are qubits made out of semiconductor materials. They typically store information in the spin of localized charge carriers. The manipulation of that spin and the corresponding computation is possible through electrical signals. However, due to the operation requirements of the qubit the electronic-qubit interface is very complex and current control methods are not feasible for large qubit numbers.

The goal of this work is a systematic study of the scalability of integrated control electronics based on existing, industrial complementary metal-oxide-semiconductor (CMOS) technology. Included in this goal is also the identification of potential hindrances to the scalability and necessary subsequent research and the interaction of the electronics with other parts of the quantum computer. In this work, the so called gallium-arsenide S-T qubit is used as a reference and most of the technology parameter values take a 65 nm CMOS process into account.

In a first step, a control concept for the qubits was developed and its scalability judged on the estimated area and power consumption of the integrated circuit. Next to the 65 nm technology parameter values, also extrapolated values for smaller nodes were used. Results show that the main hindrance to scalability is the power consumption of the electronics and in order to scale up to millions of qubits technology advancements are necessary, among others. In the more near term application technologies with low digital supply voltage are promising.

The second step was to derive a behavioral model not only of the electronic control concept but the interface to the rest of the quantum computer and the qubit, as well. Simulations of the complete system show that the electronics concept works as designed and qubit control is possible. The interaction of the different units also highlights that processes critical to the scalability are for example the measurement and the adaption of pulse sequences to each individual qubit.

In order to test the effect of imperfect electronics on the operation a qubit, several exemplary qubit gates and the corresponding voltage pulse sequences were defined. On these gates effects like interferer signals or process variations were tested. For the simulated quality of qubit gates, the outcome is that for high precision computation a co-optimization of pulse sequences and electronics is vital. Thus, a tight interdisciplinary cooperation is advisable. Overall, the developed behavioral model is a good tool for further investigation of scalability issues and electronic-qubit interaction.

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# Acronyms

| | |
|---|---|
| $\epsilon_0$ | voltage-exchange interaction fit constant |
| **2DEG** | two-dimensional electron gas |
| **AlGaAs** | aluminum-gallium-arsenide |
| **ASIC** | application-specific integrated circuit |
| **AWG** | arbitrary waveform generator |
| **CE** | control electronics |
| **CMOS** | complementary metal-oxide-semiconductor |
| **CNOT** | controlled-not |
| **DAC** | digital-to-analog converter |
| **DC** | direct current |
| **DNP** | dynamic nuclear polarization |
| **FPGA** | field-programmable gate array |
| **GaAs** | gallium-arsenide |
| **HDL** | hardware description language |
| **HQC** | higher levels of the quantum computer |
| **IC** | integrated circuit |
| **ID** | identifier |
| **LHC** | Large Hadron Collider |
| **m&h** | multiplex-and-hold |
| **MIM** | metal-insulator-metal |
| **NISQ** | noisy intermediate-scale quantum |
| **PCIe** | peripheral component interconnect express |
| **pdk** | physical design kit |
| **QAM** | quadrature amplitude modulation |
| **QC** | quantum computer |
| **QEC** | quantum error correction |
| **qubit** | quantum bit |
| **RAM** | random-access memory |
| **RF** | radio frequency |
| **RMS** | root mean square |
| **RSA** | Rivest-Shamir-Adleman |
| **RT** | room temperature |
| **S** | singlet |

| | |
|---|---|
| **s&h** | sample-and-hold |
| **SHF** | super high frequency |
| **SiGe** | silicon-germanium |
| **SOI** | silicon-on-insulator |
| **SPICE** | Simulation Program with Integrated Circuit Emphasis |
| **SRAM** | static random-access memory |
| **T** | triplet |
| **UML** | Unified Modeling Language |
| **VHF** | very high frequency |
| **VLSI** | very large-scale integration |
| **wgn** | white gaussian noise |

# Chapter 1

# Introduction

Quantum computing research is a topic of increasing popularity. The reason is the large variety of proposed use cases for a universal quantum computer with a potential high impact on research, economy and thus society. In this case 'universal' describes the ability of the quantum computer to be application unspecific and programmable to solve different problems. Example use cases in which quantum computer show superior performance in comparison to classical computers are quantum chemistry, quantum communication, cryptography, big data and optimization problems.

Quantum chemistry, for example, analyzes reaction properties of atoms and molecules on the basis of their quantum mechanical structure. The simulation is an intractable problem for a classical computer but can be done on a quantum computer [1]. The insights resulting from the simulation would not only have an impact on theoretical chemistry and material research but could influence whole economy branches. For example, chemical reactions like fertilizer synthesis, which consumes a few percent of the earth's electrical power, could be optimized [2] and the power consumption reduced.

In the communication sector, as another example, quantum computers have different potential applications. One is the so-called quantum network or quantum internet [3]. A quantum network could be used for distributed computing or secure communication. An advantage of the communication in quantum networks is that the quantum processor requires only a very low complexity. Thus, such a network could be implemented even if a universal quantum computer has not been realized yet. While quantum computers can establish secure communication channels, another use case of them is to crack encryptions based on standard algorithms used in classical computing.

In general, all of the potential applications of the universal quantum computer are based on the fact that there exist specific quantum algorithms for that specific problem. These algorithms employ the unique abilities of the quantum computer to solve the problems much faster. Indeed, they can potentially solve it exponentially faster such that practical intractable problems become solvable. Quantum algorithms exist for a range of problems, but not for everything. For example, there are also classical encryption algorithms that a quantum computer cannot crack. In theory a quantum computer could also run a classical

algorithm. However, due to the large overhead needed the execution would probably be even slower than on a classical computer. Research concerning the realization of quantum computers is done in wide range of topics such as algorithms, general theory, computer architecture, software and error correction and different qubit implementations.

The hardware necessary for a universal quantum computer able to run relevant algorithms is in the range of at least tens of millions of basic processing units [4] in addition to the classical backbone electronics required for any computational system. The basic processing units are called qubits, work as systems with quantum mechanical properties and need to be individually controlled.

The highest number of operational qubits reported on one chip is currently 53, with an implementation of so-called superconducting qubits [5]. Comparing this number with the millions of qubits necessary for a quantum computer makes it clear that a massive scale up is required. As the qubits need to be controlled and read out individually by currently unique signals, research effort is needed to realize scalable control and readout of many qubits.

## 1.1 Problem at hand

The work of this thesis contributes to the goal of implementing an innovative scalable electrical scheme to control a large number of qubits, i.e. up to millions of qubits. Challenges to this goal are the operating requirements of the qubits and the resulting limited access paths for the around 10 control signals per qubit. The quantum mechanical properties of the qubits relevant to this work are only observable at temperatures of maximum a few Kelvin but ideally below 1 Kelvin[1]. In practice this kind of temperature is usually produced by a dilution refrigerator that uses a mixture of helium isotopes to reach these cryogenic temperatures.

A standard dilution refrigerator is in total more than 1.5 m high and includes different chambers with varying temperatures, pressures and gases. The temperature in the fridge is mostly not distributed continuously but in discrete steps allocated to the different chambers. Thus, the temperature can also be used to identify an area or chamber of the fridge, here also referred to as stage. Interfacing qubits at the lowest temperature stage from the outside at room temperature is an intricate challenge. In nearly all current experiments all measurement and supply equipment is located outside of the fridge and connected to the qubit via, among others, coaxial cables. An example of such a wiring scheme for one qubit is shown in Fig. 1.1. The transmission of a high quality signal is non-trivial, not only because of the long distance, but also because of additional elements

[1] One type of qubits utilizing ion traps can be operated at room temperature, but as their scalability potential is low they are not relevant here.

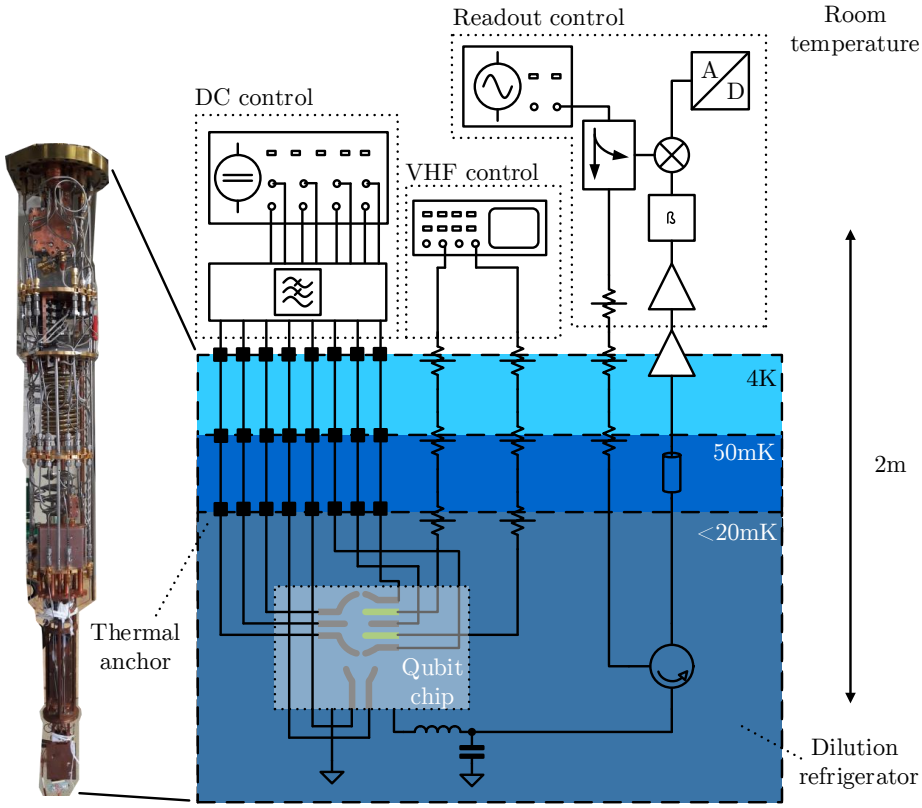


Figure 1.1: Experimental setup with wiring concept and section of inside structure of a dilution refrigerator adapted from [6]. Three different control parts are depicted for direct current (DC) voltages, very high frequency (VHF) signals and readout

.

in the signal path like attenuators, thermal anchors and amplifiers. These elements are necessary to transport a viable electrical signal across such an immense temperature difference, but they are also a potential source of delay and signal distortion.

For most of the current experiments these challenges are manageable with high quality room temperature equipment and a reasonable number of cables. The setup allows detailed research of the qubit properties precisely and flexibly. However, with increasing numbers of qubits and the goal of millions of qubits in mind, this approach reaches its limits at the latest for 1000 qubits. The heat load of the cables is increasingly relevant, as the cooling power of the fridge is at maximum only a few mW at the coldest stage. The diameter of the cables introduces problems as well. On one hand the fridge size is limited and on the other hand the qubit size of $< 1\,\mu m$ leads to a highly complex wiring challenge for the fanout to the connecting cables. In addition to that the qubits require very precise VHF (several 100 MHz) or even super high frequency (SHF) control signals ($\geq 3$ GHz). This gives rise to issue like crosstalk and data throughput considerations.

## 1.2 Approach of this thesis

In this work the approach to overcome the mentioned challenges is to use integrated circuits (ICs) and especially application-specific integrated circuits (ASICs) close to the qubits. A systematic study or implementation of such a control setup has not been done yet. The approach here transfers electrical functionality into the direct vicinity of the qubit which reduces the number of cables and the data throughput coming from circuits working at room temperature (RT). Fig 1.2 shows the concept that places the control electronics with the qubits at the coldest stage of the dilution refrigerator. Next to the control electronics at the lowest temperature stage, further electronics are depicted at higher temperature stages in the fridge. As a quantum computer is expected to have more classical electronics than the qubit control electronics, these are included in the concept. Since the power budget at the lowest temperature is extremely limited the additional electronics are envisioned to be placed at higher temperatures.

To place the electronics as close to the qubits as possible, without being on the same chip, the qubit and the electronics wafer have to be bonded together. The idea is to match electronics area and mean qubit footprint and use microfabricated interconnects between electronics and qubits, as sketched in Fig. 1.3. These interconnects are envisioned to be small enough in diameter to fit into the footprint matched to the electronics. Through this the issue of connecting many coaxial cables to the small qubits is circumvented as only few signals have to be transferred to higher temperatures.

While this approach addresses two major pitfalls of increasing qubit numbers, it brings challenges with it as well. To match electronics area and qubit footprint a very limiting

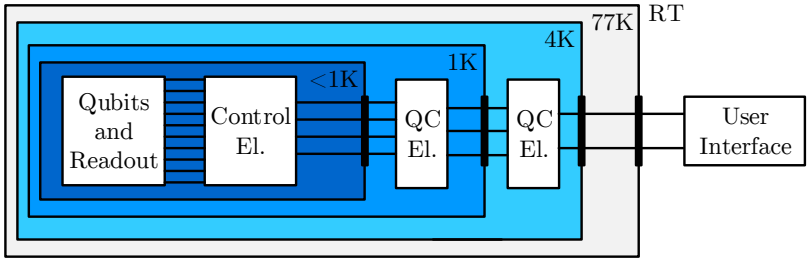


Figure 1.2: Approach for electronics placement in the available temperature stages

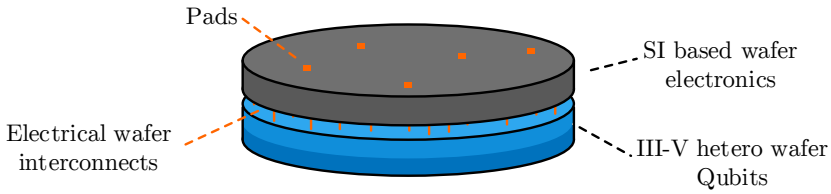


Figure 1.3: System concept of qubit and electronic interconnects

area restriction is given for the electronics. The area of spin qubits is below 1 $\mu m^2$, even if in today's device layouts a large area for pads and fanout has to be added to that. Qubits have to interact with each other to function as a quantum computer, so a placement in the direct vicinity of other qubits is ideal.Since this area is much to small for electronics with relevant functionality, the qubits have to be moved away from each other without impeding their ability to interact with each other. Current research into long distance coupling of qubits makes a distance of 10 µm seem to be possible in the future [7–9].

Next to the area the power consumption of the electrical circuits is critical. Most of the power consumed by the electronics is dissipated as heat. At the same time, the qubit operating temperature should not be increased, therefore the power consumption of the electrical circuit has to be smaller than the available cooling power of the fridge. The cooling power of a few mW at the mK stage is enough for a low number of qubits, but very challenging for many qubits. For example, for 1000 qubits the power budget is only a few µW per qubit control circuit and a few nW for 1 million qubits.

Another issue at low temperatures is the behaviour of electrical circuits. The Simulation Program with Integrated Circuit Emphasis (SPICE)-based models used to design circuits are not valid at cryogenic temperatures. While it has been shown that standard bulk complementary metal-oxide-semiconductor (CMOS) technologies at nodes <90 nm work quite well at cryogenic temperatures [10], correct and detailed models are essential for

high performance circuit design. The models for temperatures in industrial applications have to be adapted to be accurate for cryogenic temperatures. This characterization is still in the early stage for the technology at hand.

An additional element of uncertainty regarding control electronics for spin qubits is the ongoing research on qubits. New aspects and insights on how to best control qubits are continuously gained which changes the requirements of the electronics. Coupled with the fact that up to now very high-quality and high-performance equipment has been used, a fixed minimum requirements specification is not available.

To overcome the uncertainty issues of the approach this work is done through high level modeling. With system modeling a flexible tool is created to explore options which can be adapted to changing requirements. In addition to that such a model is suited to analyze the feasibility of the approach with less effort than a full ASIC implementation.

The complete system model also has advantages for verification, since no operational qubit is at hand. First verification and tests of component designs can be done with the model.

## 1.3 Organization of this work

In this work a new and detailed concept of scalable control electronics for spin qubits is developed and tested. Next to the control electronics themselves also the interfacing components have been included, resulting in a complete system model. Chapter 2 gives the reader necessary basics of quantum computing in general and a brief overview of qubit technologies. Chapter 3 discusses the specifications of control electronics and contains the feasibility analysis of the presented concept. On top of that an extensive discussion of the scalability is done. In chapter 4 a behavioral model of the qubit control electronics and the surrounding components is developed. Analogous to that in chapter 5 a model of the qubit is established. In chapter 6 these both model parts are combined together, and chapter 7 draws a conclusion.

# Chapter 2

# Basics of Quantum Information and Quantum Computing

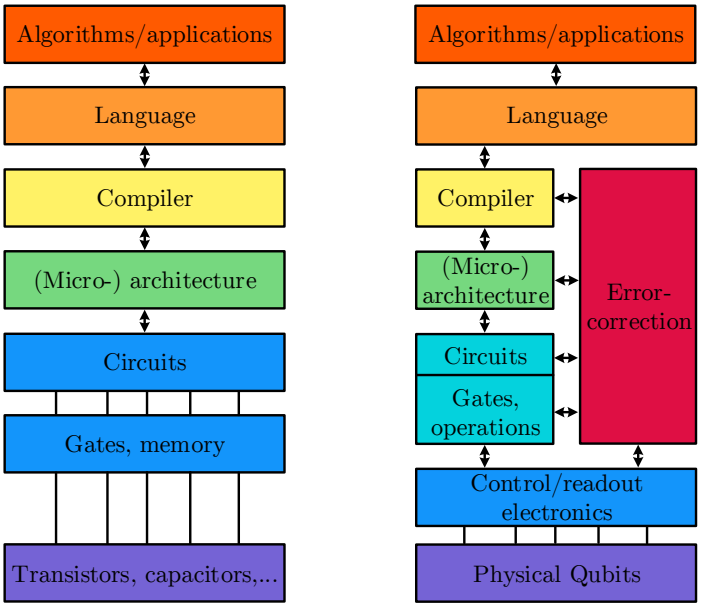


Figure 2.1: Levels of abstraction[2] of a (a) classical computer and (b) a quantum computer.

This chapter introduces the concepts necessary to understand the later parts of this work. For the interested reader publications such as [11–14] are recommended to get more involved with the topic of Quantum Computers and Quantum Information. On top of that [15] reports on an overview of current scientific results on all levels of quantum computer research.

The idea of a quantum computer (QC) is already regularly mentioned in the mainstream media, but seldom statements are made on how non-experts in the field can picture and understand such a computer. While the specific details of a QC are naturally still unclear, a direct comparison to a classical computer gives a perhaps more accessible picture of how a quantum computer could look like. Fig. 2.1 shows a 'levels of abstraction'[2] depiction of a classical computer on the left and a possible well suited one for a quantum computer on the right. A lot of components of the classical computer find their equivalent in the quantum computer, but some parts are different, especially in the lower levels. The equivalent parts in the quantum computer not only have the same functionality as the ones in the classical computer, but their hardware is classical as well. Therefore, a quantum computer will consist in large parts of classical logic.

The topmost level for both computers is the algorithm and applications level. While a classical computer can only run classical algorithms, a quantum computer could run classical and quantum algorithms. As the classical algorithms do not utilize the unique hardware properties of the QC, no advantage would be gained, as mentioned in already in Chap. 1. One example of a quantum algorithm is Shor's algorithm, which may be used to efficiently factorize large numbers into their primes. The impact of the runtime difference to the best classical algorithm is emphatically shown with the time it takes to factorize a 2048 bit number into its primes. The Tianhe-2 supercomputer [16] would need about 100 years to achieve the factorization, while a quantum computer could complete the calculation in roughly 8 hours [17]. The significant reduction in calculation time is relevant, since the current Rivest-Shamir-Adleman (RSA) encryption is based on the computational difficulty of prime factorization [11]. As a quantum computer could crack this encryption, standardization of quantum computer safe algorithms is underway [18].

Research on the software and micro-architecture parts of the quantum computer, which are similar to their corresponding classical computer versions, is varied. It reaches from object-oriented high-level languages like QCL, Q#, Qlanguage, OpenQL to lower level languages like Quantum pseudocode and instruction sets like Quil, OpenQASM, and QUISA. On top of that there are several software development kits like ProjectQ, Qiskit, Forest, Quantum development Kit, and Cirq available. A complete review or listing of the different projects does not exist, but some well advanced collections can be found in [15, 19–21]. So far, no package or language could clearly establish themselves as a quasi standard.

The next lower levels of circuits and gates in Fig. 2.1 also exist in both computer versions. For the quantum computer these levels are directly connected because no distinct hard-

[2] Among others, depicting levels of abstraction is a method used in computer science and software engineering where the same object, or principle is depicted with different amounts of abstraction. The top level usually provides the most abstraction while the lowest level includes the most details.

ware representing circuits exists. Circuits are established through actions on the basic units, as the most basic processing unit is a memory element as well.

The combination of memory and processor element leads to a completely different mode of operation compared to the classical computer, where sets of transistor basic units are hard-wired together to provide one specific logical function. The operations in a quantum computer are variable and as such a set of basic units can perform different logical operations, as explained in more detail in Sec. 2.1. There is only one basic processing unit in a quantum computer, called the quantum bit (qubit). The combination of memory and processing capability in a quantum processor makes the classical Von-Neuman architecture with separated memory and processing obsolete. In its place new gate-defined quantum architectures have been established [4, 22–24]. Another consequence of the nonexistence of dedicated long life memory elements up to now is that no working memory or hard drive[3] exist in QCs. All information to be stored must be kept in classical electronics [15].

The construction of logic operations from actions on the processing unit has a significant disadvantage which is represented by the additional layer of control/readout electronics in Fig. 2.1b. This layer contains complex electronic circuits, which are needed to operate the basic processing units in the lowest level. The basic units in a classical computer are transistors, capacitors and so forth, but a quantum computer has only the one type of unit, the qubit. While classical logic mainly needs a power supply, a reference clock and decent quality input signals, qubit operation is much more demanding. Depending on the qubit implementation it requires for example several very stable DC voltages and in addition to that VHF or SHF control signals or even lasers (Sec. 2.1).

Next to the way of implementing circuits and the operation of the qubits, the error correction is a deciding difference between quantum and classical computers (Fig. 2.1). Large-scale quantum computation is heavily dependent on quantum error correction (QEC) for several reasons. First, the error rate of the qubits [25] currently is mostly around $10^{-1}$ to $10^{-2}$ with some exceptions in the range of $10^{-4}$. Second, correcting errors in a quantum computer is much more complex than in classical electronics. Typical classical correction schemes involve copying and comparing states, which are actions that are fundamentally impossible in quantum mechanics. On top of that the errors in qubits are continuous, rather than discrete as in classical logic. These issues highlight the difficulties for QEC and explain the necessity of extensive error correction [26] on several levels of the QC. A currently popular QC code is the so-called surface code [27]. One advantage of this code is that only neighboring qubits have to be able to interact. Other codes require possible coupling of each qubit to every other qubit which is difficult to implement in hardware. Another advantage of the surface code is its fault tolerance, if the qubit's error rate is under a certain threshold. Here fault tolerance describes the code's ability to correct both the original error and the possible error introduced through

[3] So far, no method to preserve qubit states without a constant power supply has been found.

the correction mechanism. The threshold error rate of the surface code is the subject of ongoing research, but has been estimated to be 1 % [27, 28]. However, the models which contributed to this number include several simplifying assumptions. The impact of these simplifications is not yet clear, so the 1% threshold is more a minimum requirement on the quality of the qubits.

## 2.1 The qubit

The qubit is the most basic unit of a quantum computer and the term is used both for the unit of information and for the technical realization containing such information. In this work, the term 'qubit' refers to the physical implementation while the information is referred to as 'state of the qubit'.

In general, the state of a qubit corresponds to the state of a two-level quantum mechanical system. The levels are encoded into $|0\rangle$ and $|1\rangle$, similar to the classical bits 0 and 1. In the quantum computing community the state of a qubit is then given by:

$$|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle, \quad \alpha, \beta \in \mathbb{C}. \tag{2.1}$$

Eq. 2.1 is written in the so-called bra-ket notation. It has advantages when expressing quantum mechanical operators, but the same equation can also be written in a standard vector notation:

$$\vec{\Psi} = \alpha\vec{e_1} + \beta\vec{e_2}, \quad \alpha, \beta \in \mathbb{C}. \tag{2.2}$$

In this case $\vec{e_1}$ and $\vec{e_2}$ are perpendicular basis vectors of the state space of $\vec{\Psi}$ (Hilbert space of the qubit) and a state is the result of a vector addition. This vector addition is the foundation of the superposition property of the state of one or several qubits. The state cannot only be $|0\rangle$ or $|1\rangle$ but can be a bit of both at the same time. The amplitudes of the basis vectors determine the amount of superposition of $|0\rangle$ and $|1\rangle$ and are normalized to

$$|\alpha|^2 + |\beta|^2 = 1. \tag{2.3}$$

The amplitudes $\alpha$ and $\beta$ play an important role in the readout of a qubit state as well. A state can only be measured in one of the basis vectors of the state space. This means that the measurement projects the superposition state onto one of its (measurement) bases, thus destroying the superposition. This implicates that a measurement destroys the quantum mechanical property of the qubit state. The result of the measurement can only be either 0 or 1 and is not deterministic. The probability $p$ of measuring either 0 or 1 from the same state is given by $p(0) = |\alpha|^2$ and $p(1) = |\beta|^2$.

The 4-dimensional state space of a qubit can be projected onto a 2-dimensional space to make a visualization possible. Here, this 2-dimensional space is the surface of the so called Bloch sphere, as shown in Fig. 2.2. The Bloch sphere representation ignores a non-observable global phase and rewrites the qubit state as[4]:

$$|\Psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\varphi}\sin\left(\frac{\theta}{2}\right)|1\rangle, \text{ with } \varphi, \theta \in \mathbb{R}. \tag{2.4}$$

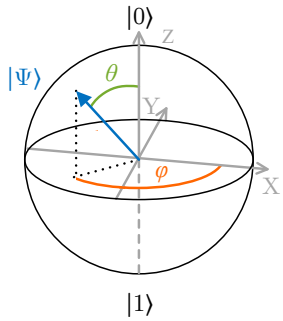


Figure 2.2: Bloch sphere with representation of qubit state $|\Psi\rangle$.

The change of the state of a qubit is described by a unitary transformation applied to a starting state $|\Psi_0\rangle$:

$$|\Psi\rangle = U\,|\Psi_0\rangle, \tag{2.5}$$

where $U$ is a unitary matrix and $|\Psi\rangle$ the resulting state. The most similar corresponding action in a classical computer is to perform a classical logic gate.

On the Bloch sphere the unitary transformation corresponds to a movement on the surface of the sphere. For example, the rotation of a state around one axis by an angle of $\rho$ can be achieved with well-known rotation matrices, as written in Eq. 2.6. Further, the so-called Pauli matrices (Eq. 2.7) describe the rotation around one axis by an angle of $\pi$. The difference to a corresponding rotation matrix with the same angle is only a global phase of $\pi$.

$$R_{x,\rho} = \begin{pmatrix} \cos\frac{\rho}{2} & -i\sin\frac{\rho}{2} \\ -i\sin\frac{\rho}{2} & \cos\frac{\rho}{2} \end{pmatrix} \quad R_{y,\theta} = \begin{pmatrix} \cos\frac{\rho}{2} & -\sin\frac{\rho}{2} \\ \sin\frac{\rho}{2} & \cos\frac{\rho}{2} \end{pmatrix} \quad R_{z,\rho} = \begin{pmatrix} e^{-i\rho/2} & 0 \\ 0 & e^{i\rho/2} \end{pmatrix} \tag{2.6}$$

[4]Note that in this work $i$ indicates the imaginary unit.

$$\sigma_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \quad \sigma_y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix} \quad \sigma_z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} \tag{2.7}$$

## 2.2 Multiple qubits

A quantum computer is not only made of single unrelated qubits but is a large system of a high number of qubits which have to interact with each other. The state of multiple qubits together can be calculated with using the tensor product $\otimes$

$$|\Psi\rangle = |\Psi_1\rangle \otimes |\Psi_2\rangle, \tag{2.8}$$

with the single qubit states $|\Psi_n\rangle$. Thus, the dimension of the state vector of $n > 0$ qubits is $2^n \times 1$ and the dimension of a gate matrix $U$ is $2^n \times 2^n$, which describes the number of possible basis states. The exponential increase in states with additional qubits can be seen as one of the reasons why a quantum computer can be more powerful than a classical one. With each qubit the information content is increasing exponentially. On top of that it is one of the reasons why even supercomputers struggle to simulate qubit numbers over 40. The number is heavily dependent on the computer and the complexity of the quantum mechanical model.

While the Bloch sphere is used to visualize single qubit gates no such well known way exists for multi-qubit states. The state of multi-qubits can be calculated from the individual states, but the reverse is not always true. There are possible multi-qubit states which cannot be separated into single qubit states, which still fulfill the normalization in Eq. 2.3. Since the decomposition into separate individual qubit states is not possible this implies that the single qubit states are dependent on each other. This is called entanglement and is another deciding feature of the quantum computer next to the superposition. Entanglement is so powerful because if $n$ qubits are entangled the state of only one has to be changed to affect the state of all of them. This can be imagined similarly to parallel computation on $n$ cores but with the computational effort of only one core.

An entangled state of several qubits is achieved through multi-qubit operations. A multi-qubit operation works analogously to a single qubit operation as detailed in Eq. 2.1. The only difference is the dimension of the state vectors and the matrix $U$. An often-used example for a two-qubit gate is the so called controlled-not (CNOT) gate whose matrix representation is [11]

$$U = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} \tag{2.9}$$

in the standard two-qubit basis $\{|00\rangle, |01\rangle, |10\rangle, |11\rangle\}$. This operation can transform two independent single qubit states into one entangled state. With the CNOT gate and a small number of single qubit gates all components for one universal gate set are given [26]. Similar to the definition of universal gates in classical logic (NAND or NOR), such a set is able to implement all functionality in a universal quantum computer.

## 2.3 Quality measures for qubits and gates

One important quality measure of a qubit is the lifetime of its state. That is the time it takes for the information encoded in the qubit state to disappear. Depending on the qubit type and the information loss mechanism the coherence time $T_2$ or $T_2^*$ is given, or the relaxation time $T_1$ [29]. The relaxation and coherence times describe time constants at which the information content of the original state is decaying until the information of the current state does not show a correlation to the information of the original state. The relaxation time is the average time an excited qubit state relaxes to its energetic ground state. The coherence time describes the time it takes until the angle of a qubit state has no relation to the original angle[5] In general the relation between these parameters is $T_2 \leq 2T_1$. Thus, different measurements of coherence apply for different qubit implementations. In contrast to $T_1$ and to $T_2$, $T_2^*$ describes the loss of information of an ensemble of spins, which is relevant for multi-spin qubits. More detailed explanations of the phenomena and the quality measures are for example given in [29, 30]. Depending on the implementation the lifetime of a qubit state can be between a few µs [31] and the order of a second [32]. The longer the lifetime of the qubit the less errors on shorter timescales happen and the longer possible operation sequences can be. That means with a longer coherence time more complex circuits with higher circuit depth can be realized.

### 2.3.1 Gate operations

The quality of a qubit operation, and the underlying state transformation, is usually described with the average gate fidelity [33, 34]

$$F = \frac{1}{n^2}|\mathrm{Tr}[U_{ideal}^T\, U]|^2. \tag{2.10}$$

Eq. 2.10 shows the calculation of the fidelity with the ideal transformation matrix $U_{ideal}$, the actual matrix $U$, and a normalization factor $n$. The value of $F$ lies between zero and one with one as best possible fidelity. In practice the infidelity $I = 1 - F$ is often given for convenience. Current research mostly reports single qubit infidelities between $10^{-1}$ and

[5] Note that here the angle described is the angle in the Bloch sphere which is subject to constant precession.

$10^{-2}$ [15], depending on the qubit implementation[6]. Possible sources of non-idealities for the operation are plenty and range from systematic control errors to noise sources in the qubit samples and the control signals.

Non-ideal gate operations with $I > 0$ lead to computation errors at an error rate $\eta$[7], that have to be corrected by error correction algorithms. The relationship between the fidelity $F$ and error rates $\eta$ is not trivial as additional information about the source of non-idealities is necessary for an exact calculation [35]. However, with assumptions on the type and amount of noise the relationship can be simplified [35]. Thus, for an error rate threshold of $\eta = 1\%$ (surface code) an infidelity of a little below $10^{-2}$ could suffice. This is then under the assumption that existing noise only has a simple dephasing effect on the qubit [2]. In reality more effects from the noise are expected, such that the required infidelity to reach so called fault tolerance would be lower. A lower infidelity is also advantageous, as the cost of error correction (additional devices, hardware and software) decreases substantially with increasing gate fidelity. In this work the infidelity benchmarks used to evaluate gate performance are set to $10^{-2}$ and $10^{-3}$, with the knowledge that a better infidelity is highly desirable.

## 2.4 Qubit implementations and their scalability potential

There are many physical two-level systems which can be used as a qubit. Research on qubit implementations is therefore done in a variety of systems. Examples are nitrogen centers in diamond [3], cold [36] and neutral atoms [37], trapped ions [38], photons [39], topological insulators, superconducting circuits [40] and spins in quantum dots [41]. The implementations vary significantly in many properties such as qubit lifetimes, gate fidelities, the control and gate operation mechanisms, environment specifications, physical size, sample production technology and their readout procedures. All these properties impact the suitability of this qubit implementation in a universal quantum computer. Ultimately, the computer requires millions of qubits, so the scalability of the qubits is a deciding factor, as first indicated by [42].

The highest chances in scaling numbers up are seen for superconducting qubits and semiconductor spin qubits. They have the advantage that their production is done with lithography techniques similar to the well-established processes in very large-scale integration (VLSI) electronics and the physical qubit size is comparably small. In addition,

[6] Qubits based on ion traps are the most advanced, but as they are not considered scalable to high numbers they are not the focus of the present discussion.

[7] A detailed introduction to errors in quantum computations, their correction and the terms associated is not in the scope of this work, but can be found in [25].

the control through electro-magnetic signals is possible. In Tab. 2.1 different potentially scalable qubit topologies and their properties are given.

For superconducting qubits, which are the most mature solid-state qubits, a maximum of 72 qubits on one chip has been announced [43] and 53 have been shown in operation [5]. In [5] the authors even claim that with their quantum processor they have shown superiority over a classical computer. The best infidelity reported to date for single qubit gates is $10^{-3}$ and below $6 \cdot 10^{-3}$ for two qubit gates [40]. These numbers all refer to todays most established superconducting qubit topology, the so-called transmon qubit. Like all superconducting qubits it is based on a resonant circuit. The circuits are cooled down to cryogenic temperatures and use quantum mechanical non-linear circuit elements to create the desired two-level qubit behaviour. The control of the qubits is done with quadrature amplitude modulation (QAM) microwave signals at a carrier frequency corresponding to the circuits' resonant frequency. While the superconducting qubits mainly can be produced with standard lithography techniques, their footprint slightly below $1\,\mathrm{mm}^2$ is very large compared to the feature size of state-of-the-art VLSI processes. The scalability potential of the superconducting qubits is limited through the size of the footprint, as millions of qubits would already occupy an area of roughly $1\,\mathrm{m}^2$, which would have to be cooled. The control and readout of the superconducting qubits also opens issues regarding frequency multiplexing and crosstalk as the variability of the qubit resonance frequency is limited.

Semiconductor spin qubits mostly use quantum dots to locally confine electrons and use the spin to encode qubits. For the quantum dot fabrication different heterostructure material combinations as silicon-germanium (SiGe) and gallium-arsenide (GaAs) are often used, but Si-MOS devices exist as well [44]. A chip with 26 SiGe qubits has been announced in [45], but no measurements have been published yet. Most research groups work with a maximum of two qubits. The best achieved single qubit infidelity is $10^{-3}$ [46] and a best two qubit infidelity of $2 \cdot 10^{-2}$ [47] has been reached. However, these numbers were not achieved in the same experiment. SiGe qubits use the spin of a single electron and have a very small footprint of around $0.02\,\mu\mathrm{m}^2$ (without electrode fanout and ohmic contacts to the electron reservoir) and the potential advantage of near zero nuclear spin. Nuclear spin is a material property that creates a small, local magnetic field which fluctuates over time and thus interferes with qubit operation. In SiGe qubits nuclear spin free isotopes like $^{28}$Si can be used to avoid this noise source. This leads to very long coherence times on the order of 1 s [48, 49], while the operations can be as short as 100 ns [50] for single- and two-qubit gates. For operation the SiGe qubit requires several DC signals, a permanent magnetic field and microwave signals for a resulting effective magnetic AC field. Again, the microwave signals could potentially limit the scalability due to e.g. crosstalk.

GaAs qubits have already been studied extensively but have the disadvantage of unavoidable decoherence due to nuclear spin. For this reason GaAs qubits either use a

combination of spin and charge or the spin of several electrons to encode one qubit which mitigates the issue [41]. The most promising implementation of this is the so-called S-$T_0$ qubit using the spin of two electrons. The maximum number of qubits realized this way is only two, but the best infidelities experimentally achieved were $5 \cdot 10^{-3}$ [51] for single qubit gates, not much worse than in SiGe. For two qubit gates only an infidelity of $10^{-1}$ [52] has been experimentally shown, but theoretical results predict infidelities down to $10^{-3}$ [53]. The duration of single and two qubit gates is several tens of ns with an achieved coherence of 0.87ms [54]. One deciding advantage of GaAs S-$T_0$ qubit is that only control at lower frequencies around a few hundred MHz is needed next to a few DC signals and a constant magnetic field. This simplifies the electrical generation of the signals compared to SiGe and transmon qubits and reduces the severity of crosstalk.

| Qubit | Lifetime | Gate duration (ns) | | Infidelity | | # | Footprint | Control |
|---|---|---|---|---|---|---|---|---|
| | ms | 1 Qubit | 2 Qubit | 1 Qubit | 2 Qubit | | $\mu m^2$ | |
| GaAs | 0.87 | 40 | 40 | $5 \cdot 10^{-3}$ | $10^{-1(-3)}$ | 2 | 0.1 | VHF |
| SiGe | 1000 | 100 | 100 | $10^{-3}$ | $2 \cdot 10^{-2}$ | 26 | 0.02 | SHF, VHF |
| T.mon | 0.01 | 20 | 30 | $10^{-3}$ | $6 \cdot 10^{-3}$ | 52 | $10^6$ | SHF |

Table 2.1: Summary of the most promising scalable qubit candidates and their best achieved properties

As a comparison, the not highly scalable trapped ion qubits have single and two qubit error rates are below $10^{-4}$ and $10^{-3}$ with a coherence time of more than 1 s [38]. QEC has been demonstrated with these qubits as well but going from the current 1D lines of ions to 2D arrangements is a challenge. On top of that the control through lasers is not trivial for large scales of qubits. For such qubits with a high quality, other timelier use cases than a quantum computer are possible. Examples are quantum sensing, quantum networks and their quantum repeaters, and proof of principles in the current noisy intermediate-scale quantum (NISQ) [55] technology stage.

This thesis focuses on GaAs qubits as a reference as one of the promising candidates for scalable qubits. Especially the fact that only VHF control instead of microwave signals is needed for this topology makes it interesting to explore the scalability of control electronics. The methods used in this work, and by this the general results, can be transfered to other qubit technologies.

### 2.4.1 The GaAs S-$T_0$ qubit

The basis of a GaAs qubit is a heterostructure made of aluminum-gallium-arsenide (AlGaAs) and GaAs as shown in Fig. 2.3. The shape of the conduction band in this

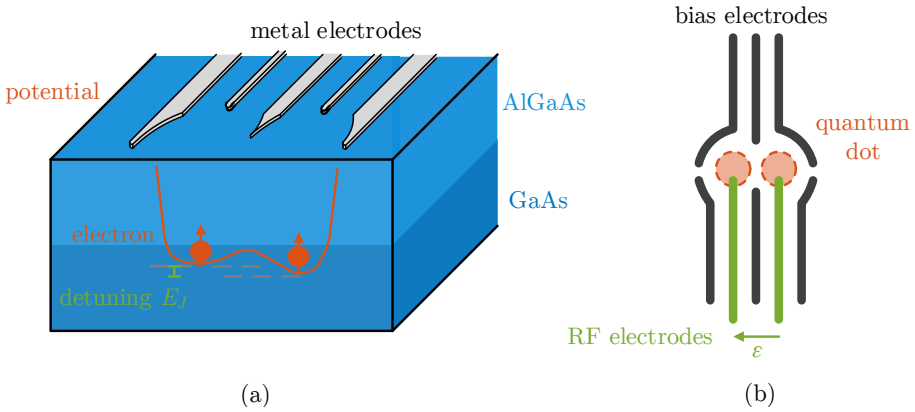


Figure 2.3: The GaAs qubit: (a) heterostructure cross-section with electrochemical potential distribution, (b) principle electrode layout of one double dot (radio frequency (RF))

heterostructure enables a two-dimensional electron gas (2DEG) of free electrons at the interface of the two materials. Electrodes on the top of the materials can locally deplete the 2DEG when a negative voltage is applied to them. With the correctly tuned voltage configuration two potential wells are created (Fig. 2.3), in which single electrons can be confined to a precisely defined location due to quantum mechanical principles. The wells are also called quantum dots. Thus, two wells together are named a double quantum dot or just a double dot.

In a GaAs qubit two electrons are confined in the double dot and their spin state is used to encode the logical basis states $|0\rangle$ and $|1\rangle$. Next to different spin states, different charge configurations are employed e.g. for readout and initialization of the qubit. The different configurations of spin and charge can be distinguished by their discrete energy levels. In the case of the charge possible configurations are the occupancy of a dot with $n$ electrons, with $n_{\in}\{0, 1, 2\}$. The notation is $(n_l,n_r)$ for the charge configuration of the double dot (left,right). In case of the spin the determining characteristic is the spin quantum number $s$. The spin quantum number is quantized and for $s = 0$ a spin state is called a singlet (S) state. With $s = 1$ the spin state is characterized as a triplet (T) state.

Figure 2.4b depicts the energy of all possible configurations dependent on the detuning voltage $\epsilon$ (Fig. 2.3), which controls the energy difference between the dots through the detuning energy $E_J$. The basis of this complete energy diagram is the reduced energy diagram with only the relevant charge configurations, which is shown in Fig. 2.4a. Through energy level splitting due to electron spin (S-T splitting), bending of the levels because of possible inter-dot tunneling, and level splitting due to the Zeeman effect

(T splitting into $T_-$, $T_0$,$T_+$)[8], the energy levels shown in Fig. 2.4b result. More detailed derivations can for example be found in [56].

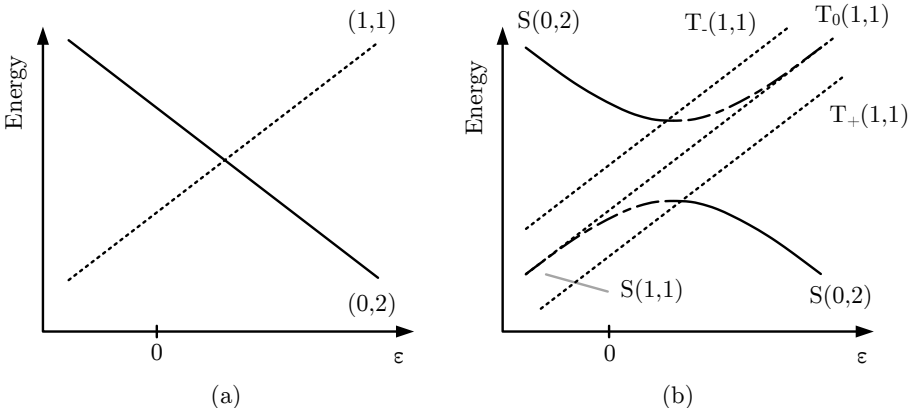


Figure 2.4: GaAs double dot energy diagrams: (a) energy levels only due to charge configuration, (b) added spin and tunneling effects (adapted from [57])

Of all these states included in the full energy diagram, only the subset of S(1,1) and $T_0(1,1)$ is used to encode the logical states $|0\rangle$ and $|1\rangle$. That means during qubit operation there is always one electron in each dot. It follows also that the qubit can potentially have other states than the ones in the logical subspace. These are called leakage states. The loss of information towards leakage states, also called leakage rate, cannot be corrected by conventional QEC algorithms, but high-fidelity qubit operation is still possible [2]. States such as S(0,2) are used during readout and initialization. For example, readout principles are based on the fact that either a (0,2) charge configuration can be distinguished from a (1,1) one, or that the singlet and triplet spin configurations behave differently (e.g. Pauli exclusion principle).

The formal description of the energy states of a quantum mechanical system is typically done with the so called Hamiltonian $H$. The Hamiltonian for the logical subspace of a GaAs qubit, with the help of the Pauli matrices from Eq. 2.7, is often given in the form of [2, 56]:

$$H = \frac{\hbar\omega_J(\epsilon)}{2}\sigma_z + \frac{\hbar\Delta\omega_z}{2}\sigma_x = \frac{\hbar}{2}\begin{pmatrix}\omega_J(\epsilon) & \Delta\omega_z \\ \Delta\omega_z & -\omega_J(\epsilon)\end{pmatrix}, \tag{2.11}$$

with $\hbar$ being the reduced Planck constant. Eq. 2.11 uses the basis $\{|S\rangle, |T_0\rangle\}$. This computational basis can also be expressed in terms of spin orientations of the electrons

[8]The Zeeman effect here is due to an applied constant magnetic field $B_{ext}$.

in the dot, with ↑ as spin up and ↓ denoting spin down

$$|\mathrm{S}\rangle = |0\rangle = \frac{|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle}{\sqrt{2}}, \tag{2.12}$$

$$|\mathrm{T}_0\rangle = |1\rangle = \frac{|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle}{\sqrt{2}}. \tag{2.13}$$

The Hamiltonian in general describes energy states and with the Planck-Einstein relation $E = hf = \hbar\omega$ ([58], p.1181) Eq. 2.11 can also be written in energy terms directly:

$$H = \frac{1}{2}\begin{pmatrix} E_J & \Delta E_{z,DNP} \\ \Delta E_{z,DNP} & -E_J \end{pmatrix}. \tag{2.14}$$

$E_J$ is the detuning energy which is equal to the energy difference of the dots and is connected to the so-called exchange interaction mechanism. The corresponding angular frequency $\omega_J$ is given by [59, 60]

$$\omega_J(\epsilon(t)) \approx \omega_s \exp(\epsilon(t)/\epsilon_0). \tag{2.15}$$

Here, $\epsilon(t)$ is a voltage defined as the potential difference between the right and the left dot and is applied through the two RF electrodes (Fig. 2.3). In contrast to convention in this work $\epsilon_0$ does not denote the vacuum permittivity but is a fit constant. In addition, also $\omega_s$ is a fit constant and thus the only parameter to actively change the state of the qubit is $\epsilon(t)$.

The other term in Eq. 2.14, $\Delta E_z$, is the result of the Zeeman effect. The Zeeman effect describes the shift of an electron energy level due to a magnetic field. In general $E_z$ is given through ([61], p.150)

$$E_z = g\mu_B B, \tag{2.16}$$

with the $g$ factor ($g = -0.44$ in GaAs [32]), the Bohr magneton $\mu_B$ and the magnetic field $B$. Of interest here is a magnetic field difference between the dots $\Delta B_z$. It is a result of the dynamic polarization of the nuclear spin of the host material leading to an angular frequency of $\Delta\omega_z = \frac{g\mu_B}{\hbar}\Delta B_z$. The procedure, which is also shortened to DNP (dynamic nuclear polarization), is for example described in [41]. The nuclear spin of the host material cannot be erased, so instead of trying to keep it as small as possible it is used here as a second axis for evolving the qubit state.

For the correct determination of the state of a GaAs qubit the absolute energy levels of in $H$ are irrelevant. Thus, in this work the Hamiltonian $\tilde{H}$ is used with

$$\tilde{H} = H \cdot \frac{1}{\hbar} = \frac{1}{2}\begin{pmatrix} \omega_J(\epsilon) & \Delta\omega_z \\ \Delta\omega_z & -\omega_J(\epsilon) \end{pmatrix}. \tag{2.17}$$

Figure 2.5 visualizes of influence of the two summands and thus the complete Hamiltonian on the qubit state while referring to the energy diagram. The exchange interaction is a measure of the amount of separation between $|0\rangle$ and $|1\rangle$, as seen on the energy diagram of the logical subspace in Fig. 2.5a. The smaller $E_J$, the larger the superposition. Some residual separation of S(1,1) and the $T_0(1,1)$ state remains at $\epsilon \ll 0$ due to the polarized nuclear spin and the resulting $\Delta E_z$. In Fig. 2.5 the basis rotation axes in the Bloch sphere, as described in Eq. 2.11 are shown. As denoted by $\sigma_z$ the exchange interaction rotates the qubit state around the z-axis. The strength and as a result the speed of the rotation is given through $\epsilon$. A state rotation due to the constant magnetic field difference happens around the x-axis and cannot be turned off. Only the relative strength of $E_J$ governs the effect that $\Delta E_z$ has.

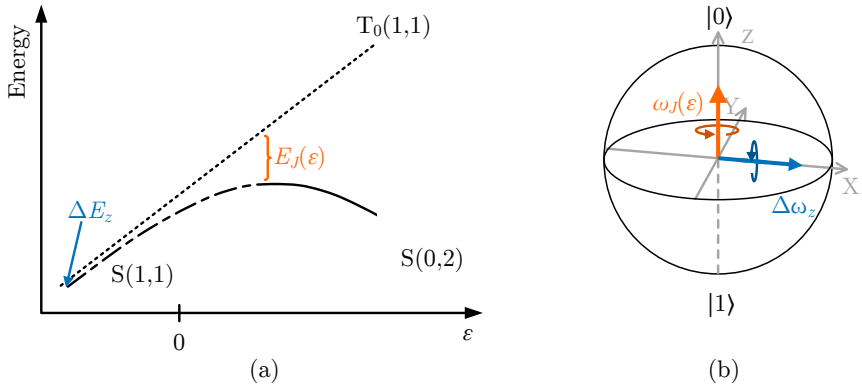


Figure 2.5: (a) Energy diagram of the logical subspace with state changing parameters and (b) visualization of state changing rotations on the Bloch sphere

The relation between $E_J$ and $\epsilon$ in Eq. 2.15 is an approximation determined through device measurements and an exponential fit. The constant values used in this work are $\omega_s = 2\pi \cdot 160\,\text{MHz}$ and $\epsilon_0 = 0.272\,41\,\text{mV}$. They were obtained from fit data from [59, 60], but differ depending on the sample geometry, the specific experiment settings and the electrode potentials that form the double dot.

To get from the Hamiltonian $\tilde{H}$ description to the calculation of the unitary matrix $U$ the following relation can be used for a piecewise constant Hamiltonian[9]:

$$U(t_M) = \prod_{k=1}^{M} \exp\left(-i \begin{pmatrix} \omega_J(\epsilon_k) & \Delta\omega_z \\ \Delta\omega_z & -\omega_J(\epsilon_k) \end{pmatrix} \Delta t_k\right) = \prod_{k=1}^{M} dU_k. \tag{2.18}$$

[9]This is derived from the Schrödinger equation $i\hbar \mathrm{d}/\mathrm{dt}|\Psi(t)\rangle = H|\Psi(t)\rangle$.

Here, the time $t_M$ is given by $t_M = \Sigma_{k=1}^{M} \Delta t_k$ with $\Delta t_k = t_k - t_{k-1}$ and $\epsilon_k$ is the constant detuning during each timestep $\Delta t_k$.

## 2.5 State of the Art (scalable) qubit control

As seen exemplary in Fig. 1.1, most of todays laboratory setups for qubit research are done with standard signal sources and measurement equipment at room temperature. For the control especially arbitrary waveform generators (AWGs), RF sources and bias sources are needed. For the S-$T_0$ qubit focused on here, the microwave source is not necessary. In Chap. 1 is already mentioned that for a large qubit number this type of room temperature setup is not realistic, even if it is perfectly suited to the variable few qubit experiments today. Depending on the qubit type different approaches are investigated to control numerous qubits.

For superconducting qubits, where extensive microwave signal generation is necessary, the focus is mainly on making the room temperature equipment more efficient and affordable, as described in the supplementary material of [5] and in [62, 63].

For semiconductor qubits the approach is to put as much electronics as possible inside the fridge. Thus, the research started with implementing small, function specific circuits for cryogenic operation [64–68] and connectors [69]. Additional research on characterizing current CMOS technologies is also a part e.g. in [70–72]. In general, the newer technology generations show similar characteristics at cryogenic temperatures compared to room temperature for many devices. Issues such as hysteresis behaviour for transistors, which existed in older technologies, does not seem to be an issue any longer. The cited works are a good basis for future use of CMOS technologies at cryogenic temperatures, however the research is not yet at a point where the results can be easily integrated in the standard circuit design flow.

In the beginning of the research on placing the electronics inside the fridge, the location for the bulk of the electronics was the same. Only limited switching functionality was placed next to the qubits, while the other components were to be located at a stage with a higher temperature of 4 K [22, 73]. Several works describe the electronics for the case of SiGe qubits [74–76]. Especially valuable from this works is the result, that a standard field-programmable gate array (FPGA) is operational at cryogenic temperatures.

Current works still place the main electronics for the SiGe qubits at that temperature [77], while the concept of this work (also included in [78]) locates the electronics at the lowest temperature stage. Also preliminary results published in [79] use that concept. The higher temperature has the advantage, that more cooling power is available. This is especially important for SiGe qubits, as the microwave circuits necessary are expected to dissipate more heat. For example only the analog power of a current qubit controller

[80] consumes 1.7 mW per qubit and an oscillator for the same system draws 4.3 mW [81]. A cooling power of only a few mW at the lowest temperature stage makes it very difficult to place these kinds of circuits in the vicinity of the qubits without a negative impact on the temperature in the fridge and thus impeding qubit operation.

A disadvantage of placing a lot of the electrical functionality on a higher temperature stage is the connectivity issue. Transferring electrical signals between temperature stages is difficult because heat conductance has to be minimized. On top of that coaxial cables are required to transport sensitive signals distortion free, which leads to a similar challenge as connecting signals to room temperature. Also, the data rate to be supported is a challenge as well as possible multiplexing for analog signals. Thus, the low frequency control of the S-$T_0$ qubit and the following potential for integration at lowest temperatures could be a crucial advantage. It can minimize the data throughput and the corresponding number of connecting cables.

# Chapter 3

# Feasibility and scalability of cryogenic control electronics for qubits

## 3.1 Motivation and method

The idea of cryogenic control electronics at the lowest temperature level was introduced earlier in Chap. 1. In this chapter the objective is to develop a fitting control electronics concept and check its practicability[10]. Doing this check before starting circuit design saves a lot of design time as non-suitable concepts can be identified in the beginning. Due to the complexity of the qubit control coupled with the high number of necessary qubits and the difficult environment of the fridge, the studies to ascertain suitability need to be detailed and in depth. The practicability criteria are the scalability and the feasibility of the electronics concept. The term scalability is not precisely defined, as the exact number of qubits necessary for a quantum computer is still unclear. Instead of the criterion itself only the factors contributing to it can be examined. The main factors for controlling a large number of qubits in the envisioned setting are the mean area of the electronics, their power dissipation and the number of cables needed for connection to other temperature stages. One aim of this chapter is to identify the parameters of the control electronics which influence these scalability factors and thus the scalability.

For the feasibility the main concern is whether the control concept geared towards scalability can comply with the specifications derived from the qubit control requirements. The research into qubits and their optimal control is still ongoing, so the existing specifications are subject to change. Next to the qubit specification also the compatibility with the general experimental setup is of concern for future testability. Moreover, this experimental setup is set to vary over time as well. With the conceptual study done in this chapter, the models behind the study can be adapted to changes easily. This is a deciding advantage compared to a complete circuit design.

All in all, the different factors of the feasibility and scalability influence each other and depend on a vast amount of parameters. This makes an accurate suitability study so

[10] Excerpts from the results of this chapter have been published in [78].

complex. The examination of specification parameters for example necessitates the electrical units in the system to be broken down to basic components like capacitors. For this, a very detailed plan for the functionality of all units and how they work together in the bigger system needs to exist. Overall, the scalability of the control electronics can be described as a complex multi-variable optimization problem where the specifications are secondary conditions.

In order to solve the challenge in this chapter, the first step is to derive the requirements for the control electronics from current qubit experiments (Sec. 3.2). Then a high-level scalable concept is developed from these requirements (Sec. 3.3). In the next steps for each unit and subunit a scalable architecture is devised, or several scalable candidates are proposed. With the architecture known, detailed circuit concepts are developed, and the feasibility of the concepts is checked.

In case of partly analog circuits the sizing of the basic components is done as well as part of the feasibility check. This is important for the analog parts, as component sizes significantly impact their performance. The sizing not only tests the compliance with the specifications in respect to noise but determines parameters relevant to the area and power consumption also. These parameters are used in a next step to ascertain and compare the area and power consumption of different architecture candidates for the units (Sec. 3.4.1). With the most scalable options known for all units, the area and power consumption estimation of the complete electronics is conducted (Sec. 3.4.2). Discussions, improvement considerations and a conclusion are presented at the end.

As basis for the area and power estimations a 65 nm CMOS process has been chosen because it is available and a well-established and specified technology. The standard models which describe the properties of devices in CMOS technologies are so called SPICE-based models. The valid temperature range of these models only goes down to 220 K, which is far away from a temperature below 1 K at which the qubits work. As the models are not valid and no extensive characterization of standard CMOS technologies at cryogenic temperatures has been done yet, only the room temperature models can be used. It has already been exemplary shown, that for technology nodes below 90 nm, the operation of CMOS at cryogenic temperatures is possible and not significantly different from room temperature [10]. Therefore, room temperature technology parameters can be used for first estimations.

Some electrical functionalities are not placed at the lowest temperature stage, for example circuits for the generation and stabilization of reference voltages, clock signals and power supply voltages. These voltages and signals are costly to generate in terms of either circuit complexity or area or power consumption. This is an issue especially with the limited resources at the lowest temperature level. As these signals and voltages can be shared by the electronics for all qubits the overall effort to connect different temperature stages for this is comparatively low. Therefore, these circuits are not in the focus of this work.

## 3.2 Requirements for qubit operation extracted from current lab experiments

Relevant scalability studies for control electronics need specifications that are based on real qubit experiments. The specifications in this work are the result of the cooperation between the ZEA-2 at the Forschungszentrum Jülich and the Quantum Technology Group of Hendrik Bluhm at RWTH Aachen University. The group provided data and experience with their current GaAs qubit experiments. Some of the specifications are unique to GaAs qubits, but a significant part of the necessary functionality is in principle usable for other types of semiconductor qubits as well. This means that the results in this work have some relevance for them too.

It was concluded that for potential scalable qubit operation and control it is necessary for the electronics to provide:

- 2 different kind of signals for in total 10 electrodes:
  - 8 independently variable DC signals
  - 2 independently variable rectangular pulse sequence signals
- A set of functionalities and properties:
  - Have an adaptable pulse sequence pool
  - Include a qubit tuning possibility through sweeping the voltage of one of the DC signals
  - Include initialization, gate operation and readout sequences
  - No waiting and delay time between pulse sequences once operation has started

Detailed performance specifications for the two signal types are listed in Tab 3.1. The number of electrodes used to define the quantum dot (Fig. 2.3) plus two for an additional sensing dot set the number of bias signals $N_{bias} = 8$. The range of the bias signals is set with a maximum value of $V_{range,bias} = 1\,\mathrm{V}$, which means the voltage is defined as negative towards the sample ground. A negative voltage is necessary to locally deplete the 2DEG at the interface of the heterostructure. A high bias resolution with $n_{bias} = 12\,\mathrm{bit}$[11] is expected to be needed, according to the room temperature setup, to create a well-defined dot. The bias voltage has to be finely adjustable to compensate for the effect of small inhomogeneities in the sample material. At the same time, the overall process variability is large compared to this. This in turn leads to the large range of 1 V with a high resolution.

[11] The absolute resolution $res_{bias}$ as a voltage is given through $res_{bias} = V_{range}/2^{n_{bias}}$. For convenience the number of bit figure $n$ will be used further.

The stability specification $\delta V$ defines the maximum deviation from the nominal value that is permissible without inadvertently influencing the qubit state too much. This not only includes effects like noise but also glitches and drift changes at all times during operation. As long time drift cannot be estimated adequately at this point, the stability is reduced to effect on a shorter time scale like noise and leakage. Other faster transient effects such as glitches are not studied further, because the impact of these effects depends heavily on parasitic components. To investigate them detailed circuit schematic and layout simulations would be needed, which are beyond the scope of this work. The stability value of $\delta V_{bias} = 3\,\mu V$ for the bias voltages is derived from the expectation of the qubit experimentalists that this is below the level of quasi static charge noise present in the sample anyway. For the state manipulation a number of $N_{RF} = 2$ RF signals are

| Specification | Symbol | Value |
|---|---|---|
| Bias signals | | |
| Number of bias signals | $N_{bias}$ | 8 |
| Bias range | $V_{range,bias}$ | 1 V |
| Bias stability | $\delta V_{bias}$ | 3 µV |
| Bias signal resolution | $n_{bias}$ | 12 bit |
| RF signals | | |
| Number of RF signals | $N_{RF}$ | 2 |
| RF amplitude | $V_{range,RF}$ | 4 mV |
| RF signal resolution | $n_{RF}$ | 10 bit |
| RF stability | $\delta V_{RF}$ | 8 µV |
| RF sample rate | $f_{sample,RF}$ | 300 MHz |
| RF pulse length | $l_{pulse}$ | 16 samples |
| Number of RF sequences | $N_{pulses}$ | 16 |

Table 3.1: Summary of current set of system specifications

necessary, one for each dot (Fig. 2.3). The RF signals are defined as rectangular pulse sequences with a sample rate of $f_{sample,RF} = 300\,\text{MHz}$. The range with $V_{range,RF} = 4\,\text{mV}$ is low compared to the bias signals. Also, the resolution given through $n_{RF} = 10\,\text{bit}$ is slightly lower compared to the bias signals. The stability of the RF output voltage $\delta V_{RF}$ should be better than $\delta V_{RF} = 8\,\mu V$[12]. The number of pulse sequences $N_{pulse} = 16$ is an approximation determined by needed operations for a universal set, potential surface

[12]The noise spectral density has to be below $v_n = 0.4\,\text{nV}/\sqrt{\text{Hz}}$. This leads to a root mean square (RMS) value of $v_{RMS} = 8\,\mu V$ for a bandwidth of $\Delta f = 400\,\text{MHz}$ with $v_{RMS} = v_n\sqrt{\Delta f}$. The bandwidth is similar to the so-called filter function [82] bandwidth as given by [83].

code error correction, and some additional operations for trouble shooting. Each of the 16 sequences has a pulse length of $l_{pulse} = 16$ samples.

## 3.3 Concept for scalable cryogenic control electronic

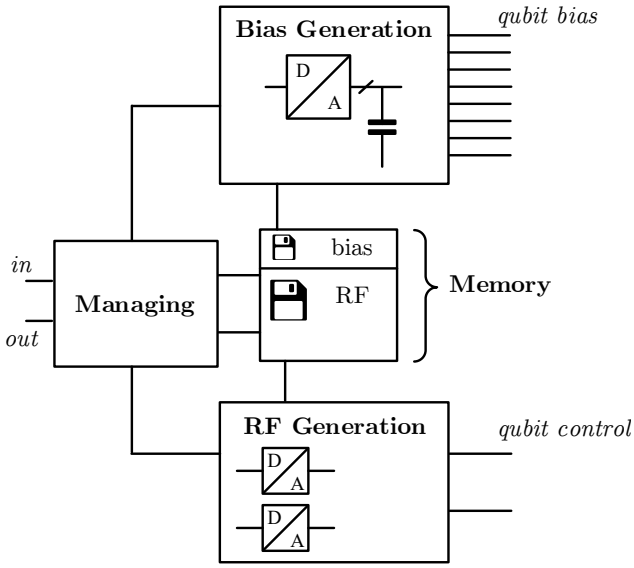


Figure 3.1: Electronics system model with its units

The system concept resulting from all scalability conditions and the qubit specifications is shown in Fig. 3.1. The concept presented contains the control electronics for one qubit. The bias and RF generation units shown provide the signals to define and control the qubit. With this placement the distortion of the signal due to transfer distance is minimized. Both signal generation units work with values stored in the local memory. This significantly reduces the data throughput in comparison to external memory. The greatest reduction is achieved with the RF generation. With the memory placed externally at another temperature stage the following data throughput would be needed (values from Tab. 3.1):

$$throughput_{external} = f_{sample,RF} \cdot n_{RF} \cdot N_{RF} = 6\,\text{Gbit/s}. \tag{3.1}$$

For 1000 qubits this amounts to a data throughput of 6 Tbit/s. In the peripheral component interconnect express (PCIe) 5.0 bus [84, 85] used in classical computers this would amount

to more than 1500 cables. With local memory, only the information which sequence has to be applied to the qubit, has to be transferred from a higher temperature level. With 16 possible sequences, two signals and an additional header bit, the data word to transfer commands during qubit operation is $l_{op} = 9$ bit long. A sketch of the dataword is shown in Fig. 3.2. Each identifier of a sequence has a bit length of $l_{id} = \log_2 16 = 4$. The resulting data throughput with this internal memory is:

$$throughput_{internal} = \frac{f_{sample,RF} \cdot l_{op}}{l_{pulse}} = 0.17\,\text{Gbit/s}. \tag{3.2}$$

This is a reduction compared to the external memory by a factor of 35. For 1000 qubits the resulting data rate of 170 Gbit/s could be covered by 44 PCIe cables, which is much more area efficient.

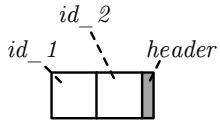


Figure 3.2: RF data word with composition

The mostly digital managing unit controls the other units and acts as a communication interface to the outside. A crucial point of the interface to higher temperatures is the number of cables necessary. In Tab. 3.2 a list of necessary outside connection signals is given. Some of the signals for one qubit can be shared with other qubits, such as reference voltages. This is indicated by the 'Share' column in the table.

| Content | Type | Direction | Share | Number |
|---|---|---|---|---|
| Data and command | digital | in | no | 1 |
| Feedback | digital | out | no | 2 |
| Reference bias | analog | in | yes | 3 |
| Reference RF | analog | in | yes | 4 |
| Digital Supply | digital | in | yes | 5 |
| GND | analog | in | yes | 6 |
| Clock | digital | in | yes | 7 |

Table 3.2: Minimum necessary connections to electronics from outside for one qubit

The digital data and feedback signals cannot be shared between qubits. However, time multiplexing is possible here, as for example the usual clock frequency of the PCIe bus

is significantly higher than the sample frequency of the RF generation dictates. This would again reduce the number of cables needed to connect the control electronics chip to higher temperatures. For a more conservative number, the number of cables $N_{cable}$ with the cryogenic control system can be given by:

$$N_{cable} = 2 \cdot N_{qubit} + 5 \tag{3.3}$$

Compared to the minimum number of wires $N_{cable,exp} = 10 \cdot N_{qubit}$ used in current experiments, this is already some improvement. However, besides the number of cables necessary, also the shielding and therefore the cross section can be reduced. This helps to simplify the connectivity challenge outlined in Chap. 1. While in current experiments all the 10 cables transmit highly noise sensitive analog signals, now the main number of signals are digital signals. These signals are less sensitive to noise. With the opportunity to time-multiplex the digital signals the connectivity concept is further scalable for higher numbers of qubits.

Not included in the model are additional circuits which enhance the quality of the non-digital and the supply signals after transmission through cables. The details depend a lot on the specific implementation of the circuits which puts it beyond the scope of this work.

The model presented in Fig. 3.1 contains all necessary functionality for one qubit. However, some units, such as the memory, could be further shared between qubits to reduce the hardware effort.

The following subsections present the units of the control electronics as depicted in Fig. 3.1. The more detailed functionality of the units and subunits is not described in this chapter, as an in-depth study of the functionality and the behaviour of the units will be presented in Chap. 4. For this reason, all circuit concepts not directly relevant to the discussion in the text have been put in App. A. A detailed understanding of them is not necessary at this point, but they are included for completeness.

### 3.3.1 Memory

The memory subunit is divided into RF and bias memory parts. This keeps the hardware costs as low as possible, because the two parts work with different dataword lengths. The signal resolution of the RF signal is lower than the bias signal and thus the dataword used in the RF memory can be shorter than the one in the bias memory. This leads to a reduction in the memory needed. The bias memory part stores only one word per electrode $N_{bias} = 8$ with a resolution of $n_{bias} = 12\,\text{bit}$. On top of that one additional dataword (+1) is allocated to the bias memory. This extra word is necessary for the tuning

functionality (see Sec. 4.5.1). With $N_{pulses} \cdot l_{pulses} = 256$ datawords in the RF memory at a resolution of $n_{RF} = 10\,\text{bit}$ the complete memory space is:

$$(8 + 1) \cdot 12\,\text{bit} + 256 \cdot 10\,\text{bit} = 2.7\,\text{kbit}. \tag{3.4}$$

In order to address the complete RF memory space, an address with the length of $l_{address} = \log_2(256)\,\text{bit} = 8\,\text{bit}$ is necessary. In this system concept the memory is envisioned as Flip-Flop register memory which is driven by a clock signal (detailed concept can be seen in App. A, in Fig. A.3). This type of memory has been shown to work at cryogenic temperatures [86]. Other and more area efficient technologies such as SRAM have not yet been proven to be functional at low temperatures. The operation of these technologies at cryogenic temperatures is also expected to be more challenging as analog functionalities are employed. A deviation in functionality between cryogenic and room temperature can be expected. The whole memory is implemented with serial-in-parallel-out registers. As such writing data into one register takes as many clock cycles as the register is long, while the readout is possible in one clock cycle. A parallel readout is advisable, because the timing during qubit operation is critical and no unspecified delay can be tolerated. In contrast to that the exact timing during data read in is insignificant because no qubit is active at that time. The serial write process takes longer but simplifies the wiring and therefore could reduce the area consumption. On top of that it fits together with the serial data transmission from higher temperature levels (see managing unit). In the RF memory part two values are read out simultaneously. This is necessary to supply both electrodes with values at the same time.

### 3.3.2 Managing Unit

The managing unit is the second mainly digital subunit next to the memory. It is the part which steers the actions of all other subunits and is responsible for the communication with the higher levels of the quantum computer (Fig. 2.1). For data input that means the unit decodes the different datawords coming into the input and acts accordingly. Datawords can for example be data to be stored into the memory, IDs of pulse sequence to apply to the qubit and simple action commands. Through the action commands the state of the managing unit and thus the mode of operation of the control electronics can be changed. Like that a direct steering possibility is provided. The different modes of operation provide the functions listed at the beginning of this chapter. The managing unit also gives feedback after e.g. successfully writing a value into the memory. Besides steering and communicating, the managing unit also improves the clock signal quality through buffers. Further functionality to improve the quality of other signals such as the references is not included in the model. A detailed discussion of the functionality of the managing unit will be given in Sec. 4.5.1, together with all behavioral modeling.

The detailed circuit concepts on which the estimations in this chapter are based on are included in Appendix A, in Fig. A.1 and A.2.

### 3.3.3 Bias generation

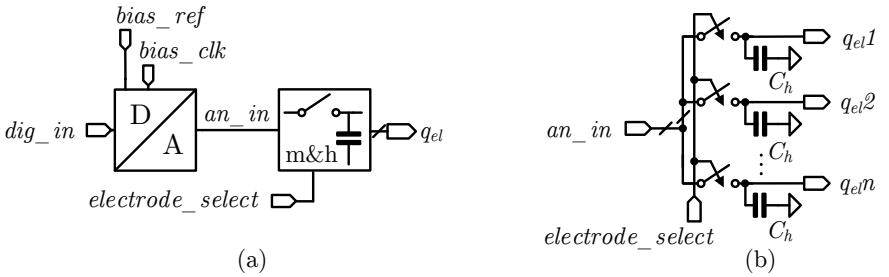


Figure 3.3: (a) Bias generation unit and (b) detailed multiplex-and-hold (m&h) subunit

The bias generation is one of the units responsible for the quality of the signals provided to the qubit. Thus, a detailed discussion of its performance and structure is of great significance for the feasibility of the electronic control system. Especially important are considerations related to the stability of the bias generation output signal. These include the noise produced by the bias generation as well as transient effects. At the same time, the area and power consumption of the circuits have to be kept in mind for scalability. Thus, the feasibility examination is done in two steps, as mentioned in the beginning of the chapter. First, a circuit architecture promising a low area and power consumption is chosen for the complete bias generation unit. Second, the element sizing is not only defined through the performance requirements but with area and power considerations as well. Additional parameters besides the elements sizing like the input resistance $R_{in}$ are also studied. They are necessary for the scalability discussion in the next chapter.

The bias generation consists of two different parts, a digital-to-analog converter (DAC) and a multiplex-and-hold (m&h) unit as shown in Fig. 3.3a. The concept uses time multiplexing to reduce the area consumption of the complete system. As such one DAC supplies the m&h with signals for all 8 bias electrodes of the qubit. The m&h then directs the voltage towards the correct electrode and stores the voltage. The storage elements for the analogue voltages are capacitors (Fig. 3.3b).

First the m&h circuit, which applies the bias voltages to the qubit, is examined in more detail. Two circuit parameter values have to be determined for this component, the size of the storage capacitor $C_h$ and the frequency at which the voltage on each capacitor is refreshed $f_{refresh}$. The general boundaries of appropriate $C_h$ sizes are given by the technology manufacturer rules. On top of that, the specifications influence the capacitor

size through the stability requirement $\delta V_{bias}$ (see Tab. 3.1). The voltage stability is in turn influenced by noise and by different leakage possibilities. However, the leakage effects not only the capacitor size but $f_{refresh}$ as well.

In the referenced CMOS technology several capacitor realizations exist, but metal-insulator-metal (MIM) capacitors have the highest capacitive density and are thus chosen [87]. The technology determined minimum capacitance for MIM capacitors is $C_{min} = 10\,\text{fF}$ (see Tab. 3.4) [87] and for area scalability the best choice is the smallest capacitor. The noise effect seen at the electrode outputs is approximately given by the Johnson-Nyquist noise [88]

$$\overline{v_n^2} = \frac{k_B T}{C_n}, \tag{3.5}$$

with the Boltzman constant $k_B$, the operating temperature in Kelvin $T$ and the noise accumulating capacitor $C_n$. In this case $C_n = C_h$[13], which gives the noise produced at every electrode output. With the specified bias voltage stability $\delta V_{bias} = v_n = 3\,\mu\text{V}$ the noise determined minimum value is $C_h = 307\,\text{fF}$. In total the minimum capacitor value is thus $C_h = 307\,\text{fF}$.

The leakage examinations are only done for the electronics parts with the assumption that no significant leakage is possible through the electrodes of the qubits. Remaining possibilities for leakage in the electronics are one, the storage capacitors themselves and two, the switches connected to *electrode_select* (Fig. 3.3b) and the DAC output *dac_out* (*reset* switch, Fig. 3.4c). All the following considerations regarding leakage are done with room temperature results in mind. There exists no comprehensive study on leakage at cryogenic temperatures. First results indicate a leakage reduction at low temperatures at least for some leakage mechanisms [10].

The referenced MIM capacitors have an insulator thickness around $t_{ins} = 10 - 30\,\text{nm}$ [89]. This is expectedly thick enough to avoid measurable electrical currents through it with a maximum voltage of $V_{range,bias} = 1\,\text{V}$. Other sources of leakage currents are the mentioned MOS switches. In the used 65 nm technology the dominant leakage effects in transistors are gate and sub threshold leakage [90]. Since the *electrode_select* switches do not separate large voltage domains during operation (assuming similar electrode voltages), only insignificant sub threshold leakage is expected to occur. If gate leakage is an issue here, thick oxide transistors could be used instead of regular ones.

For the *reset* switch the most relevant leakage is the sub threshold leakage. The leakage effect through the *reset* switch can be significant because the potential difference between the capacitors and ground can be up to $V_{range,bias} = 1\,\text{V}$, with a resistance $R_{off} = 1\,\text{T}\Omega$ of the open transistor. The resulting leakage current warrants periodic updates of the

[13] The electrodes of the qubit also have a small capacity, which are neglected here.

voltage on the capacitors with a frequency

$$f_{refresh} = \frac{V_{range,bias}/R_{off}}{\delta V_{bias} C_h}. \tag{3.6}$$

In the numerator of the fraction in Eq. 3.6 the maximum leakage current is given, and in the denominator, the maximum tolerable mean charge loss from all capacitors together is calculated. For the set minimum value $C_h = 307\,\text{fF}$ and the given values of Tab. 3.4, $f_{refresh} = 1.1\,\text{MHz}$ is obtained.

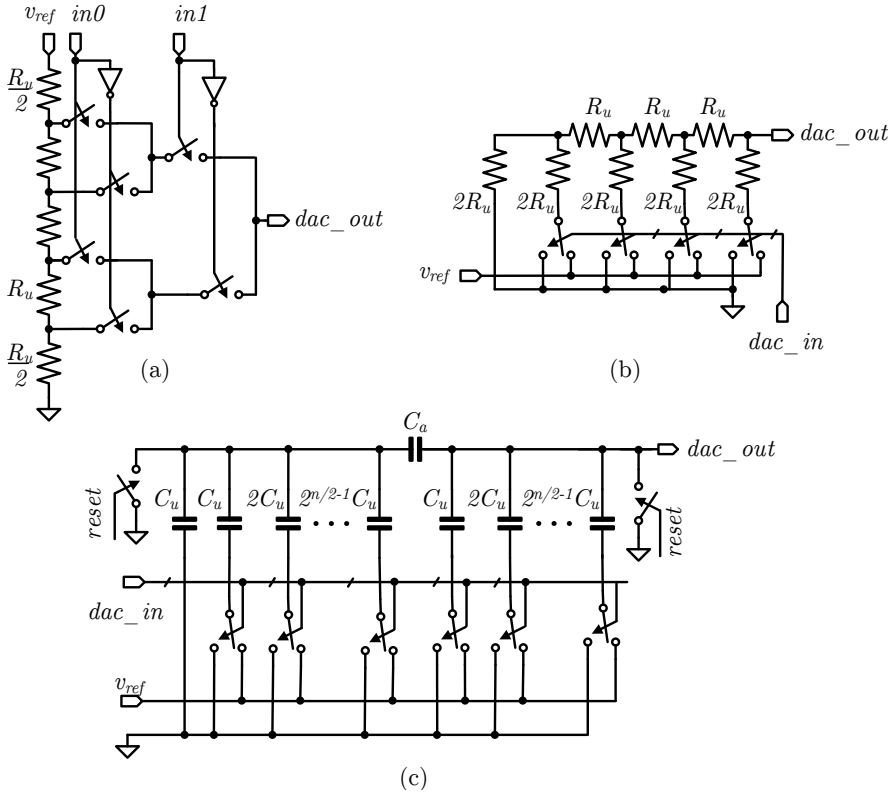


Figure 3.4: Circuit architectures of all DAC types considered: (a) Kelvin Divider DAC, (b) Ladder DAC, (c) Capacitive Divider DAC

In the second step of discussing the bias generation part, the other component, the DAC, is examined. For the DAC itself different architectures are possible [91] and the best suited architecture is to be found. Considered here are DACs shown in Fig. 3.4a Kelvin

Divider DACs (Kelvin DAC), Fig. 3.4b Ladder DACs and Fig. 3.4c Capacitive Divider DACs (Cap DAC). The other two existing types of DACs, oversampling and current source DACs are not suitable here. Oversampling DACs run at a higher speed and need significant digital circuitry. This leads to a comparatively high power consumption, which makes them unsuitable for this very low-power application. DACs made with current sources employ transistor current mirrors to create accurate, weighted currents. As matching significantly deteriorates at cryogenic temperatures [67, 72, 92, 93] and with it the quality of current mirrors, these DACs are considered to be not precise enough. The types of DACs investigated here is therefore reduced to the DACs shown in Fig. 3.4. In the schematics the output of the DACs is denoted by *dac_out*, while either *dac_in* or *inX* denote the input. The *dac_in* includes all input bits, while *in*0 for example is only one digital input bit. As a reference for all DACs a voltage source with voltage $v_{ref}$ is assumed.

Similar to the m&h, the sizing of the DAC elements has to be determined. In case of the Ladder DAC and the Kelvin DAC the size boundaries of the unit resistor $R_u$ have to be found, while for the Cap DAC the unit capacitor size $C_u$ is to be set. The components are again subject to the technology rules and also the stability requirements specified in Tab. 3.1 are to be taken into account. Next to that also scalability considerations for power and area consumption have to be observed. This can be done with the input resistance $R_{in}$ or capacitance $C_{in}$ looking from the supply. For the stability requirement the noise produced at the output of the DAC is of interest. This noise can be calculated with the output resistance $R_{out}$ or output capacitance $C_{out}$ respectively.

In case of the Cap DAC a lower bound is to be found for the unit element $C_u$. The output noise of the Cap DAC is given by Eq. 3.5 for $C_n = C_{out}$, so that a lower area is in accordance with a lower noise and a lower $C_{in}$. Here, $C_{out}$ denotes the output capacitance with $C_{out} \approx 2^{n/2} C_u$ and with $n$ the resolution. For a 12 bit DAC with a maximum noise of $v_n = \delta V_{bias} = 3\,\mu\text{V}$, the lower bound of the unit capacitance is to be set to $C_u \geq 4.8\,\text{fF}$. As this is lower than the minimum capacitance determined by the technology, the unit element size of $C_u = C_{min} = 10\,\text{fF}$ is chosen for further considerations (all values summarized in Tab. 3.3). However for bias resolutions smaller than 10 bit, a bigger minimum capacitance would be necessary to comply with the stability requirements.

For the DACs with resistor elements the expected dominant Johnson-Nyquist noise is given by

$$\overline{v_n^2} = 4 k_B T R_{out} B, \tag{3.7}$$

with again the Boltzmann constant $k_B$, the operating temperature $T$, the output resistance $R_{out}$ and the bandwidth $B$ of the DAC. The bandwidth of the DAC is assumed to be 10 MHz. This is high enough not to distort the output signal and low enough not to collect too much noise. The bandwidth of the DAC itself is expected to be higher, but additional

low pass filtering can reduce it accordingly. The noise is proportional to the resistance value $R_{out}$. For this reason the resistor values calculated with Eq. 3.7 represent an upper bound. In general, this means a lower resistance leads to lower noise, however the trade off to area and power consumption is different. While a lower resistance increases the power consumption, the area is reduced.

In case of the Kelvin divider DAC the output resistance $R_{out}$ and therefore the output noise are dependent on the digital input code. In the worst case $R_{out}$ is given by $R_{out} = 2^{n-2}R_u$. At an operating temperature of $T = 200\,\text{mK}$, with a resolution of $n = 12\,\text{bit}$, the unit resistance is determined with $R_u \leq 80\,\Omega$ (using Eq. 3.7) to comply with the noise requirements. For the maximum considered resolution of $n = 16\,\text{bit}$ that upper bound is lowered to $R_u \leq 5\,\Omega$. The resistor type used is assumed to be polysilicon and has a minimum resistance of 15 Ω in the considered CMOS technology. Thus, the unit resistance cannot be implemented for lower values, which sets $R_u = 15\,\Omega$ (Tab. 3.3). Several resistors in parallel would decrease $R_u$ but also increase the area, which is not wanted. The lowest possible resistance value is chosen, because with $R_{in} \geq 2^n \cdot R_u$ the input resistance is high enough for an overall low power consumption. For the resolutions of 15 and 16 bit the Kelvin divider DAC would produce more noise than allowed in the specification. This has to be kept in mind for the decision on the architecture suitability.

In case of the Ladder DAC the output resistance is $R_{out} = R_u$, which leads to $R_u \leq 81\,\text{k}\Omega$ (using Eq. 3.7) at the cryogenic temperature with a resolution of $n = 12\,\text{bit}$. Even for a maximum resolution of $n = 16\,\text{bit}$ the unit resistance is still higher than the minimum value. The input resistance of the Ladder DAC is code dependent [94]:

$$R_{in} = 3R_u \left[ \sum_{x=1}^{n} b_x \left(1 - 2^{-2x}\right) - \sum_{x=1}^{n-1} \sum_{y=x+1}^{n} b_x b_y \left(2^{2x-1} + 1\right) \left(2^{-x-y+1}\right) \right]. \tag{3.8}$$

Here, $R_u$ is the unit resistor, $b$ is the digital input code to the DAC and $n$ the resolution of the DAC. As the input resistance is quite low in the worst case (an input of e.g. [0101010101010101], the unit resistance is set to $R_u = 150\,\Omega$ (Tab. 3.3). This lowers the power consumption of the DAC (see Sec. 3.5) at an acceptable trade of to the area and the noise.

| | Kelvin | Ladder | Cap |
|---|---|---|---|
| Unit element | $R_u$ | $R_u$ | $C_u$ ($C_a$) |
| Unit value | 15 Ω | 150 Ω | 10 fF |
| No. unit elements | $2^n$ | $3n$ | $2 \cdot 2^{n/2} - 1$ |
| No. switches | $2^{n+1} - 2$ | $2n$ | $2n$ |

Table 3.3: Parameter of suitable DAC types dependent on the resolution $n$

Tab. 3.3 summarizes the chosen unit element values for the different DAC types. With these unit elements the DACs in general comply with the requirements on the voltage stability. All in all the values were chosen to be as low as possible in order to be as scalable as possible. In summary the qubit control is feasible with all these DAC topologies, however for a final decision on a candidate more detailed area and power estimations will be made in the next section.

### 3.3.4 RF generation

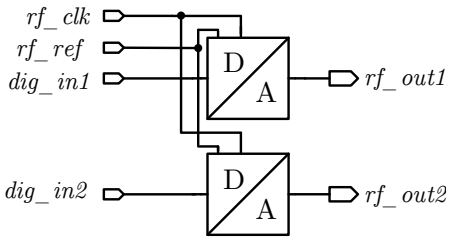


Figure 3.5: RF generation model with units

As shown in Fig. 3.5 the RF generation part consists of two DACs. Each of these DACs supplies the RF pulse sequences to one of the RF electrodes. The concept avoids multiplexing in favor of a reduced complexity. The DACs operate at a sample rate of $f_{sample} = 300\,\text{MHz}$ which is set by the requirements (Tab. 3.1). This leads to a clock frequency of 600 MHz due to refresh phases e.g. in the Cap DAC. The bandwidth of the DACs is assumed to be 600 MHz, which is enough for the signal generation, even though the effects of the low pass filtering are expected to be evident. Again the bandwidth of the DAC itself can be higher but can be reduced with additional filtering.

The considerations for the sizing of the DAC unit elements are similar to the bias generation. In principle all the DAC candidates for the bias generation (Fig. 3.4) could be used for the RF generation, as well. However, some parameters are different for the RF generation. One, the stability is more relaxed with $\delta V_{RF} = 8\,\mu\text{V}$. Two, the assumed resolution is less challenging with $n = 10\,\text{bit}$. Three, the bandwidth is $B = 600\,\text{MHz}$. Not changed from the bias generation considerations is the operating temperature $T$ of 200 mK.

In case of the Cap DAC $C_u$ is bound to $C_u \geq 1.3\,\text{fF}$ from the noise considerations. All examined resolutions from 6 to 16 bit lead to capacitance values lower than the minimum technology value. Thus, the unit element is set to the lowest possible value with $C_u = 10\,\text{fF}$. For the Kelvin DAC, the upper bound of $R_u$ is $R_u \leq 38\,\Omega$ for $n = 10\,\text{bit}$. However, for resolution above 11 bit the maximum tolerable resistance due to noise is lower than the

technology minimum value. Thus, the unit element is set to the technical minimum of $R_u = 15\,\Omega$, with the reminder that resolution above 11 bit are problematic because of noise. In case of the Ladder DAC the upper bound is given with $R_u \leq 10\,\mathrm{k}\Omega$. This value is independent of the resolution. As for the bias generation, the Ladder DAC suffers from a potential low input resistance and a resulting high power consumption. For this reason the unit resistance is set higher than the minimum technical value to lower the power consumption. With $R_u = 150\,\Omega$ the same value is chosen as for the bias generation. In conclusion the values summarized in Tab. 3.3 are valid for both the bias and the RF generation DACs.

### 3.3.5 Feasibility conclusion

In summary the prospects for a feasible CMOS control electronics with sufficiently low noise are given under the constraint of an optimized area and power consumption. Limitations to that could be the resolutions of the bias or RF signals, at which point the unit element sizes could have to change. For the unit elements always the smallest possible values have been chosen, as this is favorable for the power and area consumption. However, the minimum sizing effects the matching negatively. In general it is known that the smaller a device the worse the matching is. The matching among others, influences the linearity of the DACs. The linearity of the DACs is not a high priority, as the qubit control does not require it and some nonlinearity effects can be reduced by pre-distortion. Still, the DAC performance has to be reevaluated after circuit design and layout and the unit element sizes might have to be adjusted.

## 3.4 Area and Power estimations

After the feasibility assertion of cryogenic control electronics the next step is to study the scalability in more detail. The criteria employed are the estimated power and the area consumption of the circuit concepts of the last section. The area and power estimations use the parameters of the referenced 65 nm CMOS technology in addition to the knowledge of the circuit concepts. A summary of all used parameters is given in Tab. 3.4. In the first block of the table, the used effective densities for the analog circuit elements are listed. Here, effective means that area for device terminals is included. The relevant parameters for the digital parts follow in the next block. These describe the mean properties of a transistor as used in the digital circuit parts. The next block in Tab. 3.4 contains the technology defined supply voltage $V_{dd}$ and the minimum values for resistors and capacitors that were already mentioned in the last section. The second to last block lists the unit element sizes for the signal generation parts, as set in the last section. That means that these parameters are dynamic and have to be re-calculated for

changed settings. The last block of Tab. 3.4 lists the operational parameters, which are the basis for the power estimations. The activities are set by the circuit concept and the RF clock frequency is determined by the circuit specifications, but the bias clock frequency $f_{clk,bias}$ is derived from the refresh frequency $f_{refresh}$. Thus the bias clock frequency can change with different settings like the temperature.

| Parameter | Symbol | Value |
|---|---|---|
| Resistive density | $\rho_R$ | 21.4 $\Omega/\mu m^2$ |
| Capacitive density | $\rho_C$ | 1.75 fF/$\mu m^2$ |
| Mean transistor area | $A_{MOS}$ | 0.375 $\mu m^2$ |
| Mean transistor cap. | $C_{MOS}$ | 150 aF |
| Mean transistor off res. | $R_{off}$ | 1 TΩ |
| Mean transistor on res. | $R_{on}$ | 5 kΩ |
| Min. Resistance | $R_{min}$ | 15 Ω |
| Min. Capacitance | $C_{min}$ | 10 fF |
| Digital supply voltage | $V_{dd}$ | 1 V |
| Hold cap. s&h bias gen. | $C_h$ | 307 fF |
| Unit cap. DACs | $C_u$ | 10 fF |
| Bias memory activity | $\sigma_{biasmem}$ | 0.306 |
| RF memory activity | $\sigma_{RFmem}$ | 0.026 |
| Managing comp. activity | $\sigma_{con}$ | 0.5 |
| Clock freq. bias | $f_{clk,bias}$ | 2.22 MHz |
| Clock freq. RF | $f_{clk,RF}$ | 600 MHz |

Table 3.4: Parameters used for area and power estimation for the 65 nm CMOS technology extracted from room temperature models

The area and power estimations are done with a framework of different Matlab functions. An overview of the framework is given in Fig. 3.6. The different Matlab estimation functions are mainly set apart by the different electrical architectures options that they consider 3.6. For example, there are functions just for the different DACs, but also for different options in the complete control electronics. The complete power and area consumption is only calculated when the underlying electronics include the complete system. Next to the architectures the functions are also distinguished by the set of technology parameters they use. In the current setting those parameters refer to a 65 nm technology, but other technologies will be used later in addition (see Sec. 3.5). All functions use the same set of specifications as derived in Sec. 3.2 and all of them have the same input variables. Not all of these variables are used in this section, but they are

in place for studies in later sections. Before the calculation of any area or power can be done the dynamic circuit parameters have to be defined. This process has already been described in Sec. 3.3.3 and 3.3.4.

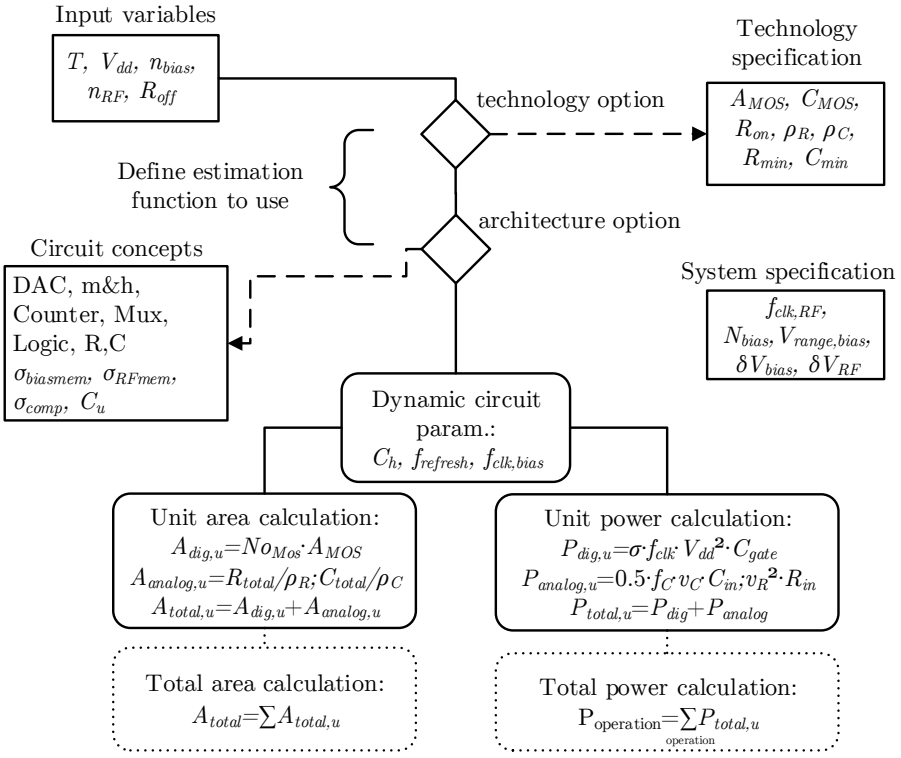


Figure 3.6: Matlab framework for power and area estimations

With the dynamic circuit parameters set, all information for the estimations is at hand. Both area and power modeling starts with the single units or even subunit and splits the model into analog and digital parts. For each modeled part the logical circuit concepts are broken down to the number of transistors $No_{MOS}$ and with the mean area of a transistor in a logic circuit $A_{MOS}$, the digital area for each unit is estimated with $A_{dig,u}$. The analog area of the unit $A_{analog,u}$ is given through the summed up resistance $R_{total}$ or $C_{total}$ and the respective mean effective density $\rho_R$ or $\rho_C$. With the total unit area added up to $A_{total_u} = A_{dig,u} + A_{analog,u}$ the area of the complete control electronics can be calculated with the sum. For units where no analog components are included $A_{analog,u} = 0$. Additional area for wiring is however not considered.

The estimation for the power consumption follows the principle of the area modeling, but a few more parameters are relevant. The power modeling of the digital circuits is based on the switching power of a transistor $P_{switch} = \sigma \cdot f_{clk} \cdot V_{dd}^2 \cdot C_{MOS}$, with the switching frequency $f_{clk}$, the supply voltage $V_{dd}$ and the transistor gate capacitance $C_{MOS}$. This is based on the assumption that the other contributors to the digital power consumption, the short-circuit power and the leakage power [95], can be neglected. For the considered technology these contributions are small compared to the switching power [90, 95–100]. It follows that for one unit or subunit the power consumption $P_{dig,u}$ is given by

$$P_{dig,u} = \sigma \cdot f_{clk} \cdot V_{dd}^2 \cdot C_{gate}, \tag{3.9}$$

with the total circuit gate capacitance $C_{gate}$. The capacitance is defined as the sum of the gate capacitances of all transistors. The other variables are the digital supply voltage $V_{dd}$, the clock frequency $f_{clk}$ and the activity $\sigma$ of the circuit. The activity is the rate of switching done in the circuit in relation to the clock frequency. It can only be measured exactly through extensive statistical testing for more complex circuits. The maximum for common clocked and edge triggered logic is 0.5. For the memory the activities can be estimated with the circuit concept, its regular structure and the knowledge of the frequency of read operations. Since the circuit design and the statistical testing is out of the scope of this work the value is set to its maximum of 0.5 for the managing component.

The power consumption of the analog parts in a unit is modeled with $P_R = v_R^2/R_{in}$ for resistors and $P_C = 0.5 \cdot f_C \cdot C_{in} \cdot v_C^2$ for capacitors. In both cases $v_R$ or $v_C$ denotes the voltage across the resistors and capacitors while $R_{in}$ and $C_{in}$ are the input resistance and capacitance. The total power of one unit with analog and digital parts is thus given by $P_{total,u} = P_{dig,u} + P_{analog,u}$. In case of a purely digital unit the analog power consumption is set to zero $P_{analog,u} = 0$.

The power consumption that is used to evaluate the scalability of the control electronics is not the sum of the power consumption of all units. The power relevant for the scalability is the power dissipated during qubit operation. During operation the temperature in the fridge has to stay constant for the qubits to work properly and as such the heat produced by the electronics has to be conducted away by the fridge. Outside the operation, for example during the electronics initialization, the heat dissipated by the electronics can temporarily exceed the cooling capabilities of the fridge. The temperature rises, but with additional waiting time before qubit operation the temperature can be lowered again. Thus the total power considered in this chapter is the power of all units active during qubit operation. The units active include the bias and RF generation, the memory and parts of the managing unit which deal with the incoming commands for the RF generation. More details on the behavior of the electronics is discussed in Chap. 4.

### 3.4.1 DAC area and power

The first area and power estimations are done for the different DAC architectures. This helps to find the optimum DAC architecture for the bias and RF generation. The circuit concepts for the DACs and the component sizing options have already been studied in detail in Sec. 3.3.3 and Sec. 3.3.4. As such the necessary input resistances $R_{in}$ and capacitances $C_{in}$ are already defined. Tab. 3.3 lists the respective numbers of logic switches, unit elements and the value of the unit elements. In order to estimate the different DACs power and area only the voltage across the resistors and capacitors and the load frequency for the capacitors have to be set. The input voltage for the power estimation is $v_{ref}$ which is assumed to be equal to $V_{range}$. This is done for simplicity, even if for some DAC architectures a slight adjustment has to be made. Depending on the DACs use case either the bias range $V_{range,bias}$ or the RF range $V_{range,RF}$ is used (see Tab 3.1). The frequency $f_C$ at which the capacitors in the Cap DAC are reloaded is either $f_{clk,bias}$ for the bias generation case and $f_{clk,RF}$ for the RF generation case.

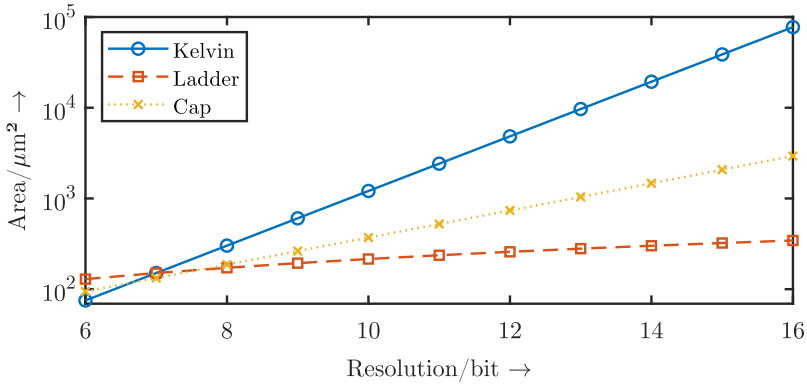


Figure 3.7: Area consumption estimation of the different DAC architectures

The estimations are calculated for different resolutions, as the needed accuracy of the signals is not final yet. Figure 3.7 shows the results of the DAC area estimation and the power consumption of the DAC types is shown in Fig. 3.8. The power consumption discerns between the bias generation configuration in Fig. 3.8a and the RF generation configuration in Fig. 3.8b. The estimation is not only done for the different signal generation conditions but also for different digital supply voltages $V_{dd}$ as well. This enables the discussion of possible improvements through the use of smaller technology nodes with lower supply voltage. As these nodes are more advanced, they also have lower feature sizes. For clarification, for the Ladder DAC only the power consumption with $V_{dd} = 1\,\mathrm{V}$ is depicted in Fig. 3.8, as this DAC type shows very little variation in the power consumption with changing $V_{dd}$.

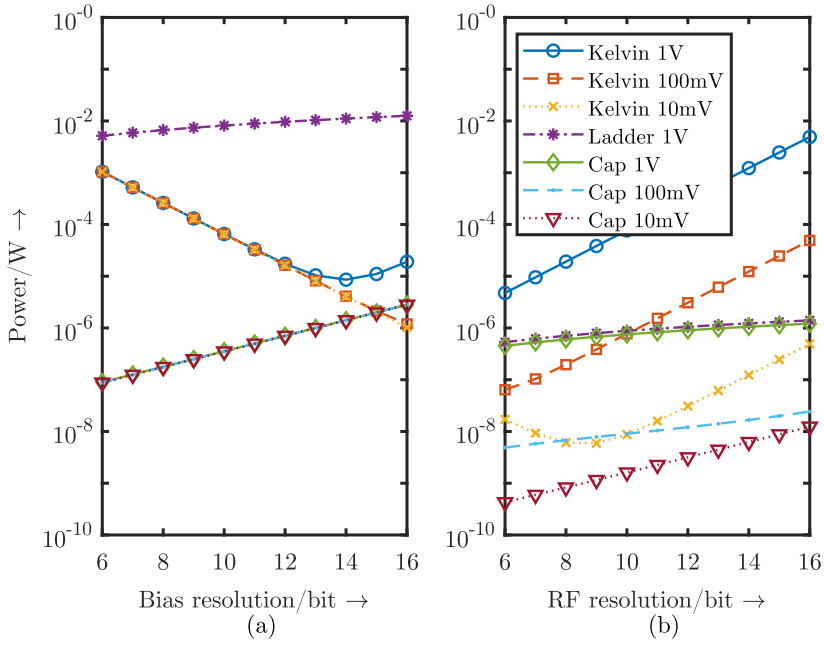


Figure 3.8: Power consumption estimation of different DAC architectures. (a) Power with varied bias resolution for the bias generation configuration and (b) power with varied RF resolution for the RF generation configuration. In both cases the power was estimated for different supply voltages.

For the Kelvin DAC the results of the power estimations seem counter intuitive for some resolutions. For all the supply voltages in the bias configuration and for the lowest supply voltage in the RF configuration, the power decreases with increasing resolution in some places. The underlying reason is the method used to estimate the power consumption. The power is the sum of the contribution from the analog and the digital part (see Fig. 3.6):

$$P_{DAC,R} = R_{in} v_{ref}^2 + 0.5 \cdot f_{clk} \cdot V_{dd}^2 \cdot C_{gate}. \tag{3.10}$$

The number of elements always increases with the resolution (see Tab. 3.3) and so does the digital power consumption. However, the input resistance also increases with the resolution $n$ as $R_{in} = 2^n \cdot R_u$. Thus, if the analog parts consumes the major part of the power, the power decreases with increasing resolution for the Kelvin DAC.

The overall best architecture for both bias and RF generation is the Cap DAC. The area consumption of that DAC type is medium while consuming the least power for most of the resolution range of the bias generation part (Fig. 3.8a). For the RF generation condition the Cap DAC consumes the least power for the complete resolution range, for each $V_{dd}$ supply voltage. For the current supply voltage of $V_{dd} = 1\,\mathrm{V}$, the Ladder DAC has only an insignificantly higher power consumption than the Cap DAC, but a much lower area consumption in comparison. As the overall goal is to move towards more advanced technology nodes and thus lower supply voltages, the Ladder DAC is nevertheless discarded as an option. From now on the Cap DAC architecture is used in all further estimations.

### 3.4.2 Control electronics area and power

With the DAC architecture chosen the area of the complete system (see Fig. 3.1) can be estimated. This is done with the Matlab framework shown in Fig. 3.6 again. From the detailed concepts the number of basic digital units and the number and value of the analog basic components are extracted. With these and the parameters of Tab. 3.4 the area of the complete system and its units can be estimated, with the results shown in Fig. 3.9. The estimations are modeled for different bias resolutions (Fig. 3.9a) and RF resolutions (Fig. 3.9b), as the requirements are subject to change. If not stated otherwise, the bias resolution is 12 bit and the RF resolution 10 bit.

For all resolutions the memory has by far the biggest contribution to the complete system area. In case of the varied bias resolution the only part significantly changing with the resolution is the bias generation. However, the effect on the overall area consumption is small (Fig. 3.9a). In contrast to that the change of the complete systems area with the changing RF resolution is obvious. Not only the area of the RF generation part increases with higher resolution, but the memory area increases too (Fig. 3.9b). With the

parameters from the current set of specifications (Tab. 3.1) the total area is 33 000 µm$^2$ which is much larger than the assumed qubit footprint of 100 µm$^2$. This means the area has to be reduced by more than two orders of magnitude to allow direct chip-to-chip bonding, as envisioned in the introduction. The power consumption is estimated the

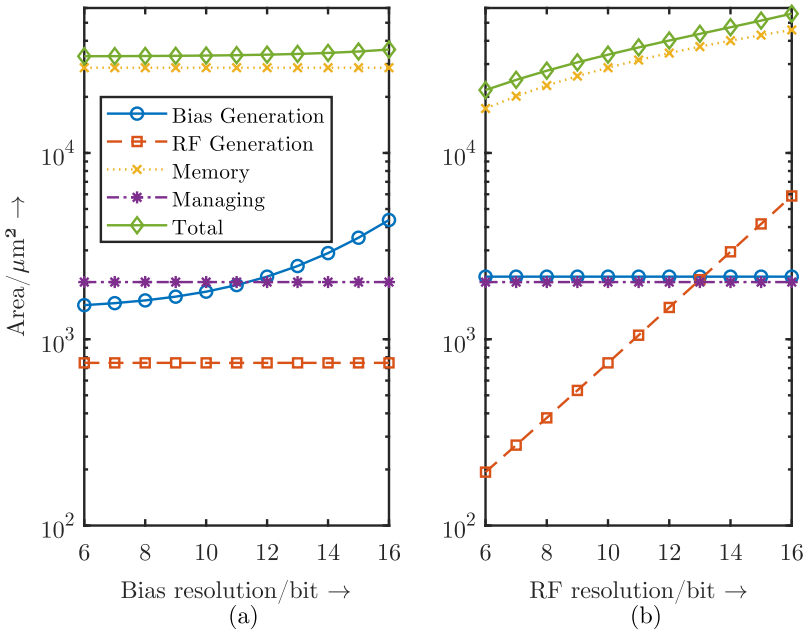


Figure 3.9: Area estimation results of the complete system: (a) variable bias resolution and (b) variable RF resolution

same way as for the DACs with the results for varying bias and RF resolution shown in Fig. 3.10. The memory not only contributes the most area, but also has the biggest part in the complete systems power consumption. As seen in Fig. 3.10 the total power consumption changes little with the resolutions. With the current specifications (Tab. 3.1) the power consumption is 0.2 mW. As the cooling power of the fridge is only a few mW at the qubit temperature, only few qubits could be controlled this way. If millions of qubits should be controlled with the current cooling power, the power consumption of the electronics has to be drastically reduced into the nW range. Compared to the needed reduction in area this is several orders of magnitudes more. Thus, reducing the power consumption is expected to be a more difficult challenge than the area consumption. However, working with a smaller number of qubits of 100 or 1000 would already be a

significant improvement compared to current experiments.

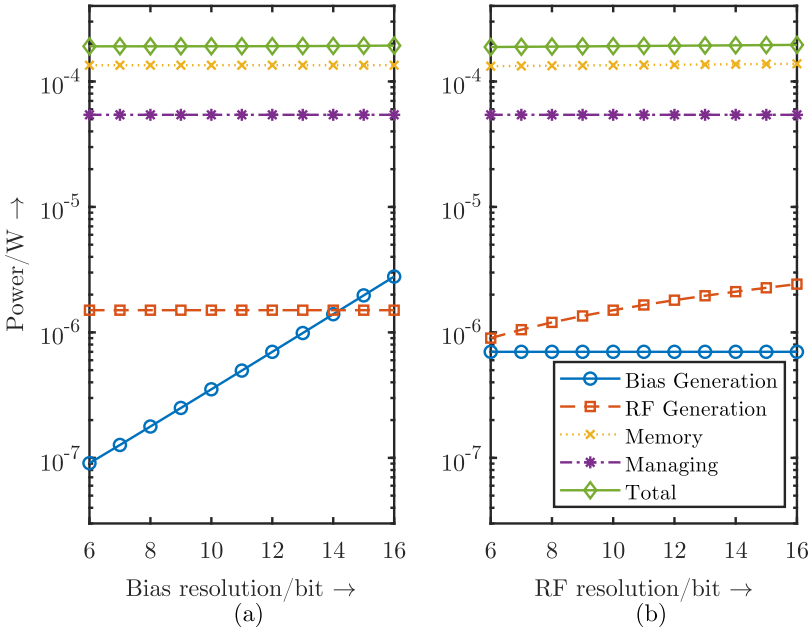


Figure 3.10: Power estimation results of the complete system: (a) variable bias resolution and (b) variable RF resolution

## 3.5 Reduction possibilities of area and power

The memory is the biggest contributor to both area and power consumption and therefore the most crucial subunit to optimize. Up to now, the memory technology used in the estimations were Flip-Flop registers as they are quite robust. Using static random-access memory (SRAM) as a low-latency and non-refresh alternative instead, reduces the total area to 7200 $\mu m^2$ (Tab. 3.5 third column). This could be possible with minor technology adaptations. The area reduction is a product of the smaller and simpler memory cells, (from 10 $\mu m^2$ to about 0.5 $\mu m^2$) which also consume less power. Thus, the switch to SRAM memory reduces the power consumption to 81 µW. Next to substituting memory cells with simpler ones, the CMOS technology node has an impact on the area and power consumption. For example the move from the referenced 65 nm to a 14 nm CMOS

technology reduces the total area to $3.0 \cdot 10^2 \mu m^2$. This is possible as the mean transistor area is reduced by a factor of 24 and the SRAM cell area shrinks by a factor of 7 [101, 102]. This area reduction also includes the use of new capacitor technologies (so-called trench capacities) with higher capacitive densities [103].

| Settings | | | | |
|---|---|---|---|---|
| Node/nm | 65 | 65 | 65 | 14 |
| $V_{dd}$/V | 1 | 1 | 100m | 10m |
| Architecture | FF | S | S | S |
| Area/$\mu m^2$ | | | | |
| Bias Gen | $2.2 \cdot 10^3$ | $2.2 \cdot 10^3$ | $2.2 \cdot 10^3$ | $1.1 \cdot 10^1$ |
| RF Gen | $7.5 \cdot 10^2$ | $7.5 \cdot 10^2$ | $7.5 \cdot 10^2$ | $3.8 \cdot 10^0$ |
| Memory | $2.9 \cdot 10^4$ | $2.6 \cdot 10^3$ | $2.6 \cdot 10^3$ | $2.1 \cdot 10^2$ |
| Managing | $2.0 \cdot 10^3$ | $1.7 \cdot 10^3$ | $1.7 \cdot 10^3$ | $7.0 \cdot 10^1$ |
| Total | $3.3 \cdot 10^4$ | $7.2 \cdot 10^3$ | $7.2 \cdot 10^3$ | $3.0 \cdot 10^2$ |
| Power/W | | | | |
| Bias Gen | $7.0 \cdot 10^{-7}$ | $7.0 \cdot 10^{-7}$ | $7.0 \cdot 10^{-7}$ | $7.0 \cdot 10^{-7}$ |
| RF Gen | $1.5 \cdot 10^{-6}$ | $1.5 \cdot 10^{-6}$ | $1.8 \cdot 10^{-8}$ | $3.2 \cdot 10^{-9}$ |
| Memory | $1.3 \cdot 10^{-4}$ | $5.0 \cdot 10^{-5}$ | $5.0 \cdot 10^{-7}$ | $3.6 \cdot 10^{-9}$ |
| Managing | $5.4 \cdot 10^{-5}$ | $2.8 \cdot 10^{-5}$ | $2.8 \cdot 10^{-7}$ | $2.2 \cdot 10^{-9}$ |
| Total | $1.9 \cdot 10^{-4}$ | $8.1 \cdot 10^{-5}$ | $1.5 \cdot 10^{-6}$ | $7.0 \cdot 10^{-7}$ |

Table 3.5: Area and power consumption for different technology and architecture options included in the model: flip-flop memory (FF), SRAM memory (S), $V_{dd}$ =digital supply voltage, Node=CMOS technology generation

Newer technologies not only have a smaller feature size which leads to a reduced power, but typically run on a lower digital supply voltage $V_{dd}$ as well. This also decreases the power consumption for newer technology nodes. On top of that, this points to another factor to lower the critical power consumption. The lowering of the digital supply voltage $V_{dd}$ has a big impact on the power consumption of the mostly digital units e.g. the memory. The mostly analog units are less effected.

A moderate reduction of the supply voltage is possible with e.g. silicon-on-insulator (SOI) processes, as these allow back body biasing. A current 22 nm process works with supply voltages down to 400 mV for example [104], and new nodes are expected to go even lower. Power supplies lower than that are possible but require extensive changes in transistor implementation techniques and are the subject of current research [105,

106]. An extrapolation of the power consumption of the whole system and its subunit for different digital supply voltages is shown in Fig. 3.11. The total power consumption depicted in Fig. 3.11 is quadratic with the supply voltage in the region between $V_{dd} = 1\,\mathrm{V}$ and 200 mV. This is due to the fact that the major contributors to the overall power consumption, the purely digital memory and the managing parts, have a quadratic function with respect to $V_{dd}$ (Eq. 3.9). Below $V_{dd} = 200\,\mathrm{mV}$ first the bias generation and at lower $V_{dd}$ the RF generation, consume a significant part of the overall power. Since the power consumption of the analog parts of these subunits do not reduce with the digital supply voltage the decrease lessens. At the minimal supply voltage of $V_{dd} = 10\,\mathrm{mV}$ the total power consumption is $7.0 \cdot 10^{-7}\mathrm{W}$, which is nearly completely attributed to the bias generation unit.

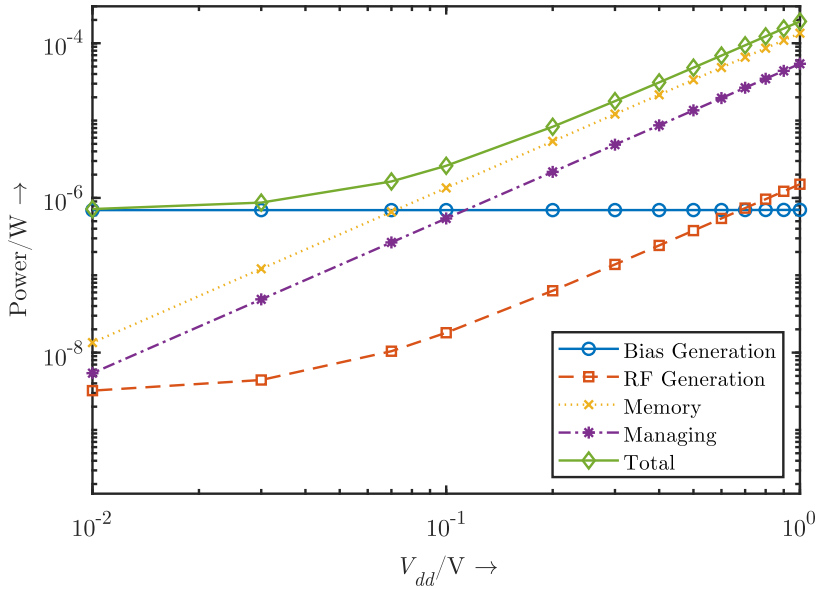


Figure 3.11: Power estimation results of the complete system for different digital supply voltages $V_{dd}$. Circuit specifications were used from Tab. 3.1 and estimations done on the basis of the 65 nm technology with parameters in Tab. 3.4.

## 3.6 Critical discussion of assumptions

For the DAC the minimum possible capacitance has been assumed for the unit element $C_u = 10\,\text{fF}$. As the summed up parasitic capacitances can go up to a similar range, the potential need for bigger unit capacitances is there. In addition to that, nonlinearity in the DACs can be a potential reason for larger unit capacitances. For the final specification of the minimum capacitance circuit schematic and layout simulations are needed. One example could be the need for unit capacitors of $C_u = 30\,\text{fF}$ instead of 10 fF for both bias and RF DACs. This capacitor increase might improve the DAC performance, but it leads to a higher power and area consumption. In Fig. 3.12a the more critical power consumption is depicted for different digital supply voltages $V_{dd}$ and $C_u = 30\,\text{fF}$. For all the power estimations in Fig. 3.12 the extrapolated values for a 14 nm technology have been used in the same way as shown in Sec. 3.5[14]. This gives an idea of the performance potential of state of the art CMOS technology. Besides that the power consumption has been estimated with SRAM technology. The overall resulting power consumption is higher than the one depicted in Fig. 3.11, with the 65 nm technology. The part wise distribution of the power to the units is still the same. This means an increase in $C_u$ has a significant impact on the overall power consumption.

The assumption of the $R_{off}$ resistor with 1 TΩ stems from the room temperature leakage current worst-case estimations. Detailed measurements on leakage at cryogenic have not been done yet, but first results show subthreshold leakage to be smaller by roughly two orders of magnitude [10]. This has an influence on the power consumption of the bias generation, and at low $V_{dd}$ on the complete power consumption. The power of the bias generation at low $V_{dd}$ is given by

$$P_{bias} = \frac{f_{refresh}}{2}(C_{in,DAC}V_{range,bias}^2 + C_{m\&h}\delta V_{bias}^2), \tag{3.11}$$

which is the power of periodically loading the capacitances of the DAC and the m&h. With the current settings the second summand can be neglected and with adding Eq. 3.6 Eq.3.11 is reduced to:

$$P_{bias} \approx \frac{C_{in,DAC}}{2 \cdot R_{off}\delta V_{bias}C_{m\&h}}V_{range}^3. \tag{3.12}$$

Thus with less leakage current and a resulting higher effective $R_{off}$, now given by $R_{off} = V_{range}/I_{leak}$, the power consumption can be significantly reduced. The reduction effect is achieved by a lower refresh rate (Eq. 3.6), while the unit capacitor is kept at $C_u = 10\,\text{fF}$. With a leakage rate lower by a factor of 100, the refresh rate can be calculated to 11 kHz and a resulting effective $R_{off} = 100\,\text{T}\Omega$. In Fig. 3.12b the power consumption vs. $V_{dd}$ with the higher $R_{off}$ is shown. Again a 14 nm technology with SRAM memory is used

[14] The technology should be able to provide the necessary capacitor values.

for the estimations. The overall power consumption is again somewhat lower than with the 65 nm technology, which results from the dramatically reduced power consumption of the bias generation. From the µW range (Fig. 3.11) the power consumption is lowered by roughly two orders of magnitude. The big impact on the overall power consumption is seen only for $V_{dd}$ below 200 mV. Below that supply voltage value the bias generation consumes a good portion of the systems power and the reduction is obvious. For a supply voltage of $V_{dd} = 10$ mV the total power consumption is only 20 nW.

If both of these assumptions are combined together, the power consumption results shown in Fig. 3.12c can be estimated (14 nm, SRAM). For a supply voltage of $V_{dd} = 10$ mV the power consumption is only 40 nW. This highlights that even with slightly higher unit capacitors still very low power consumptions are possible. However it is necessary to take a close look at the CMOS characteristics at cryogenic temperatures.

## 3.7 Scalability Discussion and Conclusion

From the estimations presented it becomes clear that for scalable control electronics the power in conjunction with the performance is the biggest challenge. A lot of research still has to be done to be able to build electronics which are scalable and can control a very large number of qubits. Nevertheless, the results point out that the here proposed solution is feasible if some actions are taken concerning the power consumption.

One possibility to relax power constraints on the electronics is to change the environment. The standard dilution refrigerator has a cooling power of a few mW at 200 mK [107], but technology is improving. More cooling power directly translates to more controllable qubits. Besides these lab environment fridges there are large scale experiments which require cryogenic temperatures with a lot of cooling power. One example are the cooling plants used at the Large Hadron Collider (LHC) at CERN, which produce 2.4 kW at 1.8 K [108]. This implies another idea to increase the power budget: to move the qubits to higher temperature as that relaxes the power constraints. Even smaller fridges have already around 1 W of cooling power at 1.8 K. However, the power consumption of the electronics also increases somewhat due to e.g. necessary bigger unit capacitors[15].

Already today conservatively estimated around 26 qubits can be controlled with a current 22 nm process [104]. Even more than 300 qubits could be controlled with the presented circuit concept, with little changes to existing technologies. A summary of different technology, temperature and cooling power options with the resulting number of qubits controllable, is given in Tab. 3.6. It highlights what configuration is suitable for cryogenic control electronics with a qubit number scaled up to millions.

[15] At higher temperatures more noise is present which forces an increase of the minimum capacitor size.

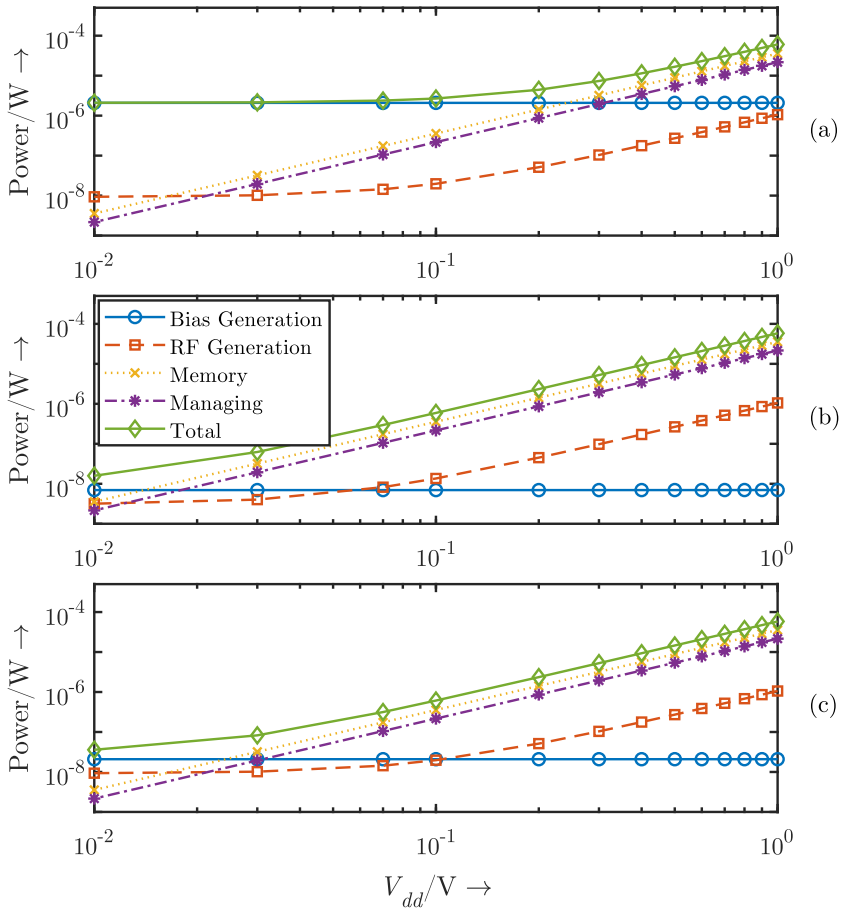


Figure 3.12: Power estimation results of the complete system for different digital supply voltages $V_{dd}$. Technology parameters are extrapolated to 14 nm and SRAM memory. Results in (a) include bigger $C_u$ caps for better linearity with ($C_u$ = 30 fF, $R_{off}$ = 1 TΩ), (b) takes lower leakage into account ($C_u$ = 10 fF, $R_{off}$ = 100 TΩ) and (c) combines both options ($C_u$ = 30 fF, $R_{off}$ = 100 TΩ).

| $T_{el}$ | $\dot{Q}$ | Architecture | Node | $V_{dd}$ | No. Qubits |
|---|---|---|---|---|---|
| 200 mK | 1 mW | FF | 65 nm | 1 V | 5 |
| 200 mK | 1mW | S | 22 nm | 400 mV | 26 |
| 200 mK | 1 mW | S | 14 nm | 100 mV | 328 |
| 200 mK | 1 mW | S | 14 nm | 10 mV | $1.4 \cdot 10^3$ |
| 1.8 K | 1 W | S | 65 nm | 1 V | $1.3 \cdot 10^5$ |
| 1.8 K | 10 W | S | 14 nm | 10 mV | $6.1 \cdot 10^8$ |

Table 3.6: Controllable number of qubits, as limited by the power consumption, for different environment, architecture and and technology settings. $T_{el}$ is the estimated electron temperature and $\dot{Q}$ the available cooling power. Architecture options are flip-flop memory (FF) and SRAM memory (S). The technology parameters are the digital supply voltage $V_{dd}$ and Node is the CMOS technology generation.

# Chapter 4

# Behavioral modeling of electronics

## 4.1 Motivation

The results from the last chapter indicate that a scalable electronic control system is feasible at cryogenic temperatures. Draft schematics were used for the estimations of the power and area consumption. In a next step a behavioral model is developed from these drafts to validate the system architecture However, the architecture validation is not the only reason to develop this model. Other reasons are the facilitation of a top-down design process and the simplification of verification procedures [109–111]. As part of the top-down process the model is at a fairly abstract level now, with the opportunity for adding details in later process steps. Nevertheless, for all of the dynamic behaviour of the control electronics (CE) and its components, a thorough study is needed. So the model is set up with enough details to support that. On top of that also the interaction of the control electronics with its surrounding parts is of interest and is also included in the model. The simulation results of the model have to be compared to two different sets of requirements. One set includes the specification derived from the physics experiments and describes mainly the bias and RF output signals (see Sec. 3.2). The other requirements are the functionalities of the control electronics components as they have been briefly described in Chap. 3. Efficient simulation of the necessary signals for both requirement sets leads to two different simulation setups as described in more detail in Sec. 4.2.

The model developed in this chapter is a highly flexible one, as the model is parameterized. All relevant input parameter values of the model, e.g. the number of sequences in the memory, can be easily changed. This enables reconfiguration due to changing specifications and also exploration of different system settings. One of the model parameters ($exp$) even controls whether a complete qubit experiment with an initialization and a configuration phase (tuning) is included in the simulation or these steps are skipped to only include the operation of a quantum circuit. Additionally, with these time domain simulations the scalability of running experiments, for example in terms of runtime, can also be explored.

For functional validation of the concepts presented in Chap. 3 a reasonably abstract behavioral model with interfaces to circuit design programs and widely used programming languages like C is suited best. It enables flexible system validation without the large effort associated with exact physical models or schematic implementations. Especially the abstraction from the schematic is useful here, as SPICE-based models are not specified for cryogenic temperatures. Nevertheless, detailed models from circuit schematics can be included and combined with the more abstract parts through the interface. An interface to programming languages is useful to integrate existing model for example from physics oriented research of QC.

## 4.2 Simulation with Simulink

The model presented here is implemented in the Matlab based Simulink environment. Several reasons support this, for example the compatibility with existing circuit verification protocols and with the estimation codes from Chap. 3. Moreover, co-simulation with the SPICE simulator Cadence is possible. Work on designing circuit components for the control electronics based on the system considerations in Sec. 3.2 and 3.3 is ongoing [112, 113] and the tool used there is Cadence. Beyond that Simulink/Matlab is also compatible with C and has the possibility for generating hardware description language (HDL) from models. With HDL code digital circuits can be directly synthesized and run on field-programmable gate arrays (FPGAs). Simulink has the possibility to create user specific blocks and to use self-written Matlab functions, but the behavioral model as described in this chapter contains is completely based on blocks from the Simulink libraries. These libraries are the standard libraries and additional libraries from the different toolboxes[16].

Simulink simulates the state of a model including the value of all signals in the time domain. To compute the state at any given time different programs, also called solvers, are available. Which solver is suited best depends on the dynamics of the model, the stability and robustness of the solver and the solution and the tolerable computation effort. Here, the complete system model uses variable time continuous solvers. It uses variable time steps with a maximum step size of 417.7 ps and can deal with the continuous signal values that ire required by the output of the system. The maximum step size is given by the maximum frequency at which signal values can change which is $f_{max} = 2.4\,\mathrm{GHz}$ in the model. The maximum step size in the variable step solver ensures that the accuracy is good while the time steps are chosen as large as possible to reduce the computation effort.

[16] Toolboxes used in this work are: Communications Toolbox, DSP Systems Toolbox, Signal Processing Toolbox, HDL Coder.

As mentioned earlier, in this chapter two different simulation setups are used to efficiently produce the desired results. One setup includes the model of the complete system and is used to show the functionality of the system concept and of all its components. With the detailed dynamic behaviour of the system and its components a comparison to the functionalities assigned to the components in Chap. 3 can be made. This simulation setup is referred to as 'digital setup' or shortened to 'dig setup', because all the relevant signals are digital and based on binary words. The other simulation setup looks in more detail on the behaviour of the partly analog output stages, which produce the qubit control bias and RF voltages. This part is relevant to check whether the system complies with the specifications derived from experiments as discussed in Sec. 3.2. To observe this behaviour efficiently, a reduced system model generates only the signals necessary for the bias and RF generation units. This lowers the computation effort of the simulation and this simulation setup is referred to as 'analog setup'. More detailed information on this analog setup is included in Sec. 4.5.3 and 4.5.4.

For the digital setup simulation the so called ode15s solver is employed, while the analog setup simulation uses the ode45 solver. The ode45 solver utilizes a one-step method based on the Dormand-Prince pair belonging to the Runge-Kutta formulae [114, 115] and is a general first try variable time continuous solver [116]. To solve the equations for the model state at the current simulation time point, the ode45 solver only needs the solution of the previous time point. However, the ode45 solver is computationally slow for the digital setup simulation and thus the ode15s solver is employed. The odes15s solver is based on the numerical differentiation formulas in Ref. [117]. In contrast to the ode45 the ode15s solver uses multiple steps to find a solution [118]. Depending on the system type this multiple steps can still be less computational intensive compared to one step of the ode45. More detailed information on the solvers employed by Simulink, their comparisons and options can be found in [114, 116, 118]. Details are also included in the general manuals of Simulink and its toolboxes. The references also include suggestions on how to improve accuracy or lower the computational effort.

## 4.3 Top Level Model

The top-level system model derived in this and the next chapter is shown in Fig. 4.1 with temperature stages. The temperatures are assigned according to the QC implementation concept described in previous chapters. The inclusion of the temperature visualizes the interface between the two stages, but no temperature specific effects are included in the present abstract model. At cryogenic temperatures (<1 K) the system model includes the control electronics, the qubit and the measurement. At higher temperature stages (>1 K) the functionality of other levels of the quantum computer is located. The characterization of the qubit and the derivation of a qubit model deals in large parts with

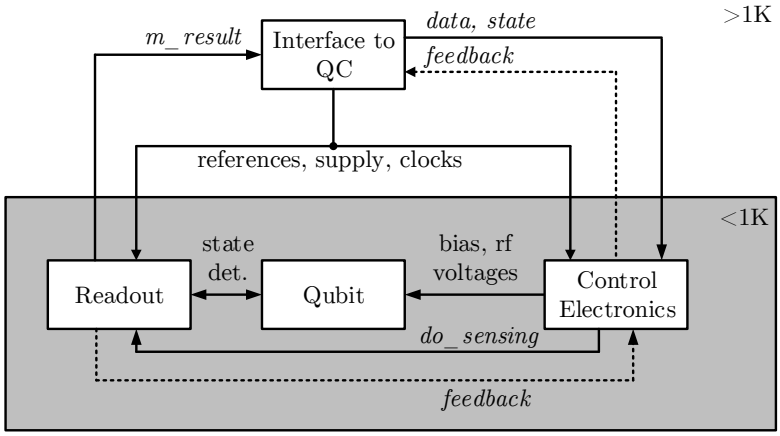


Figure 4.1: Behavioral model structure with temperature stages

quantum mechanics. In order to understand this better, there is a full chapter dedicated to this topic (Chap. 5).

The control electronics follow the specifications and concepts of Chap. 3. However, some structural details were adapted and improved while building the model. The general flexibility of the behavioral model developed here is due to high degree of parameterization. Tab. 3.1 lists all parameters and the corresponding symbols and values as used in Chap. 3, if applicable. The table includes two columns of parameter values for this chapter. These columns correspond to the two different simulation setups, the digital and the analog setup respectively.

All the parameters in Tab. 4.1 can be easily changed by the model user and are sorted by functionality. The first parameter on the top is the already mentioned $exp$. If $exp = 1$ all the functionalities of the behavioral model are included in the simulation, which corresponds to a complete qubit experiment. Otherwise, with $exp = 0$, some functionalities are skipped and only the steps necessary for the operation of a quantum circuit are included in the simulation (see also Fig. 4.5 and the corresponding explanations in Sec. 4.4). The next set of parameters describes the output signals which are connected qubit with their maximum range ($dc\_range$, $rf\_range$), their resolution ($dc\_resolution$, $rf\_resolution$) and their sample rate ($dc\_srate$, $rf\_srate$). These parameters then define additional properties for the modeled circuits producing these signals. Important for them are the clock frequencies ($dc\_frequ$, $rf\_frequ$) and the bandwidth of the associated lowpasses ($dc\_lp\_f$, $rf\_lp\_f$). For the resolution of the RF signals a lower value of 6 bit is used in this chapter in contrast to the 10 bit of Chap 3. The reduction makes the simulation results display clearer, other than that it has no effect on the overall model.

| Model parameter/Unit | Chap. 3 | | Dig. setup | Analog setup |
|---|---|---|---|---|
| | Symbol | Value | Value | Value |
| *exp*/bit | - | - | 1 | 1 |
| *dc_range*/V | $V_{range,bias}$ | 1 | 1 | 1 |
| *rf_range*/V | $V_{range,RF}$ | $4 \cdot 10^{-3}$ | $4 \cdot 10^{-3}$ | $4 \cdot 10^{-3}$ |
| *dc_resolution*/bit | $n_{bias}$ | 12 | 12 | 12 |
| *rf_resolution*/bit | $n_{RF}$ | 10 | 6 | 6 |
| *dc_srate*/MHz | $f_{refresh}$ | 1.1 | 1.1 | 1.1 |
| *rf_srate*/MHz | $f_{sample,RF}$ | 300 | 300 | 300 |
| *dc_frequ*/MHz | $f_{clk,bias}$ | 2.2 | 2.2 | 2.2 |
| *rf_frequ*/MHz | $f_{clk,RF}$ | 600 | 600 | 600 |
| *dc_lp_f*/MHz | - | 20 | 20 | 20 |
| *rf_lp_f*/MHz | - | 600 | 600 | 600 |
| *no_samples* | $l_{pulse}$ | 16 | 7 | 7 |
| *no_sequences* | $N_{pulses}$ | 16 | 3 | 3 |
| *address_bits*/bit | $l_{address}$ | 8 | 8 | 8 |
| *id_length* | $l_{id}$ | 4 | 4 | 4 |
| *t_measure*/µs | - | - | 0.2 | 0.2 |
| *sweep_f*/MHz | - | - | 600 | 5.5 |
| *no_sweepel* | - | - | 1 | - |

Table 4.1: Parameters for the simulation/model and the corresponding variables of Chap. 3

The parameters in the set after that determine the amount of data the system handles and transfers together with the already mentioned signal resolutions. The sample and sequence count (*no_samples*, *no_sequences*) define the number of datawords in the memory which have to be written and read during the simulations. The parameters *address_bits*, *id_length* and the signal resolutions determine the length of the datawords that transfer data to the control electronics (more details see Sec. 4.4). In the specification of Chap. 3 the number of sequences and samples per sequence is set to 16, but the numbers are reduced to 7 and 3 in the simulations here (Tab. 4.1). The value of = 7 is chosen because it has been shown already that with this number of samples qubit operations can be accomplished [59]. As a result of this reduction the overall simulation conducted in this chapter are significantly shorter and thus the results are easier to display. At the same time no information or understanding of the system dynamic is lost, as an often repeated transferral of digital data does not produce any noteworthy additional insights

into the systems functionality.

In the last section of Tab. 4.1 all parameters have an influence on how the configuration of all the bias voltages of the qubit is happening. The process is called tuning and will be explained in more detail in Sec. 4.5.1. However, the basis of tuning is the iterative application of a stair signal (also called sweep signal) to a number of electrodes *no_sweepel*. While the varying voltage is applied, the qubit is measured at each different voltage value. With the measurement time given by $t\_measure = 0.2\,\mu s$, the fastest possible frequency of changing the applied voltage is $sweep\_f \leq 1/t\_measure = 600\,\text{MHz}$[17]. For the analog simulation setup the voltage changing frequency was reduced to $sweep\_f = 5.5\,\text{MHz}$ for clearer visibility in the result plots.

## 4.4 QC levels at higher temperatures

The model of the higher levels of the quantum computer (HQC) includes all the functionality of a quantum computer that is relevant to the qubit. Thus the HQC acts as an interface for the control electronics to the QC and is additionally used as a testbench for the other model parts.

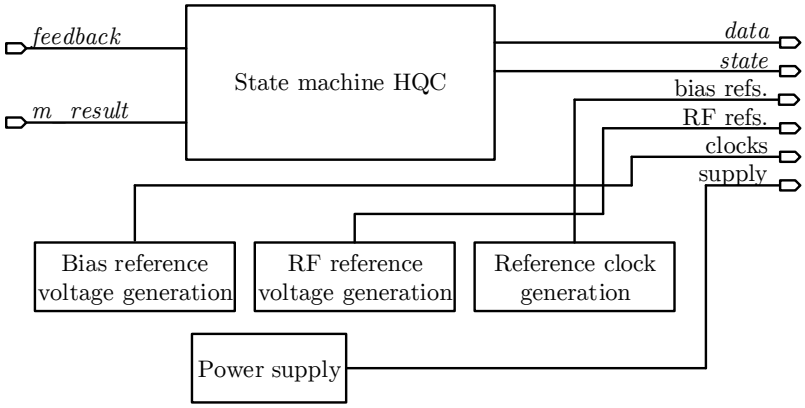


Figure 4.2: Inner structure of the 'Interface to QC' model part in Fig. 4.1 also referenced to as HQC. It provides reference signals and supply voltages and has a state machine implementing digital functionality.

[17] In current lab experiments the measurement time is $t\_measure = 1\,\mu s$, but a reduction is expected from current work on integrating the measurement circuits. The work is in progress at the ZEA-2 at the Forschungszentrum Jülich, but no publications are available so far.

The HQC provides time-invariant signals for general operation of all electronics, such as reference voltages, clock signals and the supply voltages (Fig. 4.2). For communication, time-variant signals with various datawords are employed. Sending information from the HQC is done via the *data* and the *state* signals. A handshaking and acknowledgment response is provided through the $feedback$ signal. All dataword formats used in communication with the HQC are shown in Fig. 4.3.

The length of the memory datawords depends on the type of data contained, as the RF and bias data have different resolutions (Tab. 4.1). The length of the memory dataword $length_{mem}$ is calculated with: $length_{mem} = resolution + address\_bits + 2$. The $data\_type$ bit is set to 1 if the data belongs into the RF memory, otherwise it is 0.

Another dataword of the *data* signal, also called operation dataword, is used to transmit pulse sequence identifiers (IDs) and is shown in Fig. 4.3b. The IDs are sent instead of the pulse data or the pulse addresses in order to minimize the data throughput (compare Sec. 3.3). Next to the overall reduced data throughput, this concept has the second advantage of a low transmission duration with the current one transmission cable setup and a clock frequency of $f_{clk,RF}$. With the short transmission time of the pulse IDs it is possible to apply pulse sequence one after another without any potential non-deterministic waiting time in between. This is beneficial as the qubit state changes even when no pulse is applied. Therefore for a well-defined qubit state the amplitude and duration of any input connected to the qubit have to be specified exactly at any time. The dataword starts with a header as depicted in Fig. 4.3 and contains one ID for each of the two RF electrodes. With the length of the IDs $id\_length$ the total length of the operation dataword is calculated with $length_{id} = 2 \cdot id\_length + 1$ (+1 for the header).

With the current definition of the operation dataword the sequences on the two RF electrodes can be defined independent of each other (see Sec. 3.2). This feature is useful for qubit experiments, but with advancement of the qubit technology this is expected to become obsolete. Then only one ID for both of the electrodes would be sufficient and the data throughput would decrease from 170 MS/s (Eq. 3.2) to 94 MS/s.

The *state* signal dataword depicted in Fig. 4.3c is 3 bit long. Information in the *state* word is encoded in the number of consecutive bits set to 1 without any header bit, which can be efficiently decoded in this case. Transmitted through this dataword is the info regarding which state M1, M2 or M3 of the managing units state machine in the control electronics is to be activated (see Sec. 4.5.1).

The handshaking and acknowledgment communication from the CE to the HQC is done via the $feedback$ signal with a 1 bit dataword (Fig. 4.3e). After sending data to be stored into the CE memory for example, the HQC does not undertake further actions. Only when $feedback = 1$ is detected, the next dataword will be sent. A visualization of the dynamic communication with the *data*, *state* and $feedback$ signals is given through the simulation results in Fig. 4.4. In the very beginning the state signal is sent, which ensures

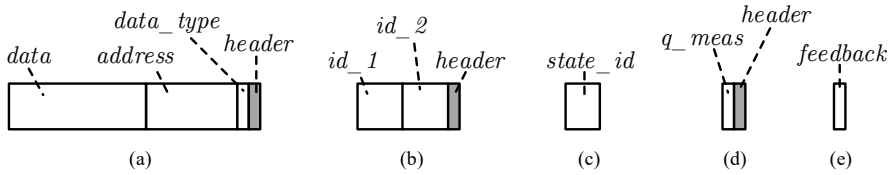


Figure 4.3: Data words: (a) memory transfer, (b) qubit operation (c) state signal (d) measurement, (e) feedback

the right behaviour of the control electronics. It is directly followed by the transmission of a dataword with memory data. After this and each following word a $feedback = 1$ is sent back.

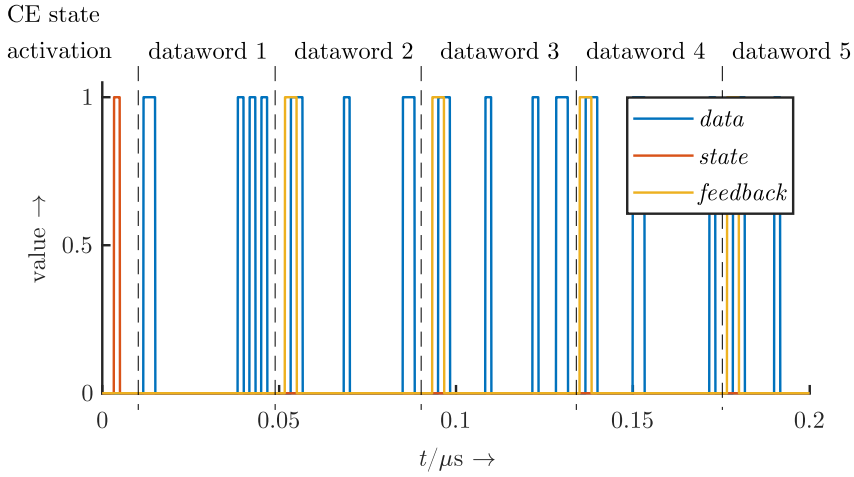


Figure 4.4: Simulation results for data transfer from the HQC (*data* and *state*) to the control electronics memory (*feedback*). Handshaking can be observed as well as the state activation.

The heart of the HQC is a state machine which produces the *state* and *data* signals and reacts to incoming signals. It has states for each stage of a complete qubit experiment and the operation of a quantum circuit. The corresponding state flow chart is depicted in Fig. 4.5 in the Unified Modeling Language (UML)[18]. At the start of a simulation the decision for a complete experiment or the execution of a quantum circuit is made based on the parameter *exp*. After that the qubit experiment begins with the state S1, the

[18]Detailed information on UML state diagrams can e.g. be found in [119].

initialization of the system. During S1 all the needed data is transfered to the internal memory of the CE. This data includes the RF pulse sequences to operate the qubit and the bias data. The bias data includes the correct voltage values to be applied to the bias electrodes in order to form the double quantum dot (Sec. 2.4.1). To enable the tuning of one electrode the bias memory has space for one additional dataword which contains the specific electrode number. The tuning of one electrode is done in S2, which follows S1. At each activation of S2 the information on which electrode to tune is written in the bias memory.

After the qubit is at the right operating point, the qubit state is initialized. As seen in Fig. 4.5 the initialization is represented by the state S3. This is also the first activated state of the HQC when only a quantum circuit is run. After the initialization the qubit can be operated (S4). At the end of the qubit experiment or the quantum circuit run, the qubit is read out in S5.

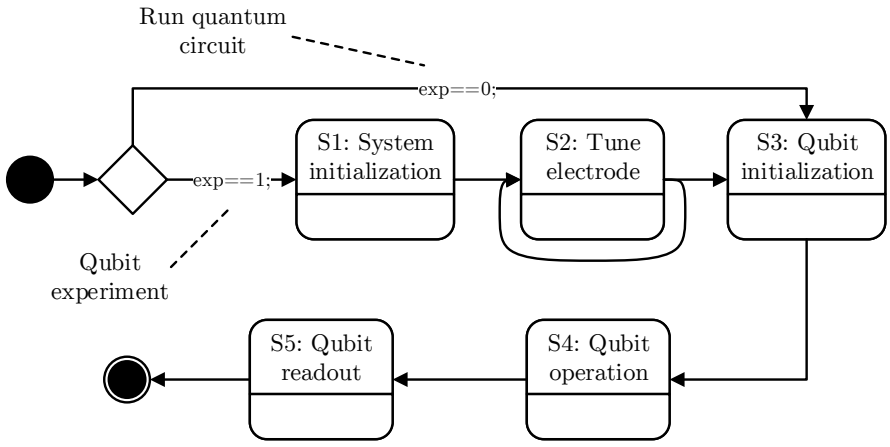


Figure 4.5: UML state flow of the HQC state machine

During a simulation, the current state of the HQC can be observed through the internal variable *state_mult*. For this the enable signals $\in [0, 1]$ of the states are multiplied with their state index. The resulting signal showcases the progression of the simulation and is depicted in Fig. 4.6.

In this system configuration only a few gates are executed, thus the time needed for qubit operation is small. The durations of the initialization and the tuning are significantly longer than the operating time, even with their already shortened nature.

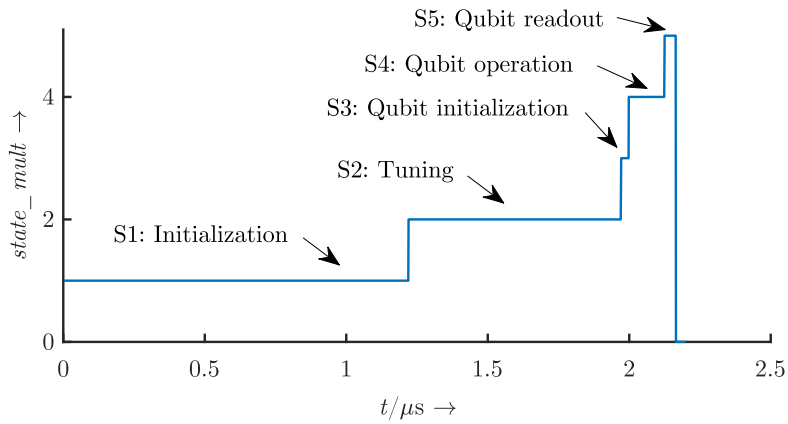


Figure 4.6: Progression of the HQC state machine over time. The *state_mult* signal is defined through the sum of the individual *state_enable* signals weighted by their state index.

## 4.5 Control electronics

Fig. 4.7 shows the structure of the behavioral model of the control electronics. The structure is the same as the one presented in Chap. 1 and 3, but includes more details of the interfacing signals. These details are helpful in understanding the interactions of the control electronics parts.

### 4.5.1 Managing unit

Like the HQC, the managing unit is implemented as a state machine which processes incoming data and directs the activities of the other units accordingly. The different states cover different functionalities of the managing unit, as seen in Fig. 4.8. There are fewer states here than in the HQC. The reason behind the fewer states is that the initialization, readout and the operation of the qubit require the same type of actions from the managing unit. In other words, initialization and readout are also qubit operations, similar to gate sequences.

The similarity of the different qubit operations can be well understood with the energy diagram of the GaAs qubit in Fig. 2.4b. After forming an empty double dot with the voltages found during the tuning, two electrons are loaded in a controlled way. This loading is the initialization and happens through applying a positive voltage form $\epsilon(t)$. Then the qubit is in the S(0,2) state. The qubit state manipulation is achieved through $\epsilon(t)$

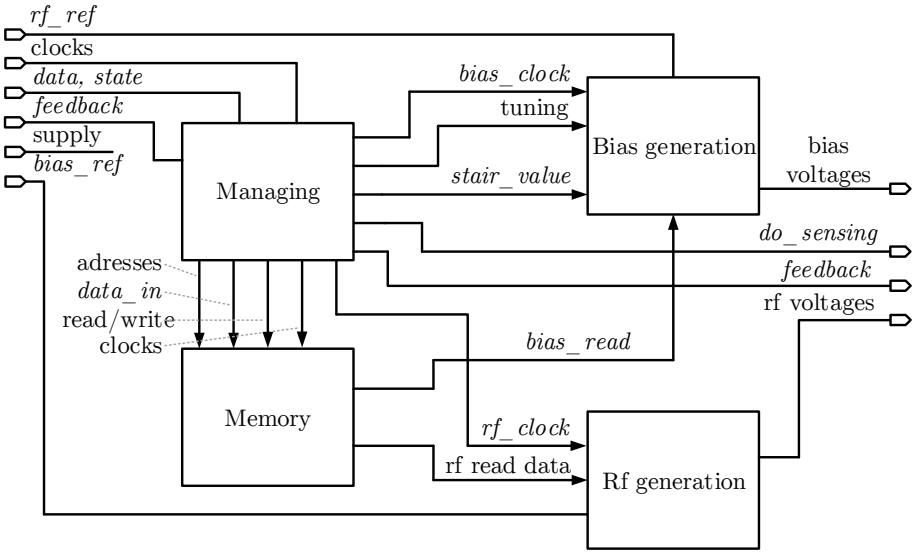


Figure 4.7: Structure of the control electronics with internal signals

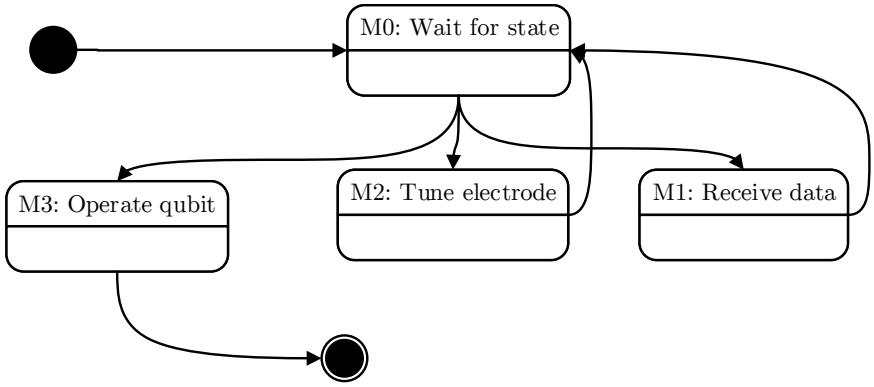


Figure 4.8: UML state flow for the state machine in the managing unit

signals that are negative to slightly positive. After the last state manipulation through gate pulses is done, again a positive $\epsilon(t)$ form is applied as a readout pulse. The qubit ends up either in the S(0,2) state or in the $T_0$(1,1) state which can be distinguished by a measurement.

The starting state of the managing unit is the state M0, where it waits to receive further information in the *state* signal. With a dataword received there (see Sec. 4.3), the corresponding next state M1, M2 or M3 is enabled. In the current model implementation, a *state* dataword is sent by the HQC shortly after simulation start. The internal state variable of the managing unit *enabled_mult* indicates the progression of the simulation the same way *state_mult* does for the HQC. The managing unit starts with M0 and the associated *enabled_mult* = 0 as can be seen in Fig. 4.9. Using results from the same simulation run as in Fig. 4.6, the next state to be activated is M1. After the first transition from M0 to M1 near the beginning of the simulation time, M0 is activated again several times in the simulation (Fig. 4.9). This is in accordance with the state diagram, where M1 and M2 transition back to M0 after finishing their internal processes.

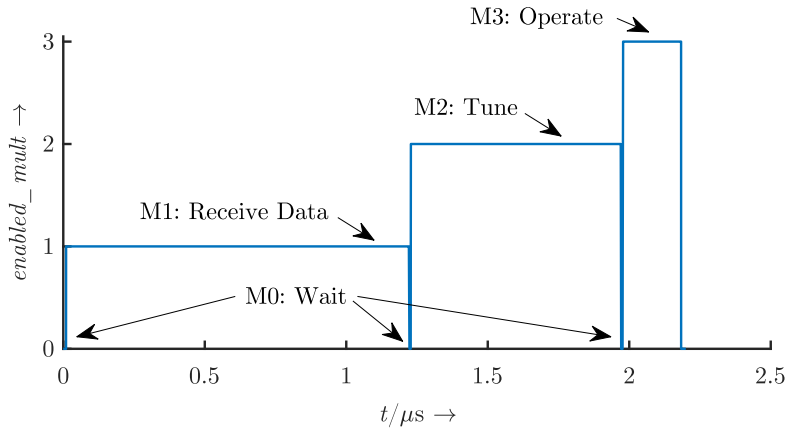


Figure 4.9: Progression of the managing unit state machine over time. The *enabled_mult* signal is defined through the sum of the individual *state_enable* signals weighted by their state index.

In general M1 is activated first after the initial enabling of M0. In M1 most of the data transfer to the local memory is done, corresponding to the S1 state of the HQC. The signals relevant to understand the write processes to the memory are shown in Fig. 4.10. During data reception, the transmitted dataword is split into its components *data*, *address*, and *data_type* (Fig. 4.3). Depending on the *data_type* value, the write enable signal to the correct memory is set to 1 (*write_bias*, *write_rf* in Fig. 4.10). Then the data is written

into the memory at the location of *address*. Depending on the memory part that address is either fed to the *add_bias* or the *add_rf1* signal (Fig. 4.10b). In the setup here first the RF data is received and written and subsequently the bias data. The *bias_write* signal is enabled a second time during the simulation at $t = 1.3\,\mu s$. At that time the state machine is already in M2 (Fig. 4.9). In the reduced system here only few datawords have to be written $no\_words = no\_sequences \cdot no\_samples = 3 \cdot 7 = 21$. This can be seen in Fig. 4.10, where data is written to addresses from 0 to 20. The shown address signals are converted to integer values from the binary words. In a complete system RF data would be written into the full range of 256 addresses in the RF memory.

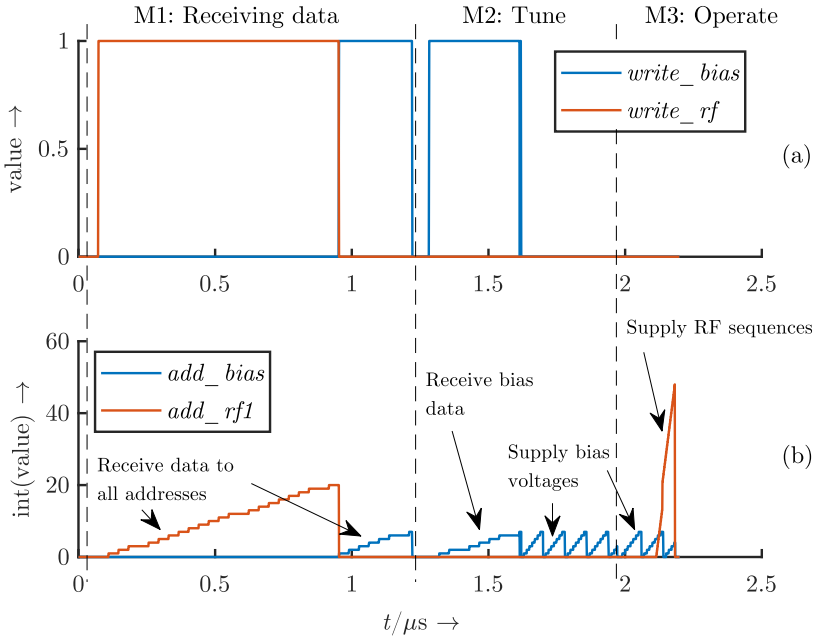


Figure 4.10: Signals for writing received signals into the memory

The next state to be activated is M2. This state deals with the already mentioned tuning process of the qubit. The main goal of the tuning process is to find the right voltages for all the bias electrodes in order to create a double quantum dot which is used as a qubit with one electron in each dot[19]. The double quantum dot is given through a potential distribution defined with the 8 bias voltages applied to 8 bias electrodes, as explained

[19]Besides this one voltage combination more complex voltage dependencies are also of interest for the qubit operation, however these details are not in the scope of this work. Further information can be found in [6, 120], for example.

in Sec. 2.4.1. However, due to random inhomogeneities in the material the correct bias voltages are individual to each qubit and are unknown at the beginning of an experiment. Thus, the voltages have to be found through tuning.

The overall method to find the right voltages is to start with a best guess voltage on all except one electrode. The voltage on this electrode, in the following called tuning electrode, is stepped through the complete possible voltage range up to an amplitude of *dc_range* with the available maximum resolution *dc_resolution*. Due to the finite resolution, the voltage sweep signal looks like a staircase and is thus called *stair_value* (see Fig. 4.11). During this voltage variation the electron occupancy of the dot is observed with the readout sensor of the qubit. The observation method varies as does the readout sensor, one method is to measure the current flowing in or out of the double dot. In this way possible bias voltage values for the wanted (1,1) charge configuration (Sec. 2.4.1) can be identified. When the voltage sweep on one electrode is finished, the measurement results indicating the occupancy are processed. With the new data the values of the electrode voltages are adjusted and a new electrode is set as the tuning electrode. This process is continued until a satisfactory double dot can be defined.

This description of tuning only gives a rough idea about the process, the procedures for tuning used in today's experiments are very intricate with different steps employed for varying characteristics. These tuning processes are currently still done mostly manually [6]. Beyond that the procedures are still changing and the work on automatization is a research topic still at the beginning [120–123]. Thus, a tuning algorithm cannot be incorporated in the presented behavioral model at this point. However, an iterative application of stair signals to one electrode is a vital electrical functionality for tuning, which is implemented in the model.

The tuning procedure, as enabled by the managing unit state M2, is visualized by the plotted signals in Fig. 4.11, with the *stair_value* signal in Fig. 4.11a. In the beginning of the tuning a starting voltage is set for all electrodes except one which is tuned. The voltage values to be applied to all bias electrodes except the tuning electrode are sent from the HQC to the control electronics and are stored in the bias memory. This can be observed by the progression of the *add_bias* signal (Fig. 4.11, converted to integer values) in the 'Receive bias data phase' in Fig. 4.11. Next a voltage sweep is applied to the tuning electrode up to the maximum value of *dc_range*. The voltage sweep is accomplished with the stair signal (*stair_value*) at the input of the bias generation DAC. However, the nature of the bias generation implementation prevents a simple continuous stair signal in the 'Supply bias voltages phase' in Fig. 4.11.

The reason for the non-continuous stair signal in Fig. 4.11 is multiplex concept of the DAC. The output of the DAC is multiplexed to the m&h capacitor array (Fig. 3.3), which stores the analog voltages. This way one DAC is enough to provide voltages for all bias electrodes and enable scalable qubit operation. A disadvantage of this implementation is the necessary constant cycling through all electrodes at a frequency of $f_{refresh}$ for the

qubit to operate properly. This process mitigates leakage and the resulting unwanted voltage drop on the electrodes. The cycling has to happen even if the nominal voltage is constant, which is the case for the non-tuning electrodes in the 'Supply bias voltages' phase. The recurring selection of electrodes common to the tuning and the bias operation of the qubit, is driven by the *electrode_select* signal. The *electrode_select* contains a 8 bit hot one value[20], which means exactly one bit is 1 at all times. The progression of the electrode number selected like this is plotted in Fig. 4.11b.

As long as one of the none-sweep electrodes is selected, the corresponding voltage value is read out from the bias memory at address *add_bias* (Fig. 4.11) and applied to the DAC input. If the electrode to be swept is selected however (here $electrode\_select = 2$), the *stair_enable* signal is set to 1. In Fig. 4.11 this is marked with a grey background. Then the *stair_value* signal is applied to the bias DAC input instead of the bias memory output. As long as $stair\_enable = 1$, *stair_value* also increases its value to continue voltages sweep (Fig. 4.11a,c)[21]. The tuning of one electrode is complete, once *stair_value* has covered the complete number range. The displayed signal is an example for a system configuration with a RF resolution of $rf\_resolution = 6$ bit (Tab. 4.1), leading to a maximum value of $2^6 - 1 = 63$. The stair value increases with a frequency of $sweep\_f$ for which the upper border is set by the measurement time.

The next state activated following the flow chart of the HQC is M3 with the qubit initialization, gates and readout (Fig. 4.9). The S3, S4 and S5 states of the HQC each send a state dataword when enabled. However, the sent dataword is the same and the managing unit stays in M3 until a feedback from the measurement unit is given. The reason for the state split in the HQC is greater flexibility with regard to future inclusion of QEC. As the initialization, gates and the measurement are all operations on the qubit, it is important that they are applied without a non-deterministic delay (see Sec. 4.4). The combination of the processing of the different operation types into one state helps with this. To ensure a seamless sequence of all types of operations on the qubit, a queue is implemented in M3. A detailed model of M3 and the queue is depicted in Fig. 4.12 with the relevant signals shown in Fig. 4.13.

At the input of the M3 model and before the queue, the two pulse sequence IDs are extracted from the operation dataword. During the extraction of the IDs also the transformation from the serial input signal to two parallel binary words is carried out (serial_2_parallel block). With a short burst of $push = 1$, a binary word is added to each of the two rows of the queue (Fig. 4.13a). In a first phase the queue first accumulates four ID words in each of the rows without generating any output, which is labeled as 'Fill queue to threshold' in Fig. 4.13. The number of words inside the queue is meanwhile tracked by the internal variable *inside*. Only when the threshold of $inside = 4$ is reached, bursts of

[20] In a hot one code only one bit in the dataword is set to 1 and all others are 0.

[21] Due to the visualization in combination with the variable step size the *stair_enable* looks like a spike but is the duration of one step.

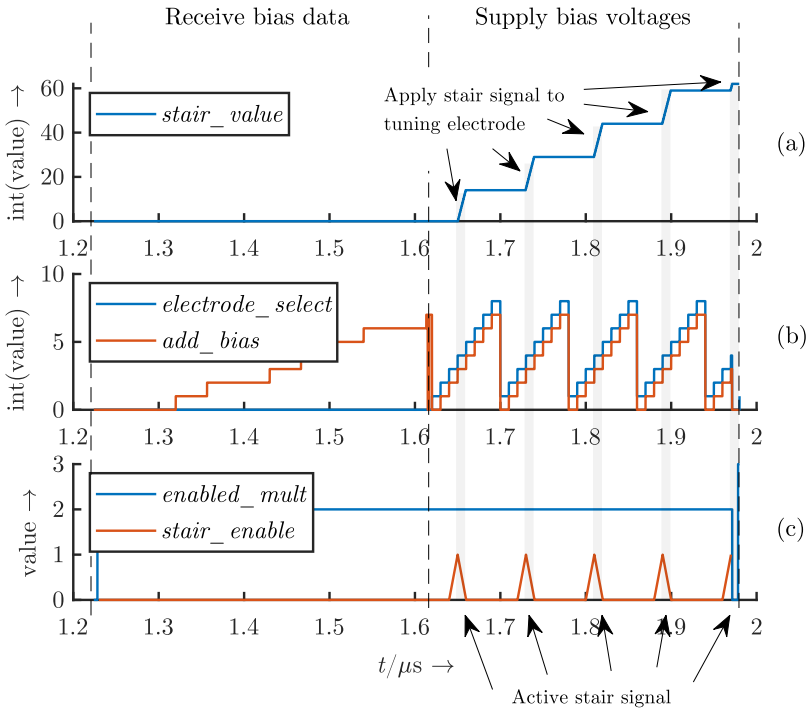


Figure 4.11: Relevant signals during tuning in state M2

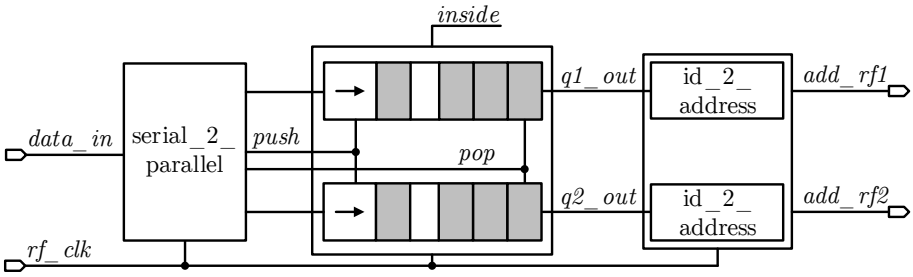


Figure 4.12: Model concept for qubit operation

*pop* = 1 start to remove words from the queue rows and make them available at $q_{1,2}\_out$ (Fig. 4.13b). This is labeled as the 'Add to queue, produce output' phase in Fig. 4.13.

After the queue, the addresses of all samples belonging to the pulse sequence of the ID at $q_{1,2}\_out$ are generated in the right order (Fig. 4.13c). In other words the decoding from ID to the addresses of the sequence samples is done in the id_2_address block. Until four IDs are collected in the queue, the $feedback = 1$ signal is sent right after the reception of the dataword. After *inside* = 4 has been reached the feedback signal is given when an ID leaves the queue. This protects the queue from overflow. In the presented simulation results only five IDs are sent from the HQC. Therefor after reaching *inside* = 4 a second time, the number of IDs in the queue drops until it is empty.

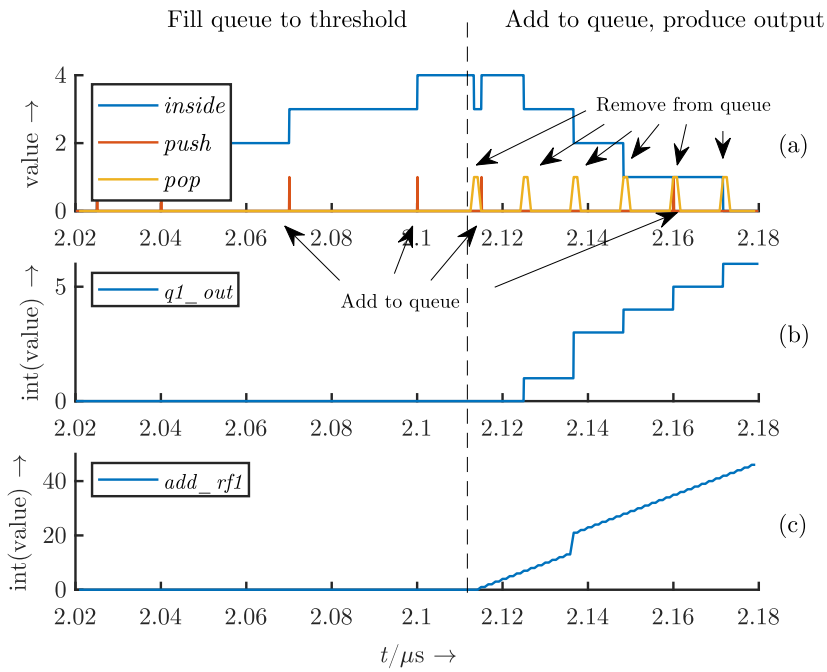


Figure 4.13: Relevant signals for qubit operation of the queue in M3

### 4.5.2 Memory

The memory model contains the bias and RF memory part, as depicted in Fig. 4.14. The memory parts are based on basic random-access memory (RAM) blocks that are available

in the HDL Coder Simulink library with added elements for synchronized read and write.

During the complete simulation of one qubit experiment or the run of a quantum circuit (see Fig. 4.5), the memory works with different clock signals to optimize the efficiency. For example the write process of the complete data at the beginning of an experiment (M1) takes a significant amount of time. To keep the time of the data transfer as low as possible, the clock signal with the highest frequency of $rf\_frequ$ is used for all write processes. In contrast to that the read processes are realized with varying frequencies. If M2 is active and tuning in progress, the clock with the frequency $sweep\_f$ is used to read out data from the bias memory ($clk\_biasmem$). During the operations on the qubit in M3 the bias memory is read out with the frequency set by $dc\_frequ$. At the same time the RF memory is read out at a much faster frequency (via $clk\_rfmem$) set by $rf\_frequ$ to supply the values for the pulse sequences.

The pulse sequences applied to both of the RF electrodes stem from the same sequence pool stored in the RF memory. As explained earlier, the data to the memory is written via one signal $data\_in$. The write enable signals $write\_rf$ and $write\_bias$ select into which part of the memory the input word at $data\_in$ is written. Therefore the two write enable signals are never set to 1 at the same time. For the location of the write, the $add\_rf1$ and the $add\_bias$ signals are used.

The read operation of the memory is also directed via enable signals, here the $read\_rf$ and $read\_bias$. The read processes of the two parts are independent of each other. The bias memory part uses again the $add\_bias$ signal for the location of the read. For this reason a simultaneous read of two values from the RF memory is implemented. Thus the read utilizes two address signals $add\_rf1$ and $add\_rf2$ simultaneously.

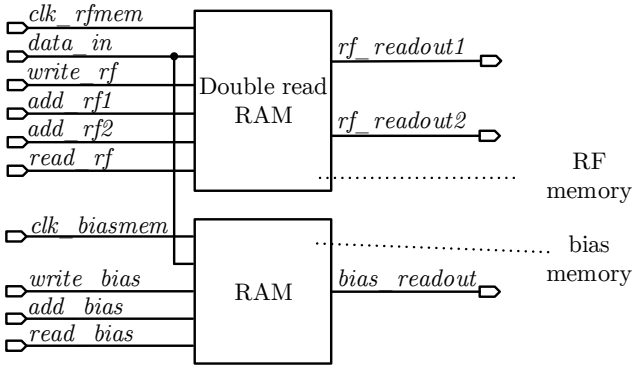


Figure 4.14: Memory

### 4.5.3 Bias generation

The bias generation behavioral model is shown in Fig. 4.15 and follows the concept of Fig. 3.3 in Chap 3. The bias generation includes abstract behavioral models of the DAC and the multiplex-and-hold (m&h) the capacitor array.

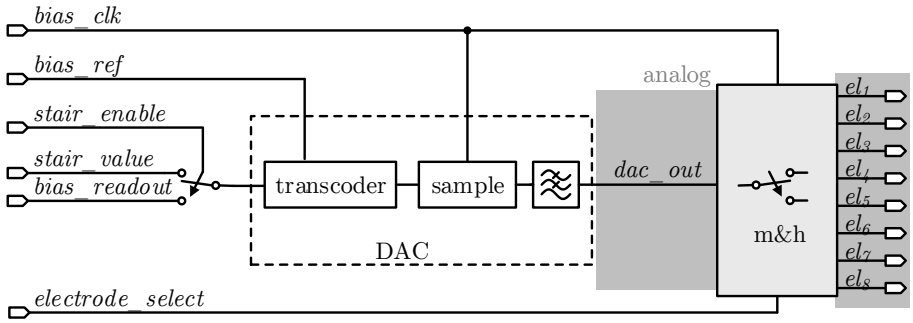


Figure 4.15: Bias generation mode

The behaviour of the DAC is modeled with a transcoder, a sample-and-hold (s&h) and a lowpass filter. The m&h model consists of an array of sample-and-holds. For modeling the performance of the bias generation the detailed digital behaviour of the complete system from the last section is not of interest. Therefore, the 'analog' simulation has been set up using the corresponding parameters in the last column on the right in Tab. 4.1. In this reduced model only the digital signal necessary for the operation of the bias generation are included. Part of the model are all input in Fig. 4.15. The input signals are configured to show the behaviour of the bias generation during the tuning state M2, where all functionalities of the bias generation are used. The simulated results of the relevant signals are shown in Fig. 4.16.

The progression of the digital input signals of the bias generation during M2 have already been discussed in Sec. 4.5.1 and shown in Fig. 4.11. Depending on the value of *stair_enable*, the DAC input is switched between the stair and the memory value. Figure 4.16a shows the analog output signal of the DAC *dac_out*. Some effects of the lowpass filtering are evident compared to an ideal rectangular pulse shaped signal, but the *dac_out* signal is not significantly distorted. Electrode number 2 is again set as electrode to be swept, which can be seen in the DAC output signal and the voltage of the electrode in Fig. 4.16a,b. Figure 4.16c shows the voltages of the other electrodes. The electrode voltages go up to their nominal value one after another. This is due to the cycling mechanism. The bias electrode voltages stay completely constant once the nominal value is reached because no charge loss from the capacitors has been modeled at this level of abstraction.

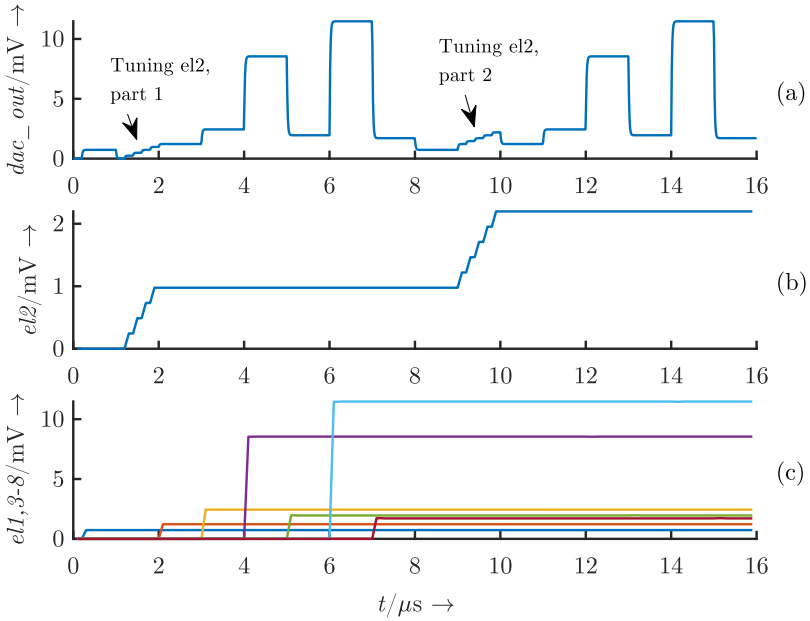


Figure 4.16: Bias generation signals

### 4.5.4 RF generation

The RF generation is modeled in accordance with Chap. 3 as well and is composed of two DACs. Similar to the bias generation part, the DACs are each modeled with a transcoder, a sample-and-hold, and a lowpass filter (Fig. 4.17).

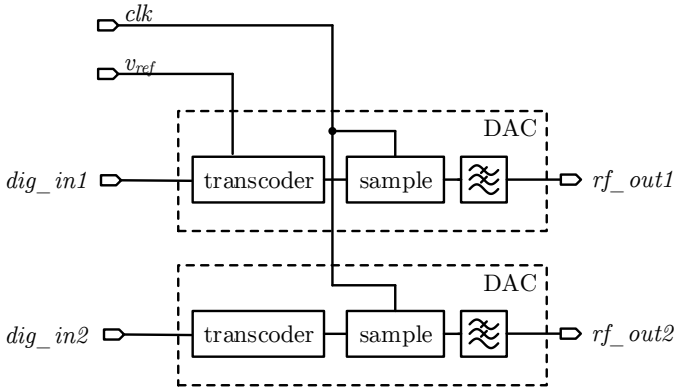


Figure 4.17: Model of the RF generation unit

The RF generation is also part of the analog simulation setup to efficiently characterize the behaviour of the DACs. Thus also for the following simulation results in Fig. 4.18 the analog setup parameter values in Tab. 4.1 have been used. As explained before in Sec. 4.3, that means, in contrast to the specification Chap. 3, the number of samples in one operation sequence is $no\_samples = 7$. For the RF generation in this reduced simulation setup the input signal behaviour matches the one of M3. The qubit operation (M3) is the only state where an output of the RF generation is produced and thus the only relevant one. The simulated example output $rf\_out1$ for one of the RF electrodes is shown in Fig. 4.18. The goal of applying the gate sequences with no delay between the different sequences has been met. In contrast to the bias generation part the effect of the lowpass filter is much more evident in the RF DAC output and distorts the signal. Here the bandwidth of the lowpass is set to $rf\_lp\_f = 600\,\text{MHz}$, in accordance with Sec. 3.3.4. The finite bandwidth and the resulting distortion potentially lead to reduced fidelities of qubit gates if this behaviour is not taken into account while designing the pulse sequences.

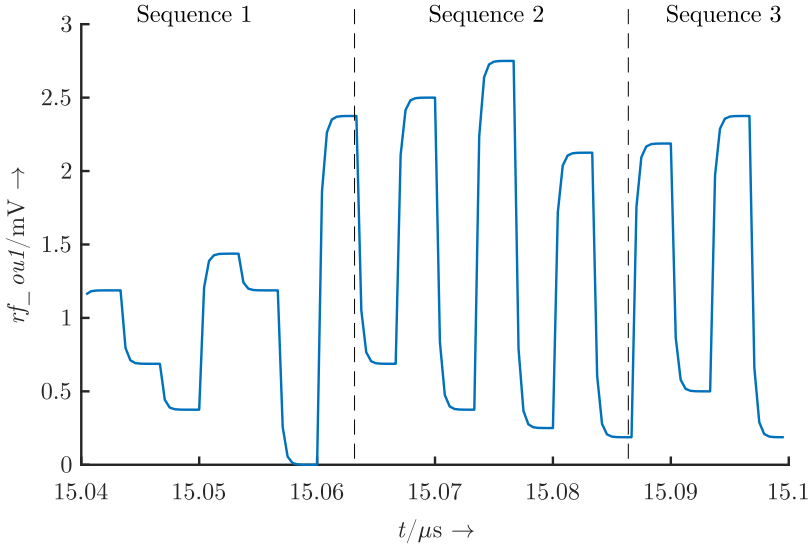


Figure 4.18: One output signal of the RF generation unit with indicated sequence borders

## 4.6 Readout

The concept of the readout and measurement model is depicted in Fig. 4.19. In this work readout refers to the process of translating the qubit state into a measurable classical quantity. One example for that is spin to charge conversion [32]. The measurement is then the process of detecting and evaluating that classical quantity. The model is based on the theoretical mathematical retrieval of the qubit state. In practice, for the readout the qubit state information is projected on the $|0\rangle$,$|1\rangle$ axis which are S(1,1) and $T_0$(1,1). The spin information is translated into a stable charge information through application of a positive voltage $\epsilon$ in the readout pulse. If the projected state was $|0\rangle$ the resulting charge configuration is (2,0), otherwise it stays (1,1). The difference of the charge configurations can be detected by measuring with a nearby charge detector. The qubit model here does not include states outside the Bloch sphere like the (2,0) state, so the readout and measurement model is an abstract one.

The input signal *q_signal* contains the state of the qubit in a vector format such that:

$$|\Psi\rangle = \begin{pmatrix}\alpha\\ \beta\end{pmatrix} = \alpha|0\rangle + \beta|1\rangle, \tag{4.1}$$

as defined by Eq. 2.1 and Eq. 2.3. After the processing is enabled the values of the qubit state are extracted. As discussed in Sec. 2.1 the measurement of a qubit state is a stochastic event. The probability whether 0 or 1 gets read out is calculated from $\alpha$ and $\beta$ values of $|\Psi\rangle$:

$$p\,(0) = |\alpha|^2 \tag{4.2}$$
$$p\,(1) = |\beta|^2. \tag{4.3}$$

With these probabilities the processing parts determines either 0 or 1 as the measurement result *q_meas*. The detection of the charge configuration takes a certain time *t_measure*, due to this the processing of the qubit state signal is delayed. In order to get the right state from the qubit, the *q_state* signal is sampled and held. For transmission the measurement result is packaged in the measurement dataword with a header bit of 1 (Fig. 4.3). With the header included in the dataword, the *m_result* signal is also suitable as feedback signal for the control electronics.

## 4.7 Discussion and implications on scalability

The model presented here shows all the specified functionality and thus presents in general proof of concept. By design the model works with abstract and idealized blocks and thus more detailed simulations are advisable in the next design steps. This is also in

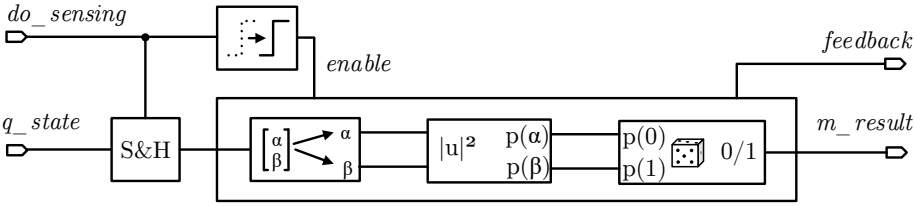


Figure 4.19: Readout behavioral model including measurement

line with the typical top-down methodology and in general opens up the opportunity for many additional research topics either in more detailed components or adaption to similar systems. In further work detailed simulations could for example contain added non-linearities, or use extractions of schematic simulations or the schematics themselves in a co-simulation. Furthermore, the model can be used to verify component concepts e.g. for the bias and RF generation parts.

A concrete conclusion on the scalability due to the runtime of a complete qubit operation process cannot be drawn from these simulations only. For that detailed information on the automated preparation and calibration of the qubits is necessary. This would potentially lead to additional control electronics functionality. However, these details are not clear yet as research is ongoing. Nevertheless, the simulations results and preceding reflections provide a useful base to identify potential hindrances to the scalability.

One thing to investigate in terms of scalability is the duration of the data transfer from the HQC to the memory. This could be critical because the system concept assigns only one data line for all qubits. With the current state of research the pulse sequences cannot be shared between qubits, as they are individual. Thus the complete data transfer in M1 has to be done sequentially for all qubits. For the data transfer to memory, the transfer time of one dataword takes about 23 clock cycles[22]. With a frequency of $rf\_frequ = 600\,\text{MHz}$ and 256 datawords this takes 9.4 µs for one qubit. With only one data line connected to the cryogenic electronics and a frequency of $rf\_frequ = 600\,\text{MHz}$ this would take only 9.4 s for $10^6$ qubits. Thus the data transmission time is not expected to be a hindrance for scalability. The data transfer is not time critical, as no qubit is in operation at that point. In addition to that the duration of a few seconds is in the same range as the time it takes PCs to boot and is therefore acceptable.

A potential issue with the sequence data is that according to the current state of research the sequences have to be tailored to each qubit which could take a significant amount of time. Work on optimizing pulse sequence to individual qubits and experiment setups is

[22]The data to be stored is only maximum 12 bit long (equals 12 clock cycles) but overhead in the dataword and the wait for feedback lengthen the transmission time

in progress [51, 124]. These works employ sophisticated methods to obtain high fidelity gates. However this sophistication comes with a non-negligible computation effort which doesn't support scalability. Cerfontaine et al. in [51, 124] did not discuss the potential for scalable implementation of their work and it is also out of the scope of this work.

The second potential issue for scalability is the tuning. The full tuning process of one GaAs qubit is much more complex than the one implemented here, but only vaguely defined and thus not in the scope of this work. Next to single qubit tuning also neighboring qubits have to be tuned to each other in a similar process. The details on the complexity of the tuning algorithms are not clear yet, but the model has the possibility to easily test code candidates in the system environment. Current research on automated tuning can be found in [120, 122, 123, 125, 126], for example.

For tuning and the complete qubit operation, also the readout mechanism and the measurement circuit are important. These methods are not yet set and work on the topic is ongoing [65, 127]. For the scalability of qubit operation, the measurement time *t_measure* is important and the shorter the measurement time, the better for scalability. However, a certain accuracy is necessary as well, so overall a trade-off between the accuracy, the measurement time and the complexity or size of the measurement circuit has to be made. Once more specifics about the readout are clear, these details can be included the model.

## 4.8 Summary

The proof of principle model in this chapter shows that all specified functionality for qubit operation is included in the control electronics system proposed in Chap. 3. The behavioral model is a good basis for further design and verification work including interfacing the system to physical simulations. It also brings attention to scalability issues of the system running qubit experiments and quantum circuits. Challenges to the operation of a large number of qubits have been identified to be the complexity of the tuning process, potential pulse sequence adjustments and the measurement time and circuitry.

# Chapter 5

# Qubit Modeling and Characterization

## 5.1 Motivation and Method

To complete the behavioral system model as shown in Fig. 4.1, the model of the qubit's behaviour is still missing. The physics of qubit operation is extraordinary complex, therefore the behavioral model needs a certain level of abstraction to fulfill its purpose. For that reason the model is 'simplified' to the most pertinent features. The behavioral model of the qubit is implemented in this chapter as a dedicated Matlab function. The use of Matlab for this is more convenient due to the nature of the calculations included. As Matlab and Simulink are widely compatible the Matlab function can easily be integrated into the overall behavioral model. With the complete model qubit behaviour under the control of the electronics can be simulated. This opens up opportunities to study the effect of for example electrical noise and inaccuracies of the control electronics on the qubit operation. This will be discussed in detail in Chap. 6.

The complete behavioral model allows simulations of the qubit and the control electronics together, but a more systematic study of qubit characteristics is also useful. Especially the quality of qubit operations under the influence of different interfering signals are characteristics with importance for a growing number of scientists working in different domains of quantum computing. Through the increasing research into quantum computers in general and the scalability aspect of qubit operations more and more engineers are working on the topic. Due to a different education, naturally existing works from theoretical and experimental physicists are not as accessible for these researchers as it is for other physicists. However, a certain level of understanding of qubit characteristics is vital, for example to design the circuits of the control electronics concept developed in this work.

The characterization efforts in this chapter in Sec. 5.3 to 5.6 aim to study the effect on the fidelity (see Sec. 2.3) in a way that is easily accessible to for example circuit designers. There has been already a lot of research focused on the behaviour of qubits, but the simulations in this chapter provide an engineering perspective which is still missing for GaAs qubits. The model used in this chapter does not aim to reach the accuracy

and complexity of theoretical physics simulations, but rather appraises the dynamics and dimensions of the qubit behaviour from an engineer's perspective. This way also statements on specs for control electronics can be made.

In order to study characteristics of the qubit operation an implemented behavioral model by itself is not sufficient. That means qubit operations in the form of voltage pulses are needed. Only with the known fidelity of an operation the influence of interfering signals can be ascertained. As no conclusive set of qubit operations is defined up to now, an exemplary set of operations and the corresponding voltages sequences have to be found first. This is part of an optimization process described in Sec. 5.3.1.

## 5.2 Behavioral modeling of the qubit state

In this work, the simulation of the qubit is limited to its state as influenced by the RF input signal. Detailed simulations of for example tunnel currents between the dots, the electro-magnetic field distribution and spin-environment interactions are not of interest at this level of abstraction. The simulation includes the change of state over time under the influence of the control signal which is defined through the RF electrodes. The biasing signals are assumed to be constant, however the noise influence is very similar to that of the control signal[23].

The concept of the work in this section[24] was inspired by the implementation of the 'SPINE' called Matlab program by J. van Dijk [129], who investigated the influence of control electronics on the fidelity of SiGe qubits.

The simulation of the qubit state $|\Psi(t_M)\rangle$ at time $t_M$ is done in accordance with Eq. 2.1 and Eq. 2.18 leading to

$$|\Psi(t_M)\rangle = \prod_{k=1}^{M} dU_k \cdot |\Psi_0\rangle, \tag{5.1}$$

with $dU_j$ the unitary transformation matrix for a small time step $\Delta t_k = t_k - t_{k-1}$ and $M$ the $M$th simulation time step. With Eq. 2.18 $dU_k$ is defined as:

$$dU_k(\epsilon_k, \Delta t_k) = \exp\left[-i\frac{\hbar}{2}\begin{pmatrix}\omega_J(\epsilon_k) & \Delta\omega_z \\ \Delta\omega_z & -\omega_J(\epsilon_k)\end{pmatrix}\Delta t_k\right]. \tag{5.2}$$

The exchange interaction (see Sec. 2.4.1) is here used as given by the fit in:

$$\omega_J(\epsilon_k) = \omega_s \exp(\epsilon_k/\epsilon_0), \tag{5.3}$$

[23] This is based on discussions with H. Bluhms group at the RWTH Aachen University.
[24] Some results of this chapter are in preparation for publication [128].

with $\omega_s = 2\pi \cdot 160\,\text{MHz}$ and $\epsilon_0 = 0.272\,41\,\text{mV}$. The term $\Delta\omega_z = \omega_s$ is assumed constant and set to the specified value using DNP for the duration of the simulation.

Eq. 5.2 can be further broken down [59] to

$$dU_k(\epsilon_k, \Delta t_k) = \cos\left(\frac{\delta_k}{2}\right)\mathbf{I}_2 - i\sin\left(\frac{\delta_k}{2}\right)\vec{n}_k \cdot \boldsymbol{\sigma}, \tag{5.4}$$

with $\delta_k = \omega_k \Delta t_k$ as the trace on the Bloch sphere. The trace is defined with the momentary precession rate of $\omega_j$ given by $\omega_k = \sqrt{\omega_J(\epsilon_k)^2 + \Delta\omega_z^2}$ and the time step $\Delta t_k$. The vector $\vec{n}_k$ is given by

$$\vec{n}_k = \frac{1}{\omega_k}\begin{pmatrix} \Delta\omega_z \\ 0 \\ \omega_J(\epsilon_k) \end{pmatrix} \tag{5.5}$$

and $\mathbf{I}_2$ is the 2x2 identity matrix and $\boldsymbol{\sigma}$ the vector of the Pauli matrices (Eq. 2.7) given by $\boldsymbol{\sigma} = (\sigma_x\ \sigma_y\ \sigma_z)$. Important to notice is that except for the timestep length $\Delta t_k$ the only input parameter potentially changing with the timesteps is $\epsilon_k$. That means the only parameters to influence the state progression are the amplitude of the input voltage $\epsilon$ and the duration of the voltage given by the sum of the corresponding $\Delta t$. It also follows that naturally piecewise constant input signals, the number of timesteps $M$ is given by the number of piecewise constant input amplitudes.

The evaluation of Eq. 5.4 at each timestep is the core of the Matlab function modeling the state progression of the qubit and is shown in List. 5.1. The Matlab function has an input variable *signal* which contains the voltage applied to the qubit for the time in $t$. With a for loop the $dU$ is calculated at each time point (line 10 in List. 5.1) and the overall $U$ is calculated in line 10.

```
1  for k = 2:M %each point in time starting nonzero
2      % Calculate Hamiltonian parts
3      omega_J=Js*exp(signal(k)/eps0); % exchange interaction
4      omega_k=sqrt(omega_z^2+omega_J^2);
5      dt=t(k)-t(k-1);                 % time step
6      delta=omega_k*dt;
7      n_sigma_bold=(1/omega_k)*(omega_z.*sigma_x+...
8          omega_J.*sigma_z);
9      % get dU
10     dU=cos(delta/2)*eye(2,2)-1i*sin(delta/2)*n_sigma_bold;
11     U = dU * U;% get overall U
12 end
```

Listing 5.1: Core of the Matlab function modeling the qubit state

## 5.3 Qubit operation

The characterization of the qubit's susceptibility to interfering signals and noise is mostly only expressive during qubit operation. With a so far missing conclusive definition of a universal gate set (see Sec. 2.2) for this type of qubit, an exemplary gate set of rotations around all axes of coordinates in the Bloch sphere is used. Through a combinations of these rotations an effective rotation around any axis is possible, which is an essential feature for quantum computation [11]. Similar work has already been presented in [2, 83], but with complex pulse forms optimized for a specific experimental setup. In this chapter, basic pulse forms without specific electronics in mind are studied. This is useful in getting a general idea about the dynamics of the qubit itself without additional effects through for example the electronics.

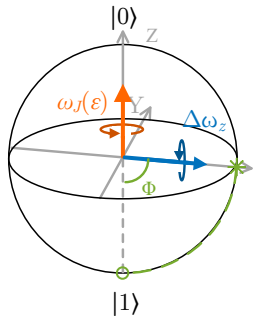


Figure 5.1: Rotation of an angle $\delta = \frac{\pi}{2}$ around the y-axis in the Bloch sphere. Starting state is denoted by '$*$' and '$\circ$' is the end point. Included are the base rotations around the z- and x-axis with the precessions $\omega_J$ and $\Delta\omega_z$, adapted from Fig. 2.4b.

The gates used in this chapter rotate the state of a qubit around the different axes in the Bloch sphere by an angle of $\delta = \frac{\pi}{2}$. This can be used as a basis for future constructions of a universal gate set candidate which contains different single qubit rotations together with one two qubit gate [11]. An example for such a rotation around the y-axis is shown in Fig. 5.1. The shown rotation takes the shortest possible way, but any other progression on the sphere surface is valid as well. For the quality of the operation only the accuracy of the location of the end point in relation to the starting point is of interest.

Mathematically rotations on the surface of a sphere are described by the rotation matrices in Eq. 2.6. For an angle $\delta = \frac{\pi}{2}$ these matrices define the unitary operators $U$ (see Eq. 2.5), discounting the global phase (see Sec. 2.1). This leads to the unitary matrices $U_{\frac{\pi}{2},x}$, $U_{\frac{\pi}{2},y}$

and $U_{\frac{\pi}{2},z}$ to rotate a qubit state around the respective axis given by:

$$U_{\frac{\pi}{2},x} = \frac{1}{\sqrt{2}}\begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}, \quad U_{\frac{\pi}{2},y} = \frac{1}{\sqrt{2}}\begin{pmatrix} 1 & -1 \\ 1 & 1 \end{pmatrix}, \quad U_{\frac{\pi}{2},z} = \frac{1}{\sqrt{2}}\begin{pmatrix} 1-i & 0 \\ 0 & 1+i \end{pmatrix}. \tag{5.6}$$

In this chapter these matrices define the target qubit operations. In the following subsection the minimum number of $dU_j$ to be multiplied and the input parameter values defining these part operation matrices will be investigated.

To be relevant the analyzed gates need to have a low infidelity. In this case the infidelity should be significantly below the surface code benchmark of $b = 10^{-2}$. Other works have analyzed in detail how to find and implement the best fidelity possible, but that is not in the scope of this work. The less complex investigation here is sufficient to draw qualitative conclusions about the severity of the noise influence and derive control circuit specifications from that. Focusing on the possible circuits and connecting this to qubit simulation has not been done this way in previous publications.

### 5.3.1 Finding pulse sequences

A minimum of two different amplitudes in a rectangular pulse sequence is needed to enable rotations around any axis in the Bloch sphere. This is due to the fixed sign of $\omega_J$ and $\Delta\omega_z$ because of the physical qubit implementation. The effect of the fixed sign can be understood with the help of Fig. 5.1. The rotation axes vectors of the base rotations are shown there and any resulting rotation axis vector given through vector addition is limited to the first quadrant of the x-z-plane. The use of more than one amplitude expands the potential rotation to all directions in the Bloch sphere.

Two different voltage amplitudes lead to a pulse sequence as depicted in Fig. 5.2 with four variables $t_1$, $t_2$, $\epsilon_1$ and $\epsilon_2$ describing the pulse. In other works on pulse optimization a constant time step was assumed, as that is easier to implement in clocked systems [83]. However, for a qualitative study of the influence it is more straight forward to use varying durations. The variables are still limited in their viable range. For the durations $t_1$ and $t_2$ the minimum is given with a potential circuit realization in mind where the time resolution is finite. The coherence time of the qubit poses the upper border for the time [59], leading to $t_{1,2} \in [0.1\,\text{ns}, 30\,\text{ns}]$. The range of the amplitude variables $\epsilon_{1,2}$ is limited by the constrained validity of the $\omega_J(\epsilon)$ fit [59, 60]. Therefore, the amplitude variables are set $\epsilon_{1,2} \in [-1.4\,\text{mV}, 1.4\,\text{mV}]$, here.

The search for a good gate fidelity is complex, even with a simple pulse as in Fig. 5.2. Minimizing the infidelity (1-$F$) is a nonlinear four-dimensional optimization problem with secondary conditions. Conditions besides minimum infidelity are the restricted

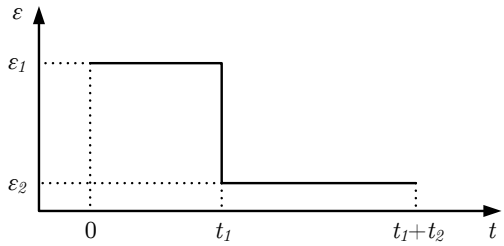


Figure 5.2: Concept of pulse sequence for any rotation defined by four variables $t_1$, $t_2$, $\epsilon_1$ and $\epsilon_2$

parameter ranges of a realizable technical system. The objective function results from Eq. 2.18 and 2.10 leading to the following problem:

$$\min \left(1 - \frac{1}{n^2} |\mathrm{Tr}[U_{ideal}^T \cdot U_{21}]|^2\right). \tag{5.7}$$

The overall unitary matrix $U_{21}$ is calculated with $U_{21} = dU_2 \cdot dU_1$ and the part operation matrices $dU_2$ and $dU_1$ are defined by the four variables $t_1$, $t_2$, $\epsilon_1$, $\epsilon_2$ and Eq. 5.2. The matrix multiplication is an efficient and accurate way to calculate the unitary matrix of the ideal complete signal because of the piecewise constant nature of the signal.

The optimization problem can in general not be solved analytically. For this reason a sweep of all four parameters has been done first to get a first overview of the parameter dynamic. This leads to a better understanding of the problem at hand. Out of this sweep also a first approximation for a good solution with minimum infidelity can be gained. Extracted results of the sweeps can be seen in Fig. 5.3, with 2D slices of the complete 4D parameter space. In each subfigure two parameters are varied while the other two are set to the value of the global minimum found for that gate. The infidelity value for a given set of parameter values is indicated through the color. While only solutions of nearly zero are potential solutions for the problem, the linear color scale gives more information on the parameter dynamics. Overall the results of the sweeps are not intuitively accessible, as the optimization problem is quite complex. The plots in Fig. 5.3 illustrate this complexity, but also allow some insights into the dynamics of the minimum infidelities and the parameter dependencies. This makes first statements about how easily optimization algorithms will deal with this problem possible.

One challenge in the optimization of the pulse forms is $\epsilon$, whose parameter range leads to $\omega_J \in [5.9 \cdot 10^6, 1.7 \cdot 10^{11}] s^{-1}$. This parameter used in calculating $dU$ spans several orders of magnitude, which makes numerical accuracy an issue. However, the use of $\epsilon$ as an input parameter makes sense, as this is the signal produced by the control electronics. Another challenge are the different dynamics of the parameters. For all plots with a

time variable involved, a periodic dependency of the infidelity on the time variables can be observed. With the 4D parameter space in mind, this makes finding an overall minimum difficult. For example, during the optimization the nearest best optimum keeps changing during the process. Next to the regular periodic behaviour also chaotic behaviour can be observed. In plots involving the $\epsilon$ parameters some areas seem partly or even completely chaotic in the infidelity dependence on the parameters. Startling is the fact that in these chaotic parts, the lowest infidelity value is found in some cases. Similar to the periodicity this behaviour makes finding the overall minimum more difficult. The periodic and chaotic behaviour in some areas leads to very high infidelity changes with a small parameter difference. In contrast to that also bigger parameters regions with little infidelity change exist. One example for that is to be found in the $\epsilon_1/\epsilon_2$ plots. This dynamic difference can also be a challenge for some optimization algorithms.

A clear minimum in all parameters has not been found through this sweeping method. On top of that the parameter resolution with 50 points per parameter is not high enough for a very accurate solution, so the next step in finding good solutions is to employ numerical optimization tools. As this is a difficult problem, several methods to define starting points were used. The first method is to start numerical optimization algorithms from the points with the smallest infidelity in the sweep. This is under the assumption that a good solution is nearby the sweep solution, but that the step width was too big. A numerical optimization fixes that. The second methods is to use random starting points under the assumption that some minima were not registered by rough stepping. The optimization was done with Matlab with the fminsearch and fsolve functions which use the Nelder-Mead simplex [130] and the Levenberg-Marquardt [131] algorithm. For both starting methods both algorithms were tried for a comparison. Both showed similar performances in coming up with minimum infidelities.

In case that some possible candidate for a solution was overlooked by starting from best infidelities of the step sweep, also random starting points were used. For the $U_{\frac{\pi}{2},y}$ gate this method provided the lowest infidelity.

Since both optimization algorithms work with unconstrained variables, the optimization problem from Eq. 5.7 has to be rewritten (similar to [59]). Thus, all parameters $x_j$ are substituted with $\tilde{x}_j$, such that $x_j = A + B\sin(\tilde{x}_j)$. Optimizing with the parameters $\tilde{x}_j$ has the result that the parameters $x_j$ are bound to $x_j \in [A - B, A + B]$ through the sine function. The resulting $x_j$ parameters found are summarized in Tab. 5.1. The infidelity solutions are in all cases notably below the threshold of the error correction.

For all rotations an improvement of the fidelity through the numerical optimization in comparison to the sweep minimum infidelity has been observed. In the case of the y-rotation the infidelity change from the best sweeping solution is the largest. It spans several orders of magnitude.

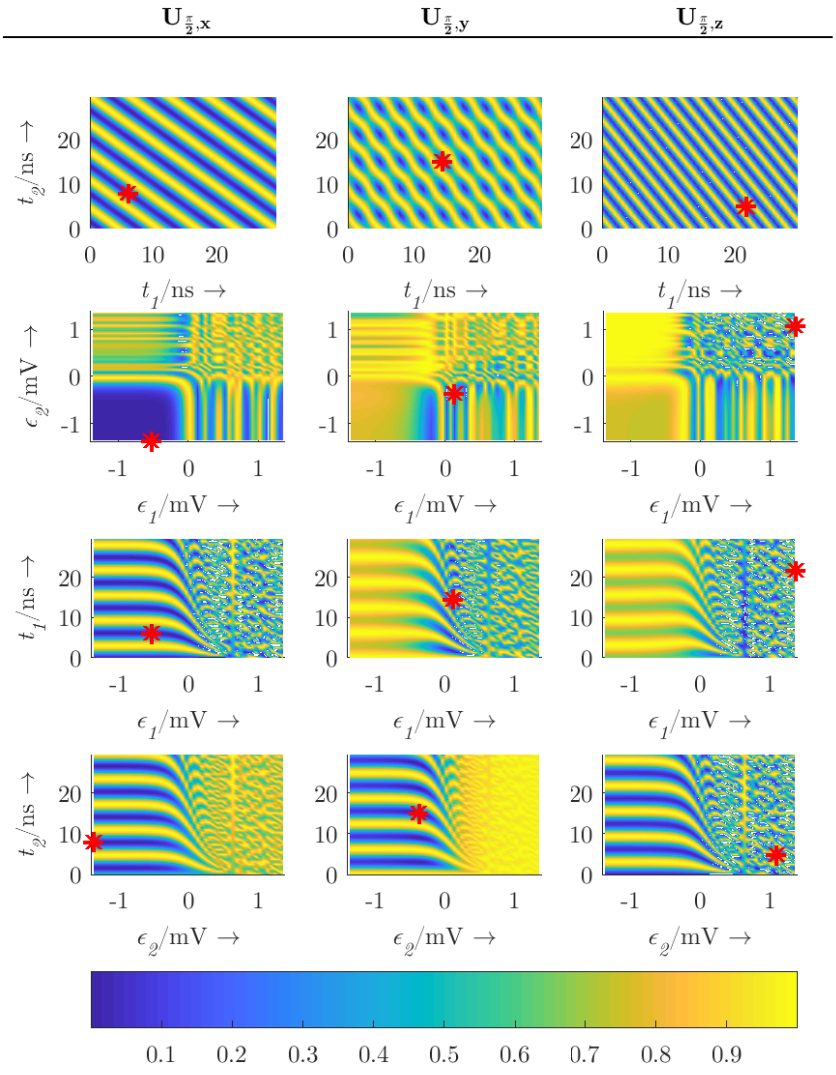


Figure 5.3: Infidelity for 2D extracts of the swept 4D parameter space. All plots include the point of overall minimum infidelity (red '∗'). Values of the two parameters not on axis are constant.

| gate | $t_1$/ns | $t_2$/ns | $\epsilon_1$/mV | $\epsilon_2$/mV | $1 - F$ |
|---|---|---|---|---|---|
| $U_{\frac{\pi}{2},x}$ | 6.1 | 7.9 | -0.5 | -1.4 | $1.1 \cdot 10^{-5}$ |
| $U_{\frac{\pi}{2},y}$ | 1.9 | 3.1 | 0.07 | -0.6 | $7.1 \cdot 10^{-13}$ |
| $U_{\frac{\pi}{2},z}$ | 21.3 | 18.5 | 0.4 | 1.4 | $1.1 \cdot 10^{-5}$ |

Table 5.1: Parameter values found through numeric optimization with reached infidelity

The signals found for the best infidelity solutions are depicted in Fig. 5.4. As the durations of the two amplitudes in each pulse are independent, the pulses have varying total length. For further simulations, the simulation time is set to the total length of the pulse. Noticeable is also, that all gates have two distinct values, even though a x- and z-gates are possible with just one. Only one value would be enough as these rotations are in the direction of the base rotations given by $\omega_J$ and $\Delta\omega_z$ (see Fig. 5.1), but this type of pulse leads to higher infidelities. The reason why two amplitudes are beneficial is that through the limited $\epsilon$ range the error with a single pulse is too big. Due to the physical implementation of the qubit and the resulting exponential dependence on $\epsilon$, $\omega_J$ cannot be turned off completely. $\Delta\omega_z$ is a property of the host material and effort in the form of DNP is made to keep the value at a set and constant value during the experiment. Both of these limitations lead to a unavoidable residual rotation around the unwanted axis during a x- or z-rotation. With a two-value pulse compensation for this unwanted rotation is possible.

The fact of a certain unavoidable residual rotation is also the reason for the extreme $\epsilon$ values in the x- and z-rotation pulses. If $\omega_J$ is turned on as much as possible (big positive $\epsilon$), the effective rotation is nearly a z-rotation. However, if $\omega_J$ is turned off as much as possible (big negative $\epsilon$) the result is nearly a x-rotation because $\Delta\omega_z$ is still constant. For the y-rotation these extreme values and behaviors are not necessary and as such also the infidelity of the y-rotation is several orders of magnitude lower than for the other rotations (Tab. 5.1). This very low infidelity cannot be realistically implemented in a real system but gives an indication on the quality of the found solution. The specific form of the pulses does not follow any easy recognizable systematic, as they are the result of the optimizer in a complex problem. That also means that somewhat different looking pulses could achieve similar infidelity results.

The Bloch sphere representations of the found solutions are included in Fig. 5.5. For this simulation now a lot of part operation matrices $dU$ are calculated at timesteps of $\Delta t = 0.9\,\text{ps}$. Also, in Fig. 5.5 the contrast between the y-rotations and the other two rotations is clear. While the y-rotation path from the start to the end point is fairly direct, the other rotations have several complete turn around the sphere. The reason for the exact number of turns here is that this combination produced the best infidelity during the optimization, but the phenomenon should be looked into more deeply.

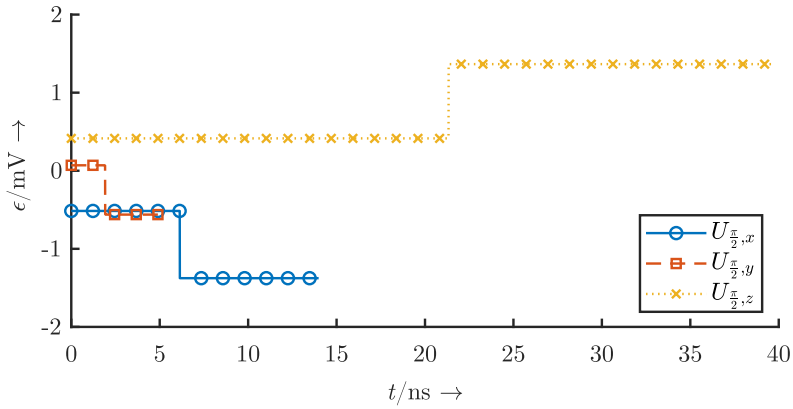


Figure 5.4: Optimized voltage signal progression for $\frac{\pi}{2}$-rotations around different axis

While not all characteristics of the surface sweeps in Fig. 5.3 are intuitively accessible, the periodicity of time plots $t_2$ vs $t_1$ can be understood with the several turn rotation results in Fig. 5.5. As already mentioned, for the fidelity of a gate operation the path around the Bloch sphere is irrelevant. The only interesting characteristic is the accuracy of the end point in relation to the starting point. The qubit perpetually precesses around an axis $\vec{S}_{pre}$ defined by $\omega_J$ and $\Delta\omega_z$ with

$$\vec{S}_{pre} = J\left(\epsilon\left(t\right)\right) \cdot \vec{e_z} + \Delta B_z \cdot \vec{e_x}. \tag{5.8}$$

The angular frequency of the precession around that axis is given by

$$\omega_{pre} = \sqrt{\omega_J\left(\epsilon\right)^2 + \Delta\omega_z^2}. \tag{5.9}$$

That implies that a rotation of $\delta = \frac{\pi}{2}$ can in fact be a rotation of $\delta = \frac{\pi}{2} + 2\pi k$ with $k \in \mathbb{N}$. That means that with the same applied voltage, many solutions of $t_1$ and $t_2$ combinations are possible. The minimum duration is set by the possible $\epsilon$ values and the maximum duration solution is given by the maximum time limit.

## 5.4 Sensitivity

With a set of gates chosen, the next step is the study of inaccuracy effects on the gate fidelity. Static inaccuracy happens for example due to limited time and amplitude resolution of the circuits supplying the control signals. The influence of inaccuracies

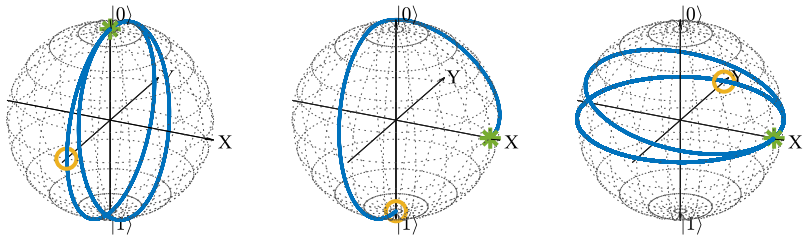


Figure 5.5: Bloch sphere representations of the found gate solutions with '$*$' as the starting point and '$\circ$' as the end point. (a) x-rotation $U_{\frac{\pi}{2},x}$, (b) y-rotation $U_{\frac{\pi}{2},y}$ and (c) z-rotation $U_{\frac{\pi}{2},z}$.

as constant offsets on any of the parameters is shown for all gates in Fig. 5.6. For better comparison, the relative parameter deviations $\Delta x/x$ are plotted with $\Delta x$ the deviation and $x$ the norm value. The data lines were cut at the point where the infidelity first reaches $1 - F = 1$. For higher deviations there exist also values with again lower infidelities due to the periodic behaviour, but the characteristics of such solutions show a very sharp minima and is therefore not useful as a stable solution. The deviations $\Delta x/x$ are all positive, which was the worst-case scenario for all gates and parameters.

All rotations converge to one infidelity value for small deviations from the norm value in the available plots (for better visibility the $1-F$ parameter is not always plotted down the convergence value, which is not relevant for very low values.). The value these rotations converge to is the infidelity of the solution found by the optimizer, as expected.

For large portions of the parameters and the deviation range the slope of the increase of infidelity vs. the increase of relative deviation is 2. This is because most found solutions are minima where a quadratic fit can be made near the minimum. Exceptions to the quadratic behaviour are for example the $\epsilon_1$ and $\epsilon_2$ values for the x-rotation in Fig. 5.6a. The reason for that is that in these cases the found solution is an atypical minimum or a border solution. The effects of this are for example visible in the corresponding $\epsilon_1/\epsilon_2$ surface sweep depicted in the left column of Fig. 5.3. Due to this the slope of infidelity vs. deviation is smaller, as no sharp minimum is found. While the solution found for the z-rotation is also at the very edge of the parameter range, the found solution is nevertheless a minimum.

The placement of the infidelity plots of all the gates on top of each other makes different sensitivity ranges obvious and even for one gate the sensitivity varies somewhat. By comparison, the z-rotation has the highest sensitivity to parameter deviations of all the gates. This is due to dependence of the sensitivity on the voltage value. In general, the

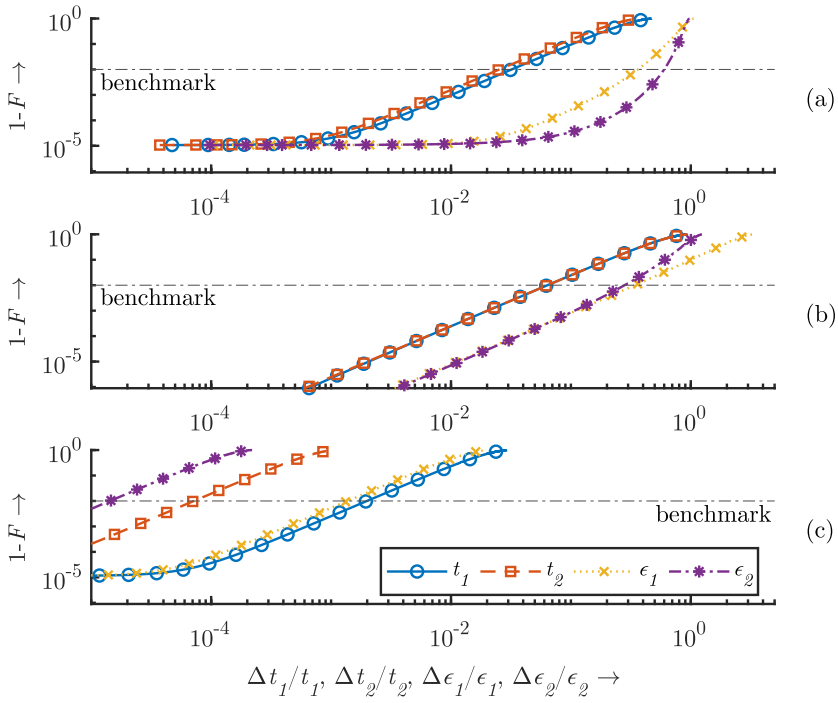


Figure 5.6: Sensitivity diagrams: infidelity for relative deviations from the norm value for all gates and all parameters. The results include only values for deviations until the infidelity first reaches $1 - F = 1$. (a) x-rotation $U_{\frac{\pi}{2},x}$, (b) y-rotation $U_{\frac{\pi}{2},y}$ and (c) z-rotation $U_{\frac{\pi}{2},z}$.

sensitivity of the parameters can be approximated through looking at the gradient of the $\omega_J(\epsilon)$ curve (Sec. 6.6.2 in [2]):

$$\text{sensitivity} \propto \frac{\mathrm{d}\omega_J(\epsilon)}{\mathrm{d}\epsilon}. \tag{5.10}$$

This implies that the bigger the $\epsilon$ values of a given gate sequence are, the bigger the sensitivity towards inaccuracies is. This effect is enhanced by the fact that the $\epsilon$, $\omega_J$ relation is exponential leading to huge sensitivities for bigger $\epsilon$. This is confirmed by the results presented in Fig. 5.6 which makes the differences of the gates and the variation in one gate clear.

From the big range of results in Fig. 5.6 some expressive points can be extracted. The first set of indicative values is the infidelity reached through a 1 % deviation in one of the pulse parameters. These infidelities are listed in Tab. 5.2. This helps also in a comparison with other electrical systems. For the x- and y-rotation a 1 % deviation in one parameter is still viable. The resulting infidelity is still smaller than the fault tolerance benchmark value of $10^{-2}$. However, for the z-rotation the 1 % change from the norm value is increasing the infidelity to value beyond possible fault tolerance with a maximum infidelity of 1. The deviation from the norm of several parameters at once is not meaningful, as unpredictable compensation effects are very likely to occur.

| parameter | $U_{\frac{\pi}{2},x}$ | $U_{\frac{\pi}{2},y}$ | $U_{\frac{\pi}{2},z}$ |
|---|---|---|---|
| $\epsilon_1$ | $9.8 \cdot 10^{-4}$ | $2.5 \cdot 10^{-4}$ | $4.5 \cdot 10^{-1}$ |
| $\epsilon_2$ | $1.6 \cdot 10^{-3}$ | $2.4 \cdot 10^{-4}$ | $> 9.9 \cdot 10^{-1}$ |
| $t_1$ | $1.2 \cdot 10^{-5}$ | $7.6 \cdot 10^{-6}$ | $2.3 \cdot 10^{-1}$ |
| $t_2$ | $1.2 \cdot 10^{-5}$ | $6.9 \cdot 10^{-6}$ | $> 9.9 \cdot 10^{-1}$ |

Table 5.2: Infidelity values for 1% deviations of the norm values of one parameter for the different gates and parameters

In reverse it is interesting which maximum deviation can be tolerated without compromising the fault tolerant operation with the surface code. This determines the minimum requirement for electrical circuit producing the gate signals. The extracted deviation values are summarized in Tab. 5.3. The minimum tolerable relative deviation is given for the z-rotation and the parameter of $\epsilon_1$. The relative deviation of $1.4 \cdot 10^{-5}$ corresponds to a small $\Delta\epsilon_2 = 19.6\,\text{nV}$, which is extremely hard to achieve as circuit implementation gets increasingly more complex with rising accuracy. The smallest relative deviation of a time parameter is tolerable for $t_2$ in the z-rotation. The absolute derivation acceptable is calculated to $\Delta t_1 = 1.3\,\text{ps}$.

| rotation | $t_1$ | $t_2$ | $\epsilon_1$ | $\epsilon_2$ |
|---|---|---|---|---|
| $U_{\frac{\pi}{2},x}$ | $3.2 \cdot 10^{-2}$ | $2.5 \cdot 10^{-2}$ | $3.6 \cdot 10^{-1}$ | $6.0 \cdot 10^{-1}$ |
| $U_{\frac{\pi}{2},y}$ | $6.4 \cdot 10^{-2}$ | $6.4 \cdot 10^{-2}$ | $3.4 \cdot 10^{-1}$ | $2.8 \cdot 10^{-1}$ |
| $U_{\frac{\pi}{2},z}$ | $2.0 \cdot 10^{-3}$ | $7.2 \cdot 10^{-5}$ | $1.4 \cdot 10^{-3}$ | $1.4 \cdot 10^{-5}$ |

Table 5.3: Maximum relative deviation from the norm value for each parameter for $1 - F = 10^{-2}$

### 5.4.1 Conclusion

All the results in this section point to the fact that key parameters like the sensitivity are not static characteristics of the qubit, but rather properties that change with the voltage signals applied to the qubit. This type of behaviour can be compared with the small signal characteristics of a transistor with a set width, length, and operation point. The difference here is that the 'operation point' is a fast-changing voltage signal dependent on the logical function of the qubit.

As the sensitivity is proportional to $\epsilon$ and thus $\omega_J(\epsilon)$, a preference for low $\epsilon$ values is indicated. This means that more complicated pulse forms with lower voltage values can be beneficial for the sensitivity.

## 5.5 Frequency behaviour

The study of the frequency dependent behaviour is relevant to see if filtering or techniques such as noise shaping are useful in the operation of qubits. Due to the highly sensitive qubit such techniques could greatly influence the requirements of the control electronics. As straight forward calculation of the noise to infidelity transfer function is not possible due to the complexity of the qubit state and the gate fidelity calculation. One method to approximate a transfer function in the frequency space is to add sinusoidal signals on top of the control signal and simulate the infidelity of the qubit. Another method to study the frequency dependent susceptibility to noise is the calculation of so-called filter functions of the qubits. They are employed in the physics dominated quantum computing community to among others study noise mitigation techniques [82].

### 5.5.1 Sinusoidal interference signal

In Fig. 5.7 the infidelity of all the gates is shown vs. the frequency of the added interference sine signal. As the lowest frequency of 10 kHz is quasi-static in comparison to the pulse

length of $< 40\,\text{ns}$, the phase of the sinusoidal signal is set to $\eta = \frac{\pi}{2}$ to get a worst case scenario. The sample time for all signals is set to $t_s = 40\,\text{fs}$ to achieve comparable, accurate results even at high frequencies.

In general, all gates show a lowpass behaviour. Thus, signals with lower frequencies have a bigger impact than signals at higher frequencies. The bandwidth of this lowpass changes only little from one gate to another. However, the amplitude of the sinusoidal signal used to cover the complete infidelity range at low frequencies shows a significant variation. While the maximum amplitude shown for the x-rotation is 0.7 mV the largest amplitude is only 3 µV for the z-rotation.

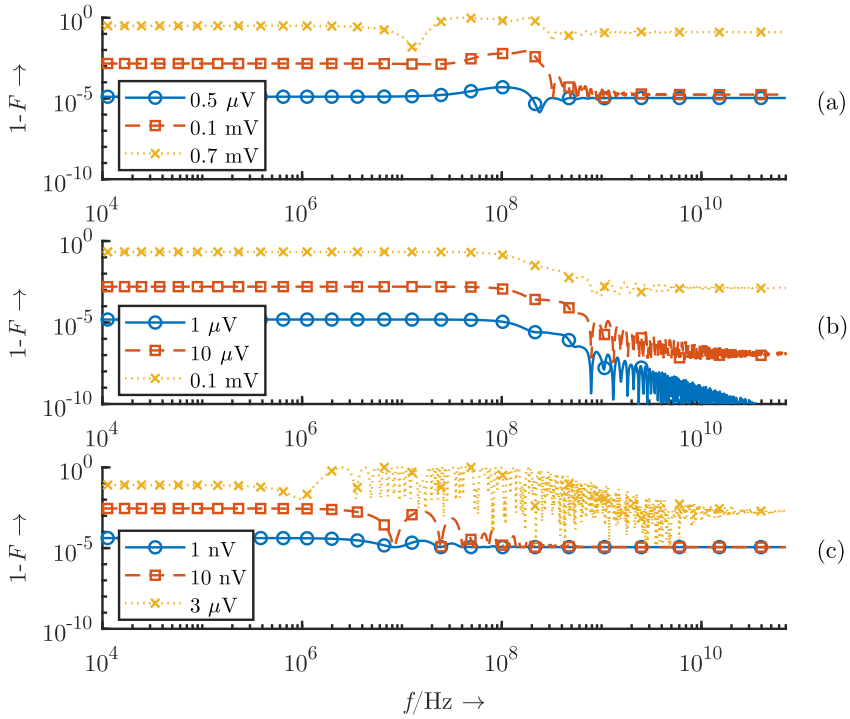


Figure 5.7: Infidelity with differing amplitudes of sinusoidal interfering signal (phase $\eta = \pi/2$ for worst case behaviour) at given frequencies $f$ for all gates. (a) x-rotation $U_{\frac{\pi}{2},x}$, (b) y-rotation $U_{\frac{\pi}{2},y}$ and (c) z-rotation $U_{\frac{\pi}{2},z}$.

### 5.5.2 Filter functions

In the filter formalism the relation between the fidelity and the noise spectrum is given ([34, 82]) by

$$F = \frac{1}{2}\left[1 + \exp\left(-\chi\left(t\right)\right)\right], \text{ with } \chi\left(t\right) = \frac{1}{\pi}\int_0^\infty F_{filt}\left(\omega\right) S\left(\omega\right) \mathrm{d}\omega. \tag{5.11}$$

Here, the $S(\omega)$ is the single side power spectral density and $F_{filt}$ the single side filter function of the qubit which is defined through Eq. 23, 27, 29 and 30 in [34]. The filter function for the found gate solutions in this chapter are depicted in Fig. 5.8. The derivation of the filter function is quite complex, but there exist software packages that help with that. Here the filter functions have been calculated with the help of filter_functions python software package by T. Hangleiter in the Quantum Technology Group of H. Bluhm at the RWTH Aachen [132]. The behaviour shown in Fig. 5.8 is similar to the one simulated through the sinusoidal signals in the last subsection. All the filter functions are lowpass functions with similar bandwidths compared to the sine results. A difference is however the behaviour at high frequencies. While the results from the sinusoidal simulation in some cases converge to a value, there is no such effect to be seen for the filter functions.

The filter functions of the different gates show a large range in the amplitude at low frequencies. Between the largest amplitude of the z-rotation and the x-rotation with the smallest, a difference of eight orders of magnitude can be seen. The different magnitudes lead to varying impact of interfering singals on the fidelity. The lower the filter function magnitude, the lower the impact of the interfering signal. This is attributed to the sensitivity differences of the gates (Eq. 5.10).

In Fig. 5.9 a direct comparison of infidelity calculation with the sinusoidal signals ('sine added') and with the filter function ('filter function') can be seen. As expected from the shape of the filter function, the results are similar to the ones from the sine signals. However, differences in the low frequency infidelity value can be seen and the behaviour at very high frequencies diverges. One potential reason for the difference at very high frequencies is the numerical accuracy of Matlab, as increased errors in the infidelity calculations have been observed for high sample rates. As the sample rate cannot be lowered significantly due to the high frequency of the sine signals, this error cannot be mitigated easily. The deviating infidelity at low frequencies is expected to be due to the simplified nature of the state simulation implemented here.

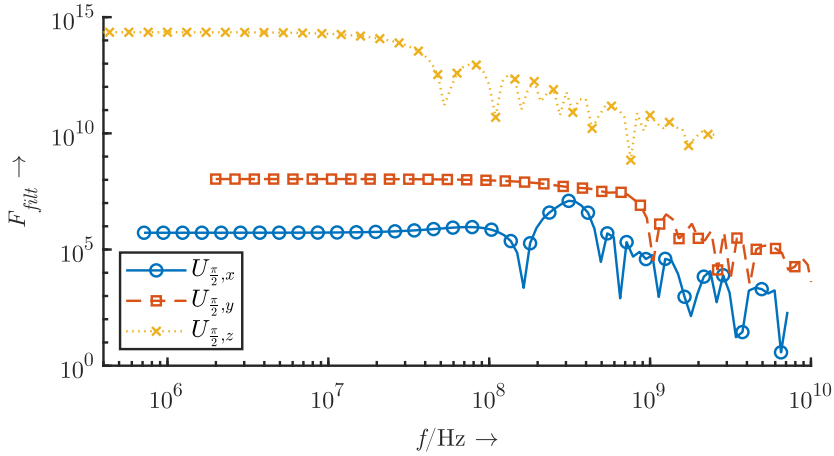


Figure 5.8: Filter functions $F_{filt}$ that are used to describe the frequency noise filtering behaviour of the different qubit gates

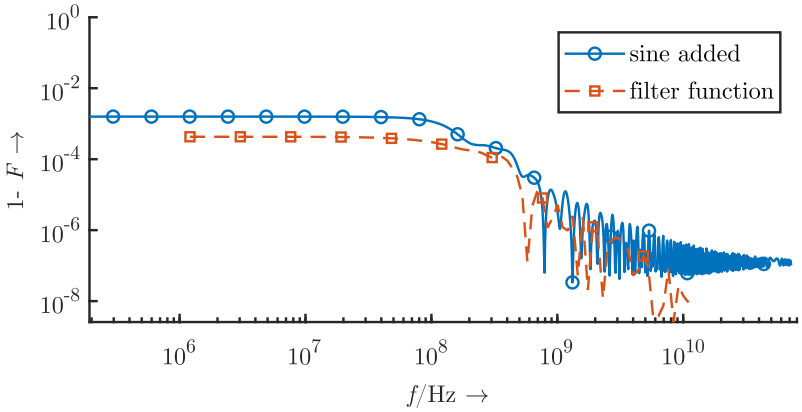


Figure 5.9: Comparison of the infidelity 1-$F$ vs frequency simulated with the sinusoidal signal added and a following state simulation and the simulation using the filter function

### 5.5.3 Summary

Overall, the frequency dependence of the sensitivity to interference signals is that of a lowpass filter. That means that signals at frequencies beyond a few hundred MHz have less of an effect. This could be used for noise shaping considerations, however any additional circuit power consumption due to this has to be critically examined. While the high susceptibility to quasi static noise is an issue here, studies show that this effect can be mitigated through so called echo techniques [82]. In general, the sensitivity to the noise amplitude relates to the sensitivity (Eq. 5.10).

The comparison of the sinusoidal implementation and the filter function show a similar behaviour but with significant differences. The sine test and the qubit state simulation derived here are simplistic compared to the exact and highly complex models that are employed by the physical modeling. That the simple model nevertheless gives a good idea of how the qubit behaves is promising. This means that such type of simulation is suitable for determining circuit specifications without going too deep into theoretical physics.

## 5.6 Noise power influence

Next to the influence of interfering signals at specific frequencies, the influence of broadband white noise is of interest. For example, background noise is typically broad band and plays an important role as it can be difficult to reduce. The influence of white noise is here investigated for different noise power levels $P_n$. To avoid statistical simulation effects, for every noise power level several different random noise traces are used in the investigation. On top of that the random noise traces generated by Matlab's white gaussian noise (wgn) function are adjusted to have no mean, as the traces provided by the function do not have a mean of completely zero. The white noise is added to the $\epsilon(t)$ control signal and both are sampled with $t_s = 10\,\text{fs}$. The short sampling time is used to avoid relevant lowpass filtering effects through the sampling. The results of the infidelity simulation of all gates with added noise are shown in Fig. 5.10. For better comparability the mean of the individual noise traces is plotted together in Fig. 5.11. All the lines in the plot converge to a value for very low noise power levels. For the x and z-rotation that value corresponds to the infidelity value of the optimizer solution in Tab. 5.1. However, the convergence value for the y-rotation is about two orders of magnitude higher than the optimizer solution. The reason for that is the finite sample time of the simulation. Investigations have shown that even a time resolution of 10 fs introduces a noticeable error and the value of the y-rotation converges to a lower minimum with decreasing sample time.

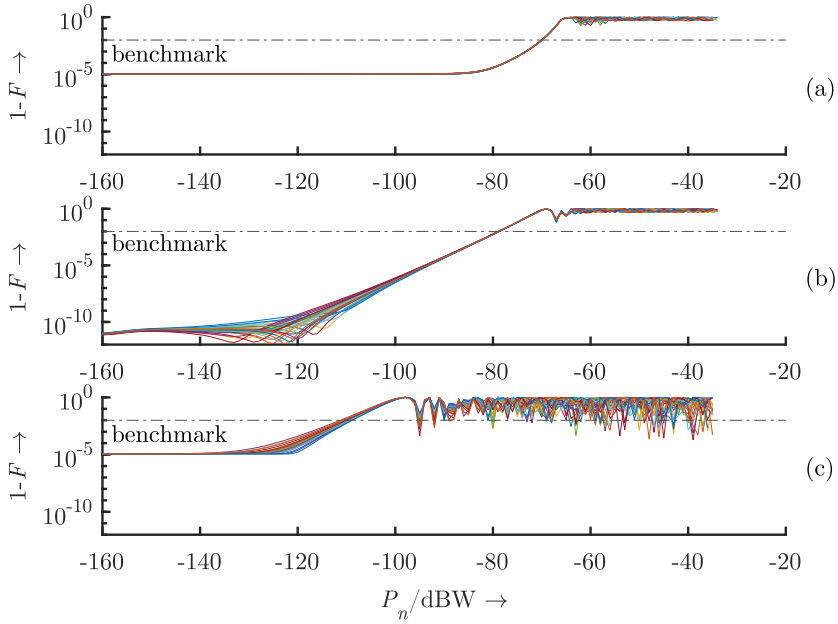


Figure 5.10: Infidelity of all gates for different white noise powers $P_n$ and different white noise seeds (lines): (a) x-rotation $U_{\frac{\pi}{2},x}$, (b) y-rotation $U_{\frac{\pi}{2},y}$ and (c) z-rotation $U_{\frac{\pi}{2},z}$.

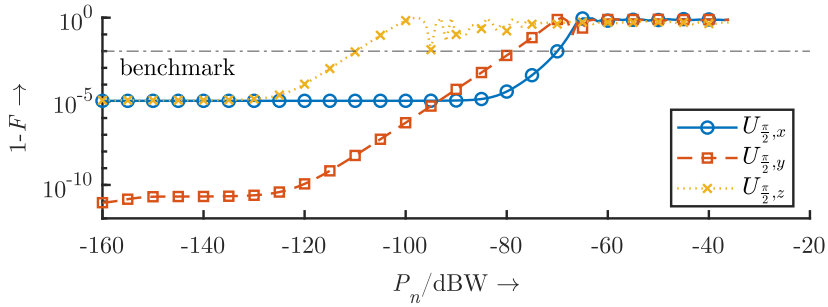


Figure 5.11: Mean infidelity of all gates vs. the white noise power level $P_n$

As in the studies before, the gates differ significantly in their ability to tolerate noise. Again, the x-rotation can tolerate the most noise and the z-rotation the least. The noise levels acceptable for qubit operation, which means that the infidelities are below the fault tolerant benchmark, are summarized in Tab. 5.4.

| | $U_{\frac{\pi}{2},x}$ | $U_{\frac{\pi}{2},y}$ | $U_{\frac{\pi}{2},z}$ |
|---|---|---|---|
| allowed noise power level | −70 dBW | −79 dBW | −110 dBW |

Table 5.4: Maximum possible white noise power level for fault tolerance ($1 - F = 10^{-2}$)

### 5.6.1 Summary

In the susceptibility towards noise power the general sensitivity of the different gates plays a deciding and perceivable role. It greatly influences at which noise power level the surface code benchmark is crossed. A factor influencing the gradient is the type of minimum found. The x-gate especially highlights this, as both $\epsilon$ values had not a sharp minimum but rather a fringe solution. Due to the differing slope of the sensitivity, a changed gradient can also be seen in the noise power simulation here.

## 5.7 Conclusions and implication for circuit designer

From all the results in this chapter a set of specifications can be extracted which are summarized in Tab. 5.5. In the different columns specifications for the individual gates are included, but also values for all gates together are listed. In all cases the specified values for all gates are determined by the z-rotation. This is in line with the results of the last subsections and can be explained by the sensitivity- voltage-relation. However, for the x- and y-rotation the specified values would much stricter than necessary for high fidelity operation. For the voltage and time accuracy that difference is nearly two orders of magnitude. That means an electrical system complying with these specification would be much more difficult to implement than needed for the x- and y-rotations.

The investigations show that the specifications are always critical but this challenge can be mitigated through close cooperation of the people designing the gate sequences and the people designing the qubit control circuits. Tools which include knowledge and experience from both fields as presented in this chapter are vital to that.

As the magnitude of the control pulse is proportional to the sensitivity regarding noise, sequences with the lowest possible magnitude are in general advisable (Eq. 5.10).

| Parameter | $U_{\frac{\pi}{2},x}$ | $U_{\frac{\pi}{2},y}$ | $U_{\frac{\pi}{2},z}$ | all |
|---|---|---|---|---|
| Deviation voltage/μV | 824.8 | 157.5 | 0.02 | 0.02 |
| Deviation time/ps | 196.7 | 122.0 | 1.3 | 1.3 |
| Interfering sine amp./μV < 1 GHz | 100 | 10 | 0.01 | 0.01 |
| White noise power level/dBW | −70 | −79 | −110 | −110 |

Table 5.5: Specification summary for every gate and all gates together, for each effect to stay below $1 - F = 10^{-2}$

# Chapter 6

# Modeling qubits and electronics together

## 6.1 Motivation and method

So far in this work behavioral models of scalable control electronics and the qubit have been presented. Individually they are tools to investigate critical parameters for feasibility and scalability of the lowest levels of the quantum computer. In a last step to complete the system simulation, the control electronics and the qubit model are combined together in this chapter. The overall model is again based on Simulink/Matlab as a standard software environment, which has extensive options to combine it with other tools and programming languages, as mentioned in Chap. 4. Together with the modularity of the model this makes the system model easy to modify, extend and thus to utilize it in future research projects.

Besides combining the model parts, the behavioral model of the electronics is refined through added parasitic effects. With the included non-idealities it can be investigated how typical non-idealities and noise sources in electrical circuits influence the qubit. This is relevant for circuit design in order to give a perspective on what characteristics are the most important to optimize for best gate fidelity.

In the abstract qubit model only the RF signals influence the qubit state (see Chap. 5). Since the RF generation part is only active during the qubit operation (state M3 of the managing unit, see Sec. 4.5.1), not the complete simulation of all states is necessary. The model used here is thus the reduced model as described in Sec. 4.5.4. The influence of the RF generation non-idealities is exemplary investigated with two different pulse forms for a rotation around the y-axis by an angle of $\phi = \frac{\pi}{2}$.

## 6.2 Modeled non-idealities

The principle of the RF generation model including non-idealities is shown in Fig. 6.1 and was derived from the RF generation model in Fig. 4.17. The model in this chapter includes

only one RF electrode. This is possible with the assumption that the other RF electrode is held at a constant voltage, which simplifies the investigation. The manipulation of two RF electrodes as set in Chap. 4 gives a higher flexibility for exploratory experiments.

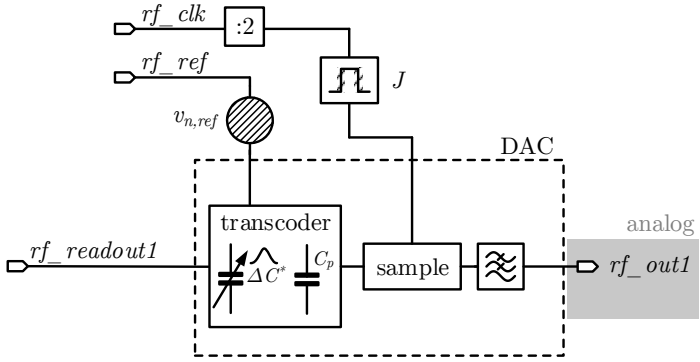


Figure 6.1: RF generation model with non-idealities

Typical noise sources in mixed-signal electrical circuits are noise on the reference voltage $v_{n,ref}$ and noise on the clock signal. The noise on the clock signal is here described through the jitter $J$. Next to noise also parasitic effects in the DAC - besides the lowpass filtering - have been added. The DAC non-idealities are parasitic capacitances $C_p$ connected to ground and the inclusion of process variations for the DAC unit capacitors.

For the numerical investigation of these effects typical parameters have been used in the simulation. Tab. 6.1 gives an overview of the values. A more detailed explanation is included in the following subsections.

| $J$ | $v_{n,ref}$ | $\Delta C^*_{3\sigma}$ | $C_p$ |
|---|---|---|---|
| 300 ps | 10 µV | 9% | 50 fF |

Table 6.1: Parameter values of non-idealities

### 6.2.1 Jitter

One typical result of noise in clocked systems is jitter. Jitter describes the phenomena of the time uncertainty of the clock signal edges. These can differ from the nominal timing through systematic errors, but also random errors occur. Here, only random jitter $J$ is considered. As seen in Fig. 6.1 jitter is added to the sampling clock of the DAC. However, as the same clock signal is typically driving all events of one sub-circuit, the identical

time uncertainty is apparent at the digital input $rf\_readout1$. Like this, the jitter cannot be responsible for wrong input codes and only errors in the input sample time occur.

The jitter is modeled through a gaussian distributed time delay in comparison to the nominal edge time. Thus, the error has a constant effective mean of $\mu_J = 0$. The standard deviation is set to $\sigma_J = 300\,\text{ps}$ (Tab. 6.1), which corresponds to the jitter root mean square (RMS) value of typical laboratory test equipment [133–135]. The value of $\sigma_J$ is set to twice the value of the total jitter of a typical AWG used in current qubit experiments [133].

### 6.2.2 Noise on the reference voltage

The stability of reference voltages for mixed-signal circuits is relevant, as it sets one fundamental limit for the analog performance. Here, white gaussian noise is added to the reference voltage. The amount of noise is given through the RMS voltage $v_{n,RMS}$. The noise sample rate is set to the sample rate of the input signals, as the sampling would filter out noise at higher frequencies. The reference noise is set to $v_{n,RMS} = 10\,\mu\text{V}$, which is slightly above the specification from Chap. 3.

### 6.2.3 DAC nonlinearities

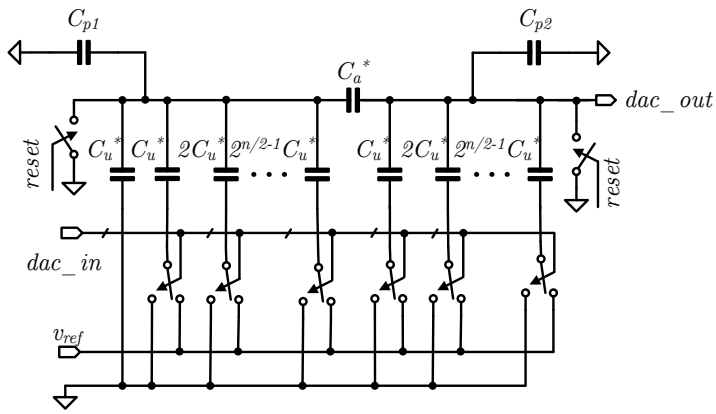


Figure 6.2: Concept of DAC nonlinearities

Parasitics in a DAC have a deciding effect on the quality of the analog output signal. The lowpass characteristic of the DAC has already been included and explained in Sec. 4.5.4. One new addition in this section is the existence of parasitic capacitors $C_{p1}$ and $C_{p2}$ (cf.

Fig. 3.4). They are connected to ground from the middle node of the two capacitor arrays, as depicted in Fig. 6.2. The reason for these capacitors is the geometry of MIM caps in the CMOS technology process. The conservative estimate of these capacitors is here $C_{p1} = C_{p2} = 50\,\text{fF}$.

The second addition to the DAC model in this chapter is the inclusion of process variations. Despite the high-quality production processes of CMOS technologies, some property variations occur nevertheless. This leads to statistically varying device properties with constant dimensions. For the capacitive DAC especially the capacitance variance of the unit capacitors $C_u$ and the capacitor $C_a$ influence the performance. In Fig. 6.2 the existence of capacitor variability is indicated through a '*'. The device variability follows a normal distribution. The key specifications are described in the physical design kit (pdk) of the referenced 65 nm technology, as they are part of the schematic SPICE-based models. Here, the standard deviation is $\Delta\sigma_C^* = 3\%$ for a mean of $\mu_C = C$ for a capacitor C. This is valid for $C_u$ and $C_a$. Often, the so-called process corners are given, which is a deviation by $\pm 3\sigma$ from the nominal value. This value in percent $\Delta C_{3\sigma}^* = 9\%$, is listed Tab. 6.1.

All the non-idealities of the DAC have an influence on its transfer characteristic. In Fig. 6.3 the effect of the different parasitic components is exemplary shown for a resolution of $n = 4\,\text{bit}$. The effect of $C_{p1}$ is mainly a nonlinearity of the transfer characteristic. The gain error is relatively small. In contrast to that the gain error introduced through $C_{p2}$ is significant. Varying process parameters have little effect on linearity and gain.

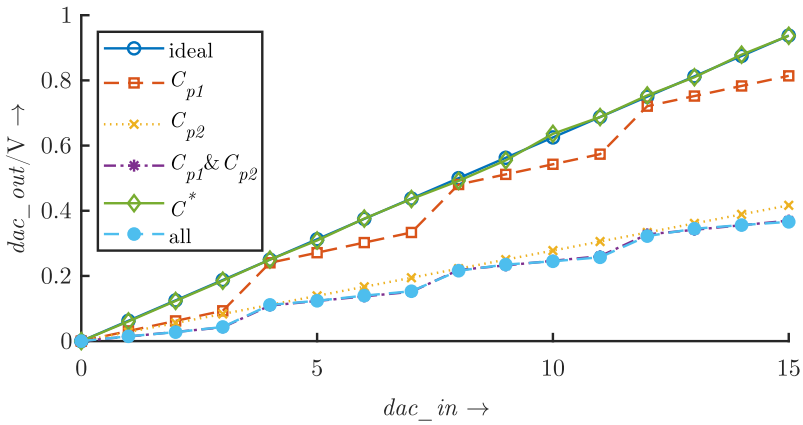


Figure 6.3: Transfer characteristic of a 4 bit DAC

## 6.3 Combined simulation with exemplary pulses

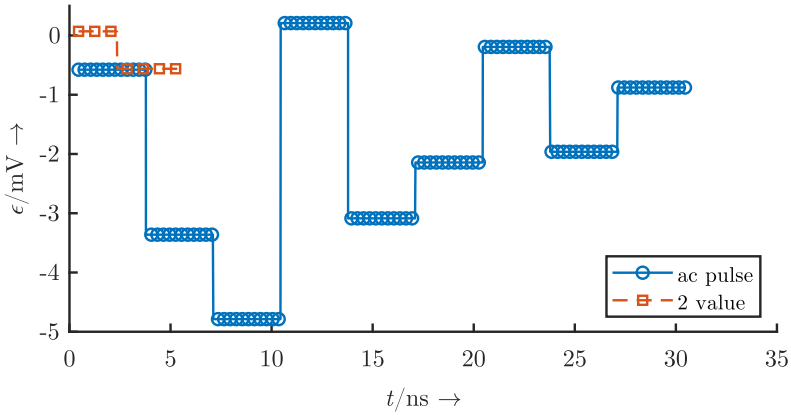


Figure 6.4: Theoretical 'ideal' signals as programmed into the source

The combined simulation is a powerful tool for the investigation of the infidelity of a qubit operation with non-ideal control electronics behaviour. Nevertheless, the infidelity as the key performance indicator is also strongly dependent on the pulse sequence of the RF signal controlling the qubit. As shown in Sec. 5.3 the synthetization and optimization of a pulse sequence suitable for high fidelity values is a critical task and the requirements on the precision are extremely high. This means in practice, that the absolute voltages and the transition characteristic from the signal source to the qubit need to be perfectly accurate for high fidelity results. The effects are strongly influenced by the electrical system generating and transmitting the pulse sequences. Thus, for accurate prediction of the pulse form at the qubit, this electrical system has to be precisely known, too.

With a theoretical system setup all these characteristics are accurate by definition. Thus, the effect of varying disturbing effects such as reference noise can be clearly seen and distinguished from other effects.

However, the investigation of experimental results is much more complex, since statistical and systematic errors of the system are often not known as precisely. Error or distortion sources are for example noise and the transfer functions of critical signal lines, which cannot always be characterized completely accurate. If a well-known error or distortion exists however, it can be partly compensated for during the pulse sequence optimization. Like this the fidelity of a pulse sequence can be increased if the signal transfer function from the source to the qubit is clear.

In contrast to that unknown errors or imprecise system characteristics limit the potential fidelity severely. Nevertheless, the non-idealities of the practical setup like jitter or noise of the generator limit the reachable result as well.

The first exemplary pulse form for the y-rotation is the result of optimization by J. Teske (Quantum Technology Group of H. Bluhm, RWTH Aachen University) and its ideal form is depicted in Fig. 6.4 ('ac pulse'). It has to be pointed out, that this sequence is the optimized theoretical waveform which is to be programmed in the RF-signal generator. The pulse form is optimized for the current experimental setup used by the group. For the specific setup the infidelity of the simulated gate is $1 - F_{ac,setup} < 10^{-2}$. One important setting is the constant sample frequency of the pulse of 300 MHz, which leads to clock frequency of 600 MHz. This is in conformity with the modeled electrical system with a clock frequency $rf\_frequ = 600$ MHz. The pulse itself is 9 samples long leading to a total simulation time of $stoptime = 30$ ns. Long pulses in general make it possible to reduce the maximum positive voltage value for rotation-axes pulses. This expertly leads to a reduced sensitivity to noise, as discussed in the last chapter. In the simulation settings for this pulse the reference potentials of the DAC are set to ±5 mV to map the pulse to symmetric potentials. The resolution of the DAC is set to $n_{RF} = 11$ bit which leads to a similar voltage step size as used in Chap. 3. This is consistent as the specification there are derived from the experimental setup of the Bluhm group. All simulation parameters are summarized in Tab. 6.1. The optimization procedure used for this pulse, which is based on the work in [83], takes the frequency response of the experimental setup into account. That means, among other non-idealities of the practical setup, some lowpass behaviour is included in the numerical optimization. With the sensitivity of the qubit in mind, the infidelity with these diverging system characteristics in the model and in the optimization, the fidelity simulated here is expected to be limited. This is apparent in the fact that the simulated infidelity with the ideal signal is with $1 - F_{ac,ideal} = 8.5 \cdot 10^{-1}$ significantly worse than $1 - F_{ac,setupt}$.

| | stoptime/ns | rf_frequ/Hz | $v_{ref}$/V | $n_{RF}$/bit |
|---|---|---|---|---|
| ac pulse | 30 | $600 \cdot 10^6$ | 5 | 11 |
| 2 value | 5 | $40 \cdot 10^{12}$ | 5 | 11 |

Table 6.2: Simulation parameters

The second pulse shown in Fig. 6.4 ('2 value') is the optimizer solution found in Chap. 5, which theoretically has an extremely low infidelity of $1 - F_{2v} \approx 10^{-11}$ (see Tab. 5.1). As shown in Fig. 6.4 the pulse consists of two voltage levels with different time durations defined with an exceedingly high time resolution. The given infidelity from Chap. 5 has been calculated with a sample time of $t_s = 0.05$ ps, which corresponds to a clock frequency of $rf\_frequ = 40$ THz in the electrical model here. This value is not practicable in reality, but necessary for the time resolution needed for the theoretical realization

of the calculated infidelity[25]. Next to the time resolution, the lowpass filtering with a corner frequency of 600 MHz has a major influence on the time behaviour. The pulse is in total much shorter than the ac pulse (see Fig. 6.4, '2 value'), which sets the simulation time $stoptime = 5\,\text{ns}$. With the original specifications in Chap. 3 in mind, the reference potentials for the DAC are set to ±4 mV. With this the DAC can easily map the '2 value' signal in the ±1.4 mV range. The voltage resolution is again set to $n_{RF} = 11\,\text{bit}$.

### 6.3.1 Results

| pulse | gen | $J$ | $v_{n,RMS}$ | $C^*$ | $C_p$ | all |
|---|---|---|---|---|---|---|
| ac | $8.5 \cdot 10^{-1}$ | $9.2 \cdot 10^{-1}$ | $8.6 \cdot 10^{-1}$ | $8.7 \cdot 10^{-1}$ | $6.6 \cdot 10^{-1}$ | $6.0 \cdot 10^{-1}$ |
| 2v | $3.8 \cdot 10^{-2}$ | $3.7 \cdot 10^{-2}$ | $3.8 \cdot 10^{-2}$ | $3.8 \cdot 10^{-2}$ | $5.6 \cdot 10^{-1}$ | $5.5 \cdot 10^{-1}$ |

Table 6.3: Infidelity values for the signals produced by the RF generation 'gen' with several added non-idealities

Both pulse sequences have in common, that if they are used as inputs for the RF generation unit in the simulation model the infidelity value increases in comparison to the theoretical values. The overall infidelity is very high ('ac pulse') or moderate ('2 value', 'gen' in Tab. 6.3). The reason for the infidelity increase compared to the theoretical values is the lowpass behavior of the DAC in the RF generation unit. This is an expected result, as Chap. 5 showed that the infidelity is quite sensitive towards inaccuracies. The use of the in the optimization not included RF generation circuit introduces significant changes from the nominal shape of the pulse. Fig. 6.5 shows in detail the influence of different non-idealities on the waveform at the output of the RF generation model. Clearly seen is the influence of the RF generation lowpass in all the signals except 'none' which is the theoretical pulse.

The infidelity values for the ac pulse in Tab. 6.3 are especially high and as such the results are only transferable in a limited way. The additional deviation resulting from the added non-idealities of the RF circuit has only a small negative influence on the infidelity in case of the reference noise and the process variations. Additionally, the signal with the added jitter does not deviate much from the RF generation signal (Fig. 6.5), even if the change in the infidelity is somewhat larger (Tab. 6.3). Besides the negative influences on the fidelity however, a positive one is found as well. The addition of parasitic capacitors lowers the infidelity and all non-idealities together even produce the lowest infidelity. This can be explained with the fact that the transmission characteristics were included in the pulse generation, which produces the low infidelity $1 - F_{ac,setup}$. Through adding

[25] As seen in Sec. 5.4 the infidelity of the given pulse is highly sensitive towards the accuracy of amplitude durations. The high clock frequency makes a high time resolution available.

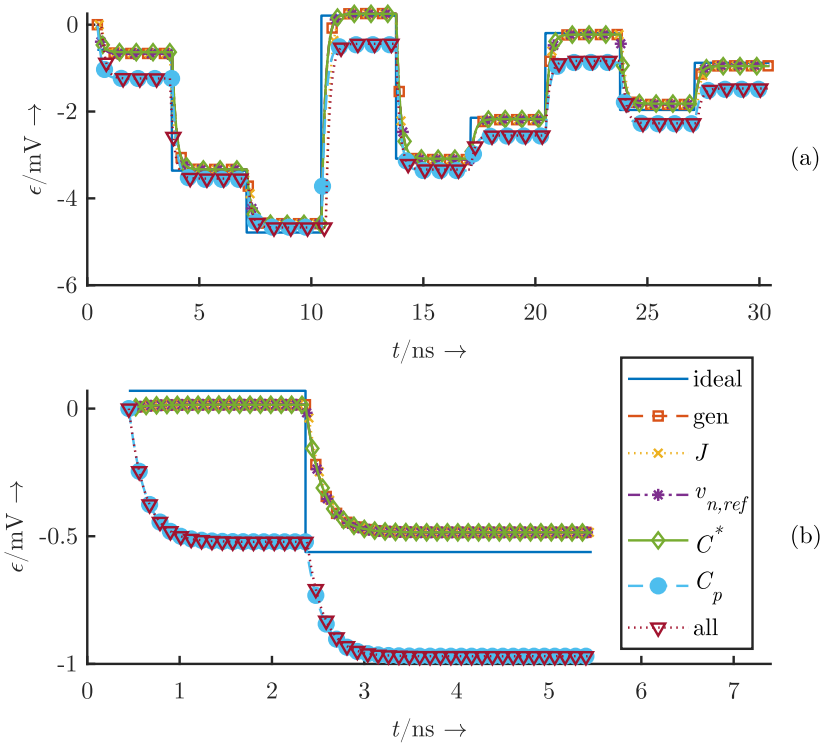


Figure 6.5: Signals in the ideal form 'none' and simulated through the RF generation part 'gen' as well as with additional impairments: (a) 'ac pulse', (b) '2 value pulse'

non-idealities in this model, errors in the transition characteristics are compensated and thus the infidelity decreases.

For the 2v pulse a significant infidelity change can again only be seen for the parasitic capacitor addition and the inclusion of all noise sources (Tab. 6.3). With the high necessary time resolution for this pulse, the infidelity change through the jitter is expected to be larger than it is the case in Tab. 6.3. The reason for that is that only the clock uncertainty of a single edge plays a role in the simulation for this pulse. As the jitter phenomenon is statistical, the time error can also be quite small, which is the case here.

In contrast to the ac pulse the observed infidelity change with the non-idealities is here always negative and thus towards higher infidelities. As no signal transition affects such as lowpass filtering have been included in the optimization process, this is to be expected. The difference of the ideal signal ('none', Fig. 6.5) and the different outputs of the RF generation unit can be clearly seen. Also, in the Bloch sphere representation of the varying signals, the difference of the resulting infidelity can easily be detected (Fig. 6.6).

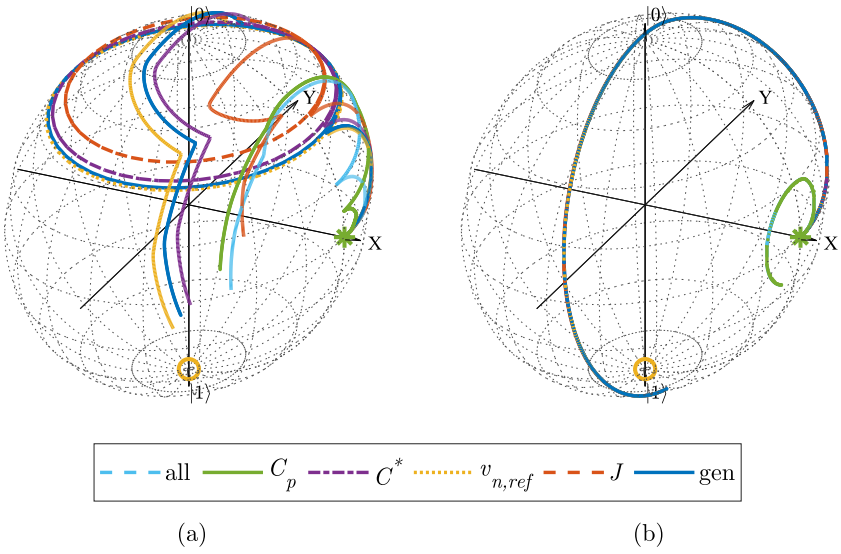


Figure 6.6: Bloch spheres after simulation of the RF generation generation and different added impairments: (a) 'ac pulse', (b) '2 value pulse'. Starting point is denoted by '∗' and the ideal end point by '○'.

Larger noise for the clock or the reference voltage produce a more significant infidelity deviation than the values in Tab. 6.1. The same is true for the process variation effect.

However, the values to produce this significant deviation are larger than expected in a typical circuit.

## 6.4 Conclusion

The results of the combined simulation show that the in Chap. 5 synthesized pulse still works in principle with the electronics. The infidelity value of the gate rotation with the electronics is significantly higher, because the lowpass filtering inherent in the DAC already introduces non-neglectable distortions in the signal transfer characteristic. Additional results with more non-idealities show that the parasitic capacitance of the DAC $C_p$ has the biggest influence on the infidelity. This is a valuable insight for circuit design. It means that mitigation techniques for parasitic capacitances are advisable.

The studies in this chapter are simplified because non-quantifiable errors occur due to the discrepancy of the electrical system the pulses were optimized for and the system model here. The pulse optimized in Chap. 5 does not take signal transfer characteristics into account at all. This leads to a significant lowering of the fidelity, but still gives reasonable results. In case of the pulse from the Bluhm group signal transfer characteristics have been considered. However, these are characteristics from the experimental setup and not the electronics presented in this work. This is also leading to low fidelity results. Nevertheless, some signal transfer features of both systems are similar, which leads to a higher fidelity with some added non-idealities. That means the added non-ideal effects compensate some errors introduced with the electrical model.

All in all, the simulations with the theoretical example pulses give first insightful results. In addition, these results showcase the usefulness of such combined simulations. In future work with this simulation model, the pulses with the system they are optimized for and the system model presented in this work, should be brought into a greater accord. This way the accuracy of the simulations would increase, and the results of different pulses should align with the ones found for the Chap. 5 pulse.

# Chapter 7

# Summary, Conclusion and Outlook

## 7.1 Summary

The goal of this thesis was to investigate the scalability of control electronics for GaAs spin qubits. To analyze the scalability in a well-structured way, the complete system around the control electronics was included. A general introduction to the problem at hand was given and a general overview of the quantum computer topic.

One major challenge for this topic is the fact that qubits are typically operated inside a dilution refrigerator with limited connection capabilities. Current experiments place all control electronics on the room temperature side, but for scalability the electronic circuits have to be moved inside the fridge and as close to the qubits as possible. This introduces a new challenge as no device models are valid at the cryogenic temperatures of $< 1\,\mathrm{K}$. Next to limited space and connectivity the fridge also poses the challenge of a limited cooling power, which restricts the affordable heat dissipation of the electronics in the fridge. The number of connections from a qubit to its electronics is in the range of 10. In order not to have an insurmountable wiring problem for a large number of qubits, direct 3D interconnects are advisable. For this to be possible the footprint of the qubit and its control electronics have to match. This limits the mean control electronics area to about $10\,\mu\mathrm{m} \times 10\,\mu\mathrm{m}$ per qubit.

With these scalability boundary conditions, and the performance specifications derived from current qubit experiments, a concept for the control electronics was developed. The system was studied in terms of performance capabilities for noise and voltage stability to ensure proper functionality. On top of that the control electronics' area and power consumption were estimated in a detailed study. For the first results a well-established 65 nm CMOS technology was used. It became apparent that with this technology and the current very conservatively assumed properties of devices at cryogenic temperatures, no large numbers of qubits can be controlled inside the fridge. Thus, available options today and technologies in the near future were employed to discuss the scalability potential. With todays available technology like 22 nm CMOS SOI already more qubits than in typical current experiments with room temperature control could be operated. Very

high numbers of qubits can also be controlled by the concept presented here, however significant advancements in technology research are necessary for that goal.

With a general scalable architecture, the functionality of the designed control concept was implemented. For that, a behavioral model of the control electronics and surrounding units was developed. That system model also includes a representation of the higher quantum computer levels functioning as a testbench. Simulating a complete qubit experiment shows that all specified functionality is working. That means a cycle of sending data to the qubit, tuning the qubit and qubit initialization, operation and readout is possible. Regarding the scalability of the experiment cycle the results highlight that the tuning part is a possible hindrance to the scalability. Other potential scalability issues are the adaption of sequences to the individual qubit, the measurement method and circuit, and error correction. However, a detailed analysis can only be made when more specific solution approaches than today exist for these topics.

The behavioral modeling of the qubit and a characterization of it based on that were performed. This detailed investigation completes the full system model of the electronics and their surroundings. The effect of different types of interfering signals and noise on the quality of performed qubit gates were tested. Types of noise introduced were constant offsets, frequency dependent noise and white noise. The gates were derived as well in a basic form. The characterization efforts show that the qubit is very sensitive to noise and time and amplitude offsets in the control signal. However, the actual sensitivity depends on the current logical operation on the qubit and the corresponding varying voltage pulses. The large sensitivity range of the pulses makes the definition of one conclusive specification of the control electronics difficult. It follows that for a detailed circuit specification the interdisciplinary work with the people optimizing the pulse sequences is essential.

The behavioral models of the qubit and the electronics were combined in order to complete the overall system simulation. Next to the combination of the model parts also non-ideal effects are added to the electronics model. With these, effects of typical imperfections in electrical circuits such as clock jitter, reference noise, parasitics and process variations on the gate fidelity can be studied. Exemplary gate pulses show that the control electronics can control the qubit state. From the non-idealities the parasitic capacitance has the biggest effect on the gate fidelity. More expressive results could be gained if pulse sequences optimized for the model developed in this work could be used. This shows again that tight interdisciplinary cooperation is necessary.

## 7.2 Conclusion

This work has shown that scalable qubit control is in principle feasible and that the derived concept is a good starting point for such a system. However, a lot of research is still to be done for a circuit implementation scalable towards thousands or millions of qubits. The research for scaling up qubit numbers is ongoing, so there is time to tackle the points brought up in this thesis to have a fully scalable system. In this way the work presented here is a basis for future research as it points out many necessary steps to take towards building a quantum computer.

The different investigations into scalability and the complete system show that close cooperation is necessary on many topics in order to realize the vision of a universal quantum computer. One example for cooperation is that the pulses implementing the logical qubit gates have a big impact on the specification of the electrical system providing them. On the other hand, the pulses have to be tailored accurately to the electrical system in order to achieve a high gate quality. A high-quality qubit control system in the implementation is therefore only achievable by a good cooperation with frequent knowledge exchange.

This work is a foundation for combined simulation of qubits and electronics that did not exist in this way up to now. Through the engineering viewpoint of the up to now mostly physics dominated topic, a structured scalability analysis of the whole system was done. As mentioned, this not only brings up many points for further research, but also provides a tool for simulation and facilitates electrical engineers, and especially circuit designers to work on this topic. With the models implemented during the work on this topic circuit specification and verification can be done in one tool. With that a detailed knowledge of the quantum mechanics behind it is not necessary.

## 7.3 Outlook

Opportunities to continue the research started in this thesis are many. For one, a next step would be to cooperate with the qubit experimentalists to obtain a set of pulses which are fitting to the system here. With continued adaption of these pulse sets and the simulation with the electrical model, a good pulse for integrated qubit control can be found. With these pulses in turn noise and jitter specifications for the electrical system could be derived. If also the knowledge from the estimations are considered, the scalability potential of the optimized pulse electronics would be given in detail as well.

Furthermore, more detailed models of the DAC could be implemented with measurement data. This would make it possible to test electronics and qubits together before placing

them together in the fridge. More detailed inaccuracies like mismatch, device nonlinearities, additional noise sources and leakage can also be built into the DACs and other parts of the model for more detailed investigations on their effect on the gate quality.

The electrical system here includes all the necessary functional components. However, next to that circuitry also support circuits such as voltage reference and clock reference generators and stabilizers are still open topics. These could be added to the current model, as well as it is an system easy to extend.

All the models in this work assume GaAs qubits. These qubits are a good candidate for implementing a quantum computer but not the only one. SiGe spin qubit have similarities with GaAs qubits and therefore a similar study of the scalability of SiGe control electronics are a good choice of future research.

The points of research that came up during this thesis which are not a direct continuation are various. This starts with further measurements of CMOS devices at cryogenic temperatures for pdks and includes chip interconnect technology. Closely connected to the qubit are the measurement circuits for the qubit readout sensors, which are not scalable at the moment. Then the tuning algorithms for the qubit could even influence the electronics and the scalability in general. On top of that, even the error correction algorithms have an influence. For all of these the scalability and the influence on the electronics are only being started to be explored.

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# Curriculum Vitae

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# Publications and additional contributions

## Publications

C. G. Almudever et al. “The Engineering Challenges in Quantum Computing”. In: Design, Automation & Test in Europe Conference & Exhibition (DATE). 2017, pp. 836–845.

Author contribution to: Example for ultra-low-power circuit concept

C. Degenhardt et al. “CMOS Based Scalable Cryogenic Control Electronics for Qubits”. In: 2017 IEEE International Conference on Rebooting Computing (ICRC). IEEE, Nov. 2017. doi: 10.1109/icrc.2017.8123682.

Author contribution: Section II: Methodology

C. Degenhardt et al. “Systems Engineering of Cryogenic CMOS Electronics for Scalable Quantum Computers”. In: 2019 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, May 2019. doi: 10.1109/iscas.2019. 8702442.

Author contribution: Section III: Top-down system modeling

Lotte Geck et al. “Control electronics for semiconductor spin qubits”. In: Quantum Science and Technology 5.1 (Dec. 2019), p. 015004. doi: 10.1088/2058- 9565/ab5e07.

Lotte Geck et al. “Influence of Electrical Noise on GaAs Qubit Gate Quality”. In preparation.

## International conference contributions

Lotte Geck et al. "Interfacing Qubits: Cryogenic Control Electronics", Silicon Quantum Electronics Workshop 2017

Lotte Geck et al. "Scalable Cryogenic CMOS Electronics for Spin Qubits", 656. WE-Heraeus-Seminar, 2019

## Further

Workshop organization, "Bridging the Quantum Computer Gap", RWTH Aachen University

# Appendix A

## Estimations block diagrams

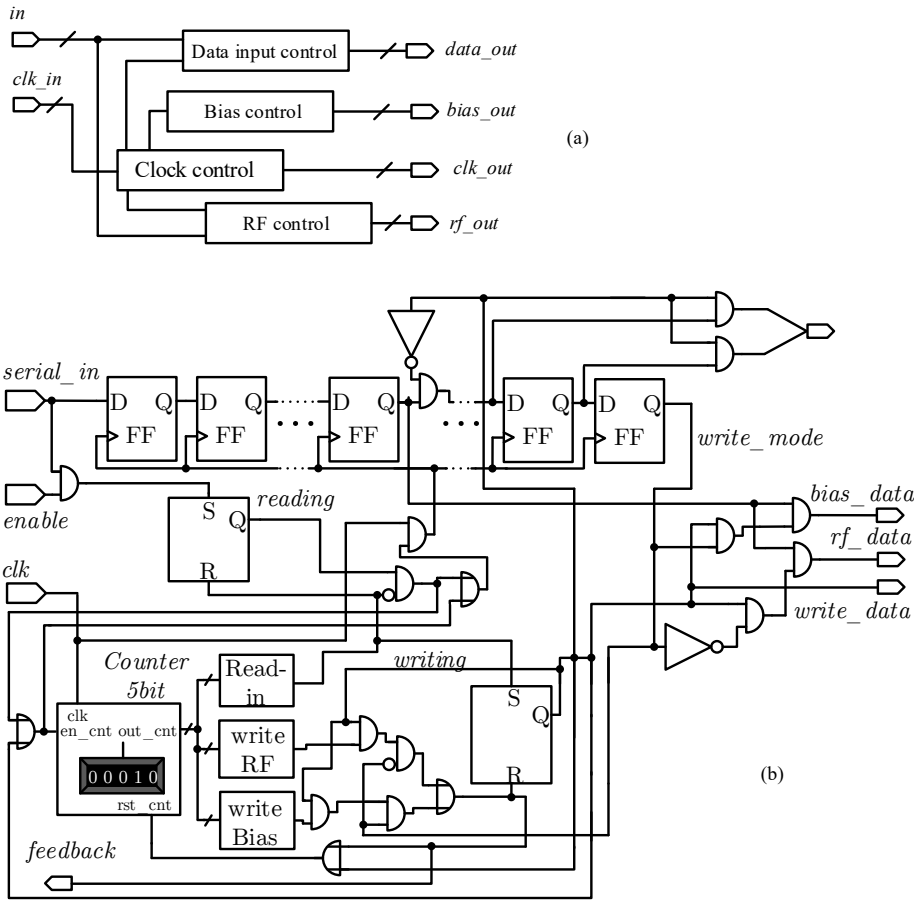


Figure A.1: (a) managing unit components (b) data input control concept

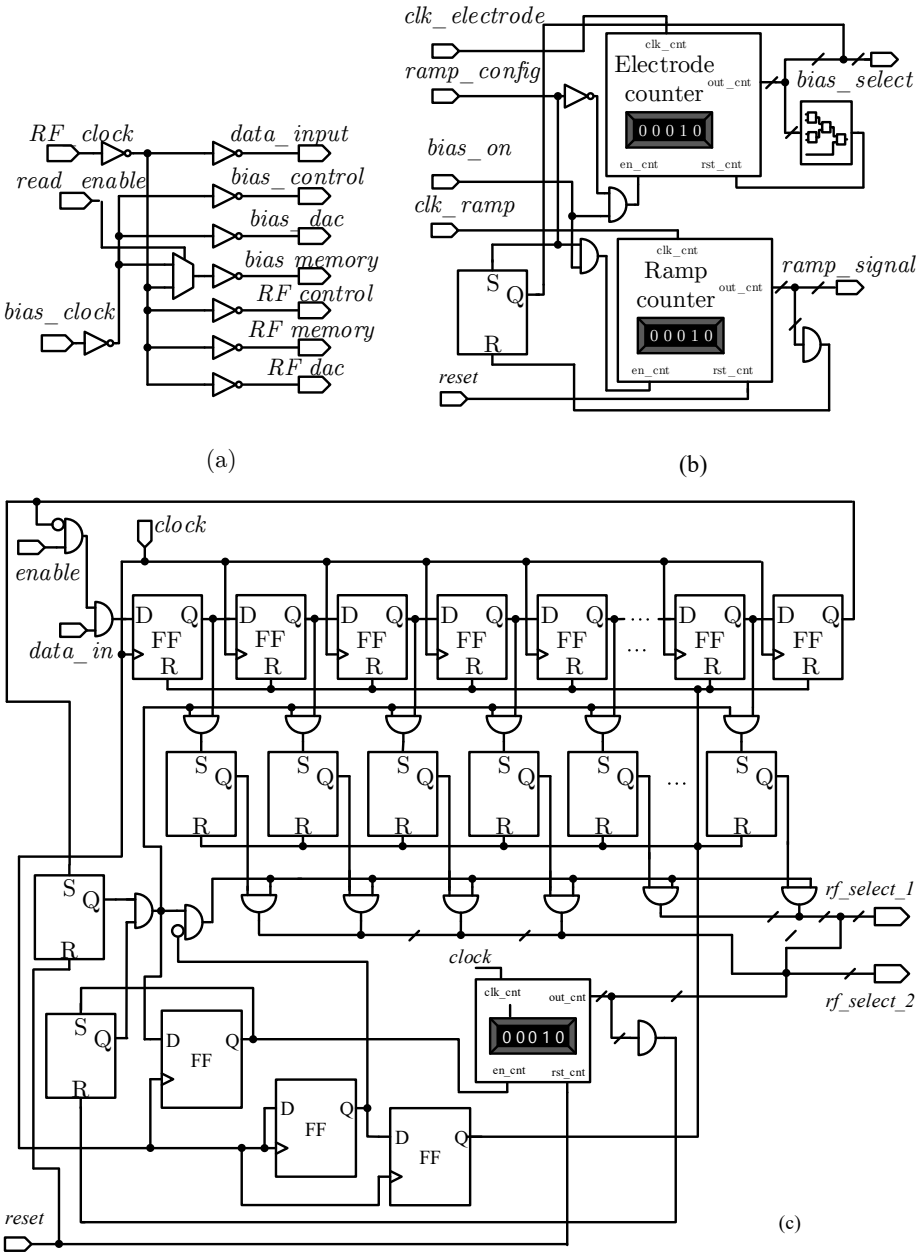


Figure A.2: (a) clock control concept (b) bias control concept (c) RF input control concept

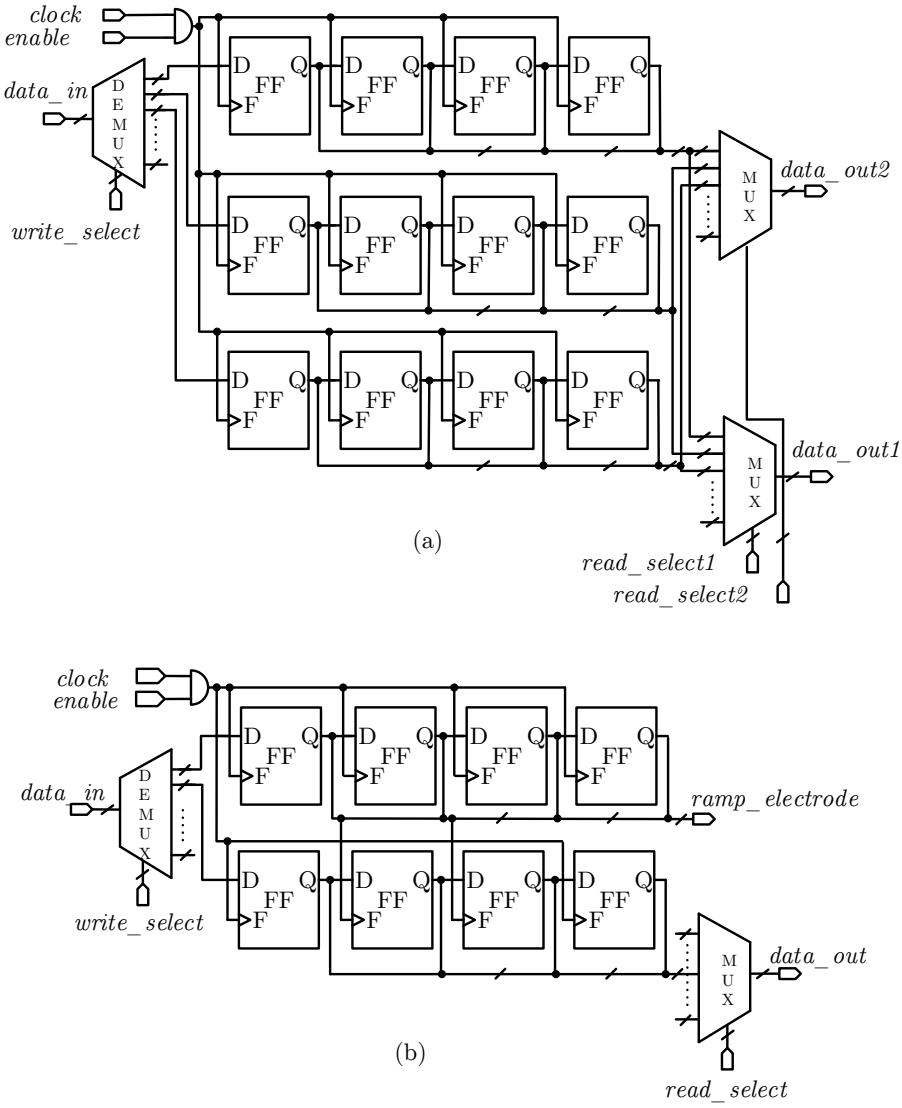


Figure A.3: Memory concept (a) RF memory (b) bias memory

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