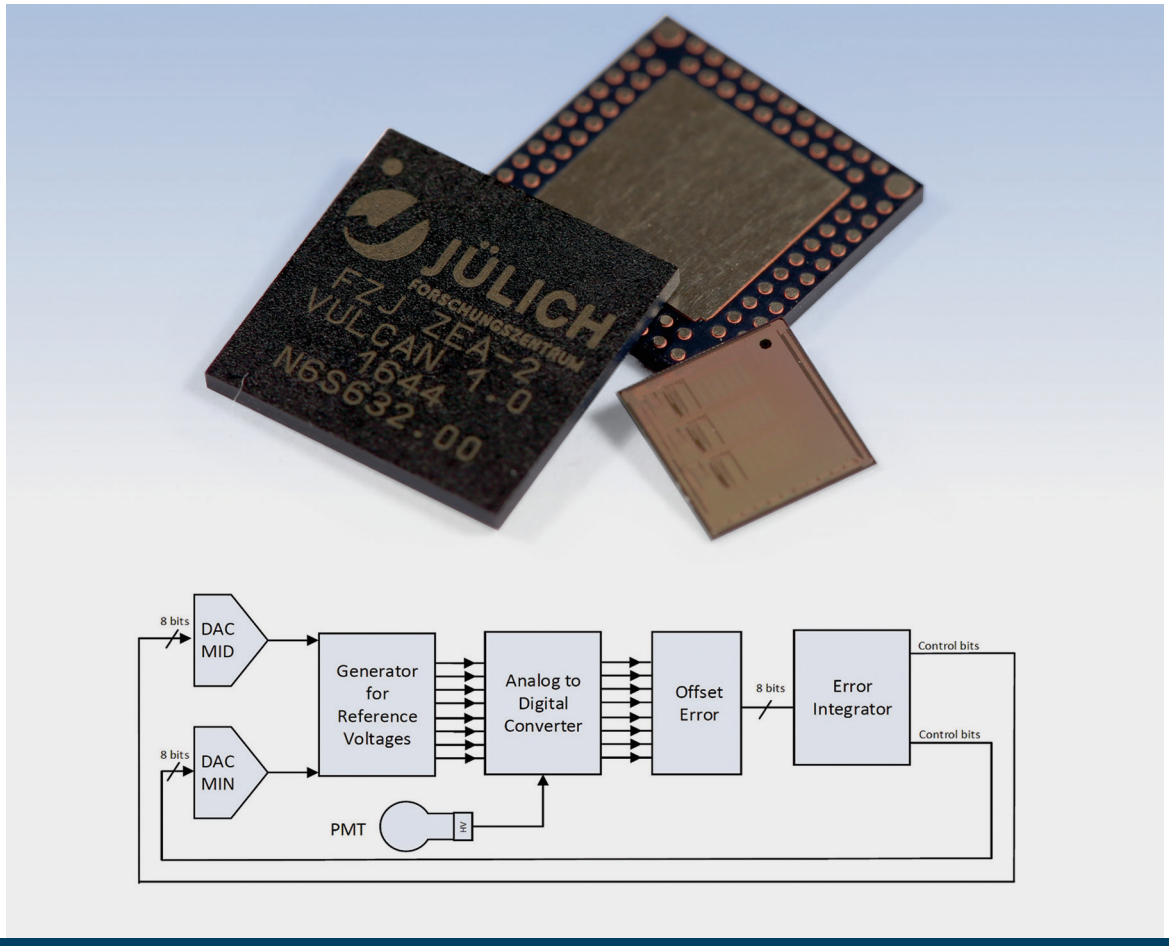

Digital Signal Processing and Mixed Signal Control of Receiver Circuitry for Large-Scale Particle Detectors

Pavithra Muralidharan

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Dedicated to Mom, Dad, Elangho, and Indirani

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Zusammenfassung

Das Jiangmen Underground Neutrino Observatory (JUNO) ist ein Vielzweckexperiment basierend auf einem 20 000 Tonnen Flüssigszintillator dessen Hauptziel die Bestimmung der Neutrino-Massenhierarchy ist. Die Signalerkennung wird durch Photonenvervielfacher (PMT) und integrierten Ausleseschaltkreisen durchgeführt. Die zentrale Komponente für den Digitalisierungsprozess ist ein Empfänger-Chip mit einem stromsparenden Analog-zu-Digital-Wandler System-on-Chip (SoC) mit einem großen Dynamikbereich. Um diesen großen Dynamikbereich effizient verarbeiten zu können sind ein Datenprozessor und ein Regelkreis im Chip integriert. In dieser Dissertation wird das Design, die Entwicklung und die Prototypenmessungen des Datenprozessors sowie des Regelkreises beschrieben, die in dem SoC integriert sind. Der Prozessor analysiert die Daten und führt eine Datenreduktion durch, um die verfügbare Ausgangsbandbreite effizient zu nutzen. Basierend auf den System- und Ereignisinformationen, die durch den Prozessor zusammen mit den Daten übertragen werden, wurde die Signalrekonstruktion erfolgreich durchgeführt. Die Regelschleife reduziert das Rauschniveau und erhöht damit die effektive Anzahl der Bits, die für die Auflösung des Signals zur Verfügung stehen. Durch die Komplexität der PMT-Integration ist ein Austausch von fehlerhaften Komponenten während der Experimentlaufzeit schwierig. Daher ist eine Design-for-Test-Struktur in den Empfängerchip integriert, mit der Intention nur fehlerfreie Exemplare nach der Massenproduktion zu erhalten. Durch das Einführen von Teststrukturen in das Design wurde die generelle Testabdeckung erfolgreich erhöht. Abschließend werden die Erkenntnisse des entwickelten Modells der Empfangskette präsentiert.

Abstract

The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose underground experiment based on a 20,000 ton liquid scintillator with the primary objective of determining the neutrino mass hierarchy. The signal detection is performed by photomultipliers PMT and integrated readout electronics. The central component for the digitization process is a receiver chip with a low power analog to digital conversion unit of large dynamic range. In order to efficiently utilize the conversion unit's dynamic range, a custom data processor and a regulation circuit were included in the chip. In this thesis, the design, development and prototype measurements of the data processing unit and a regulation circuit included in the analog to digital conversion unit are presented. The processor analyzes the data and performs data reduction resulting in efficient utilization of output bandwidth. Based on the system and event information transmitted by the processor along with the data, successful signal reconstruction was carried out. The regulation circuit reduces the noise level thereby increasing the effective number of bits available for the signal. The complexity of the PMT installation poses difficulty to replace faulty electronics during runtime of the experiment. A design for test structure included in the receiver chip with the intention to extract defect free electronics during testing of the mass-produced chips is also described. The introduction of test structures in the design successfully increased the overall test coverage. Finally, the insights from the developed model of the receiver chain are presented.

Introduction 1

1.1 Motivation

In recent years the demand for precise signal extraction in high energy physics experiments is dramatically increasing. Generally, in physics experiments sub-atomic particles are studied by observing their interactions and measuring the by-products like gamma rays which lie in the high-frequency range of the electromagnetic spectrum (above 10^{18}Hz). These high energy and high-frequency signals require different processing techniques in comparison to the commonly used radio waves.

Among the various sub-atomic particles in the standard model, characteristics of neutrinos such as neutral electric charge and low mass lead to low interaction rates further complicating their detection and measurement [1]. Dedicated experiments have been constructed to study the properties of neutrinos. Although several traits of neutrinos have been understood by the previous experiments, features like the mass hierarchy of neutrinos, flavor transformations, mixing angles, etc. are yet to be understood. A new generation of experiments has been developed to understand these open questions by constructing detectors with high accuracy in the spectrum of interest handed over from the previous experiments.

Jiangmen Underground Neutrino Observatory (JUNO) is an upcoming neutrino detector experiment aiming for high precision measurement to determine the neutrino mass hierarchy. For increasing detection efficiency and accuracy in a narrow bandwidth of the energy spectrum, a highly configurable System-on-Chip (SoC) solution (Vulcan) was developed to readout the signals from the PMT used for detection.

In order to improve the signal integrity and reduce signal loss during transmission, a new intelligent PMT concept was developed with Vulcan in which the readout electronics is placed in proximity to the PMT and enclosed in a casing along with other supporting electronics and kept underwater. The Vulcan readout chip is currently customized for this specific concept. The readout electronics has been designed to meet the specific requirements of the neutrino detector.

Among the various sub-modules of the Vulcan readout chip, architecture, implementation, measurements of the main data processing unit and a baseline regulator are presented in this

thesis. A model of the front-end electronics generating overshoot and a model of the developed overshoot compensator is also presented. Besides the developed model, a new regulation technique to preserve the pulse shape of the signal is proposed.

Due to the complexity of the PMT installation, tight reliability requirements were set on the readout electronics. In order to comply with the reliability requirements, a Design for Test (DFT) feature is included in the receiver chip. The methodology, development, implementation, and verification of the design for test structure is included in this thesis.

1.2 Structure of this work

The scope of this thesis is divided into three major parts:

1. Modeling and analysis of overshoot effects and baseline shift on the pulse in the mixed signal domain.
2. Development of a main data processing unit and a baseline regulator in the digital domain.
3. Inclusion of a design for test structure - the scan chain.

Chapter 2 provides a brief description of the JUNO experiment and is followed by a short summary of the chain of events starting from neutrino interactions until the generation of the current signal by the PMT. The requirements for the readout electronics derived from the requirements of the experiment are also summarized.

In chapter 3, the architecture of the Vulcan chip and sub-components are briefly described as a primer to understand the baseline regulator, the main data processing unit, the proposed residual overshoot compensator and other topics described in this thesis.

In chapter 4, the system model developed to analyze the effect of overshoot and the developed overshoot compensation are presented. This is followed by the baseline regulator model, implementation and simulation results.

Chapter 5 provides an overview of the parallel signal chain in the Vulcan readout chip. A detailed description of the sub-modules of the main data processing unit of the Vulcan chip along with its simulation results are presented.

Chapter 6 describes the necessity to introduce a design for test structure in the complex integrated circuit. A design for test structure scan chain was included to increase the test points in the design and thereby improving the testability for designs in sub-micrometer technology. Along with the design for test feature, the sub-modules surrounding the data processor that facilitate in successful chip configuration are discussed.

In chapter 7, the verification and measurement of results of the data processor and the baseline regulator from two Vulcan design step prototypes are presented. A description of the measurement setup is also included.

Chapter 8 concludes this thesis with a brief summary of the model, design and development of the blocks presented in the previous chapters.

Jiangmen Underground Neutrino Observatory

2

The Jiangmen Underground Neutrino Observatory (JUNO) is a neutrino detection experiment under construction in Jiangmen, China, based on a liquid scintillator. The experiment's main goal is to determine the neutrino mass hierarchy by detecting reactor anti-neutrinos from the Yangjiang and Taishan nuclear power plants [2]. The measurement of signal in JUNO is expected to begin from the year 2022.

Among various unapprehended topics, the JUNO experiment aims to investigate the neutrino mass hierarchy, mixing parameters of neutrino oscillations and measurements of neutrino bursts from the next nearby supernova [3]. By precise measurements of reactor anti-neutrino oscillations and by measuring interactions from other neutrino sources (solar neutrinos, atmospheric neutrinos, geo-neutrinos, nucleon decay) the experiment is aiming to resolve the unknowns mentioned above. A brief description of the physics behind the JUNO experiment and the constraints that led to the specification of the Vulcan chip are described in the sections below.

2.1 Physics Background

Neutrinos belong to the lepton group in the standard model of particle physics. Leptons are further classified into electrically charged and neutral leptons. For every charged lepton (electron (e), mu (μ), tau (τ)) there is a corresponding neutral lepton called neutrino (electron neutrino (ν_e), mu neutrino (ν_μ), tau neutrino (ν_τ)). Since neutrinos are electrically neutral and leptons, therefore, they neither undergo electromagnetic nor strong interactions. Sub-atomic particles are observed by their interaction with other particles. The only relevant remaining force is a weak interaction, therefore they rarely interact with other particles or among themselves, hence they are hard to observe [1].

2.1.1 Neutrino Mass Hierarchy

Neutrinos have flavor eigenstates (ν_e, ν_μ, ν_τ) and mass eigenstates (ν_1, ν_2, ν_3). The complete mass hierarchy of the neutrino eigenstates have not been determined. Results from the previous neutrino experiments [4] have concluded the mass of $\nu_2 > \nu_1$, while the mass hierarchy of ν_3

in comparison to ν_1 and ν_2 is still unknown [5]. This results in two possible scenarios with a normal and an inverted mass hierarchy. The normal and inverted hierarchy shown in the Figure 2.1 demonstrates the two possible mass hierarchy of the neutrino mass eigenstates which is targeted to be determined by JUNO. In normal hierarchy, the mass eigen state ν_3 will be higher than ν_2 and ν_1, while in inverted hierarchy the mass eigen state ν_3 will be less than ν_2 and ν_1.

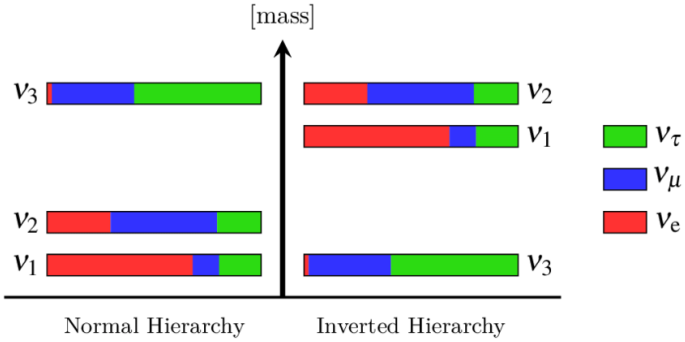


Figure 2.1: Normal and inverse hierarchy of neutrino mass eigenstates [6].

2.1.2 Supernova Event

"Supernovae are violent explosions of stars in our universe producing very high luminosity. Supernovae can be one of the largest explosion that can occur in our universe" [7], [8]. During a supernova, high energy radiations are expected to occur. A supernova radiates almost all of its binding energy in the form of neutrinos, most of which have energies in the range 10-30 MeV [8]. These neutrinos come in all flavors and are emitted over a timescale of several tens of seconds" [9], [10]. In the event of a supernova, the data rate in a neutrino sensitive detector will increase tremendously. In JUNO, the electronics is required to handle such high data rates on a supernova event [3], [11].

2.2 Neutrino Observatory

The central detector of JUNO is a liquid scintillator with a mass of roughly 20,000 tons and is situated with 700 meters rock overburden as shown in Figure 2.2. It is surrounded by 18,000 20-inch photomultipliers (PMTs) that are designed to detect the produced light by the scintillator with high timing and energy resolutions while being submerged in water [3].

2.2.1 Detection Principle

Anti-electron neutrinos ($\bar{\nu}_e$) generated from nuclear reactors are the primary source of neutrinos in JUNO, similar to many other neutrino experiments [4]. In JUNO, anti-neutrinos are detected by inverse beta decay reactions as shown in Equation 2.1.

$$\bar{\nu}_e + p \rightarrow e^+ + n \tag{2.1}$$

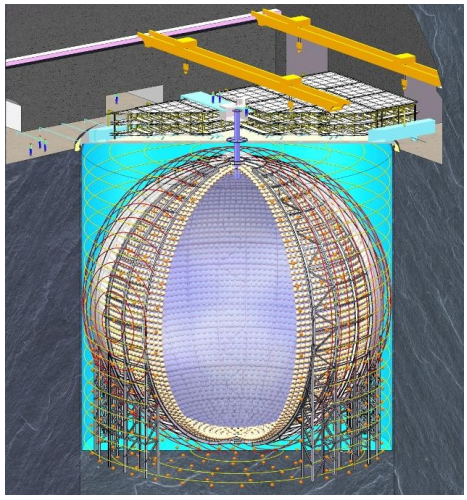


Figure 2.2: A sketch of the JUNO detector, showing the acrylic sphere of 35.4 m diameter holding scintillation liquid of 20 kt. The central detector is surrounded by 18,000 20″ PMTs and ∼34,000 3″ PMTs [12].

The reactor anti-neutrino interacts with a proton (p), creating a positron (e^+) and a neutron (n). The generated positron annihilates with an electron and produces two gamma particles (γ) that can be detected [13] as shown in Equation 2.2.

$$e + e^+ \rightarrow \gamma + \gamma \tag{2.2}$$

The generated gamma rays interact with the scintillator emitting light (photons). Liquid scintillators are organic solutions, which emit light on interaction with ionizing particles [14]. For large volume detectors, liquid scintillators are used together with PMTs to "translate the movement of an ionizing particle in the scintillator into an interpretable electronic pulse [14]". A linear alkyl benzene (LAB) based liquid scintillator is used in JUNO [3].

Both $\bar{\nu}_e$ and ν_e could alternatively interact with scintillators as shown in Equation 2.3 and Equation 2.4 to generate free positrons or electrons together with the radioactive isotopes ^{12}N and ^{12}B.

$$\nu_e + {}^{12}\mathrm{C} \rightarrow e^- + {}^{12}\mathrm{N} \tag{2.3}$$

$$\bar{\nu}_e + {}^{12}\mathrm{C} \rightarrow e^+ + {}^{12}\mathrm{B} \tag{2.4}$$

2.2.2 Energy Resolution and Key Features

The determination of the mass hierarchy is difficult owing to the high energy resolution requirement. Based on calculations [3] it was determined that an energy resolution of $\leq 3\,\%$ at 1 MeV will be necessary to determine the mass hierarchy. In terms of photoelectrons, an

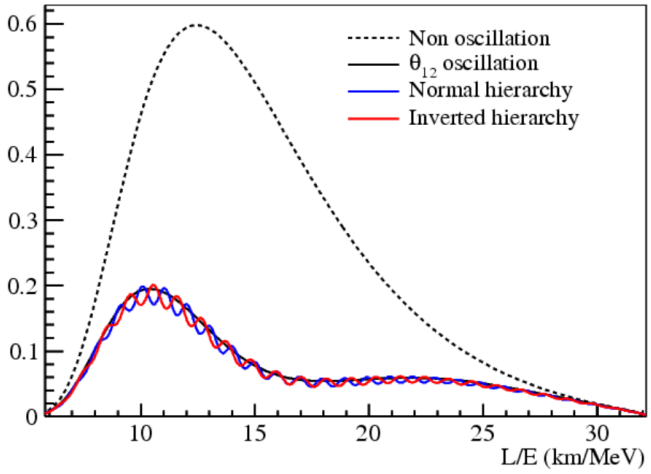


Figure 2.3: The probability distribution of events for normal and inverse neutrino mass hierarchy. The y-axis indicates the probability of neutrino events. On the x-axis, L is the distance between the reactor and the point where the neutrinos are observed and E is the energy of the neutrino generated by the reactors [15].

energy resolution of 3 % at 1 MeV means for an event of 1 MeV (energy) a minimum sum of 1100 photons must be detected in the detector. Figure 2.3 shows the probability distribution of neutrino events for normal (blue) and inverse (red) hierarchy, calculated based on the standard model of elementary particles.

The detector of the JUNO experiment has a relatively large diameter (35.4 m). While the large diameter of the detector has the advantage of increasing the probability of neutrino interactions, it poses the problem of invisibility of the events occurring at the core of the detector. For counteracting this problem, PPO (2,5- diphenyloxazole) is added into the scintillator to increase the scintillation light yield and bis-MSB (1,4-bis[2-(2-methylphenyl)ethenyl]-benzene) with wavelength shifting property is added to the liquid scintillators (LAB). Among various measures for a higher energy resolution, PMTs with an improved targeted quantum efficiency ($\approx 30\,\%$) will be used in JUNO [3].

2.2.3 Photomultiplier Tubes

Photomultiplier tubes are highly sensitive detectors, which produce a charge (current) pulse when stimulated by a photon. When a photon hits the photo-emissive surface (photocathode) of the PMT, an electron can be emitted due to photo-absorption. The conversion rate of photons to electrons is determined by the quantum efficiency of the PMT. Typically, 1-3 photons out of 10 are converted to electrons [16].

The ejected electron from the cathode is directed towards dynodes, which are maintained at higher voltage potential than the cathode. Successive dynodes are biased at incremental voltage

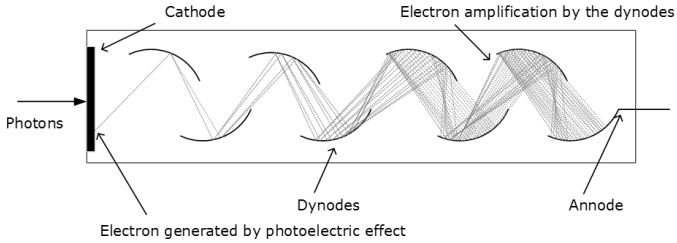


Figure 2.4: An illustration of components inside a generic PMT. When a photon hits the photocathode, an electron is emitted by photoelectric effect. The emitted electron is multiplied at each stage of dynode by the process of secondary emission [16].

potential to focus the generated electrons towards the anode and to amplify the number of electrons. When an electron hits the dynode, it produces secondary electrons, which are focused towards the next higher potential dynode as shown in Figure 2.4. The electron multiplication factor depends on the number of dynode plates and the potential at which the dynode plates are biased. Usually, the potential difference between the dynode plates ranges between 100 V-150 V [17].

A PMT with 10 dynodes and the first dynode biased at 300 V as well as a potential difference of 100 V between successive dynodes results in the last dynode to be biased at 1300 V. This biasing requirement of the PMT requires a dedicated high voltage module. Since the electron multiplication is proportional to the dynode voltage, it is necessary to have stable high-voltage during measurement [18].

The signal produced at the anode of the PMT by a single photoelectron generated at the cathode is called single photoelectron response and is measured as 1 p.e.. The amplitude of the signal produced by one photoelectron at the anode highly depends on the gain and biasing of the individual PMT.

2.2.4 Intelligent Photomultiplier Tubes for JUNO

Among the various PMT installation schemes proposed for JUNO, Figure 2.5 portrays the underwater electronics scheme where the front-end electronics and the high voltage module are potted along with the PMT and kept underwater. With this particular arrangement of front-end electronics, the electrical pulses are digitized before being transmitted via a 100 m cable to the local computer farm. The digitized signals are robust against noise in comparison to analog signals. By placing the readout electronics next to the PMT, signal integrity is maximized as it is inversely proportional to the cable length used for signal transmission [3].

In this scheme of underwater electronics, the electronics are arranged in three stacked Printed Circuit Boards (PCBs) inside a water tight housing at the end of each PMT. The top PCB, which is in proximity to the PMT, contains the high voltage unit providing the voltages for the dynodes of the PMT. It is followed by the General Control Unit (GCU), which contains the Vulcan chip, a Double Data Rate (DDR) memory of 2 GB and an FPGA. The GCU performs data processing and

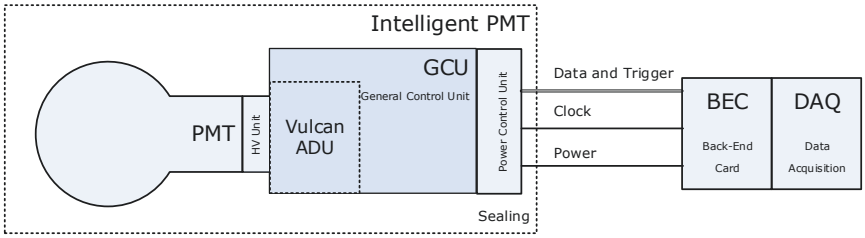


Figure 2.5: Overview of the intelligent PMT for the underwater scheme for JUNO. The high voltage unit (HV), analog to digital conversion unit (ADU), general control unit (GCU) and a power control unit are potted along with the PMT and kept under water. Data is transmitted to the data acquisition unit outside the water through a 100 m cable via the back-end card.

provides control signals for the Vulcan chip and the high voltage unit. The final PCB contains the power supply for the high voltage and all components of the GCU.

In this underwater system, a level discriminator is used to trigger the readout of a single PMT. When the integrated signal of the PMT crosses the configured threshold, a local trigger is generated indicating the occurrence of an event of interest. For an intelligent PMT (iPMT), the trigger threshold can be set just above noise level (for example 0.3 photoelectron (p.e.)). On generation, this local trigger is sent to the data acquisition unit above water. When a sufficient number of PMTs have generated trigger signals and when the event is qualified as a non-background event, the data acquisition unit generates a global trigger to extract signal data from all iPMTs.

The main tasks of the Vulcan readout chip are the conversion of the current signal to a voltage, digitization of analog voltage and transmission of the digital data. The data acquisition unit analyzes the triggers from the PMTs for a defined time frame (around 300 ns) or until a defined number of photoelectrons are generated by all PMTs combined before choosing to send commands to either overwrite the data or transmit the data. During this time period, the GCU buffers the digitized data in the local DDR3 RAM. The memory in the GCU also aids in buffering the data during a supernova event, which produces events at higher rates than normal.

The duration of data readout after a global trigger depends on the length of a pulse generated from a single photoelectron generated at the cathode of the PMT. In JUNO, the readout window is estimated to be around 32 ns. In case of background events, many photons can be detected by the PMT. In such cases, the signal might not return below the threshold and the logic will read for another 32 ns. The readout logic will continue to perform read operations until the signal falls below the threshold [3].

The back-end card splits the signal from the iPMT to different sub-modules of the data acquisition unit. One of the major requirement of the back-end cable is to ensure high speed

data transfer through the 100 m cable. The power for the PMT and electronics is also provided through the Ethernet cable using Power-over-Ethernet (PoE).

2.3 Requirements for the Electronics Readout

The requirements of the Vulcan chip are directly derived from the requirements of the JUNO experiment itself. Some of the requirements and the corresponding design decision for the blocks of interest are listed below.

- **Transit time spread** is the variation in time due to the different trajectories taken by the electrons inside a PMT. This time spread affects the time of flight and also broadens the pulse [3], [16]. Inaccuracies due to the finite time width of photon emission and transient time spread sets the limit on the sampling frequency. Based on the performed simulations, a time resolution of 1 ns is required for the digitization of the signal to avoid loss of information [3].
- The bandwidth of the amplification circuit must match the bandwidth of the PMT to minimize the loss due to shaping. The TIA in Vulcan the bandwidth is targeted to 500 MHz to avoid this loss.
- The signal generated by the PMTs is quantified by the number of photoelectrons generated at the photo-cathode and is measured in p.e.. For the signal range of 1-100 p.e., the charge resolution is expected to change linearly from 0.1 p.e. to 1 p.e.. For a 100 p.e. signal, the resolution must be sufficient to distinguish single photoelectron. The ADC dynamic range should range from 1 p.e. to 4000 p.e. [3].
- The cooling system of the JUNO experiment sets the power budget for the complete electronics at ≈20 W per iPMT.
- Dead time is defined as the duration during which the electronics is unable to measure a signal between events. For JUNO, the readout electronics has the requirement of zero dead time. This requirement sets the necessity for a local buffer unit to buffer the data.
- The submerged structure of the detector rules out the possibility to replace faulty electronics during the course of operation. Since the experiment can only tolerate a Failure in Time (FIT) of 95 for all the electronics [19] in the iPMTs, it is necessary to install modules that are extensively tested and have a higher reliability quotient. A FIT value is thereby defined as the failure of 1 device per billion hours of operation [20].

The following chapters narrate the translation of the system requirements into specifications of the sub-modules.

Readout Solution for JUNO 3

Based on the requirements for JUNO, the architecture of the Vulcan readout chip was designed. Figure 3.1 shows the major functional blocks of the Vulcan chip. The analog unit of the chip consists of the transimpedance amplifier (TIA), Analog to Digital Converter (ADC), Low Voltage Differential Signaling (LVDS) drivers, an internal clock generator and their biasing components. In this chapter, the overview of the Vulcan chip along with a brief description of the components and setup required for understanding the data processor and ADC regulator explained in Chapter 4 and 5 are presented.

3.1 Input Stage

The Vulcan chip contains three parallel signal tracks. Each track contains a transimpedance amplifier, a gain stage, an 8-bit analog to digital converter, buffers, a thermometer to gray encoder and biasing electronics. The Figure 3.2 shows the three parallel signal tracks of the Vulcan chip, with their respective ADCs: ADC for the high gain track (ADC HG), ADC for the medium gain track (ADC MG), ADC for the low gain track (ADC LG). The predominant difference among the signal tracks is the amplification factor of the signal by the transimpedance amplifier.

3.1.1 Transimpedance Amplifier

The first signal conditioning block in the readout chip is the TIA. The TIA of the Vulcan chip has been specifically designed to have a very low input impedance (5 Ω) to load the source significantly. The low input impedance of the TIA assures high sensitivity to the current generated by the PMT. The TIA performs current (I) to voltage conversion (V) in the first stage and amplification suitable for three signals chains (refer Section 3.1) of the ADC in the second stage.

Overshoot Compensator (OSC): A feed-forward-based overshoot compensation block is placed in parallel to the transimpedance amplifier to compensate for the overshoot produced by the coupling capacitor placed between the PMT and the transimpedance amplifier for high voltage protection (refer Section 4.7).

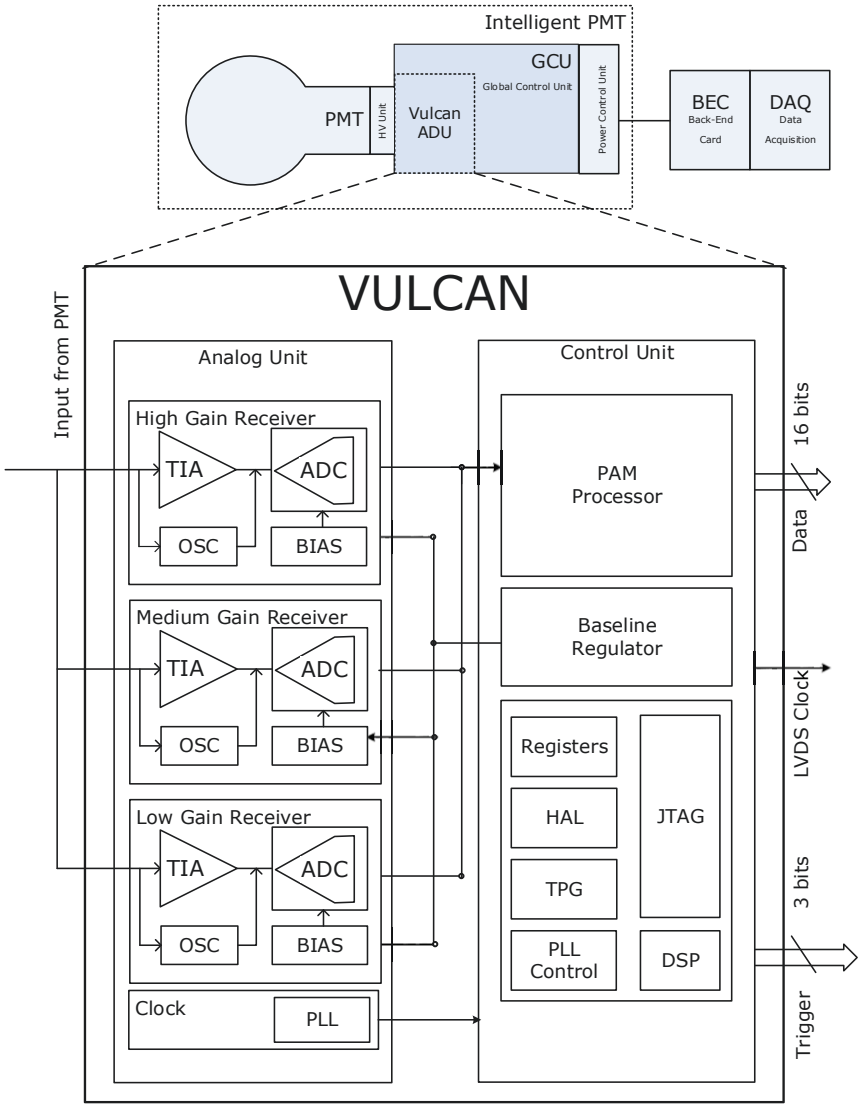


Figure 3.1: Overview of the Vulcan chip architecture and the position of the Vulcan chip in the front-end electronics signal chain.

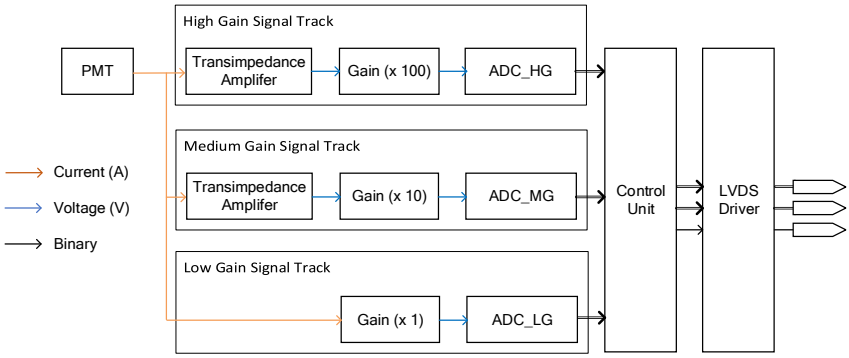


Figure 3.2: Overview of the three signal tracks in Vulcan chip and the common control unit for the tracks.

3.1.2 Phase-Locked Loop

The clock signals required for the sub-modules of the Vulcan chip are generated by an internal Phase-Locked Loop (PLL). The PLL receives a clock of 31.25 MHz from the GCU and generates a 4 GHz clock which is further divided to 500 MHz clock for the ADC and a 250 MHz clock for the digital control unit.

3.1.3 Analog to Digital Converter

The quality of the signal reconstruction is greatly affected by the resolution of the ADC used for digitization. In Vulcan, a novel ADC architecture combining parallelization, cascading and level shifting of the input signal was designed (refer A.1). Figure 3.3 shows the different dynamic range of the three parallel, 8-bits ADCs in Vulcan.

During the calibration of the PMT prototypes, "an electronic noise level in the order of 10 % of the amplitude of a single photoelectron" was measured [3]. To differentiate the noise from the signal, a resolution of 0.1 p.e. is required for an appropriate measurement of a single photoelectron response. The maximum number of photoelectrons expected are in the range of 1000 p.e.. If a constant step size of 0.1 p.e. resolution is assumed for the whole dynamic range, 10,000 ADC steps would be required for 1000 photoelectrons, translating to a minimum of 13-bit resolution. With current commercial technologies, it is not feasible to build a 13-bit high-speed flash ADC.

Using a single ADC to capture signals ranging from 1 p.e. to 1000 p.e. would result in capturing signals of low amplitude with very low precision. If the same ADC is tuned to capture small amplitude signals with higher precision the large amplitudes signal are saturated. A common solution used in high energy physics experiments to deal with such large dynamic range in conjunction with good precision of signal sampling for low amplitudes is the use of two ADCs

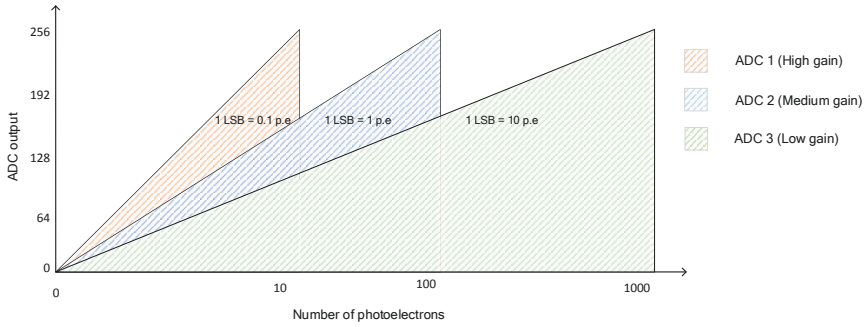


Figure 3.3: Different dynamic range of the ADCs.

with different dynamic ranges. One ADC focuses on the small amplitudes and the second focuses on signals with large amplitudes. The Vulcan chip designed for the iPMT uses three ADCs with different dynamic ranges.

Therefore, a solution of using three parallel 8 bit-ADC opted for digitizing the signals. A dedicated ADC (ADC 3) was used to cover the input range of seldom occurring large amplitude signals and the other two ADCs (ADC 1 and ADC 2) are used to capture everyday events with high precision. The idea is demonstrated by graphs in the Figure 5.4. ADC 1 has the smallest step size thereby it digitizes the input signal with a precision corresponding to 0.1 p.e.. The ADC 2 has relatively larger step size and is used to digitized signals generated by 100 photoelectrons with a precision of 1 p.e.. The ADC 3 digitizes signals generated up to 1000 photoelectrons with a precision of 10 p.e.. Theoretically, this parallel ADC architecture promises to capture the input signals with the specification required for JUNO. However, supporting electronics is required to reap the benefits of this architecture. For instance, appropriate gain stages after the transimpedance amplifier and data conditioning stages has to be built around the ADCs.

Table 3.1: Range and precision of the ADCs in the Vulcan chip.

ADC	Range	Precision
ADC_{HG}	1-10 p.e.	0.1 p.e.
ADC_{MG}	1-100 p.e.	1 p.e.
ADC_{LG}	1-1000 p.e.	10 p.e.

The transimpedance amplifiers measure the charge deposited at the cathode of the PMT by a photoelectron. Charge deposited by 1 photoelectron at the cathode is referred as 1 p.e.. The high gain track is tuned to capture the charge deposited by a maximum of 10 p.e.. The medium gain track is tuned to capture the charge deposited by a maximum of 100 p.e.. The low gain track is tuned to capture the charge deposited by a maximum of 1000 p.e.. With this architecture, the frequently occurring low amplitude signals are captured with good precision, at the same time seldom occurring large amplitude signals are also adequately captured.

3.2 Control Unit

The digital control unit processes the data generated by the ADC and provides control for the various sub-modules present in the system. A run-through of the functionality of the blocks is described below.

Head of Assigned Liabilities (HAL): A slow external clock and a fast internally generated clock are used in the Vulcan chip. During the power-up of the electronics, it is necessary to provide a stable clock signal to the sub-modules until the internally generated clock is configured and stable. HAL controls the switching of the available clock signals during this phase.

Registers: Configuration registers have been included to increase the programmability of the sub-modules included in the readout circuit. A slave module for the standard Joint Test Action Group (JTAG) communication protocol has been included to provide the pathway between the configuration registers for fine tuning the parameters of the sub-modules and configuration setup. In addition to the configuration registers, certain registers are allocated for reading the status of certain internal signals for debugging purpose.

PAM Processor: The PAM is the main data processing unit in Vulcan. By default, PAM processes the data from the ADC and transmits to the following stages through LVDS lines. Chapter 4 encloses the implementation details of PAM and measurement results.

Digital Signal Processing: This block provides alternative signal processing methods such as integration, averaging and decimation of the signal. By default, the Digital Signal Processing (DSP) block generates a trigger signal when the integrated signals cross the programmed signal threshold.

Test Pattern Generator: The test pattern generator module is used only during the debug phase to program waveforms, generate waveforms or use a generated waveform to test the functionality of the data processing blocks.

Baseline Regulator: The baseline regulator is a control loop used to regulate the reference voltage of the ADC in an attempt to adjust the baseline of the signal to a known reference.

LVDS: The voltage level of the signals transmitted out of the chip has a direct impact on the power consumption of the chip. Low voltage differential signaling method uses a lower voltage difference between the signal line and reference (350 mV as opposed to 1 V) and also has a relatively better noise rejection (due to common mode rejection). In Vulcan, 16 pairs of data lines, 3 pairs of trigger lines and a pair for the clock signal is driven by an internal LVDS driver. The LVDS driver transmits data at 500 MHz.

3.3 Configuration Setup

The Vulcan chip was developed as a multi-functional chip with the ability to be utilized in different projects in addition to JUNO. One of the key features which enables the multi-functional operation is the dedicated registers for configuration of the sub-modules that are included in the chip. There are 384 registers in total, out of which 255 registers are used for

configuration of the sub-modules called configuration registers and 128 registers are used for reading the status of the sub-modules called status registers. For instance, 12 (96 bits) registers are used by the data processor (described in Chapter 5) and 7 (56 bits) are used by the ADC regulator (described in Chapter 4).

These configuration registers provide the possibility to customize certain functions of the Vulcan chip specific to the application. This enables, the configuration bits to change modes of the sub-modules which can be modified during operation. The configuration registers are volatile and they have to programmed after power-up of the Vulcan chip.

Each configuration register is 8 bit wide. In some cases, the whole register is allocated for one functionality like a threshold value, while in others, individual bits are assigned for an individual task such as enabling or resetting the block of interest. The use of configuration registers and building sub-modules to be configurable provides flexibility and tunability.

JTAG Interface: Interfaces are predefined methods to communicate between devices (external to the chip). Following the trend of decrease in chip size, the limitation in the number of Input/Output (I/O) pins available to connect devices becomes significant. Standard interface protocols were developed to solve this issue and provide an interface with a minimum number of I/O pins.

In case of the iPMT, the Vulcan chip needs to communicate with the GCU (refer Section 2.2.4). While the majority of the data transfer between the Vulcan and the GCU is carried out using dedicated LVDS output lines, a separate interface is necessary to program the configuration registers of the Vulcan chip.

Among the various standard protocols available, JTAG was chosen for Vulcan [21]. Figure 3.4 shows the basic structure of the JTAG macro. JTAG is a synchronous protocol with four mandatory pins: test data in (TDI), test data out (TDO), test mode select (TMS), test clock (TCK) and one optional pin test reset (TRST). The JTAG protocol is implemented as a state machine (test access port controller) as shown in Figure 3.5. By default, JTAG macros have a bypass register and an instruction register. In Vulcan, the configuration and status registers are connected between the TDI and TDO, similar to the bypass and instruction register as shown in Figure 3.4.

JTAG is a synchronous interface and the clock signal is provided through the port TCK. The control signals provided at the TMS port decides the current state in the state machine and dictates how the data is interpreted.

The following steps are followed to write into and read from the configuration register.

1. As a first step in writing into the configuration registers, the address of the register to be programmed needs to be loaded. For this purpose, TMS signal "01100" is transmitted, resulting in a state change from "Test-Logic-Reset" to "Shift-IR" (refer Figure 3.5). Now by holding TMS signal at 0, the instruction code "100" corresponding to loading the register address for reading and writing into the configuration registers is sent through the TDI. Once the instruction is written into the instruction register, TMS signal "10110" is transmitted and the finite state machine returns to "Run-Test" state.

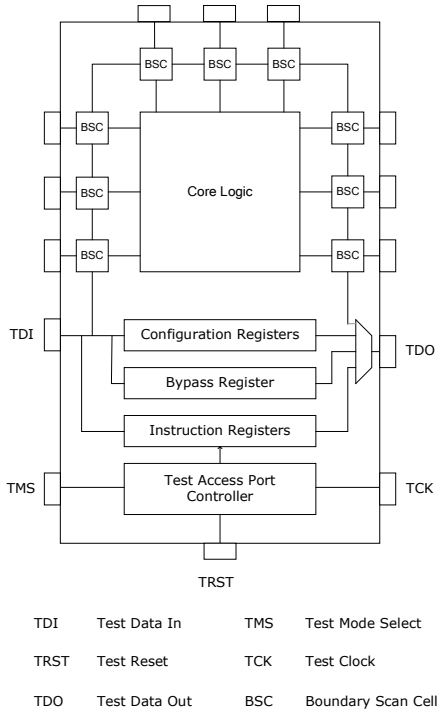


Figure 3.4: Overview of the JTAG macro [21], [22].

2. Next, execution of the instruction to write into the configuration register is performed. On sending the TMS signal "01100" state changes from "Test-Logic-Reset" to "Shift-IR" (refer Figure 3.5). By holding the TMS signal at 0, the instruction code "101" corresponding to writing into the register is sent through the TDI. Once the instruction is written into the instruction register, TMS signal "1011100" is transmitted to change the state from "Shift-IR" to "Shift-DR".

3. After successful execution of the previous steps, the write pointer of the JTAG macro points to the register address loaded in the instruction register. By holding TMS signal at 0, the value to be configured in the register is sent through the TDI. After writing into the configuration register TMS signal "10110" is transmitted to return to "Run-Test" state.

4. Similar to the writing process, address needs to be loaded for reading the register. By following step 1, register address can be loaded. By writing the instruction "110" instead of "101" the controller is instructed to read the register instead of writing and the remainder of step 2 is executed.

5. Now the read pointer of the JTAG macro points to the register address loaded in the instruction register. By holding TMS signal at 0, data in the configuration register can

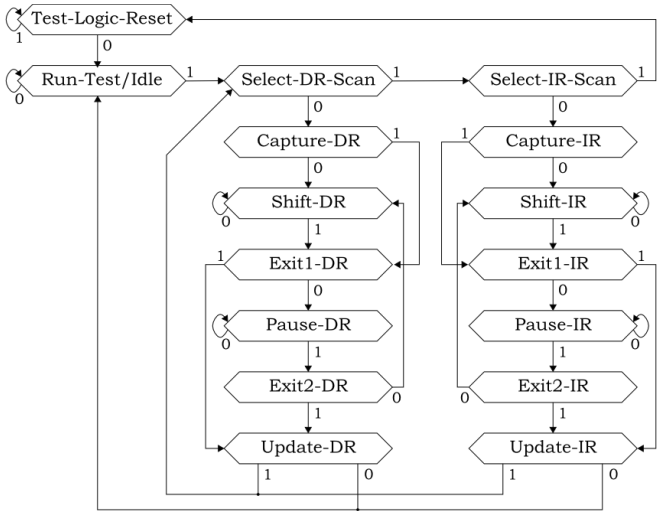


Figure 3.5: State machine of the test access port (TAP) controller [22].

be read out at the output port TDO. After reading the configuration register TMS signal "10110" is transmitted to return to "Run-Test" state.

The 255 configuration registers of Vulcan are configured through the JTAG macro implemented in the chip during the start-up/configuration process of the chip. After the start-up process, all registers are loaded with appropriate initialization values.

System Model 4

Well established and constrained Register Transfer Logic (RTL) specification of digital circuits and automation of the translation from RTL to gate-level makes a proper top-down methodology feasible for the design of digital circuits. The risk of detecting system level errors at the later stage of the design process in the bottom-up approach is reduced by following the top-down methodology as the latter approach focuses on the design and verification of the system at the block level before detailed transistor level design of the individual blocks [23], [24]. In Vulcan, the digital control unit was designed following the top-down methodology.

In this chapter, a short description of the top-down methodology and its intermediate stages are described. Following the description, the model developed during the architectural stage of a regulator and the extended model developed to analyze the combined effect of the feedforward and feedback system are presented.

4.1 Top-Down Methodology

The design phase of integrated circuits goes through different levels of hierarchy. The abstract model of the design process can be seen in Figure 4.1. Circles indicate the hierarchy levels in the design process with the outermost circle indicating the highest level of abstraction and the innermost circle representing the lowest level of abstraction.

The design process can also be sub-divided into three major domains: behavioral, structural and physical. The three domains are represented by the Y plot overlaid over the concentric circles. The intersections of the Y plot on the circle indicate various stages of the design process. The hierarchy of the design process starting from the highest to the lowest level of abstraction are described below.

- **System:** In this level, the requirements of the system are specified. After the agreement, the overall specification is divided and described in terms of functionality required to be achieved by the sub-modules. The decision of the architecture of the sub-modules and the interfacing between the sub-modules are decided.

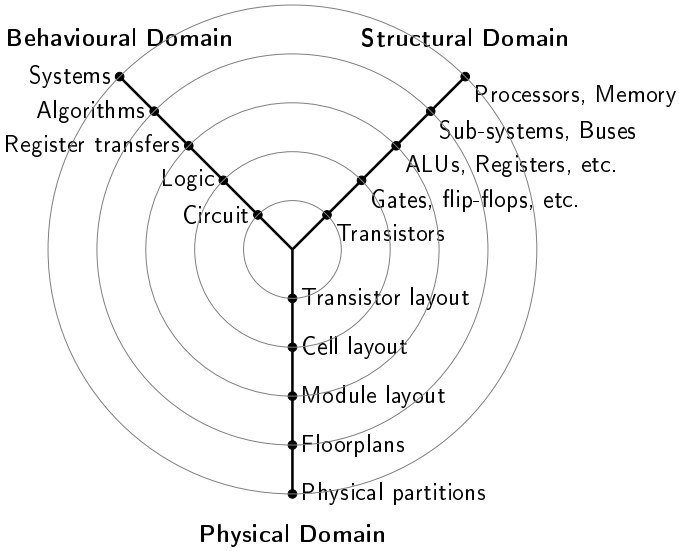


Figure 4.1: Gajski-Kuhn Y-chart [25]

- **Algorithmic:** In this phase, an abstract description of the sub-modules is described to attain the functional specification. This phase emphasizes the implementation of mixed-signal modules and signal processing algorithms. In Vulcan, the model of the baseline regulator, which provides control signals for the analog blocks, was developed to extract required parameters such as scaling factor and word length before proceeding to the RTL description phase.

- **Register transfer:** Hardware Description Languages (HDLs) are specifically developed to describe the behavior of circuits in terms of logical operations to be performed on the data and the transfer of data between the registers. Description written in HDL can be translated to a gate level description. In this phase, the functional description of the sub-modules and the data transfer between the registers and interfaces in HDL are carried out.

- **Logic:** In this phase, the behavioral description of the circuit is translated to gate level. The behavioral description and the data transfer between the sub-modules are first converted to boolean equivalent and later replaced by the logic gates and wires matching the mathematical functionality and connectivity. EDA tools perform the conversion of an RTL description to a gate level netlist.

- **Circuit:** At this phase, the electrical characteristics of the whole design is described. This concludes the final stage of the design hierarchy and the output of the stage is the layout information (GDSII) required to fabricate the silicon [25].

4.2 Overview of the System Model

In Vulcan, a digital control loop provides feedback control to the sub-modules in the analog domain to regulate the baseline of the ADC. The mentioned baseline regulator is referred as "ADC baseline regulator" in this thesis. Since the control loop encompasses both analog and digital sub-modules, it belongs to the mixed-signal domain. Mixed-signal simulation of designs in circuit level is time consuming and a computationally heavy process for complex designs. In Vulcan, a circuit level simulation combining the digital control loop with the ADC with our current computational devices deemed to be impossible due to the complex ADC architecture.

The above mentioned limitation in turn imposed higher emphasis in the development of a system model to reflect the parasitic effects and architecture of the front-end electronics as well as the development of a concept for the digital control loop. For mixed-signal designs, the envisioned architecture of the block is first defined and simulated using high-level simulators MATLAB and Simulink. Parameters and requirements for the blocks are derived from these abstract models before the RTL implementation. It is important to apprehend, that the model developed during the architectural phase cannot be automatically converted into VHDL for RTL verification. Therefore, test benches were developed in VHDL for functional verification.

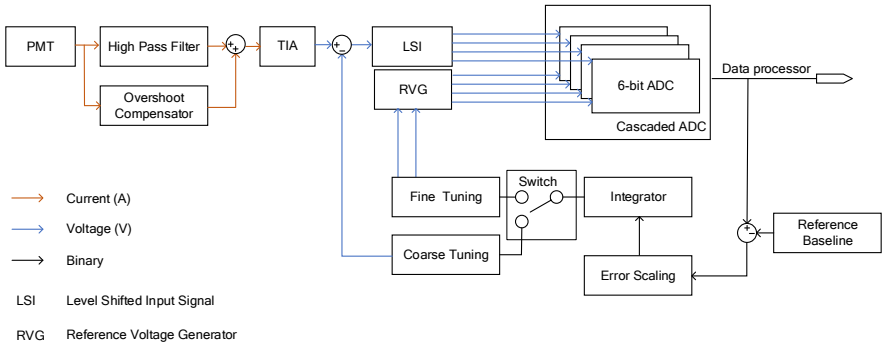


Figure 4.2: Overview of the modeled system in Simulink.

An overview of the complete system model that has been implemented in Simulink is shown in Figure 4.2. The detail description of the sub-modules are described in the rest of the chapter. The system model begins with the PMT block which generates a current signal with an exponential decay Section 4.6. Following the PMT block the high pass filter and the overshoot compensator explained in Section 4.7 and Section 4.3.2.2, are implemented in the Laplace domain. This is followed by the TIA which converts the current signal to voltage.

As described in A.1, the 8 bit ADC is composed of four cascaded 6-bit ADCs. The input signals to the ADCs are level shifted and the reference voltages of the ADCs are generated by the

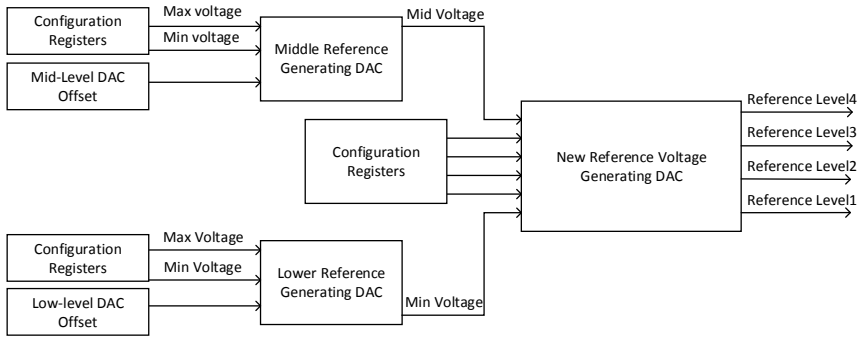


Figure 4.3: Overview of the reference generator for ADC. The new reference voltages for the ADC are generated based on the feedback from the ADC baseline regulator and the configuration registers.

reference voltage generator (refer Figure 4.3). In the feedback loop, the signal from the ADC is analyzed by the ADC regulator and based on the deviation either a coarse tuning by adjusting the gain of the TIA or a fine-tuning to the reference voltage generator is provided.

Figure 4.3 also shows the two stages in the reference voltage generator. The configuration registers sets the reference voltage of two Digital to Analog Converters (DACs): the "middle reference generating DAC" and the "lower reference generating DAC". These two DACs in turn set the middle and lower reference voltage for the second stage. In addition to the configuration registers, the feedback from the ADC regulators adjusts the output of the DACs in the first stage. The step size of the DACs adjusting the reference ladder of the ADC is smaller than the step size of the ADC. Owing to the smaller step size, a fine-tuning of the reference voltage can be achieved. In the following sections, the parasitic effects introduced by the front-end electronics, the details of the sub-modules and the analysis obtained from the system model are presented.

4.3 Non-Idealities in Analog Signal Processing

Electronic circuits are often designed to perform functions on signals within a specific band of frequencies (band-limited) and a predefined range of amplitude. The signals outside the defined bandwidth and the predefined input range are considered as noise and filtered out in the initial stages of the signal chain. By filtering out the noise and designing the circuit for a specific input range, compact and resource efficient electronic circuits can be designed [26]. For certain waveforms, the finite bandwidth of the electronics systems results in undesirable shaping. One such undesirable effect is the overshoot of a signal.

In addition to the modulation imposed by the band-limited architecture of the systems, noise and radio frequency interferences can further impair the signal of interest. The baseline or zero offset is the current level measured when there is no signal input. Typically, the baseline of a system is expected to lie at 0 A. Due to non-idealities such as interference, artifacts due to

mismatch of devices, AC coupling, thermal drift of electronics devices and electronic noise, the baseline deviates from 0 A. Small variations of the baseline are common in electronic circuits but when the deviations are high and create errors in measurement, they are classified as baseline offset or baseline shift. Various real-time and offline baseline restoration methods have been developed for nuclear physics experiments. A real-time baseline restoration method has been chosen for Vulcan for its advantage of configurability.

The overshoot generated by the coupling capacitor placed between the PMT and the Vulcan chip and the intersymbol interference of the signals are parasitic effects and cause signal degeneration. In order to understand these parasitic effects in detail, a system model was developed in the combined platform of MATLAB and Simulink. The cause of the overshoot, its effect on the measurement and possible compensation methods are discussed in the following sections. Alongside, a real-time digital baseline regulation circuit for the Vulcan chip is presented.

4.3.1 Overshoot

A signal has an overshoot when the magnitude of the signal exceeds the maximum desired level for a certain amount of time before settling down to the steady state (refer Figure 4.4). It defined as "the difference between the peak value of the step response and its steady-state value" [27]. The overshoot is expressed in percentage as shown in Equation 4.1. In physics experiments deviation of the signal from its original value is categorized as overshoot.

$$\text{Overshoot (\%)} = \frac{\text{Maximum amplitude - Steady state value}}{\text{Steady state value}} \times 100 \tag{4.1}$$

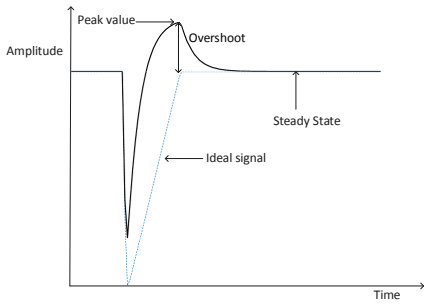


Figure 4.4: Exemplary plot showing the effect of an overshoot.

4.3.2 Impact of Overshoot in JUNO

For high precision experiments like JUNO, retaining the shape of the signal is of high importance. "An overshoot affects the trigger, dead time and charge measurement from the detector" [28]. The overshoot in JUNO is caused by a combined response of the PMT and the passive filters placed after the PMT.

The following sections describe the individual response of a PMT, a passive high-pass filter and their combined response producing the overshoot.

4.3.2.1 Photomultiplier Tube Model

A PMT can be modeled as a current source in parallel to a resistor and a capacitor as shown in Figure 4.5. The instantaneous current *I(t)* generated by the modeled PMT is dependent on the number of photoelectrons and the value of R_s and C_s connected parallel to the current source.

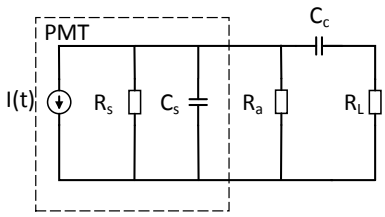


Figure 4.5: The circuit equivalent of a PMT is enclosed inside the box marked with dashed lines. Along with the anode load resistance (R_a), a decoupling capacitor (C_c) and a load resistor or input resistance of trans-impedance amplifier (R_L) is shown.

4.3.2.2 High-Pass Filter

A resistor and a capacitor are added in the signal chain between the PMT and Vulcan as shown in Figure 4.5. The capacitor (C_c) is added to decouple the readout circuit from the supply and to block the Direct Current (DC) from entering the circuit and the added resistor (R_a) provides the path for the DC current to ground. The decoupling capacitor prevents the voltage fluctuations due to the varying current load affecting the circuit. The addition of these protective and filtering elements creates a high-pass filter on the signal chain.

The voltage generated by the circuit shown in the Figure 4.5 is given by

$$V(t) = \frac{GNe}{\tau - \tau_s}\left[\exp^{\frac{-t}{\tau_s}} - \exp^{\frac{-t}{\tau}}\right] \tag{4.2}$$

Where G is the gain of the PMT and τ_s is the time constant due to the high pass filter ($\tau_s = R_a C_c$) and τ is the time constant of the PMT [29].

The value of the resistor (R_a) and capacitor (C_c) has an influence on the pulse shape and thereby on the settling time. An exemplary plot showing the effect of a varying time constant τ on the pulse shape is shown in Chapter A, Figure A.2. The resistance (R_a) and capacitance (C_c) values have to be chosen depending on the expected event rate of the experiment. For instance, a configuration with a smaller time constant τ can be chosen for an experiment with higher event rate because a smaller time constant τ ensures a faster settling time thereby avoiding the piling up of pulses.

Since the modeling focuses on analyzing the overshoot effect produced by the high-pass filter, the schematic in Figure 4.5 is further simplified. To imitate the single photo electron response,

the PMT is modeled as a current source (as shown in Figure 4.8) producing a pulse with an exponential decay.

4.3.3 Transfer Function of Combined Systems

The step response of a high pass filter will produce a simple exponential decay of the signal at the output without overshoot. The transfer function of the high pass filter is given by $\frac{\tau_2 s}{1+\tau_2 s}$, where τ is the time constant and s is a variable in Laplace domain.

The output current from the PMT is modeled as a current source in parallel with a resistor and a capacitor. The transfer function of the modeled PMT is given by $\frac{1}{1+\tau_1 s}$. The combined transfer functions of the PMT model and the high pass filter is given by Equation 4.3

$$\text{Transfer function} = \frac{\tau_2 s}{1 + s(\tau_1 + \tau_2) + s^2(\tau_1 \times \tau_2)}. \tag{4.3}$$

The step response of the resulting transfer function is an output pulse with overshoot [30].

4.4 Parasitic Effects of the RC Time Constant

The occurrence of neutrino interactions in the detector are stochastically independent therefore pulses generated from the PMT are aperiodic. These aperiodic pulses can cause interfering effects, called pile-up, when the pulse rate is high [17]. Effect of the pulse pile can differ based on their occurrence in time. Two exemplary scenarios are described below.

1. The upcoming pulses can interfere with the previous pulse and cause the signal to pile up if the tail of the pulses extends for a longer period of time. As shown in the left illustration in Figure 4.6, the second pulse overlaps on the residue of the first pulse resulting in amplitude error.

2. In Section 4.3.3, the combined transfer function of the PMT and the first order high pass filter was derived. Due to the pole created in the transfer function, the system will produce a pulse with an overshoot which recovers to zero with the RC time constant. If another pulse arrives during the time the pulse is recovering to zero or during the overshoot as shown in Figure 4.6 [Right], it results in a pulse pile-up. The error introduced by pile-up increases for large signal pulses, as the overshoots produced by the signals are proportional to their amplitude [17].

Pulse pile-up can be minimized by reducing the width of the pulse as shown in Figure 4.7. Signal to noise deterioration prevents the reduction of pulse width beyond a certain level and therefore the effects of pulse pile-up at high rates are often unavoidable.

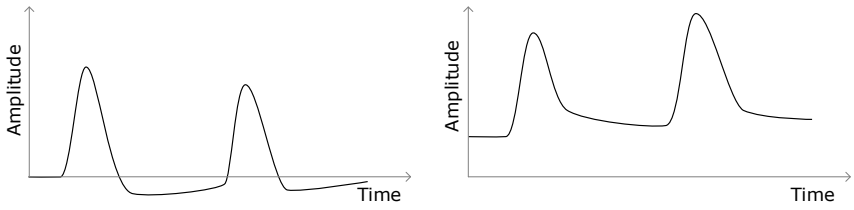


Figure 4.6: [Left] Illustration of pulse pile-up on the overshoot of the signals. [Right] Illustration of pulse pile-up on the long tail of the signal [17].

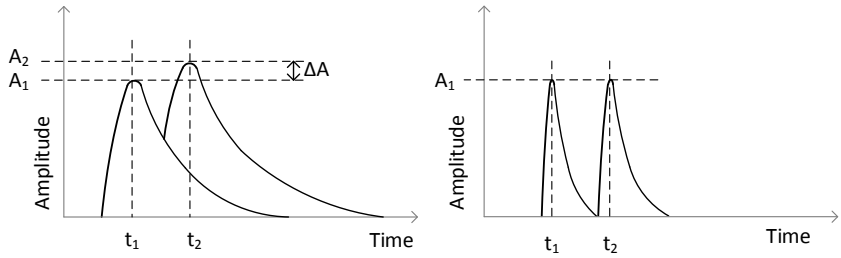


Figure 4.7: [Left] Illustration of an increase in amplitude when two pulses pile-up. [Right] The plot illustrates the effect of reducing the time constant. The first pulse returns to the baseline before the second pulse arrives, therefore, avoiding pile-up [31].

4.5 Mixed Signal Modeling

As shown in Chapter 3, the Vulcan chip contains analog and digital sub-modules. The analog sub-modules developed for Vulcan are complex and requires large computational resources and long runtime for a full design simulation. These limitations provoked the need for a high-level model to design mixed-signal sub-modules interfacing both analog and digital circuits.

A high-level model provides the platform to evaluate the system performance and develop optimal architectures. A Simulink model was developed to analyze the effect of the overshoot on the system and to evaluate the performance of the overshoot compensator. The model was further extended to analyze the baseline shift and an ADC baseline regulator was designed from the parameters derived from the model. The details of this model are described in the following sections.

4.6 Model of the System in MATLAB

A model of the system as shown in Figure 4.5 containing the PMT, the high pass circuit causing the overshoot and the load resistor was developed in MATLAB. With the intent to verify this model, the same circuit was designed in Cadence as shown in Figure 4.8. Using the rules and theorems of electrical circuit analysis, the complexity of the electric circuits can be reduced and a mathematical function relating the input and output, otherwise known as transfer function, can be derived. A circuit analysis can be done either by hand calculations or by computer-aided design (CAD) software. For the circuit shown in Figure 4.8, a circuit analysis is performed and the calculations are described by Equation 4.4 to Equation 4.10

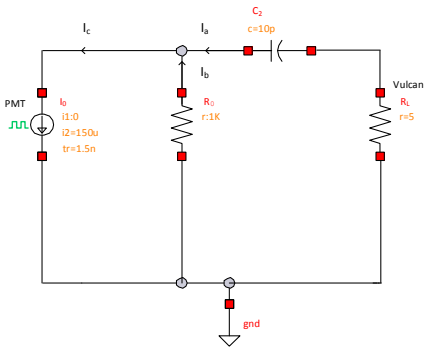


Figure 4.8: The high pass filter model creating overshoot on the signal being fed to the readout circuit. Here I_0=150 μA, t_r=1.5 ns, R_0=1k Ω, R_L=5 Ω and C_2=10 pF. The current source is a pulse with an exponential decay, R_0 the load resistance of the anode, C_c is the coupling capacitance, and the current is measured across the load resistance R_L.

Based on Kirchoff's current law, the current exiting the node is equal to the sum of the current entering the node. As shown in Figure 4.8, the PMT acts as a current sink and the current through the PMT is given by Equation 4.4:

$$I_c = I_a + I_b. \tag{4.4}$$

The voltage across the parallel branches of the network are of the same magnitude.

$$I_b R_0 = I_a X_{C_c} + I_a R_L. \tag{4.5}$$

Here X_{C_c}, is the impedance of the capacitor C_c. Substituting Equation 4.4 in Equation 4.5 leads to

$$(I_c - I_a)R_0 = I_a X_{C_c} + I_a R_L. \tag{4.6}$$

After solving Equation 4.6 for I_a we get

$$I_a = I_c \frac{R_0}{(X_{C_c} + R_L + R_0)}. \tag{4.7}$$

The impedance of the capacitance C_c is given by $X_{C_c} = \frac{1}{j\omega Cc}$. Substituting the impedance of X_{C_c} in Equation 4.7.

$$I_a = I_c \frac{R_0}{\frac{1}{j\omega C_c} + R_0 + R_L} \times \frac{j\omega C_c}{j\omega C_c}. \tag{4.8}$$

$$I_a = I_c \frac{j\omega C_c R_0}{1 + (R_0 + R_L) j\omega C_c}. \tag{4.9}$$

Substituting $s{=}j\omega$

$$\frac{I_a}{I_c} = \frac{sR_0C_c}{1 + sC_c(R_0 + R_L)}. \tag{4.10}$$

Simulation Results: The derived transfer function (Equation 4.10) is included in MATLAB and the corresponding code snippet is shown below. Refer to Figure 4.8 for the parameters and values used the simulation [32].

```
%% Calculate current through load resistor
num_RL=[R0 C2 R2 R0];
den_RL=[((C2 R0 R2) + (C2 R2 RL)) (R2 + RL)];
% Transfer function
V_RL_tf=tf(num_RL,den_RL);
% Simulation of the system with input
V_RL=lsim(V_RL_tf,u,t);
```

Listing 4.1: MATLAB code of the system causing the overshoot.

The above code is executed in MATLAB and the results are plotted together with the Cadence simulation results as shown in Figure 4.9,4.10 and 4.11. The plots show a good matching between the MATLAB model and Cadence simulations with deviations as minimal as $\sim 2.5\%$. These deviations are due to the different methodologies used. MATLAB uses equidistance steps for calculation while Cadence computes at non-equidistant points. The whole model was developed in MATLAB/Simulink, instead of Cadence due to the better high-level description capability.

By comparing the input and the output of the high pass filter (refer Figure 4.9), the effect of the high pass filter on the shape of the pulse can be observed. In the JUNO experiment, the shape of the pulse is vital to the accuracy of the measurement, hence any deformation to pulse should be avoided.

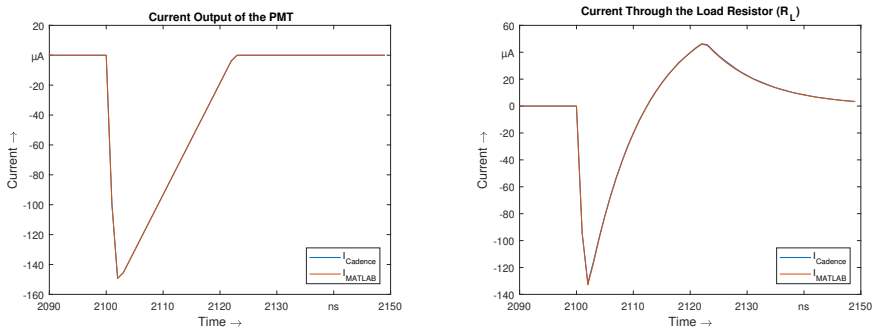


Figure 4.9: A comparison of the output of the PMT [Left] and the signal at the input of the TIA after passing through the high pass filter [Right].

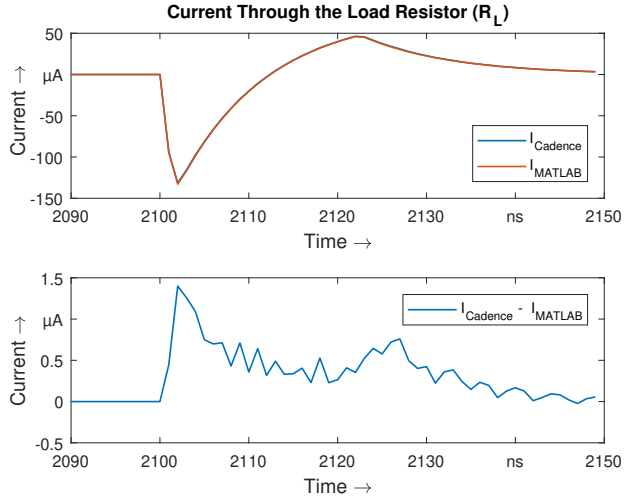


Figure 4.10: The shape of the current signal after passing through the high pass filter is highly distorted and suffers an overshoot. Additionally, the MATLAB model is compared to the Cadence simulation results in the upper plot with the lower one showing the residue.

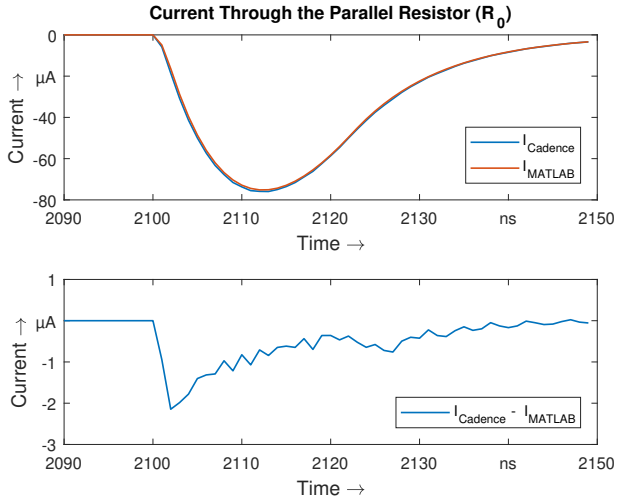


Figure 4.11: Comparison of the MATLAB model and the Cadence simulation of the current flowing through the parallel resistor R_0.

4.7 Overshoot Compensation

The overshoot of pulses is a well-known effect in neutrino experiments and overshoot compensation mechanisms such as double differentiation or double delayed pulse shaping have been used in other experiments [33]. In Vulcan, an active overshoot compensation circuit was developed and integrated.

The current drawn by the PMT is shown in Figure 4.9 (left) and the current drawn by the parallel resistor is shown in Figure 4.11. Summing up the total current drawn from the TIA results in the overshoot effect shown in Figure 4.9 (right).

The principle idea of the overshoot compensator developed for Vulcan is to use a secondary path to source the current drawn by the parallel resistor R_0. Thereby, the current provided by the TIA depends entirely on the current drawn by the PMT and is independent of the current drawn by the parallel resistor R_0.

The illustration shown in Figure 4.12, shows the current division among the electronic components and their corresponding waveforms. A generic schematic of the overshoot compensator is shown in Figure 4.13. The secondary path includes a capacitor (C_1), a voltage controlled voltage source (E_0) and a resistor (R_1). The voltage controlled voltage source provides the current for the parallel resistor R_1. Due to the arrangement of the circuit elements in the secondary path and the matching of capacitor (C_1) and resistor (R_1) to the capacitor (C_2) and resistor (R_0) of the high pass filter, the voltage controlled voltage source provides a current opposite in magnitude to the current drawn by the parallel resistor R_0. An additional resistor (R_2) is

added to replicate the matching imperfections of the resistor and capacitor in the secondary path to the resistor and capacitor of the high pass filter.

```
%% Calculate current through load resistor
num_RL=[(-R0 RL C1 C2 R2 R6) ((-R0 RL C2 R2) + (-R0 RL C1 R6 )) 0];
den_RL = [((C1 C2 R0 R2 R6) + (C1 C2 R0 R2 RL) + (C1 C2 R2 R6 RL))
    ((C1 R0 R2) + (C2 R0 R2)+ (C1 R2 R6) + (C1 R0 RL) + (C2 R0 RL)
    + (C2 R2 RL) + (C1 R6 RL))  (R2 + RL)];
% Transfer function
V_RL_tf=tf(num_RL, den_RL);
% Simulation of the system with input
V_RL=lsim(V_RL_tf,u,t);
% Current through the load resistor
I_RL=-V_RL/RL;
```

Listing 4.2: MATLAB code of the system compensating for overshoot.

The transfer function of the system with the overshoot compensator shown in Figure 4.13 was derived to the MATLAB code shown in Listing 4.2. The modeled system was simulated and the result is shown in Figure 4.14. The plot demonstrates the effectiveness of the overshoot compensation circuit. The TIA input signal shape retains the shape of the PMT input signal.

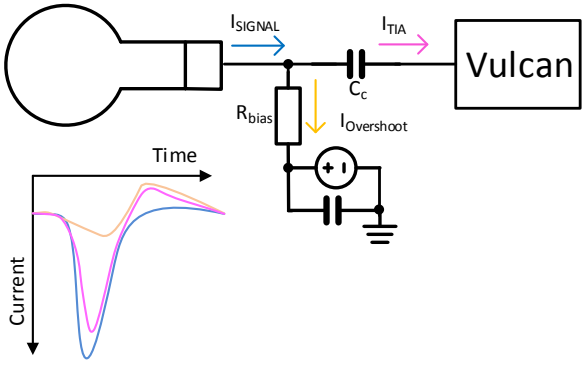


Figure 4.12: Illustration of the current division among the electronic components together with their corresponding waveforms on the bottom left.

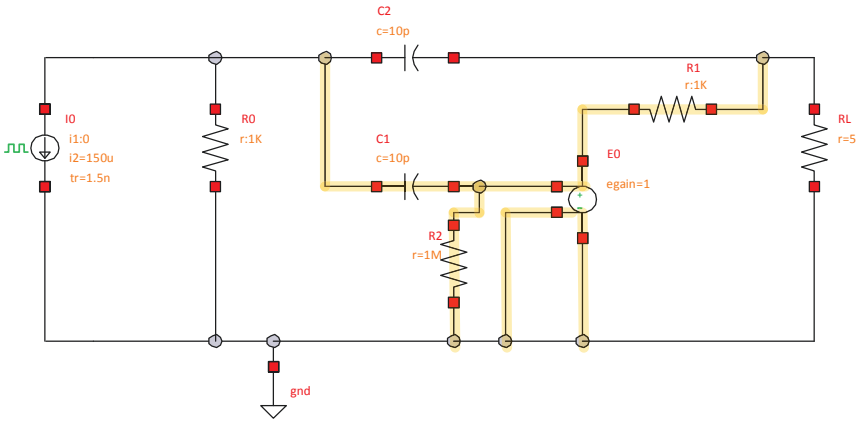


Figure 4.13: Schematic of the circuit containing PMT, high pass filter, overshoot compensator and the input stage of the TIA. The components of the overshoot compensator are highlighted in orange. The parameters are set to I_0=150 μA, t_r=1.5 ns, R_0=1 KΩ, R_L=5 Ω, R_1=1 KΩ, R_2=1 MΩ, C_2=10 pF and C_1=10 pF.

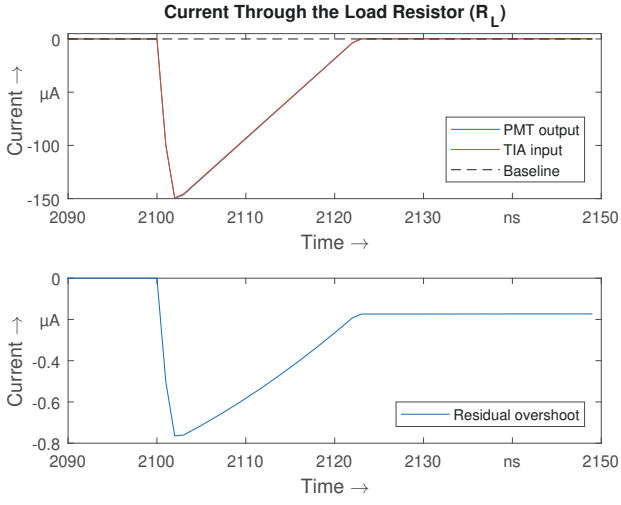


Figure 4.14: [Top] Overlay of the overshoot compensated signal on the PMT output signal. [Bottom] Difference between the PMT output signal and the overshoot compensator output.

4.8 Residual Overshoot

The performance of the overshoot compensator included in the Vulcan chip depends on the matching of the components (resistor and capacitor) of the high pass filter in the overshoot compensation circuit. The accuracy of the on-chip resistor values can vary ±25 % [34]. A mismatch of the components between the high pass filter and the overshoot compensation circuit can cause some of the overshoot to be uncompensated. This uncompensated residue is coined as residual overshoot in this thesis. Using the system model the effect of mismatch of components on the overshoot compensation is studied.

4.8.1 Impact of Mismatches in Overshoot Compensator

For the investigation, an artificial mismatch of 10 % was introduced and the effect of resistor and capacitor mismatch was studied.This mismatch percentage was sufficient to impact the pulse shape. From the plots in Figure 4.15 and 4.16 it can be observed that the mismatch of resistors has a higher impact on the pulse shape relative to capacitor mismatch. Since tunable resistors are relatively easy to implement, analysis using the model provided a path to develop a concept for a residual overshoot compensator.

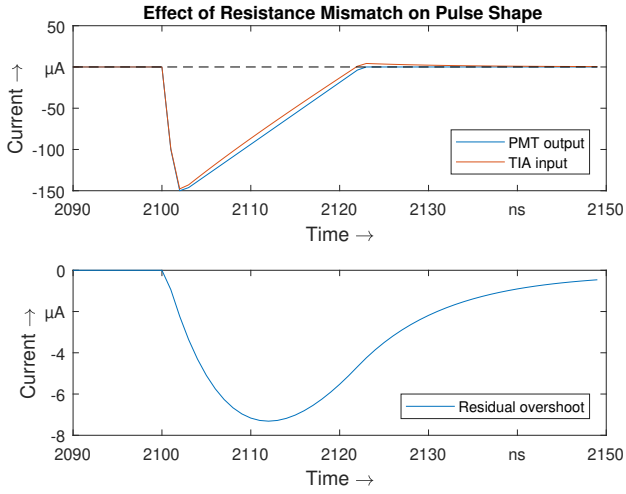


Figure 4.15: The effect of an overshoot compensator with 10 % resistor mismatch.

4.8.2 Mitigation Strategy

A possible mitigation strategy is to develop a feedback system to compensate for the residual overshoot by adjusting the resistance value of the existing overshoot compensator system. The existing resistor must be replaced by a variable resistor which is adjusted by the residual overshoot compensation system.

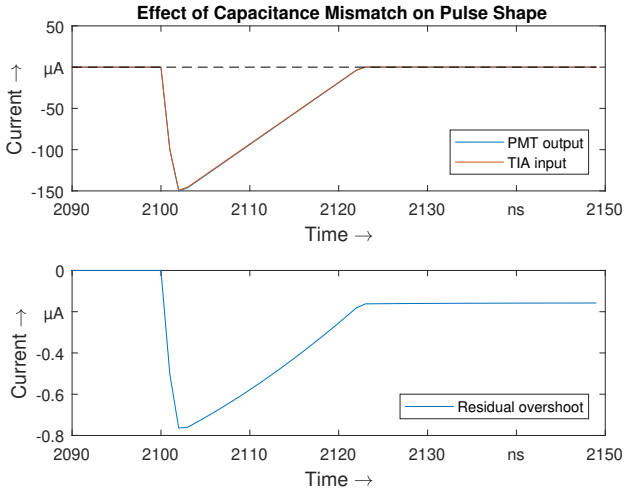


Figure 4.16: The effect of an overshoot compensator with 10 % capacitor mismatch.

The concept for the proposed system is as follows. Assuming the input signals to the system are responses from single photon electrons, the output from ADC is analyzed to find the peak value of the pulse. A sample, 30 ns [1] after the peak of the signal is extracted for analysis. The sample for analysis is chosen such that, at this sample, the signal amplitude would have settled to zero, therefore the corresponding digital output will generate a value less than or equal to 1 LSB.

The error between the value of the extracted sample (30 ns after the peak of the signal) and the speculated value is calculated and based on the sign of the error the variable resistor can be incremented or decremented in defined steps. Another option is to increment or decrement the resistor value proportional to the error value.

4.8.3 Simulation

A model was developed in MATLAB using the former idea of incrementing in predefined steps based on the sign of the error signal. The Figure 4.17 shows the effect of resistor mismatch on the pulse shape and the restoration of pulse shape by adjusting the resistor value using the residual overshoot compensation feedback loop.

For this concept, it has been assumed that the sample number after the peak of the signal which is used for analysis is already determined by studying the shapes of the expected pulses from the PMT. Further refinement of the model can be applied after the actual signal shape is thoroughly studied and the point of measurement is further investigated.

[1] This is a preliminary value used for the proof of concept.

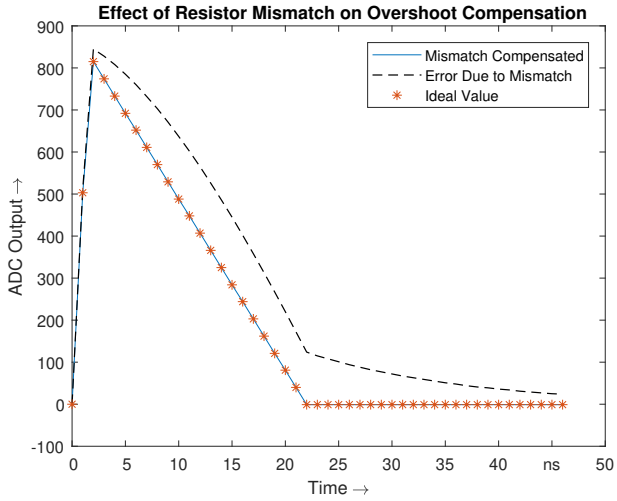


Figure 4.17: The effect of a residual overshoot compensator shown in the ADC output.

4.9 Baseline Shift

A baseline shift is a deviation from 0 A during the absence of a signal. One of the intended measurements in the JUNO experiment is the integration of the area under the pulse to determine the number of photoelectrons. The presence of any unidentified baseline shift will result in erroneous calculations as a baseline shift contributes to significant variation in charge measurement. Causes for the baseline shift and a sigma-delta based regulator to set the baseline to a predefined value are presented in the following sections.

4.9.1 Effect of AC Coupling on the Baseline

Pulses produced in JUNO are mono-polar i.e. the pulse lies either below or above the x-axis. The coupling capacitor C_2 (refer to Figure 4.8) placed between the PMT (I_0) and TIA (R_L), blocks the direct current. Due to the mono-polar nature of the signal, the coupling capacitor alters the baseline of the pulse such that the area enclosed by the waveform above the baseline and below the baseline are equal [35]. This effect of the coupling capacitor causes the baseline to shift temporarily.

In a hypothetical case of regular periodic mono-polar pulses, the baseline shift will be constant and can be later compensated. However, pulses from particle detectors are aperiodic and the nature of the event dictates the amplitude of the pulse. These irregularities causes varying shifts in the baseline, therefore the system can benefit from an adaptive baseline regulator [35].

4.9.2 Effect of the RC Time Constant on the Baseline

Similar to the dependence of overshoot and pile up on the time constant (refer to Section 4.4), the baseline shift is also dependent on the value of *RC*.

The amount of signal passing through the coupling capacitor is stored as a corresponding charge on the capacitor. This stored charge Q generates a voltage of $V_0 = \frac{Q}{C}$. The voltage V_c that develops at the coupling capacitor is related to the time constant which is determined by the coupling capacitor C_c and the combined resistor equivalent of R_0 and R_L [16].

4.9.3 Effect of High Event Rates on the Baseline

For a small pulse, the baseline fluctuation due to the RC time constant of the high pass filter might not be significant for amplitude measurements. A circuit with a time constant of 10 ns, and for a pulse shape as shown in Figure 4.18 produces a baseline shift of 175 nA.

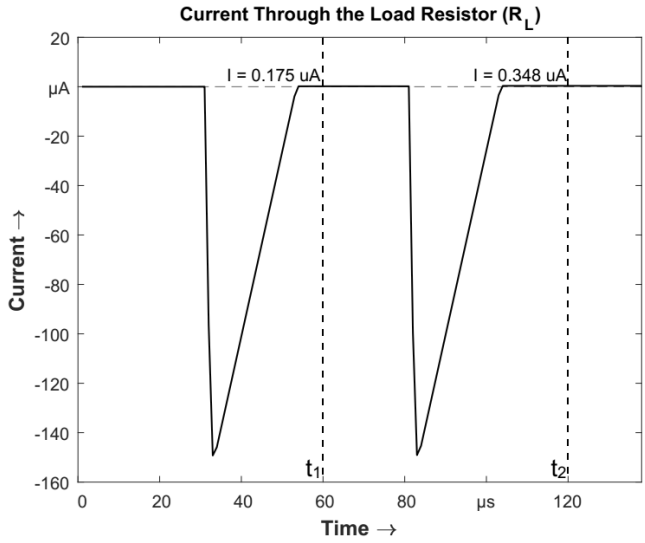


Figure 4.18: A slow baseline shift after each pulse. The baseline shift is added up for the preceding pulse hence the increment in the baseline. At time t_1 the baseline shift of 175 nA and at time t_2 the baseline shift of 348 nA is measured.

The baseline shift becomes significant when the event rate of the pulses increases. Figure 4.19 shows an exemplary scenario with varying pulse rates. For a system with a large time constant (third from the top), it takes significantly longer to return back to zero and the pulses start to pile up resulting in a noticeable increase of the baseline offset.

A reduction of the capacitor value will increase the initial voltage V_0 but shortens the discharge time of the capacitor. This reduction has the side effect of a reduced signal amplitude (ballistic deficit) and a deterioration of the Signal to Noise Ratio (SNR). Contrarily, an increase in

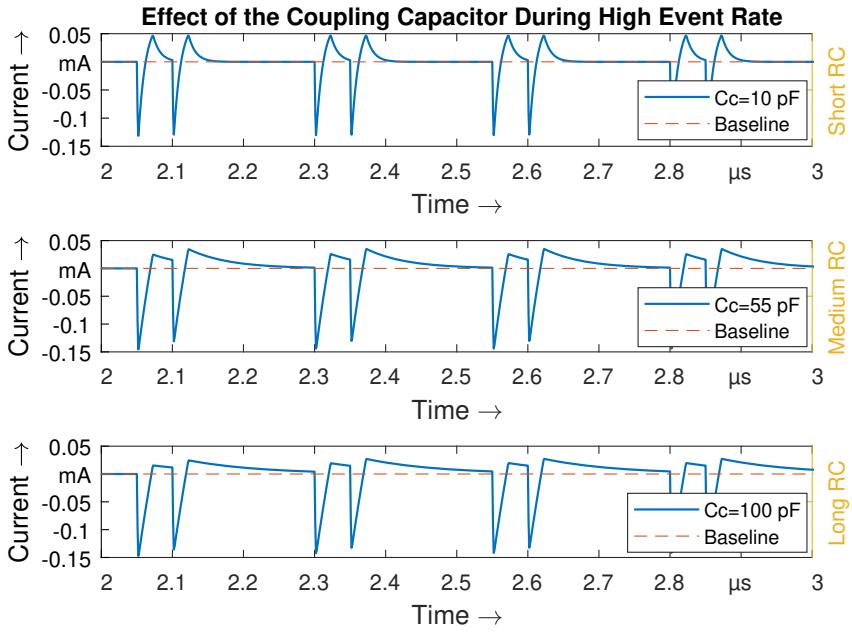


Figure 4.19: The Effect of *RC* on a high event rate signal. Observing the peaks of the signal above 0 A, it can be seen that the system with smaller capacitance [Top] produces a larger overshoot but settles to 0 A faster in comparison to the signals produced by the system with higher capacitance value [Bottom].

the resistor value preserves the signal amplitude and improves the SNR ratio but produces a baseline shift due to a relatively long settling time [16].

Summarizing the relation between the RC time constant and the effects:

- When the time constant is lower than the pulse length, a quick recovery to the baseline is achieved with the price of a higher peak overshoot.
- When the time constant is greater than the pulse width, a long recovery to the baseline and a reduced overshoot is achieved [29].

The relationship between the pulse shape, the restoration to the baseline, and the overshoot can be observed in the Figure 4.20. For a constant resistance and a coupling capacitance of 5 pF, the signal quickly recovers to the baseline at the cost of an overshoot. For a relatively large coupling capacitance of 50 pF, the signal recovery is relatively slow but the overshoot is significantly reduced. The difference in the overshoot of the signal produced by circuits with different coupling capacitance (5 pF and 50 pF) was measured as 2.7 %.

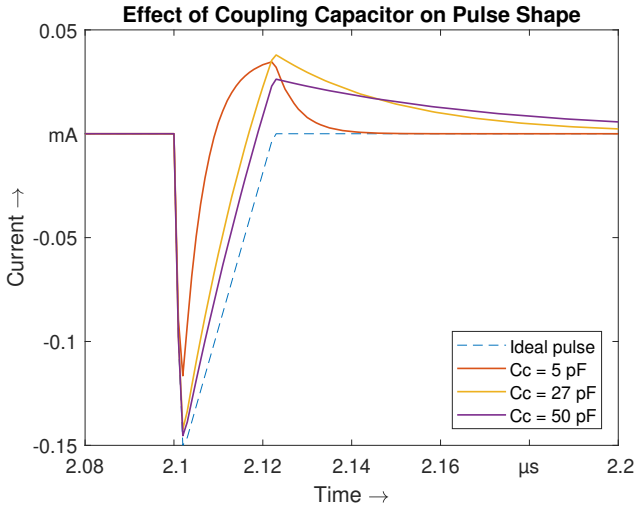


Figure 4.20: The effect of the coupling capacitance C_c on the pulse shape.

4.9.4 Passive Baseline Restorer

As counteraction for the described effects, baseline restorers are added either to the front-end electronics or integrated into the read-out circuits. The primary function of the baseline restorer is to return the baseline to the zero-level (0 A) between pulses. A passive baseline restorer is described in this section to demonstrate the contrast with the adaptive ADC baseline regulator implemented in Vulcan.

The baseline restorer shown in Figure 4.21 works by connecting the signal line to ground during the absence of a signal. The switch is turned "OFF" for the duration of the pulse i.e. when the signal level exceeds a specified threshold, thereby connecting the signal to the output path. When the switch is turned "ON", the resistor R_1 restores the output voltage level to 0 V. Often, baseline restoration circuits are placed after all the stages that introduce AC coupling effects.

The baseline restoration rate depends on the time constant RC where R is the equivalent resistance and C is the coupling capacitance (here C_c) (refer Figure 4.21). The discharge time constant must be shorter than the pulse width for this baseline restorer to work.

Another existing solution takes advantage of the pole-zero cancellation. In this method, a resistance is added in parallel to the capacitance, thereby modifying the combined transfer function to have only one pole in the denominator. Further information on this method can be obtained from [17].

Gated integrators with switches in the feedback loop of the integrators have also been used in various experiments to restore the baseline [37]. Baseline restorer circuit topologies have varied

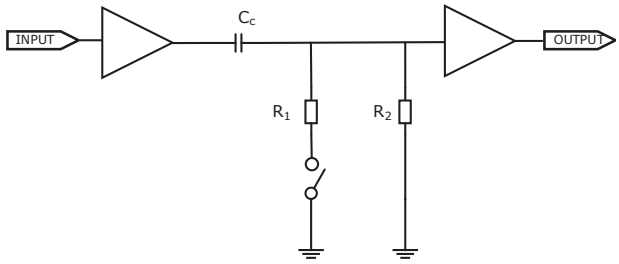


Figure 4.21: The schematic of a switch-based baseline restorer [36].

through generations from simple circuits with diodes to active circuits with gated resistors in the feedback loop of integrators [38], [39].

The switches placed in the baseline restorer circuit presented in [36] and [37] can introduce switching noise [17]. Considering the noise margin for the iPMT in JUNO an alternative solution for a baseline restorer was proposed. Instead of restoring the baseline to zero level, the baseline is regulated to a predefined level. Analog compensation techniques suffer from the mismatch of components, while an active baseline regulator can be adapted to compensate for the mismatches.

4.10 Active ADC Baseline Regulation

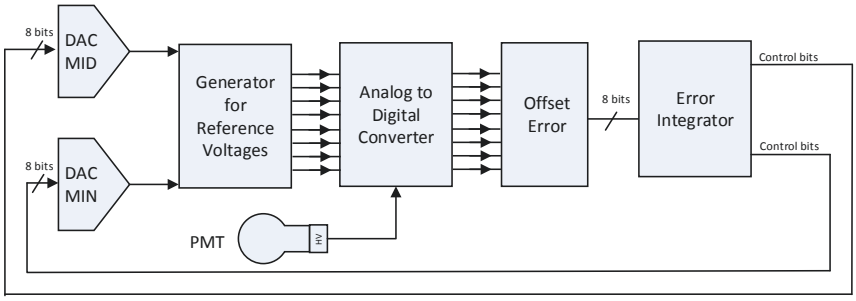


Figure 4.22: ADC baseline regulator based on a sigma delta modulator [40].

The architecture of the baseline regulator implemented in Vulcan is shown in Figure 4.22. The ADC baseline regulator is a digital control loop coupled with the principle of a sigma-delta modulator. The regulator is activated only when the measured ADC output is below the configurable signal threshold. This setup prevents any unintentional regulation of the signal.

As a first step, the regulator reads the output of the ADC and computes the deviation from the expected value. The deviation is calculated by the "Offset Error" block.

The generated error is scaled down and later integrated by the "Error Integrator" [26]. By scaling down the error signal, a low pass filtering effect is achieved as the system slowly reacts to the changes in the error signal instead of changing abruptly. The signal from the error integrator is used as a control signal to adjust the reference ladder for the comparators in the ADC thereby adjusting the baseline to the desired level.

For verification, the desired baseline was configured to be around 3 Least Significant Bits (LSBs) (binary "0000 0011") and the current output of the ADC is at 7 LSBs (binary "0000 0111"). In this case, the "Offset Error" block generates an error signal as shown in the left plot of Figure 4.23. The error integrator gradually increments and alters the reference voltages of the comparators in the ADC as shown in the right plot of Figure 4.23.

As the reference voltage increases, the ADC comparator reference voltage increases. For the same input signal, the ADC will produce a lower value. The settling time of the reference voltage depends on the error scaling factor which is programmable in Vulcan.

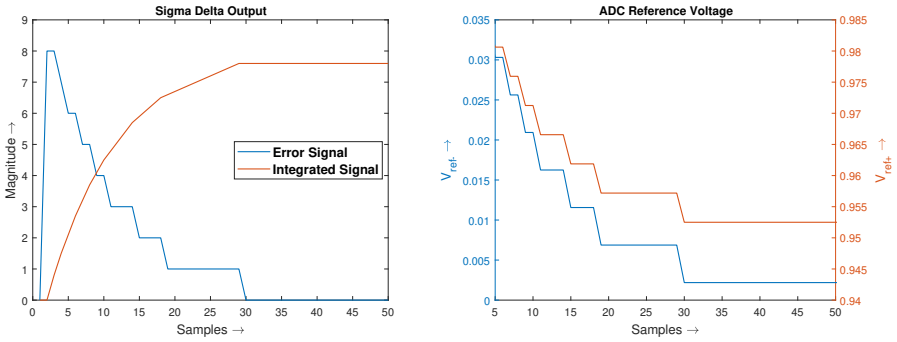


Figure 4.23: [Left] Instantaneous (black) and integrated (blue) error signals of the error integrator block. [Right] Changes in the reference voltages of the ADC, blue line marks the lower voltage level adaptation and the orange line marks the higher voltage level adaptation to the regulator output.

Figure 4.24 shows the impact of the baseline regulation on an exemplary pulse. The signal in the left plot of Figure 4.24 marked in blue, lies on the shifted baseline. On integration, the shifted signal will produce a higher charge accumulation than the actual value. A baseline corrected system (ideal) will remove the offset and the signal will lie on the true baseline as shown in the right plot of Figure 4.24.

For the second prototype of Vulcan, an improved ADC baseline regulator was implemented with coarse and fine tuning capabilities and a sigma-delta modulation. Figure 4.25 shows the effect of the sigma-delta modulation principle included in the ADC regulator. Instead of setting to the desired value, the sigma-delta modulator toggles around the desired baseline. This effect is achievable as the step size of the controlling DACs: DAC MID, DAC MIN as shown in Figure 4.22) are smaller than the step size of the ADC. Figure 4.26 shows the baseline shift effect

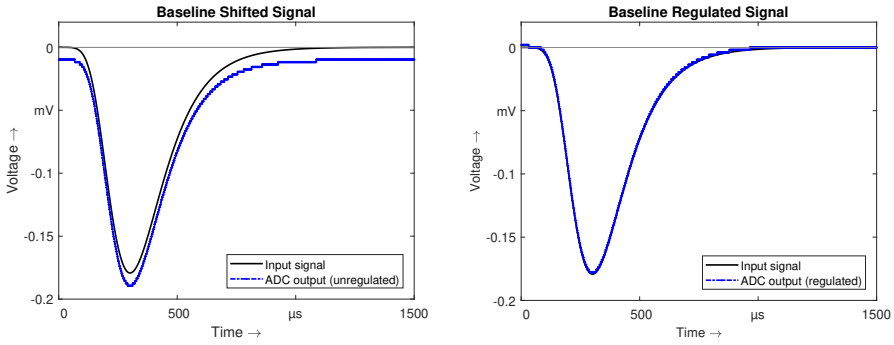


Figure 4.24: [Left] Input signal (black) and unregulated ADC output signal (blue) with a baseline shift. [Right] Input signal (black) and ADC output (blue) after the baseline shift has been compensated by the baseline regulator.

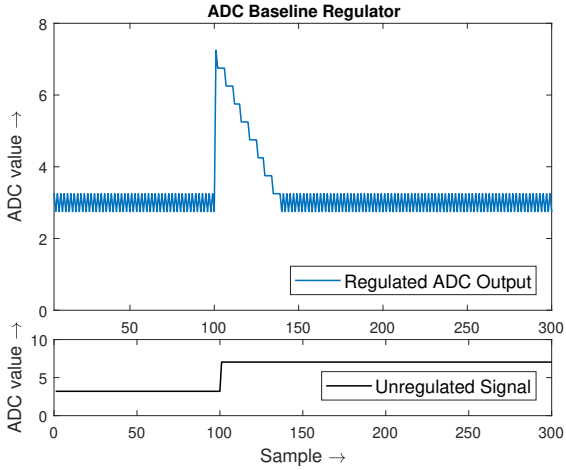


Figure 4.25: The plot shows the regulation of the ADC output. The average of the regulated ADC reaches the desired baseline of 3, even after introducing an artificial error (at sample 100). The unregulated ADC output in the lower plot is presented for comparison.

on the digitized output from the ADC. The baseline shift after the first pulse (blue pulse) is measured. This measured shift is used to adjust the baseline before the arrival of the second pulse (orange pulse). As a result of the baseline regulator, the measured signal lies on the configured predefined value.

The second modification is the use of two rates of tuning. In addition to the tuning of the reference voltages of the ADC, the transimpedance amplifier was also tuned using the control signals produced by the regulator. When the error difference is larger than the fine-tuning

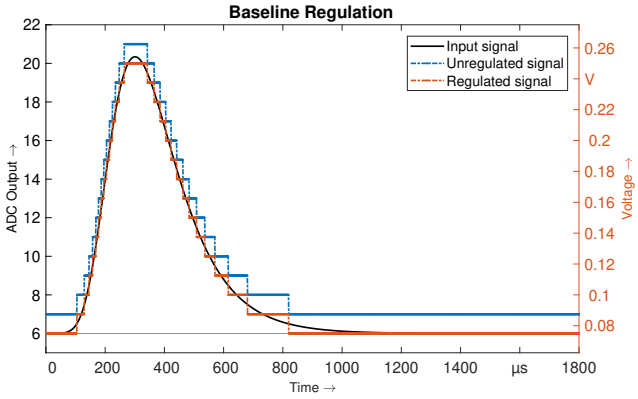


Figure 4.26: The offset after a pulse (blue) was measured. The offset correction was applied to the successive pulse by the regulator (orange).

threshold, control signals from the ADC baseline regulator can be provided to the TIA. When the error difference is less than or equal to the fine tuning threshold, control signals from the ADC baseline regulator are provided to the reference generator of the ADC as discussed earlier. The switch shown in Figure 4.2 and Figure A.1 controls the coarse and fine-tuning feature of the ADC baseline regulator.

The baseline shift occurs gradually, hence the shift is exaggerated (by a factor 10 times) in the simulations as in Figure 4.25 to demonstrate the functionality of the regulator.

4.11 Summary

For systems with a low event rate and for systems measuring the amplitude of the signals, small baseline shifts might not produce a significant impact [16]. However, for systems integrating the signal to calculate the charge accumulation like in JUNO, even small baseline shifts thus accumulate and thus introduce a considerable error in the measurement of the signal. An adaptive and configurable ADC regulator is useful especially for systems producing an aperiodic signal with varying amplitude and has been implemented to Vulcan. In addition to the baseline correction, the low pass filter reduces the effect of lower frequency disturbances along the signal line.

A baseline drift during phases with high signal rates and the overshoot effect could result in a pile-up of signals. By integrating both the baseline regulator and the overshoot compensator in the readout circuit the adverse effects could be reduced. As the implemented baseline regulator is located further away from the input signal, it works in conjunction to the overshoot compensator and it cannot be compensated for the overshoot of pulse caused by front-end high pass filter. The sub-modules of the model described in Section 4.2 has been implemented in silicon.

Integration of The Data Processor

5

The core component of the Vulcan chip is the analog to digital converter. A resource efficient and highly configurable SoC was developed by the integration of the analog to digital converters with a control unit, a data processor and other auxiliary components mentioned in Chapter 3.

One major motivation for the data processor is the reduction of data rate and required output pins. Transmitting the raw data from three 8-bit ADC would require 3×8 bit $= 24$ lines. Since the output signals are transmitted through LVDS lines, required number of pins double up to 48 lines ($= 48$ pads). This would increase the required die area which directly correlates with the Silicon production costs. Integrating a processor with the Analog to Digital conversion Unit (ADU) avoids the transmission of redundant data thereby reducing the required number of pins from 48 to 16 and in consequence reducing both the power and area required.

In addition, the data processor is utilized to combine ADC source information with other system information and transmit it as meta-data for data identification and reconstruction. After analyzing the specification, the architecture of the data processor has been decided and interfaces were defined. The RTL description of the data processor was done in VHDL and pre-silicon verifications were performed on different hierarchy levels to assure adherence of the data processor to the system requirements. In this chapter the design, implementation details of the main data processor developed for Vulcan are discussed.

5.1 Requirements

Among the various factors influencing the architecture unit of the data processor, some of the critical factors are described in this section.

5.1.1 Data Rate of Events

The expected neutrino events due to inverse beta decays are expected to be around 90/day or (≈ 0.002 Hz). In contrast, an event rate of 245 Hz is expected from background events in the liquid scintillator. The PMT dark noise contributes to an event rate of $3.3\,10^6$/day.

After considering the expected event rate from various events, the precision required for digitizing the signal was calculated [3]. Based on the calculations, the requirement to digitize signals at 1 GHz was extracted. The digital control unit including the data processor was operated at 250 MHz.

5.1.2 Supernova Event

As mentioned in Section 2.1.2, a supernova will produce a large flux of neutrinos with high energies in a short duration of time. Assuming a nearby supernova event in our galaxy is approximately 3 kpc [1 parsec ≈ 31 trillion km] away, and is expected to create up to 60,000 neutrino events in the detector in less than 10 seconds. During a supernova event, large number of photoelectrons are generated resulting in the generation of current pulses at a relatively higher frequency. The electronics in JUNO is required to be able to handle high data rates on occurrence of a supernova [3]. A supernova is a rare event, designing the electronics for supernova data rates as the typical data rate is a design overkill. At the same time, it is essential not to lose data during a supernova event. In Vulcan, the ADC structure has been designed to accommodate such large dynamic range of signal amplitude and the memory in the GCU is used to cope with the higher data rate (refer Section 2.2.4).

5.1.3 Clock

In Vulcan, a design decision was made to group sub-modules to operate in different clock domains. For instance, the ADC samples data at both rising and falling edge of 500 MHz clock, data is transmitted out of the Vulcan chip at a 500 MHz and the operational frequency of the data processing is at 250 MHz. The clocks required for the sub-modules in Vulcan are derived from a 32.5 MHz reference clock provided by the back-end card placed above water. Vulcan uses an internal phase lock loop to generate the clock required for the sub-modules.

Owing to the multiple clock domains, downsampling of data at the input of the data processor and upsampling at the output of the control unit has to be performed. As shown in Figure 5.1, the data output of the ADC is demultiplexed, buffered and transmitted at 250 MHz. After encoding, 4×8-bit data is transmitted from each ADC to the data processor. The data processor transmits 32-bit data at 250 MHz clock. The module interfacing the control unit and the LVDS driver, "the Data Mode Multiplexer", multiplexes the 32-bit data into 16 bits and transmits with a 500 MHz clock.

For the reconstruction of the signals at the data acquisition unit, it is essential to provide the timing information of the data samples. An internal digital counter operating at 250 MHz, provides the time stamp for the ADC samples. Further information on the time stamp generation will be explained in Section 5.3.1 of this chapter.

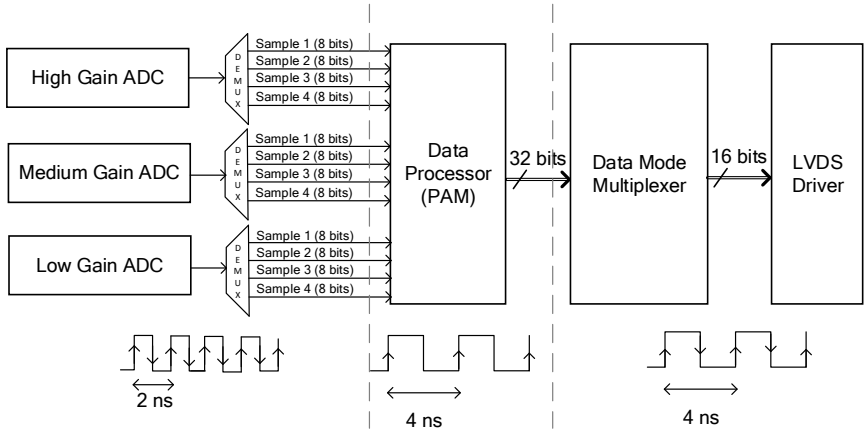


Figure 5.1: Sub-modules operating at different clock frequencies are presented. Upsampling and downsampling of data to match the frequency of operation are marked in the diagram.

5.2 Data Processor

As mentioned in Section 3.1.3, preconditioning of data, data reduction and compression of data during noise can be achieved by including a dedicated data processor after the ADC in the Vulcan chip. The architecture, functional description of the block and simulation results of the main data processing unit (Programmable Adaptive Memory (PAM)), are described in this section.

Data for track identification is required on the reconstruction side external to the Vulcan chip due to the three parallel signal tracks,. A standard method of transmitting identification information is by packing the information as meta-data and transmitting them through the data lines. Some of the system events generated by the blocks surrounding the data processor are discussed in the following sub-sections.

5.2.1 ADC Encoder and Designator

After the 256-bit thermometer code is converted into an 8-bit gray code for the purpose of bubble error detection, the data is transferred to the PAM processor. As a first step, the processor converts the gray-coded data to binary code which corresponds to the hardware description language equivalent of decimal number system. The binary to gray code conversion of an 8-bit code is performed using the following formula.

$$\text{Binary}\,[7] = \text{Gray}[7]. \tag{5.1}$$

$$\text{Binary}[n] = \text{Binary}[n+1] \bigoplus \text{Gray}[n]. \tag{5.2}$$

Figure 5.2 illustrates the gray to binary code conversion for 8 bits. By using the formulas described by Equation 5.1 and Equation 5.2, the 8-bit gray code is converted to 8-bit binary code.

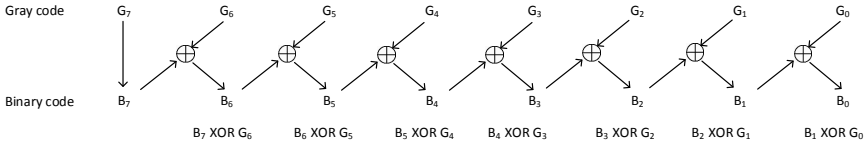


Figure 5.2: Visualization of Gray to Binary conversion as used in PAM processor.

As shown in Figure 5.3, the ADC samples are sent to the ADC assignment unit after the gray to binary conversion along with the bubble error counter value. The ADC assignment block is a multiplexer which on configuration decides which set of data samples corresponds to the high gain, medium gain and low gain track. The ADC assignment block has been included for added safety to account for any swap in wiring between the ADC and the data processor.

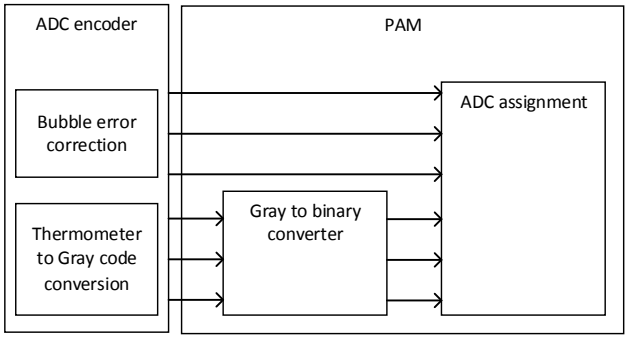


Figure 5.3: The ADC designator block as an entry stage for the signal entering the PAM.

5.2.2 ADC Analyzer

In the architecture of Vulcan, three ADCs are sampling the input signal with different step sizes (resolution). While the three ADCs are included in the design to have a high dynamic range and at the same time, a good precision for small amplitude signals, it is sufficient to transmit samples from one of the three ADCs. The amplitude of the input signals generated by the front-end electronics determines which samples of the ADCs have to be forwarded to the next stage while discarding the remaining. Since the ADCs are sampling data at the rate of 1 ns and

events are stochastic and produce varying amplitude, it is necessary to have circuits which can automatically make a decision on which samples has to be forward based on the amplitude of the signal generated by the event.

Here, data selection is the process of determining the data from the appropriate gain track (ADC for the high gain track (ADC HG), ADC for the medium gain track (ADC MG), ADC for the low gain track (ADC LG)). The ADC analyzer can be visualized as a 3:1 multiplexer which selects data based on predefined conditions. It is essential that the decision process includes all scenarios as data discarded at this stage cannot be recovered.

The key decision points are:

- The switch is based on thresholds which include the special case of ADC saturation. If the input signal exceeds the voltage range which an ADC can handle, the ADC output gets saturated to the highest possible value (i.e. 255). Saturated data samples from ADC HG and ADC MG are discarded automatically.
- General priority of data selection: ADC HG > ADC MG > ADC LG.
- On saturation, the change of data source from ADC HG to ADC MG to ADC LG should occur instantly.
- Switching of the data source from ADC LG to ADC MG to ADC HG should occur after a delay (or hysteresis).

5.2.3 Bus Mode

The switching of the data source is coined as "Bus mode change". Switching of data source adds overhead a detailed explanation follows in Section 5.3.1. For compensation of this overhead introduced due to switching, a buffer is included in the next stage of the data processor. The buffer size has been designed to accommodate 4 times the maximum expected data rate. As an additional precautionary measure two flags are generated by the buffer. The first one is generated when the buffer is 50% full and the second when the buffer is 80 % full. When these flags (50 % full and 80 % full) are generated, the ADC analyzer reduces further overhead by avoiding switching of the data source until the flags are turned off (i.e. the buffer is less than 50 % full). During this phase, the ADC analyzer selects the data from ADC HG which is most valuable for physics analysis.

The output of the ADC analyzer are data samples, that cannot be distinguished without an identifier and the data source cannot be identified. During the reconstruction of the signal in the data acquisition unit (data acquisition (DAQ)), data needs to be scaled up or down depending on the ADC gain track because all three tracks have different gain. For identification, 4 bits have been encoded to carry the data source identifier. Since there are 8 possible bus modes, 4 bits were chosen for the encoding. Details of this encoding can be found in the Table 5.1 and 5.4. In addition to the data selection, the ADC analyzer generates this bus mode information and forwards it to the following stages.

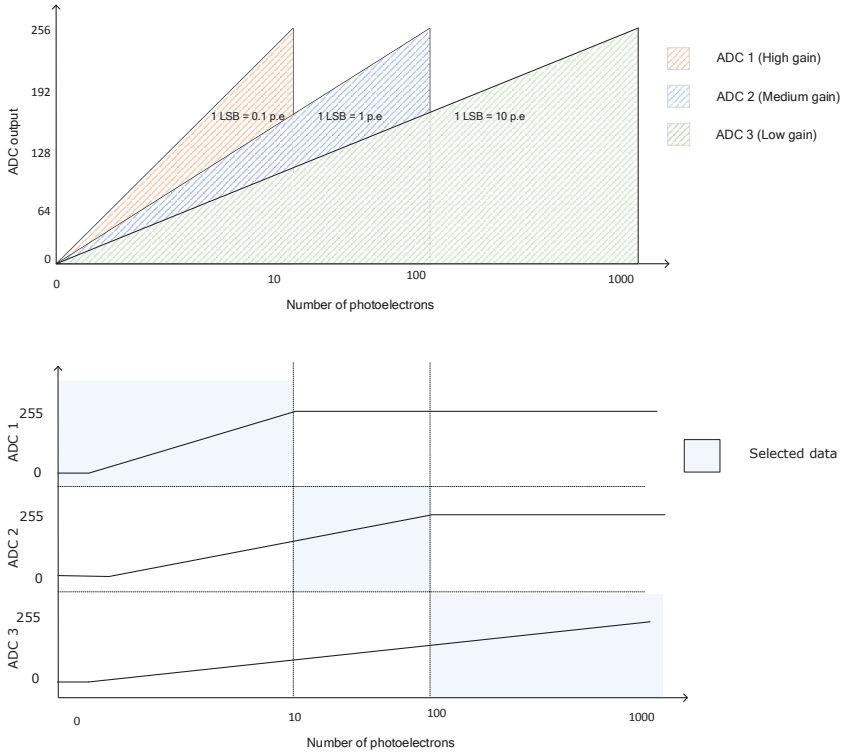


Figure 5.4: Exemplary data selection by the ADC analyzer. [Top] The dynamic ranges of ADCs are shown. [Bottom] The output of the ADCs are shown for a linearly increasing ramp signal. The slope of the output signals are different owing to the ADC's gain. The highlight blue region indicates the data saved based on the selection process.

5.2.4 Decision Process

A flowchart describing the sequence of steps in the decision process and the actions performed based on the decision is shown in Figure 5.5. As a first step, the flags of the ring buffer occupancy are checked. If the flags are not set (i.e. ring buffer is less than half full) the left side of the decision tree process is active.

As described in Section 5.1.1, the number of events expected per day in JUNO is quite low. Therefore, the ADCs of the Vulcan chip will be measuring noise most of the time. The ADC Analyzer first compares the digitized data from the ADC HG with the configured noise threshold. If the signal amplitude is below the noise level, it indicates events of significance have not been generated and the data from the ADC MG and ADC LG can be discarded and data from ADC HG is forwarded to the next stage. In the upcoming stages of the data processor compression

on non-event data (noise) can be performed.

In the next phases of the decision tree, the digitized signals from ADC HG, ADC MG and ADC LG are sequentially tested. If the digitized signal from ADC HG is more than the noise level, but is not higher than the maximum voltage ADC HG can digitize or less than or equal to THR_{HG}, then the samples from ADC HG are forwarded and the rest are discarded. When the digitized signal from ADC HG is saturated i.e. when the input signal crossed the maximum voltage level of ADC HG can digitize or greater than THR_{HG}, then the data samples from ADC HG are discarded.

In Figure 5.4, the lower plot shows an exemplary ramp signal provided as input. The slope of the output signal of the ADCs are different for the same input owing to the different gain in front of the ADCs. When the ramp signal amplitude is less than or equal to the amplitude of the signal produced by 10 p.e., ADC HG digitizes the signal with maximum precision (relative to other ADCs). When the amplitude of the signal exceeds the range the ADC HG can digitize (more than 10 p.e.) the output gets saturated. In this case, the data from ADC HG is discarded and data from ADC MG are checked. Since the data from ADC MG is valid until the amplitude crosses the upper threshold (i.e 100 p.e.) of ADC MG, data from ADC MG is marked as valid data and is forwarded to the next stage while discarding ADC HG and ADC LG.

Unlike ADC HG and ADC MG sample checks, samples from ADC LG are not checked against an upper threshold. If the digitized data from ADC HG and ADC MG has saturated it indicates the occurrence of a large signal amplitude. In that case, only the data from ADC LG can be valid, hence the data from ADC LG are forwarded to the next stage.

Like previous neutrino experiments [28], signals generated from the events in JUNO are expected to decay in amplitude and gradually return to idle state, where the ADCs are only measuring noise. When signals decay from high amplitudes to lower amplitudes necessary care has to be taken to ensure that the ADC analyzer selects the data from the right ADC track.

An exemplary input signal corresponding to 20 photoelectrons was generated. Based on previous explanations, the ADC analyzer is expected to choose the data from the ADC MG. Due to noise the signal amplitude drops suddenly for few samples. For these samples, the status of ADC HG changes from saturated and invalid to valid. If the ADC analyzer switches back and forth during signal decay, it can result in signal corruption. For avoidance of such scenarios, a hysteresis counter is used in the ADC analyzer.

A hysteresis counter is added to the decision process to avoid data mode change during the fall time of the signal. The hysteresis counter adds an additional threshold crossing to the decision process. The hysteresis counter is initially set to 0. When signal amplitude falls from a higher amplitude (ADC MG) to a lower amplitude (ADC HG), the hysteresis counter is incremented by 1 for every clock cycle until the hysteresis threshold (i.e 10 cycles) is reached. When reaching the threshold it is guaranteed that the signal change is stable and the mode change from ADC MG to ADC HG is made. Until the time the hysteresis threshold is reached, even when the data from higher resolution ADC (ADC HG) changes its status from invalid to valid, the ADC analyzer does not change its mode but rather sends data from ADC MG. The same hysteresis counter is added to avoid changes from ADC LG to ADC MG. In addition

to forwarding, the ADC sampled data to the following stages the ADC analyzer also tags the information about the ADC source and transmits this information.

As shown in Figure 5.9, an internal storage (ring buffer) follows the data selector. The capacity of the ring buffer has been chosen to be able to buffer data during high event rates such as supernovas. Due to unforeseen events and overhead generated due to bus mode changes, the ring buffer can overflow. Two flags are generated to indicate the occupancy of the ring buffer. The first flag RB 50 is set high when the ring buffer is half full. The second flag RB 80 is set high when the ring buffer is 80 % full. When these flags are set high, additional overhead generated due to change of data source or due to trigger signals (refer Section 5.2.6) are reduced. For instance, when the RB 50 is set high, the change of bus mode from ADC HG to ADC MG or ADC LG are blocked. When the RB 80 is set high the trigger signal generation is blocked in addition to the blocking of bus mode change from ADC HG to ADC MG or ADC LG. In short, when the signals RB 50 and RB 80 are set high, data from ADC HG is selected. If the ADC HG samples are below the noise threshold, the samples are marked as noise, otherwise as HG.

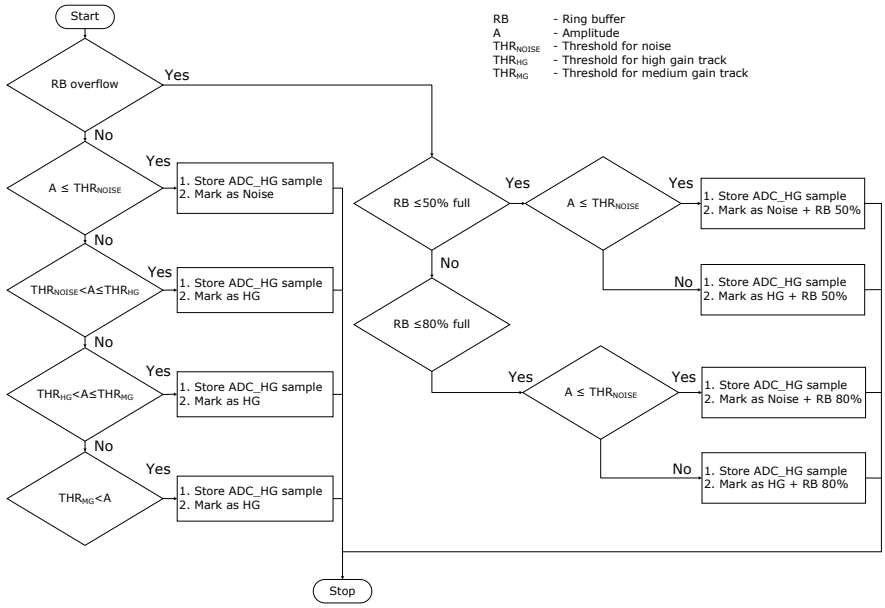


Figure 5.5: Flow chart for mode selection in PAM.

5.2.5 Counters

For the synchronization of the data processor with the GCU and timing extraction of the signals, two 10-bit counters are included in the data processor. The first 10-bit are allocated to record the number of sync signals (refer Section A.4) received by the data processor from the GCU. The second 10-bit counter increments on every rising edge of the data processor clock (250 MHz).

When these 10-bit binary counters reaches its maximum (2^{10}=1024), it wraps around. For indication that the counter has wrapped around an overflow flag is generated.

5.2.6 Trigger Generator

An internal system to keep track of the bus mode change, counter overflow and ring buffer overflows is included in the data processor. The system generates a trigger signal when any of the above mentioned changes occur and encodes the information about the changes into a 4-bit code. Details of the encoded data can be found in Table 5.3.

5.2.7 Ring Buffer

Due to the aforementioned overhead, the data transmission cannot always be instantaneous. Thus a data buffer is included after the ADC analyzer. First in First Out (FIFO) and Last in First Out (LIFO) are two methods of data processing of buffers. Among the two, the FIFO method was chosen for the PAM data processor. A circular buffer or ring buffer is an implementation of a FIFO. Unlike other FIFO architectures, where the old data is shifted to the next memory location on the arrival of new data, pointers are shifted to the next memory location in circular buffers. In scenarios where data of longer word length are required to be buffered, circular buffer implementation can be advantageous as it reduces the number of required shift operations [42].

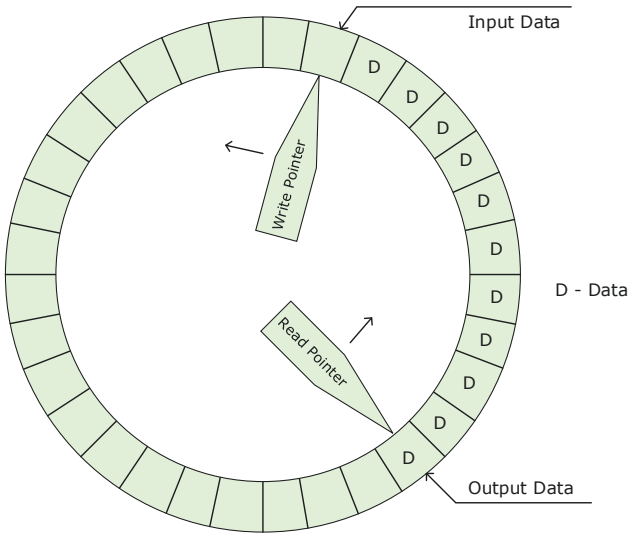


Figure 5.6: Ring buffer read and write pointer wrapping around in circular fashion [42].

In circular buffers, after the last memory location the pointer wraps to the first memory location, thereby forming a circle of memory elements as shown in Figure 5.6. Circular buffers are of finite width and in Vulcan the maximum size of the buffer required to handle high

event rates was obtained from simulation results provided by another research group within JUNO [43]. A word length of 40 bits composing of 32-bit header and 8-bit data were required to be stored in the buffer. A simulation of a supernova event was performed and the number of ring buffer slots filled for the simulations were collected. As shown in Figure 5.7, it can be observed that the maximum occupied ring buffer slots is slightly above 1000. Since the logical operations are performed in binary, values are preferably chosen to be the power of 2. It is safe to assume that the maximum ring buffer filling based on simulations is 1024 ring buffer slots. For generation of a safety margin, a ring buffer with 4096 slots corresponding to 4 times the maximum ring buffer occupancy expected during a supernova event was designed.

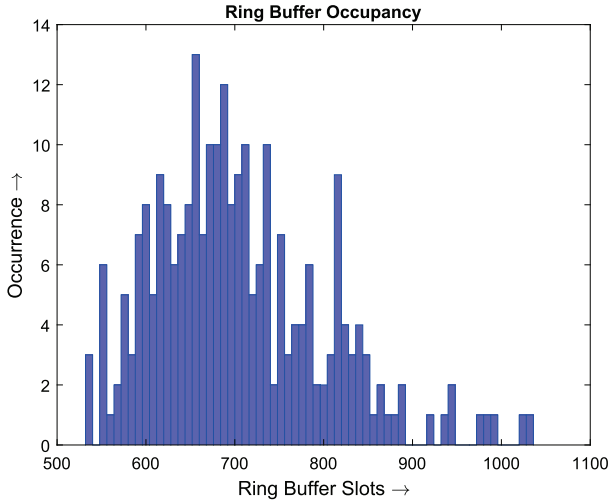


Figure 5.7: A histogram of simulation showing the filling of ring buffer slots during events generating high event rates like supernova [43].

Circular buffers have write and read pointers. Immediately after reset, both pointers are at the same memory location. Both pointers can be incremented independently from each other. In PAM, the write pointer is always incremented by 4 memory location every clock cycle, while the read pointer is incremented by 4 or 8 memory locations depending on the selected bus mode.

Due to the independence of the write and read pointers and the circular nature of the buffer, the write pointer can catch up with the read pointer indicating the buffer is fully occupied or the read pointer can catch up the write pointer indicating the buffer is empty. Since in both scenarios the address of the read pointer and the write pointer are at the same location, it is illogical to generate two separate flags for ring buffer full and empty using address information.

For counteracting this issue an extra bit is used for the address. For addressing 4096 slots in the ring buffer, 12 bits are required. By adding an additional bit to the MSB of the address, a distinction between ring buffer full and empty status can be made. The additional bit is solely

used for checking the status of the buffer and the remaining 12 bits are used the address to access the memory. The logical steps in deciding the status of the ring buffer can be understood from the flow chart as shown in Figure 5.8 and the description below.

Buffer full: In this case, the write pointer increments past the final address of the ring buffer and the additional bit (MSB) toggles due to wrap up. When the 12 bits (MSB-1 to 0) of the write and read pointer are equal, the additional bit of two pointers are compared. If the MSB of the read and write pointer are not equal then it indicates the write pointer has wrapped up and caught up with the read pointer. As a result, the ring buffer full flag is set high. This implementation follows the description in [44].

Buffer empty: Similarly when the 12 bits (MSB-1 to 0) of the write pointer and read pointer are equal, the additional bit of the read pointer and write pointer are compared. If the MSB of the read and write pointer are equal then it indicates the read pointer has wrapped up and caught up with the write pointer. In this case, the ring buffer empty flag is set high [44].

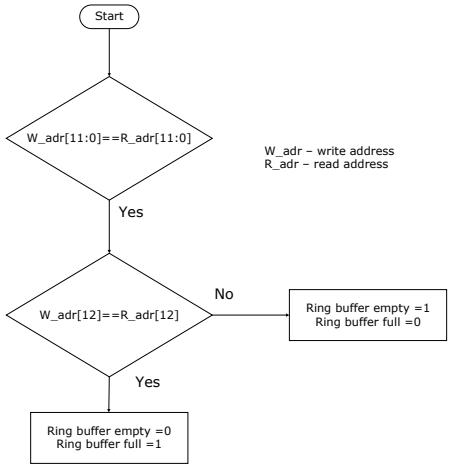


Figure 5.8: Decision process for ring buffer full and empty flag generation [42].

5.3 Header Data

The Header containing the metadata is transmitted when a trigger signal [1] is generated in the data processor. The header generator takes a snapshot of the counters and source of the data samples (bus mode) at the moment of the trigger generation and compiles them with the trigger information into a 32-bit header word. Figure 5.10 shows the composition of the header generated by the data processor. Of the 32-bit header, 10 bits are allocated for the sync counter, the next 10 bits are allocated for the digital counter, the final 12 bits are allocated for the following bubble counter, bus mode information and trigger information (4 bits each).

[1] This is not to be confused with a signal trigger based on the level

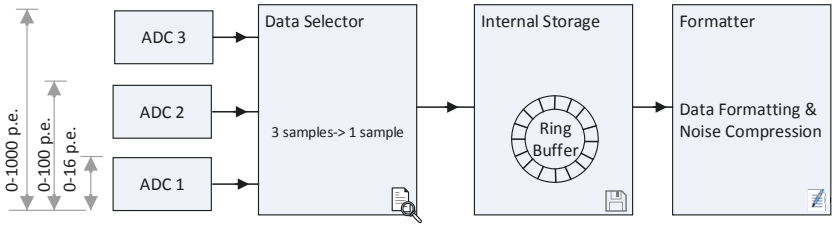


Figure 5.9: Overview of the programmable adaptive memory displaying the three stages of the data processor. In the first block data from one of the three ADCs are selected. In the second stage, the data is appended with the header information and stored in the ring buffer. In the final data transmission block, in addition to the generation of the reset signal and header information, compression of noise samples are performed based on the trigger information.

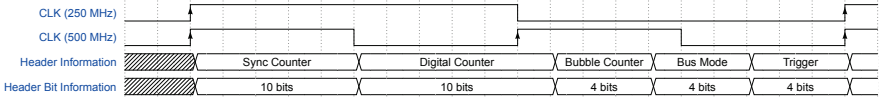


Figure 5.10: Composition of the header data in PAM.

Table 5.1: Bus mode description and its corresponding code.

Bus Mode	Mode Description	Header Code
NOISE	Lower halves of samples from ADC HG are transmitted	0001
HG	Samples from ADC HG are transmitted.	0010
MG	Samples from ADC MG are transmitted.	0011
LG	Samples from ADC LG are transmitted.	0100

5.3.1 Data Transmission Format

Header data and data samples from the ADC are in the bit stream. Header data which is generated by the processor and data samples generated by the ADC cannot easily be differentiated with the naked eye. Therefore, a bit stream of zeros (32 bits) are transmitted before transmitting the header data for a proper segregation. This bit stream has been coined as "reset" signal and is by design impossible to be generated by header or data words.

During the reconstruction of the signal from the data processor, the data stream can be scanned for the reset signal. The 32 bits following the reset signal is the 32-bit header information and the remaining data until the next reset signal are data samples from the ADC. The Figure 5.11 shows the order in which reset signal, header data and data samples are transmitted.

It can be observed from Figure 5.11 that the transmission of the reset data and the header in-

Table 5.2: Combinational bus mode description and their corresponding codes.

Combinational Bus Mode	Mode Description	Header Code
NOISE 50 (NOISE + RB 50%)	Bus mode changes to MG and LG are disabled and lower halves of samples from ADC HG are transmitted.	0101
HG50 (HG + RB 50%)	Bus mode changes to MG and LG are disabled. The latency for switching to NOISE mode is increased. Samples from ADC HG are transmitted.	0110
NOISE 80 (NOISE + RB 80%)	System triggers and bus mode changes to MG and LG are disabled and lower halves of samples from ADC HG are transmitted.	0111
HG80 (HG + RB 80%)	System triggers and bus mode changes to MG and LG are disabled. Latency for switching to NOISE mode is increased. Samples from ADC HG are transmitted.	1000

Table 5.3: Trigger description and their corresponding codes.

Trigger	Trigger Description	Header Code
BCM	Indicates a change of bus mode.	0001
DCO	Indicates an overflow of digital counter.	0010
SYNC	Indicates an assertion of sync signal.	0011
RBU	Indicates an underflow of ring buffer.	0100

formation for every trigger signal generated consumes 2 clock cycles, thereby creating overhead in the transmission. Data samples are buffered internally until the reset and header information for the corresponding samples are transmitted.

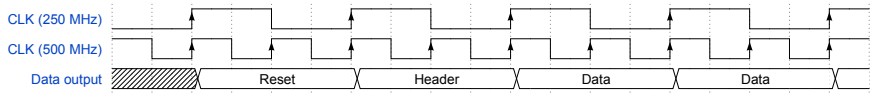


Figure 5.11: Overview of the data format. The data process is working with 250 MHz clock and the output data of the Vulcan chip is transmitted with 500 MHz clock. To initiate the data transmission a reset signal is generated followed by the header information. Until a trigger occurs in the data processor, data samples are continuously transmitted following the header.

5.3.2 Data Transmission Block

Each ring buffer slot is 40 bits wide and it stores 32 bits of header information corresponding to every 8 bits of data. The information compiled in the header is used for reconstruction of the signal and it is sufficient to transmit the header information to the data acquisition unit only when a trigger is generated.

Additionally, to the structure of the reset header, and data the compression of noise data is

Table 5.4: Combinational trigger description and their corresponding codes.

Combinational Triggers	Trigger Description	Header Code
BAD (BCM+DCO)	Indicates bus mode change and digital counter overflow.	0101
BAP (BAP+SYNC)	Indicates bus mode change and sync signal detection.	0110
SYNCO (SYNC+SCO)	Indicates assertion of sync signal and sync counter overflow.	0111
BPO (BCM+SYNCO)	Indicates bus mode change, assertion of sync signal and sync counter overflow.	1000

also carried out by the data transmission block. If the bus mode is ADC HG, and the amplitude of the signal is below the noise level, the 8-bit data samples are compressed to 4 bits by discarding the four most significant bits (MSBs) (refer Figure 5.12).

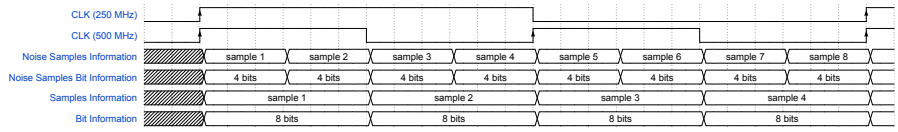


Figure 5.12: Noise compression in comparison with normal data transmission. By default, 4 samples are transmitted for every 250 MHz clock, while during noise mode the samples are compressed and 8 samples are transmitted every 4 clock cycle.

The width of the data packets is fixed to 32 bits. Both the reset signal and the header information are also 32 bits. By default, 4 samples of 8-bit data are transmitted in a packet. It is highly possible that the trigger signal can be generated during any instant of time. In this scenario, it is essential to transmit the samples before and after a trigger has occurred. Since the data frame is fixed to 32 bits, the remaining slots are filled with zeros. This concept is called zero padding and is illustrated in Figure 5.13 and Figure 5.14.

Figure 5.14 shows an exemplary scenario where a trigger signal is generated after the first sample. For compliance with the packet width of 32 bits, the remaining 24 bits are filled with zeros. The data sample before the trigger signal is transmitted before transmitting the reset signal and the header containing the trigger information. A similar procedure is followed for noise samples. In the example shown in Figure 5.13, the trigger signal is generated after the 6^{th} sample, therefore the slots for the 7^{th} and 8^{th} sample are filled with zeros.

The logical flow of the decision process in the data transmission block is shown in Figure 5.15. As a first step, the data transmission block checks if a trigger signal is generated. If a trigger signal is not generated, the left side of the decision tree takes precedence else the right side.

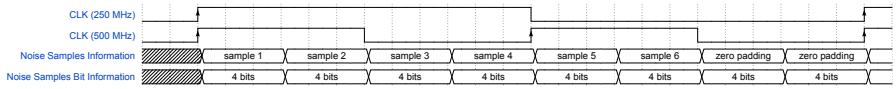


Figure 5.13: Zero padding when mode changes occur in between one of the four samples. The waveform shows the zero padding while transmitting noise data.

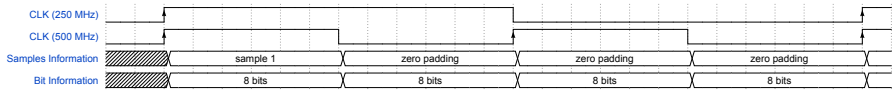


Figure 5.14: Zero padding when mode changes occur in between one of the four samples. The waveform shows the zero padding while transmitting noise data.

1. If the trigger signal is not generated and if the bus mode is noise (i.e. samples from ADC HG are selected and the amplitude of the signal is below noise level), data samples are truncated from 8 bits to 4 bits and eight consecutive samples are combined to a data packet and then transmitted. In this condition, the read pointer of the ring buffer is incremented by 8.

2. If the amplitude of the signal is above noise or if the bus mode is not "NOISE", "NOISE 50" and "NOISE 80", four consecutive samples are combined into a data packet and transmitted. In this condition, the read pointer of the ring buffer is incremented by 4.

3. If a trigger signal is generated, read pointer incrementation is paused. Instead of sample transmission reset signal and header information are transmitted.

4. For bus modes "NOISE", "NOISE 50" and "NOISE 80", 8 samples are transmitted instead of the default 4. During noise mode, data is read at a higher rate than it is written into the ring buffer. This compression of noise data and transmission at double the rate helps to compensate for the overhead generated due to the transmission of reset signal and header information after a trigger event. If the system continues in noise mode for a longer duration an underflow of data can occur.

5. Here, underflow is defined as the state when the number of samples required for transmission are more than the number of samples available in the ring buffer. For instance, if the ring buffer has only 4 samples and the bus mode is "NOISE", 8 samples are required for transmission. Hence an internal underflow event and a trigger signal are generated in this situation. The information about the underflow event is encoded in the 4 bits allocated for trigger information (refer Table 5.3). During the time the reset signal and the header data are transmitted 2×4 samples are written in the ring buffer. Now, enough noise samples are available that can be compressed into 1 packet.

6. After checking for ring buffer underflow, above mentioned step 1 and step 2 are repeated. Based on the decision, data samples or compressed noise samples are transmitted and the corresponding read pointer incrementation is performed.

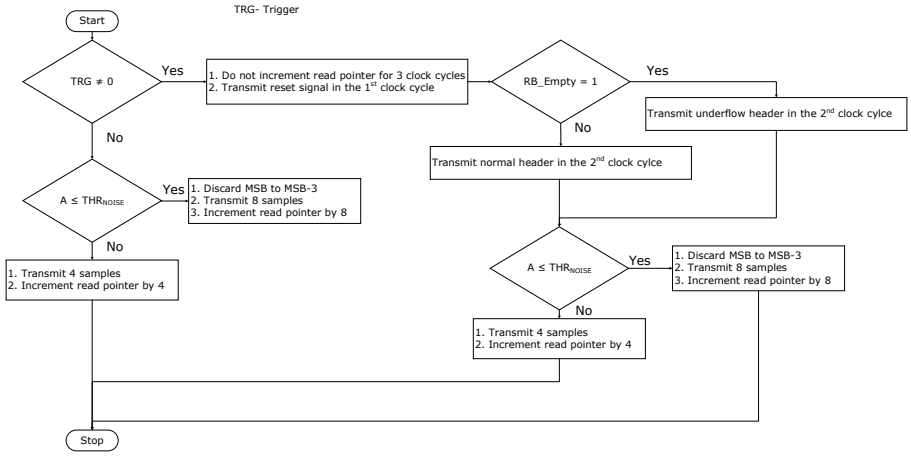


Figure 5.15: Flow chart for header selection and noise compression in PAM.

5.4 Double Data Rate

At the output of the data processor (PAM), 32-bit data packets are generated every 4 ns. The Vulcan chip uses LVDS lines for transmission of data outside the chip. The LVDS lines are operated at 500 MHz, so for compatibility, the output data from PAM is split into two 16-bit wide packets and that are then transmitted at 500 MHz by the double data rate block.

The data rate changes between the sub-modules are presented in Figure 5.1. The simulation plots and silicon measurement results of the data processor are presented in chapter 7.

5.5 Summary

A custom data process designed for Vulcan adhering the specification was implemented in VHDL. Figure 5.16 illustrates the function of the data processor. In the top plot, exemplary signals with different magnitude are generated and sent to the Vulcan chip. The data format corresponding to the signal is presented as a digital value below the plot.

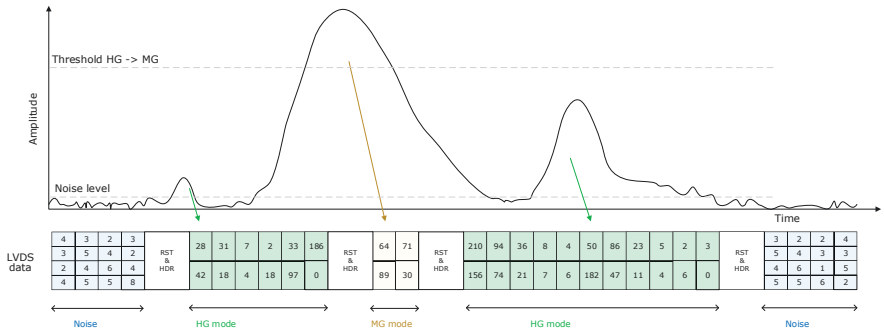


Figure 5.16: Illustration of mode selection in PAM. Disclaimer: The plot and data stream are not to scale.

Initially, the signal lies below the noise level, the noise samples are truncated and 16 samples are transmitted instead of 8. When the signal crosses the noise threshold a trigger signal is generated indicating a mode change from noise to ADC HG. As a result, a reset signal and header information are transmitted before sending data samples corresponding to ADC HG bus mode (marked in green).

When the signal amplitude crosses the upper threshold of the ADC HG, the bus mode is again changed from ADC HG to ADC MG, resulting in the transmission of a reset signal and header information followed by data samples from ADC MG. As the signal decays the bus mode is changed back to ADC HG and later to noise mode. In this exemplary plot, the hysteresis counter for ADC MG to ADC HG was set to zero hence the immediate switch over to ADC HG.

System Integration of Vulcan's Digital Circuits

6

At the RTL level of the top-down design flow as discussed in Section 4.1, the behavior of the components and their interconnections are described in VHDL. After functional verification of the VHDL code using test benches and assembly of the top level of the design, the code is converted to an intermediate boolean expression matching the behavioral description. Based on the technology and the standard cells available in the technology chosen for the project (CMOS 65 nm) the EDA tool replaces the mathematical expression with its equivalent logic gates and registers. The connections between the components are also established at this point. The translation process of the VHDL code to a netlist is called synthesis [45], [23]. During the synthesis process, the EDA tool checks if the design meets the specified timing constraints. On meeting timing requirements, optimization can be performed to improve the performance (i.e resizing the buffers).

IP blocks, hard macro and soft macro are inserted in the design during the synthesis process. The synthesis models for hard macros which include the timing and area information are provided along with the RTL description of the design. The JTAG tap controller used in the Vulcan chip was inserted at this phase of the design process. Timing verification has to be performed after the inclusion of macros and design for test structures as their insertion influences the length of the wires used for routing. The additional routing consumes space and increases congestion. The design for test structure, used in Vulcan, a scan chain, was also included during the synthesis. During scan chain insertion, the standard flip-flops are replaced with scan flip-flops (flip-flop and multiplexer). The requirement to connect all the flip-flops in the scan chain significantly increases the area of the design. Once all the test structures are in place a final timing analysis is performed to verify the timing. An Automatic Test Pattern Generation (ATPG) tool can then be used to generate scan test vectors for the chip.

The synthesis phase is followed by the place and route phase. As an initial step, the floor plan of the chip is prepared [46]. Dedicated regions are allocated for the blocks after assessment of various factors such as the power domain and proximity to the pin. Efficient floor planning is required as larger die sizes will increase the cost and tighter floor planning will result in congestion during routing leading to timing violation. The power grid for supply and ground is laid, followed by the proper placement of the I/O pins and bond pads. Once the floor plan

is prepared, the standard cells (with area information) can be placed in the designated areas. The placement is followed by routing which decides the exact layout of the wires needed to connect the placed components, power rails and clock lines [23].

After routing, the design is checked for its adherence to design rules of the manufacturing process called Design Rule Check (DRC). In addition, a Layout Versus Schematic (LVS) check is performed to guarantee that the generated layout matches the functionality of the schematic. After these verifications, the design is exported to GDSII, which is an industry standard database format for IC layout [47]. The exported file will contain the information of the actual polygons and layers that are necessary for manufacturing [48]. In this chapter, the need to include scan chain in Vulcan chip, implementation details and test pattern generation are discussed in detail. Additionally, the configuration setup used in Vulcan is also described.

6.1 Faults

In this section the need to include design for test structures for integrated circuits designed in sub-micron CMOS technology is presented. A brief introduction to faults and the fault models used to detect faults are also presented in this section.

6.1.1 Terminology and Introduction

"Defects" are unintended differences between the implemented hardware and its intended design. In some cases, defects might create a system failure. A "Fault" is a representation of a defect at the functional level. In short, defects are imperfections in hardware and faults are imperfections in function. An "error" is a manifestation of a fault that results in incorrect circuit or system outputs or states. A "failure" is a deviation of a circuit or system from its specified behavior. In summary, defects cause faults, faults leads to errors, which might lead to failures [49], [50].

Some examples of processing defects are missing contact windows and oxide breakdown. Some material defects are cracks and surface impurities causing ion migration. Exemplary time-dependent defects are dielectric breakdown, electron migration and contact degradation [51], [49].

Physical defects introduced during fabrication or packaging of an individual Application-Specific Integrated Circuit (ASIC) leads to a logical malfunction. Some examples of such physical defects are open circuits, short circuits, CMOS transistor stuck-open, short, resistive bridging, leaky transistors, partially conducting transistors and resistive contacts [49].

In addition to these, there are faults that might affect the functional operation of the circuit only when the circuit is operated at the required frequency. By reducing the frequency of operation the circuit might produce correct results. These faults are classified as delay and transition faults. These faults are mostly generated due to poorly filled vias and manufacturing errors (i.e. etching process removes or adds material which causes the resistance of the transition line).

6.1.2 Fault Models

As a preliminary step to detect the faults that can occur in a digital integrated circuit, fault models are developed. The circuit of interest is modeled to facilitate its analysis and simulation while preserving its logical function (build model stage of ATPG) [52]. The reason to develop a fault model is due to the low coverage I/O function test of complex designs. Real defects are numerous and often not analyzable.

A fault model abstracts the defects at the logic gate level and models the impact of the different type of physical effects which can occur on silicon. Corresponding to the type of fault which is targeted, different types of fault models are used. Commonly used fault models and their description are presented below.

Stuck at faults: For counteraction of the large magnitude of physical failures affecting the circuit components, many of them can be modeled as a set of logic lines permanently stuck at the value 0 or 1 at the gate level. "Stuck at faults" are faults on a boolean level of logic's functional implementation. "stuck at zero (s-a-0)" does not always mean the line is grounded and "stuck at one (s-a-1)" does not always mean the line is shorted to VDD. Stuck at faults can occur both at the input and output of a logic gate. Some of the faults manifest by setting the logic line permanently to a constant value [53].

As a rule of thumb, one can say that

- s-a-0 and stuck at one (s-a-1) are tested on all primary outputs.
- s-a-0 is tested on OR and NOR gate.
- s-a-1 is tested on AND and NAND gate.
- s-a-0 and s-a-1 are tested on XOR and XNOR gates.

Multiple stuck at faults: These faults categorize several single stuck at faults that occur at the same time. Due to the complexity of the circuits, it is also necessary to test for multiple stuck at faults. Equivalent fault models are used for testing instead of using set of all multiple faults.

Bridging fault: Faults that occur when there is a short between adjacent nets fall under this category. There are two types of bridging faults. The is input bridging, where two inputs can bridge together and form a wired logic (AND), and is the feedback bridging, where the input and output can short together and can introduce a feedback possibly leading to oscillations or latching.

Stuck open: These faults are used to model the transistor level properties. Two types of faults can be modeled. First is the stuck open fault where a single transistor is permanently stuck in open state. Second is the stuck on fault where a single transistor is permanently shorted irrespective of its gate voltage. The detection of a stuck on fault requires the measurement of the quiescent current (IDDQ). When transistors are stuck for a longer duration in between

logic 1 and logic 0 they tend to sink a relatively large amount of supply current, The fault that causes the transistors to use excessive currents are classified as IDDQ faults.

Transition delay fault: A gate output may be slow to rise or slow to fall. When this delay time is longer than a predefined level it is a called transition delay fault.

Delay fault: These faults occur when a propagation delay along a path falls outside the desired limits. Two types of delay faults can occur: path delay faults and gate delay faults. A delay defect is a physical manufacturing problem which slows down the propagation of a logical data value's transition from logic 0 to logic 1, or vice versa. Due to these faults, the time usually spent in the switching zone between logic 0 and logic 1 increases. In this switching zone, the device will consume relatively more power. For this reason, IDDQ testing was adequate to locate delay faults in older technologies. However, with current technologies, the background power consumption and leakage current is high. Stand alone IDDQ test is not sufficient to diagnose delay faults. Due to the above mentioned factors, a different method of testing is used for delay faults [50], [49].

6.2 The Testing Process

The Figure 6.1 shows the primary steps involved in the testing preparation. Even though the fault modeling and the test pattern generation are handled by the EDA tool, some examples of this process are explained in this section to give an impression about the process. A fault model among the list (refer Section 6.1.2) is chosen. After the fault model is developed for the circuit under test, the test coverage (i.e. the percentage of the circuit which can be tested) can be obtained. The test coverage is dependent on the availability of fault propagation paths without conflicts. Following that, test patterns are generated to test the circuit for the fault. Once the test pattern is generated, the patterns are simulated with the faults.

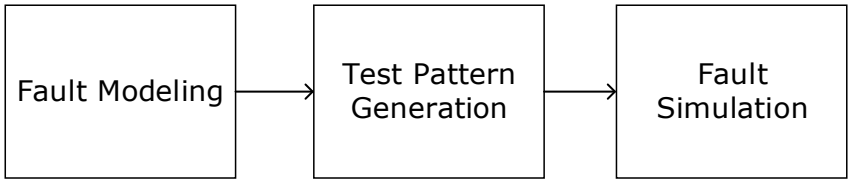


Figure 6.1: Major steps in the test process.

6.2.1 Examples Test Pattern Generation

For the generation of tests for digital circuits, the testing tool is provided with a circuit description in form of a netlist. Figure 6.2 shows a simple demonstration of the faults generated when one of the inputs to the AND gate is s-a-0 and when one of the inputs to the OR gate is s-a-1.

For generating a fault model for the AND gate, the steps below are followed

- The input to "net b" is set to 1. This allows the value at "net a" to propagate to c.
- Input at "net a" is set to 1, now the value at "net c" is checked.
- c=1 indicates the circuit is good while c=0 indicates a bad circuit.

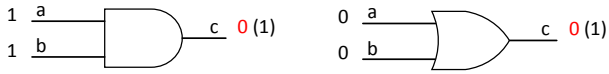
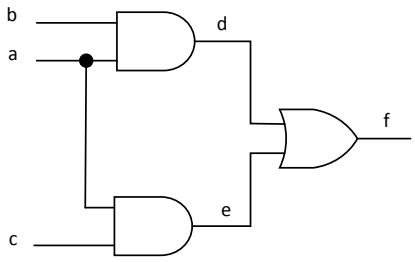


Figure 6.2: Example of patterns for testing stuck at faults. A logic value that is complementary to the polarity of the fault being tested is assigned. [Left] For the inputs a=1 and b=1, an AND gate should generate an output c=1. If one of the input lines of the AND gate is stuck at 0 then it would result in a faulty output of c=0. [Right] Similar to the AND gate, inputs a=0 and b=0 are provided to the OR gate, an error-free logic will create c=0, on the other hand, if any of the input lines is stuck at 1 and faulty output of c=1 will be observed.

Figure 6.3 shows another example of test pattern generation. In this example, a test pattern to test if the "net d" is s-a-0 is obtained from the truth table of the circuit. For the input a=1, b=1 and c=0 the output f is dependent on the value at the "net d" and the inputs a and b. This test vector is applied to the inputs and the output f is observed. If f=1, it passes the test else if f=0, then the net d is s-a-0.



Inputs	Output	
abc	f	f'
000	0	0
001	0	0
010	0	0
011	0	0
100	0	0
101	1	1
110	1	0
111	1	1

Figure 6.3: Generation of stuck at 0 for the "net d" using the truth table. "f" is the correct output and "f'" is the faulty output when the net d is s-a-0. The test vector which produces complementary values for "f" and "f'" is selected for testing.

6.2.2 Fault Propagation

Another key factor for testing is the necessity that the fault must be propagated to the point where it can be observed. The idea of fault excitation and fault propagation can be understood from the following examples (Figure 6.4 and 6.5). Fault excitation is the process of providing

appropriate input patterns to the logic which would cause the logic to arrive at the state (fault will manifest itself) appropriate for testing. For example, if an AND gate has to be tested for s-a-0, then both its inputs have to be set at logic high which should produce a logic high for a fault-free circuit and a faulty circuit will produce a logic low, thereby preparing the circuit to the condition to check for the error.

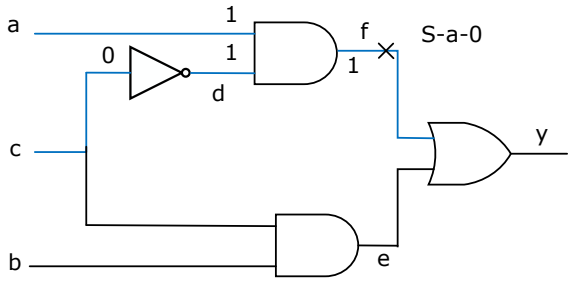


Figure 6.4: Illustration of fault excitation in a circuit.

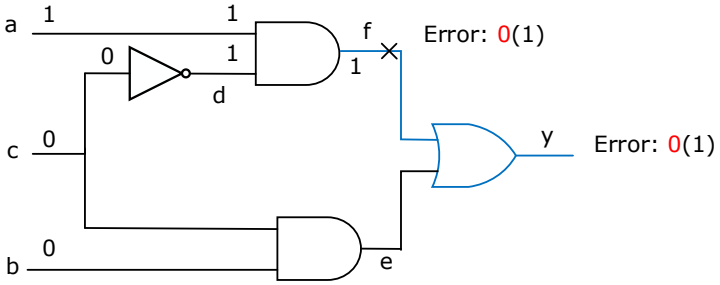


Figure 6.5: Fault propagation. A path from the site of the fault to the output of the circuit is selected. The selected path is sensitized by assigning non-controlling values to the inputs along the path so as to propagate the effect of the fault [49].

In Figure 6.4, the "net f" has to be tested for s-a-0. By feeding a=1 and c=0, the net f will be at a logic high for a fault-free circuit. For a faulty circuit, the output will be at logic low, thereby s-a-0 can be tested for this net if the inputs are excited with this value.

Now the fault at the "net f" has to propagate to the point where it can be observed. In the chosen example, the output "y" is observable. For the fault at "f" to propagate till "y" the input at the "net b" has to be appropriately selected. In Figure 6.5, the input to b is selected to be logic low so that the output "y" is dependent of the "net f" and independent of "net e". For the test pattern a=1, b=0, c=0 a logic low at the output "y" is caused by s-a-0 at "net f".

The example provided in this section are simple logic circuits and test patterns can be generated by hand, while current digital designs contain millions of logic gates and generating test vectors for fault excitation and fault propagation is impossible by hand. Among the several algorithms used for generating test patterns, the D-algorithm explained in [49] provides a primer for the steps involved in test pattern generation. The excitation of delay defects and transition defects are different compared to the remaining defects explained in Section 6.1.2. The method of excitation for the delay defects is illustrated in Figure 6.8.

6.3 Design for Test - Scan Chain

Testing combinatorial circuits are relatively easy compared to the sequential circuit. Sequential circuits contain memory elements (i.e. flip-flops) and testing them requires initialization. Initialization of all flip-flops through the primary input pins is not feasible. In order to test the sequential logic and increase the testability of the design on silicon, special design structures are introduced. These special design techniques to increase the testability of the design are collectively called as DFT [53].

Among the various DFT techniques, a scan chain is implemented in the Vulcan chip. The implemented scan chain was used to feed in the test vectors generated by the EDA tool. The basic concept of the scan chain and the key features are described in this section.

6.3.1 Scan Chain

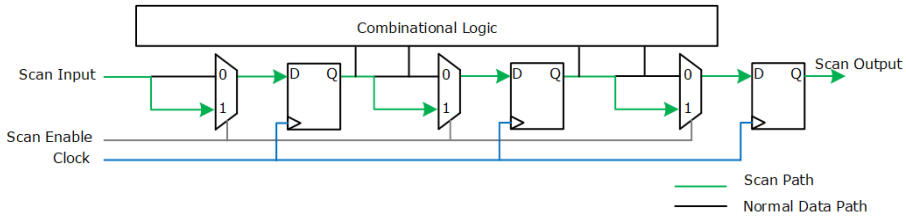


Figure 6.6: Illustration of scan chain concept.

A scan chain addresses the difficulty of testing sequential circuits by replacing all flip-flops in the design by scan flip-flops. Generally, scan flip-flops contain a flip-flop and a multiplexer added to the input of the flip-flop. By the use of a select signal, one of the two inputs to the multiplexer is fed to flip-flop.

Controllability: Controllability in DFT is defined as the ability, for the a test equipment to establish a 0 or 1 value on an internal node, by applying values to the primary input ports/scan chain inputs. The controllability of the design has a direct impact on the testability of the design. When a scan chain is reported as controllable, it indicates the ability to activate faults in the circuit and to detect them.

Observability: Observability is defined as the ability, a test equipment can propagate a fault effect (1/0 or 0/1) to a primary output, by applying values to primary inputs.

Figure 6.6 presents the concept of the scan chain. The flip-flops are replaced with scan flip-flops which have multiplexer for selection between two inputs. The flip-flops are connected in a chain forming a long shift register. By setting the scan enable signal to 1, test vectors can be fed through all the scan flip-flops and by appropriately setting the shift enable (scan enable) signal the output of the flip-flops can be captured and transmitted at the output of the scan chain. Therefore flip-flops can be initialized and also observed by using scan chain.

6.3.2 Waveforms of Scan Chains for Stuck at Faults

For the "stuck at fault" test the test patterns are fed in serially. Figure 6.7 shows the waveform of the signals at the pins scan clock, scan enable, scan input and scan output. The "scan enable" signal is pulled high for the duration of shifting the test pattern into the scan chain. When the entire pattern is shifted in the scan chain, the scan clock is stopped and the scan enable signal is pulled low causing the test patterns to be captured by the flip-flops and propagated to the combinatorial logic. After the capture phase, the results from the logic circuits is ready to be observed at the output.

As it can be observed in the figure, the output vector for the scan chain integrity test is a copied version of the input vector due to the first in first out setup of the scan chain. The output vector is compared with the input vector. Any mismatch in the values indicate a logical error and by matching with the location of the mismatch, the location of the error can be calculated. Figure 6.9 shows the error caused by s-a-1, based on the output the location and type of the error can be determined. Table 6.1 gives a list of possible output for the faults for a given input vector.

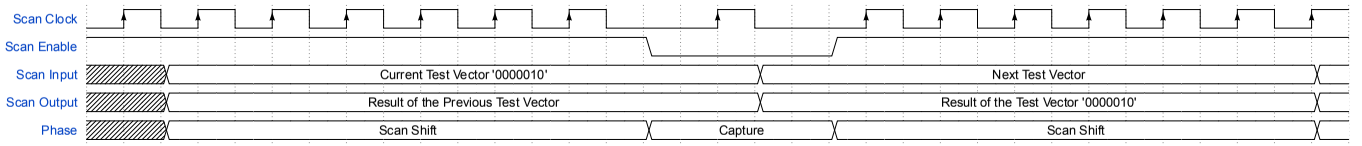


Figure 6.7: Waveform for testing scan chain test and logic test.

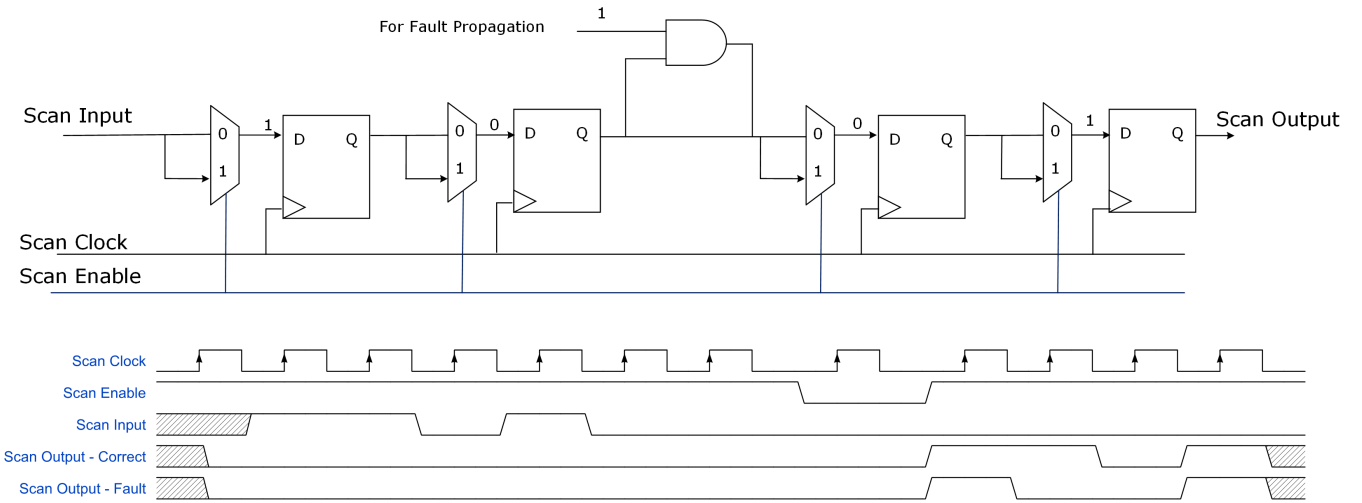


Figure 6.8: Waveform for testing transition and delay faults.

6.3.2.1 Test Pattern Simulation

An illustration of shifting in test vectors through a scan chain and exemplary output patterns are shown in Figure 6.9. This specific example illustrates the testing of the flip-flops in the scan chain before testing the combinatorial logic connected to the flip-flops. The first row shows the results of an error-free circuit, the second row shows an exemplary result when one of the logic is stuck at 1 and the third row shows the logic having hold time violations resulting in errors at the output. The output pattern marked in red indicates the mismatch of the vectors and thereby the fault in the logic [54], [55].

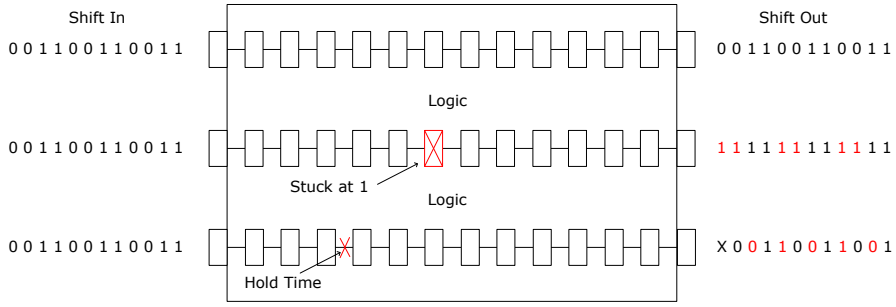


Figure 6.9: An exemplary test pattern fed through a scan chain in faulty and non-faulty logic [54].

6.3.2.2 Determination of the Type of Faults

The output patterns that can be used for detecting the types of faults based on the value observed at the output is shown in Table 6.1. Deviations (slower or faster) in rise and fall times of the signals lead to setup and hold time violation resulting in faulty signals being captured. The first row in the table shows the expected result when the logic is fault free. Output patterns for various faults are listed in the table. By comparing the output data stream (refer shifted out data stream in Figure 6.9) with the reference values in the table, the type of fault can be identified.

Table 6.1: A reference table for fault type recognition. Error bits are color coded in red [55].

Shift Out	Fault Types
0011 0011 0011	No fault
0010 0010 0010	Slow rise
0111 0111 0111	Slow fall
0110 0110 0110	Slow
1011 1011 1011	Fast rise
0001 0001 0001	Fast fall
1001 1001 1001	Fast (hold time)
0000 0000 0000	Stuck at 0
1111 1111 1111	Stuck at 1

6.3.3 Waveforms of Scan Chain for Transition Faults

The simulations of delay faults and transition faults are different from stuck at faults and bridging faults. For the creation of a test for transition faults, both the start (initial) and end (final) of the transition has to be propagated to the fault site. For example, to check a rise transition fault, a logic 0 has to be transmitted following a logic 1.

Launch cycle: The clock cycles during which the initial value is transitioned to the final value are called as launch cycles.

Capture cycle: The clock cycles during which the test vectors are captured by the flip-flop (scan enable is pulled low) are called capture cycles.

"Launch on capture" and "launch on shift" methods can be used to achieve this transition through the scan chain. Figure 6.8 demonstrates the launch of the shift method for a fall transition fault. As a first step, a logic 1 (initial value) has to launched to the fault location. This is done by sending the vector "1**1**01" where the highlighted vector corresponds to the initial value. The test vector has been generated such that the final state (logic 0) can be obtained as the output of combinatorial logic that feeds to the input of the flip. For the final value to propagate, the scan enable signal is pulled low which causes the flip-flops to be captured with the test vector and the combinatorial logic produces corresponding output. When the scan enable is pulled high, the final state (logic 0) is fed to the location to test for fault.

The last two waveforms show the result for error-free and faulty circuits. For an error-free circuit, the output is calculated to be "1001" while for a faulty circuit due to delay the output is observed to be "1101". The flip in the bit is caused due to the fault in transition.

6.3.4 Test Pattern Generation Using EDA Tool

The following steps are performed by the EDA tool during the test pattern generation process. The flow chart of the process, input and outputs from the test pattern generation are shown in Figure 6.10.

Step 1: During the "build model" phase the Encounter test tool reads the design netlist and technology libraries and translates it into a model that can be used by the tool [52].

Step 2: At the "build test mode" phase, the tools attempts to identify the test structures (scan chain in case of Vulcan). After identification of the test structure, the tool generates the test configuration for the design. For instance, the tool identifies the scan in, scan out, test mode, shift enable (scan enable) pins and assigns test functions for these pins. At this stage, the tool also reports the percentage of the logic that can be observable and the scan chain present in the design and the controllability and observability of the scan chain. The logic has to be both observable and controllable, otherwise, the tool cannot test the logic.

Step 3: During "verify test structures" stage, potential issues and conflicts in the operation of the scan chain are tested.

Step 4: At "build fault model", the model of the circuit for the selected fault model is generated. Usually, the same fault model is used for stuck at fault, bridge test and IDDQ test and a different

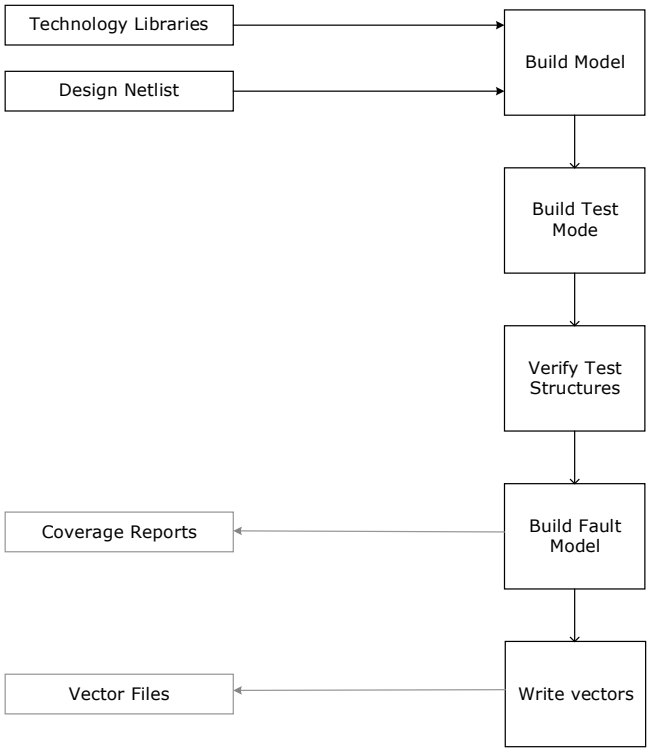


Figure 6.10: Major steps in the test pattern generation using the Cadence tool chain [52].

model is used for delay faults. After completion of the fault model, the tool generates test vectors. After the generation of test vectors, the tool runs a preliminary test to calculate the total test coverage which is the ratio of the number of tested faults to the total number of possible faults. As a rule of thumb, a coverage of more than 95% is recommended [56].

Step 5: If the test coverage is perceived adequate by the developer, test vectors are converted into a data format suitable for simulation and the tester equipment (i.e. the Standard Test Interface Language (STIL)).

As a final test in the testing process (refer Figure 6.1), the test vectors generated and the design are simulated through a test bench. Since the simulation does not include manufacturing defects, there should not be any mismatch in the result during the simulation.

6.4 Scan Chain Architecture in Vulcan

Owing to the numerous advantage, the design for test structure scan chain was included in the digital control unit of Vulcan chip. The Figure 6.11 illustrates the pads used for controlling the scan chain. The input, output and clock pins of the scan chain are shared with the JTAG macro. In addition to the input, output, enable and clock signal of the scan chain an additional pin (test mode) was added to fix the DFT violations. The shift enable signal and test mode signal are set high during scan chain test. Due to the limited availability of pins, only one scan chain is introduced in Vulcan.

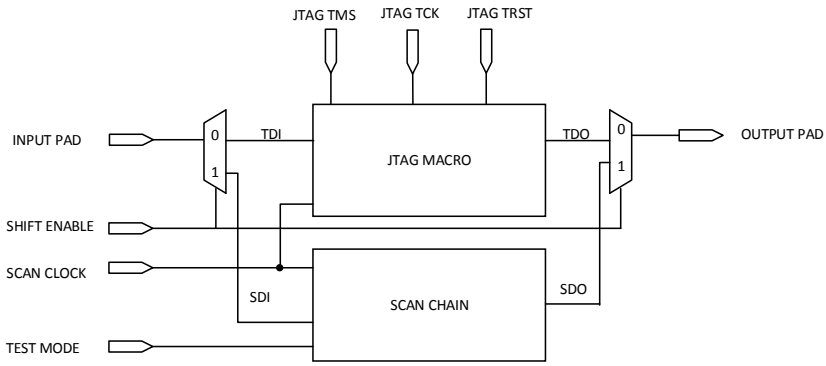


Figure 6.11: Scan chain connections.

6.5 Scan Chain Results

Synthesis: In the process of introducing a scan chain in the design, the normal flip-flops in the design have to be converted to scan flip-flops and connected serially between the scan input pin and scan output pin forming a long shift register. Each scan chain requires one dedicated test mode signal. The Table 6.2 lists the synthesis result after successful scan chain insertion [57]. The figure shows that one scan chain has been successfully configured between the JTAGTDI (input) and JTAGTDO (output) pads. The JTAG macro and scan chain share input and output pads in Vulcan.

Placement: Once the scan chain is successfully connected, the design was be placed and routed. The introduction of scan chain increases the area of the design and the length of nets connecting the logic [58]. Although the increase in area due to scan chain insertion cannot be avoided, the increase in net length can be reduced by reordering the flip-flops of the scan chain during placement and routing. This optimization was performed in the Vulcan chip.

Pattern generation: After the placement and routing of the design, a test pattern generator tool (Cadence Encounter Test) was used to generate test vectors specific for the design. The tool follows the steps described in Section 6.3.4 and Figure 6.10. During the pattern generation

Table 6.2: Synthesis result of the scan chain insertion in the digital design.

Configuring 1 chain for 25371 scan f/f Domain "TEST CLK" -(rise): 25369, (fall):2 Clock "TEST CLK" -(pin "JTAGTCK") -(rise): 25369, (fall):2 Default shift enable signal is "SHIFT EN"
Connecting scan chain "scan chain1" with 25371 flip-flop using default shift enable Connecting SDI to pin JTAGTDI Inserting mux for sharing functional output with SDO (select signal: SHIFT EN) Connecting SDO to pin JTAGTDO

Table 6.3: Test coverage of the scan chain reported by the Automatic test pattern generator tool. Here, TCov is the total coverage and ATCov is the adjusted test coverage which is calculated by excluding the redundant faults.

# Faults	# Tested	# Redundant	# Untested	% TCov	% ATCov
1,671,456	1,521,231	9,614	3214	91.04	91.54

Table 6.4: Simulation result of the scan chain with test pattern generated by the ATPG tool .

Number of good comparing vectors generated for the logic test: 16510194 Number of miscomparing vectors generated for the logic test: 0 Number of good comparing vectors generated for the scan test: 25373 Number of miscomparing vectors generated for the scan test: 0
Total number of good comparing vectors: 16535567 Total number of miscomparing vectors generated: 0

process, the tool estimates the test coverage of the design for the generated patterns. Table 6.3, shows the coverage result of the scan chain introduced in Vulcan.

The allocated "L shaped area" for the digital circuits in the Vulcan chip limits the placement area of the logic such that it met the timing constraints. The introduction of a scan chain increases the area of the digital circuits. A compromise in the test coverage of the scan chain was made in order to meet the timing constraints. Even though a test coverage above 95% is preferred, a conscious decision to exclude certain blocks from the scan chain was made.

A memory built-in self-test module was included to facilitate testing of the blocks that are excluded from the scan chain. The Table 6.3 shows the number of the faults detected using the scan chain, possible faults that can be tested. The higher the number of faults that can be tested is, the higher is the test coverage of the design. **Simulation:** The placed design was simulated using a test bench, with the test vector generated by the pattern generator tool. The simulation results are shown in Table 6.4. Since the simulation is performed for the ideal design, the output generated at the scan chain must match the input. On 100% compliance, no mismatch warnings are issued. The same procedure was performed for logic test, IDDQ test and at speed test.

Table 6.2 validates the proper connectivity and implementation of the scan chain. The scan chain was successfully implemented in the design and details are presented in the Table 6.4.

6.6 Area and Timing of the Digital Control Unit

The capability of the circuit to attain its functionality at the specified frequency of operation is a key verification parameter. Data gets corrupted if the setup and hold timing are not sufficient for the proper sampling of data. Before the design can be submitted for fabrication it is very critical for the design to be free from setup and hold timing violations [59]. Figure 6.12 and 6.13 shows the summary of the timing analysis. The green bars in the histogram indicate that all paths pass the timing constraints provided during synthesis.

The total silicon area of the Vulcan chip is 22.09 mm^2. A short summary of the area occupied by the digital circuit, the data processor and the baseline regulator are listed below. A considerable area (58%) of the data processor is occupied by the internal ring buffer included.

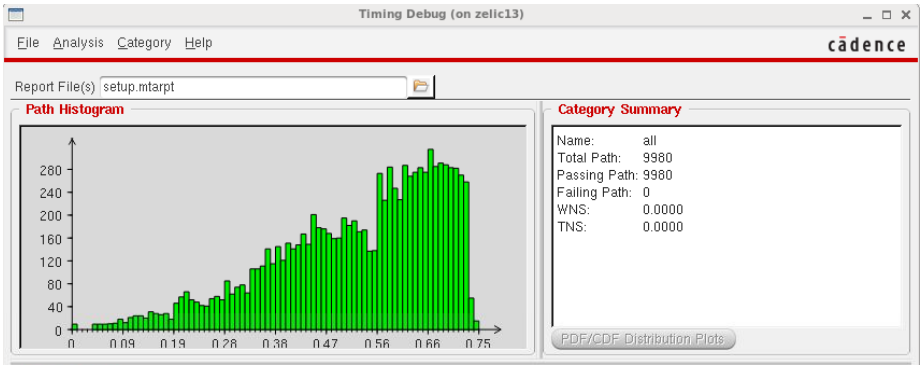


Figure 6.12: Setup timing graph.

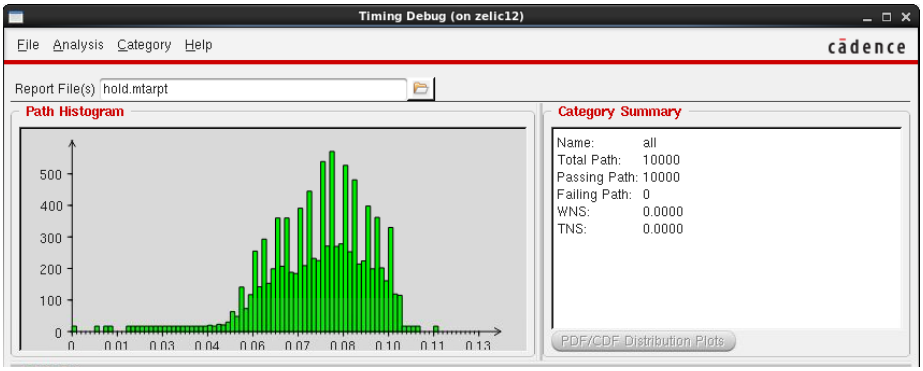


Figure 6.13: Hold timing graph.

Table 6.5: Area table for comparison of area the ring buffer consumes.

Instance	Cells	Cell Area	Net Area	Total Area (nm)
VULCAN top	354700	38353928	919648	39273577
Digital top	354407	1269764	888708	2158472
PAM	229602	737520	525203	1262723
Ring buffer readout block	226639	726086	518136	1244222
ADC regulator	496	1971	1180	3151

6.7 Summary

A design for test structure scan chain was successfully implemented in the Vulcan chip and verified using the generated test patterns. The test patterns were successfully converted to a format suitable for automatic testing equipment. Since scan chain was implemented for the first time in Electronic Systems (ZEA-2), the unfamiliarity posed several challenges in the implementation and verification process. Nevertheless, the simulated results presented in the section above validates the correctness of the implementation. Figure 6.14 shows the layout of the Vulcan chip submitted for fabrication and the packaged chips which are mounted on the test board for verification.

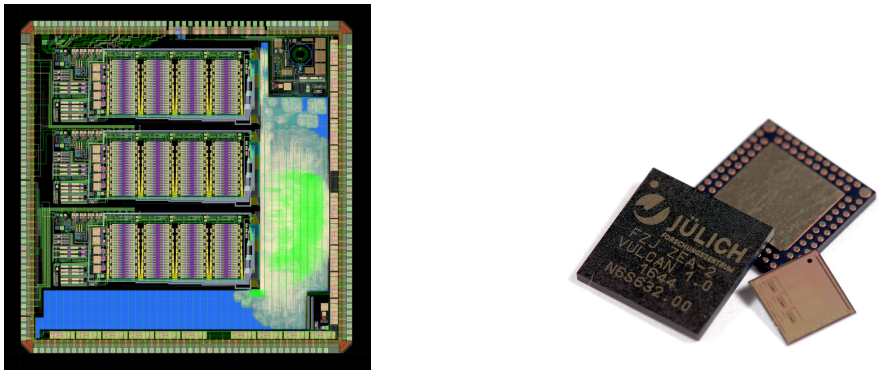


Figure 6.14: [Left] Layout of the Vulcan chip sent for fabrication. [Right] Bare die and packaged chips after fabrication.

7 System Validation

Verification is defined as the process of checking the functionality of the model at the design level using test benches. Testing is defined as the process of checking the functionality of the product at the wafer level [46]. Verification and testing are two critical and time-consuming processes in the development cycle of an integrated circuit design. Early identification of the bugs during the verification process reduces the risk of a redesign. Two prototypes of the Vulcan chip were fabricated, packaged and tested in the ZEA-2 laboratory.

Extensive testing was called out to measure the performance of the SoC and its adherence to the required specification, thereby validating the system. Crucial verification results and measurement results of the data processor and the ADC baseline regulator are selected and presented in this chapter.

7.1 Pre-Silicon Verification of the Data Processor

The data processor was implemented as VHDL code and the system was simulated along with the test benches. Critical simulation results of the sub-blocks such as proper selection of the data source, noise compression, trigger and data formatting are presented in this section.

7.1.1 ADC Analyzer

The ADC analyzer was developed based on the flow chart shown in Chapter 5, Figure 5.5. The developed ADC analyzer was verified using VHDL test benches in an HDL simulation environment (ModelSim). The simulation results should demonstrate that the ADC analyzer complies with the switching pattern as described in the flow chart mentioned above. Figure 7.1 shows the simulation results of the implemented ADC analyzer.

In this example, the noise threshold is set at 9 (8'h09), the upper thresholds of ADC HG and ADC MG at 252 (8'hFC). Until the ADC HG data is less than the noise threshold, the noise bus mode is selected and ADC HG data is transmitted. When the ADC HG data is greater than the noise threshold, the bus mode is changed to high gain. On crossing the upper threshold of ADC HG, the data is selected from the ADC MG and bus mode code is changed from 2 (4'h2) to 3 (4'h3). Similarly, on crossing the upper threshold of ADC MG, the data source is changed from

ADC MG to ADC LG. From the simulation results, the functionality of the ADC analyzer was verified.

In Figure 7.1 the first three buses are the output of the three ADCs with different gain. Samples from ADC HG are highlighted in green, ADC MG are highlighted in blue and ADC LG are highlighted in orange. The last two buses are the output from the ADC analyzer. The first one indicates the bus mode of the data and the second displays the sample selected from one of the three ADCs. The values of the samples are represented in hexadecimal notation for compactness.

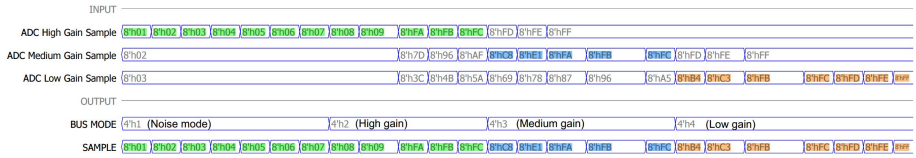


Figure 7.1: A simulation result of the ADC analyzer demonstrating switching of ADC source based on the specification.

7.1.2 Noise Compression

Figure 7.2 shows the simulation results demonstrating the truncation of samples in noise mode. During noise mode, samples are compressed to half their width. Due to this compression, data can be transmitted at twice the data rate. This effect was verified through simulations.

The four buses in Figure 7.2 represents the four samples from the ADC every 4 ns. The clock signal is added for time reference. The last bus shows the output of the data processor in 32-bit packets.

Since the generated samples are below the noise level, 8 samples can be transmitted instead of 4 samples. The header of the first noise sample is highlighted in green and the noise samples are underlined in magenta. The data processor transmits a reset signal, in the following clock cycle, the highlighted header information is transmitted. Finally, the noise samples are compressed and transmitted. The compressed noise samples are also highlighted at the output bus.

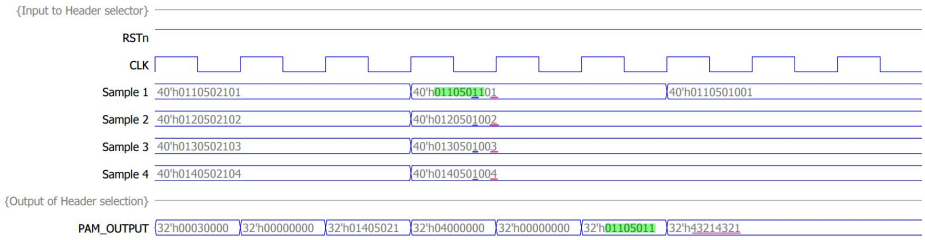


Figure 7.2: Simulation results demonstrating the truncation of samples in noise mode.

7.1.3 Trigger and Data Formatting of the Data Processor

A simulation result demonstrating the response of the data processor reacting to triggers is presented in Figure 7.3. Internal triggers are occurring at sample 3 during the second rising edge of the clock and at sample 1 on the seventh rising edge of the clock. The corresponding change at the output bus can be noticed at the 5^{th} and 9^{th} rising edge of the clock. The header of the trigger events are color coded for identification.

The four buses in Figure 7.3 represent the four samples read from the ring buffer. The clock signal is added for time reference. The last bus in the simulation is the output of the data processor. The samples are 40 bit wide and are composed of 32-bit header information and 8-bit data sample. The samples where a trigger signal has occurred are highlighted.

The first trigger occurs at sample 3 and is highlighted in orange. Once a trigger signal is generated the data samples before the trigger signal are transmitted (32'h 00000605). After the reset signal, the header of the trigger sample is transmitted. Notice the highlighted (orange) header data at the output bus. A second trigger signal occurs at sample 1 highlighted in green. Similar to the previous trigger signal the output data format is modified and the header of the sample with the trigger is transmitted and can be observed in the output bus (highlighted in green).

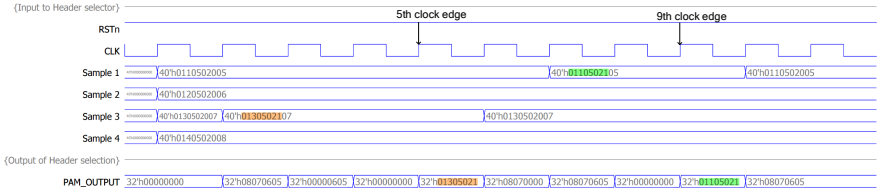


Figure 7.3: Simulation result showing the data format change in response to the generated trigger signal.

7.1.4 Underflow

As mentioned in Section 5.3.2, underflow is defined as the state when the number of samples required for transmission is more than the number of samples available in the ring buffer. This scenario is likely to occur when the data processor stays in noise mode for a longer duration. Figure 7.4 shows the simulation results demonstrating, the generation of underflow flags.

The four buses transmitting 4 samples from the ring buffer are shown in the input section and the data output and underflow flags are shown in the output section of the simulation. When an underflow event is detected, the data format is changed similar to that of a trigger event with one modification in the header data. The code of the trigger signal is overwritten with the code for an underflow event. The sample at which the underflow is detected and the corresponding header signal at the output are highlighted in green. During the time the reset signal and the header data are transmitted, 2 × 4 samples are written in the ring buffer, resulting in enough noise samples that can be compressed into one 8-bit packet.

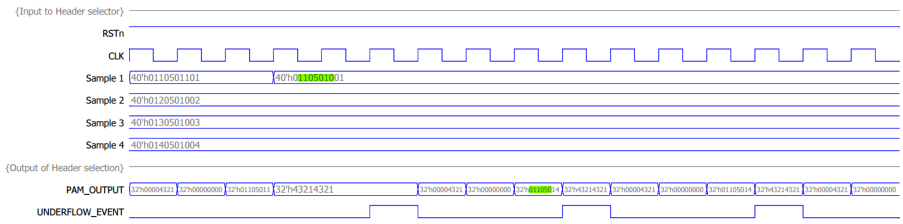


Figure 7.4: Simulation results demonstrating underflow event detection and the corresponding change in the output data format.

7.2 Laboratory setup

For the testing of the digital circuits, instruments such as logic analyzers, function generators (refer Section B.1), power supplies and clock signal generators were used. A short summary of the equipment and their functions are described below.

- A logic analyzer (Keysight U4154A) was used to display the output of the digital circuits. Logic analyzers are essentially digital oscilloscopes designed to handle high data streams.
- A signal generator (Rhode Schwarz SMB100A) was used to produce clean sine waveforms. It can only produce sine waveforms of high frequency, the Vulcan chip was supplied with 500 MHz.
- An arbitrary waveform generator (Keysight 33600A) was used for the TIA input pulse. A measured signal from the PMT prototype was programmed into the function generator. Ordinary function generator produces sine, square and triangle waveforms and the waveforms are limited to 100-150 MHz depending upon the type of waveform being selected. Arbitrary waveform generators provide the possibility to program waveforms with relatively high sampling frequencies (i.e. 500 MHz).

Figure 7.5 shows the test board used for the measurement of the Vulcan chip. Analog input ports[1], power supplies, reference clock, JTAG connectors are marked in the figure. The output of the Vulcan chip is extracted via the LVDS line (16 data lines, 3 trigger lines and 1 clock line). This is a reduced setup suited for digital circuit test, therefore the analog input lines are kept open.

7.2.1 Order of Testing

The general testing procedure for the Vulcan chip is performed in the following order.

1. The configuration of the internal registers to activate the appropriate sub-modules.

[1]This also includes the ports used for testing the analog blocks

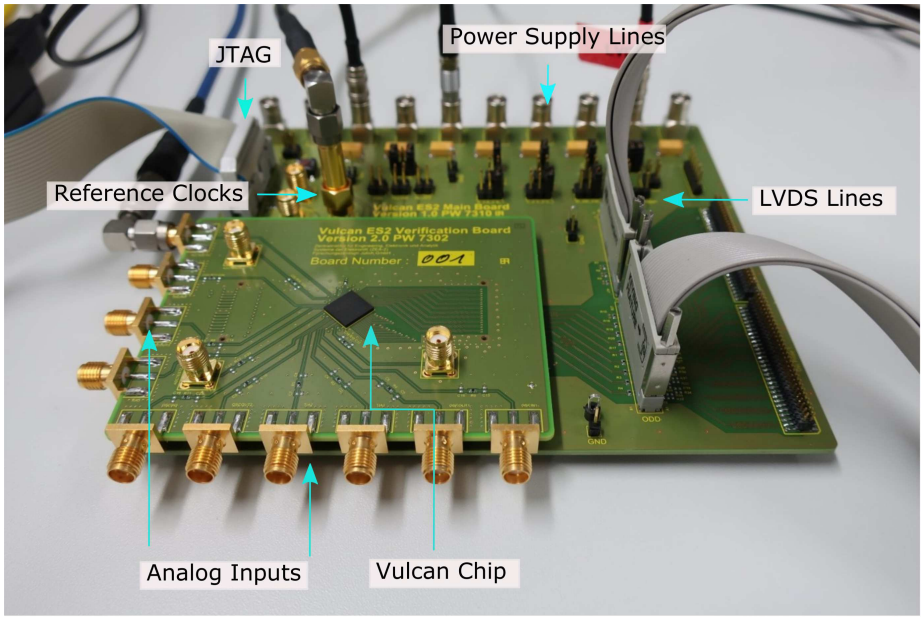


Figure 7.5: Test board with the Vulcan chip embedded on it.

2. Testing of the internal clock generator and transimpedance amplifiers.
3. Testing of the digital circuit using the internal waveform generator.
4. Testing of the analog circuits.
5. Testing of mixed-signal circuits (i.e. ADC and regulators).

In this chapter, the setup and results of step 1,3 and 4 will be presented. The internal clock generator and transimpedance amplifiers implemented in the Vulcan chip are functional. Since the measurement results of the latter mentioned blocks are out of scope for this thesis, they are not further discussed in this chapter. The basic configuration and measurement set up can be seen in Figure 7.6.

7.2.2 Configuration of Registers

As shown in Figure 7.6, the configuration registers are accessed through the JTAG macro included in the Vulcan chip. A JTAG debugger tool (JLink Pro) is used as an interface between the configuration PC (via Ethernet interface) and the Vulcan's JTAG macro (via JTAG interface). Using this setup the configuration registers were successfully configured. The values written in the configuration registers were cross-checked by reading the registers through the same setup.

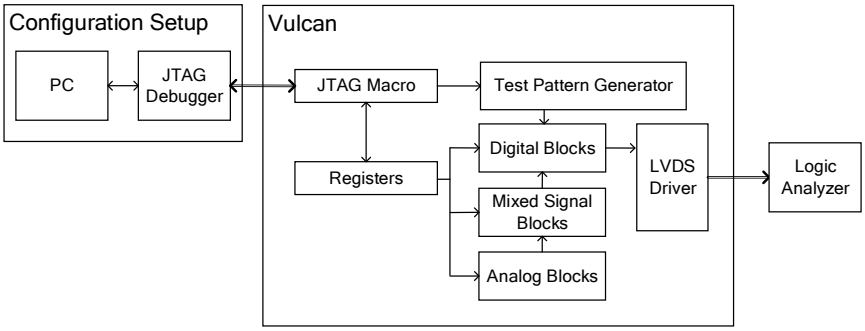


Figure 7.6: Overview of the basic test setup.

7.3 Measurement Results of the Data Processor

The output lines of the LVDS driver are connected to the logic analyzer which are specifically used to analyze bit streams of data. Figure 7.7 shows an exemplary output waveform. Using the internal digital oscilloscope of the logic analyzer the analog representation of the data bit stream can also be displayed. Figure 7.8 shows a more comprehensible analog representation of the same bit stream.

Figure 7.7: Logic analyzer output in bit stream data format with bits 0-7 shown on top and 8-15 below

Figure 7.9 shows the test setup for testing the data processor. The green line indicates the data flow during testing and the black line indicates the normal data flow. During testing, the data processor receives input from the test pattern generator instead of the ADC and ADC encoder to be independent from the much more complicated ADC testing. Data from the processor is transmitted through the LVDS driver of the Vulcan chip. The output signal is connected to the logic analyzer of the measurement setup. The data from the logic analyzer is exported to the server and later offline signal reconstruction is performed with MATLAB.

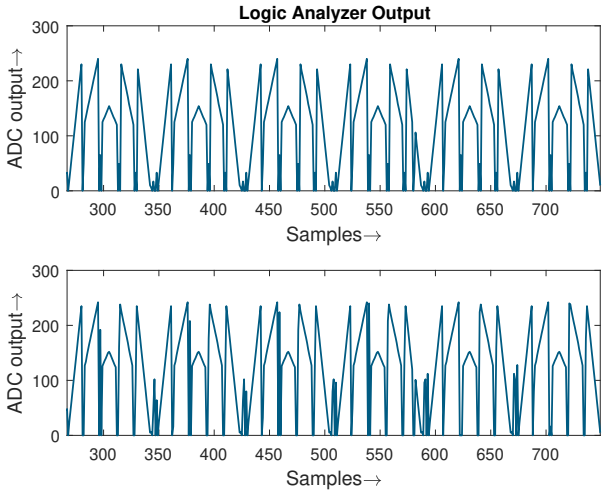


Figure 7.8: Logic analyzer output of bit stream data in analog form, with inputs from LVDS bits 0-7 shown on top and 8-15 below.

The Test Pattern Generator (TPG) is an internal circular buffer which can store 256 samples of 8 bit width. Three such circular buffers are included in the TPG to emulate the three ADCs present in the Vulcan chip. There are two modes of operation in the test pattern generator. In the first mode the TPG internally generates a pattern. In the second mode, a pattern can be programmed into the TPG, and the TPG repeatedly transmits the stored pattern to the digital blocks under test. Before verification of the data processor, the LVDS lines were tested by running an internal counter.

Various test patterns were programmed to or generated by the TPG to test the desired modes of operation of the data processor (PAM). Tests for the following key features of the data processor are presented in the following sections.

- Noise mode and ring buffer underflow
- Appropriate mode change from ADC HG → ADC MG → ADC LG and ADC LG → ADC MG → ADC HG

The header data transmitted by the data processor aids in the signal reconstruction. Timing, bus mode and trigger information are extracted to obtain the timing information and scale the signal corresponding to the gain of the bus mode.

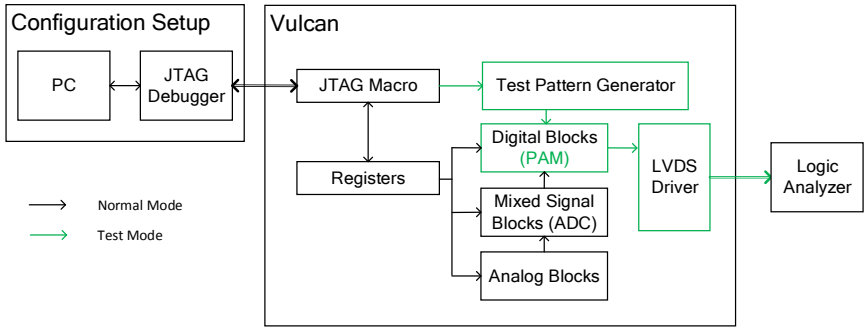


Figure 7.9: Test setup for PAM.

Figure 7.10 shows the pattern generated for testing the noise mode and ring buffer underflow. In noise mode, the samples are compressed and data is transmitted at twice the data rate. A clock like pattern with an amplitude lower than the noise threshold configured was generated. The output of the data processor corresponding to this input waveform was recorded using the logic analyzer. The reconstructed waveform is shown in Figure 7.11. Since the samples are below noise level the data is required to be transmitted at twice the speed. As there are not enough samples to send, the system starts in underflow mode, the overhead generated due to the header during underflows leads to accumulation of samples in the ring buffer. When there are sufficient samples to transmit the data at twice the clock rate, the mode is changed to noise mode which can be observed in Figure 7.11. The transmission of noise samples empties the ring buffer faster resulting in mode change to underflow. As expected the data samples were transmitted at twice the data rate during noise mode and proper switching of underflow mode was also observed.

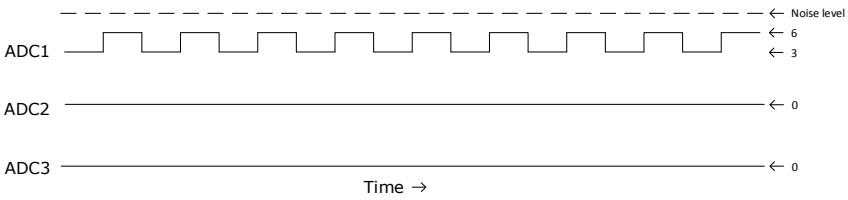


Figure 7.10: Waveform pattern for testing noise compression, with amplitude indicated on the right.

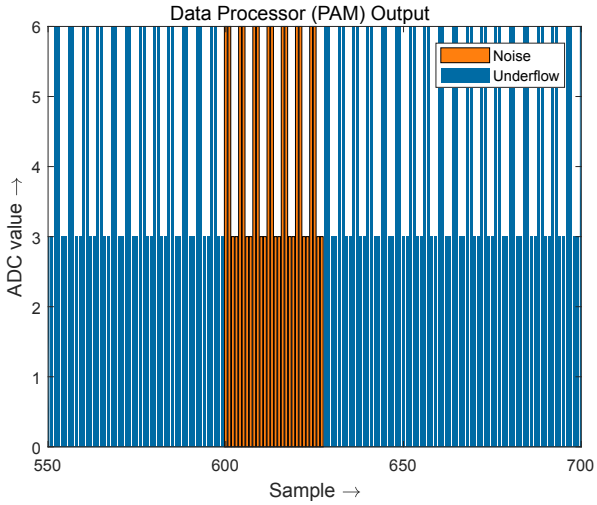


Figure 7.11: Waveform for testing noise compression and underflow.

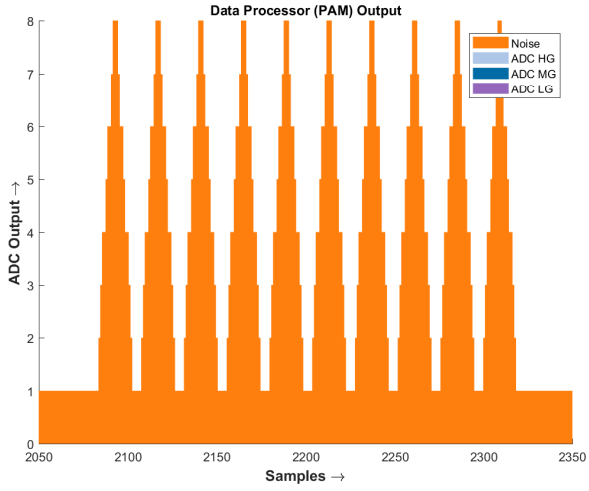


Figure 7.12: Waveform for testing noise compression and underflow.

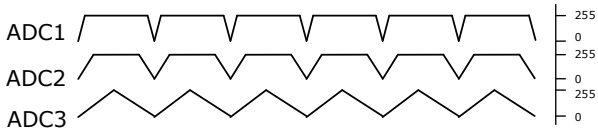


Figure 7.13: Waveform patterns for testing continuous mode change.

The Figure 7.13 shows the pattern generated for testing continuous mode changes between ADC HG, ADC MG and ADC LG. The first waveform has a larger slope and upon reaching the maximum value is held constant for few cycles. The following waveform has a relatively lower slope and follows the same pattern. The final waveform is a triangular signal. The varying slope emulates the different gain of the ADCs and the signal held at constant value emulates the saturation behavior of the ADC. The slope of the waveforms are carefully selected such that when the waveform is reconstructed with the appropriate gain factor a triangular waveform is generated. The output of the data processor corresponding to this input waveform was recorded using the logic analyzer. The reconstructed waveform is shown in Figure 7.14 validates the continuous mode change functionality of the data processor.

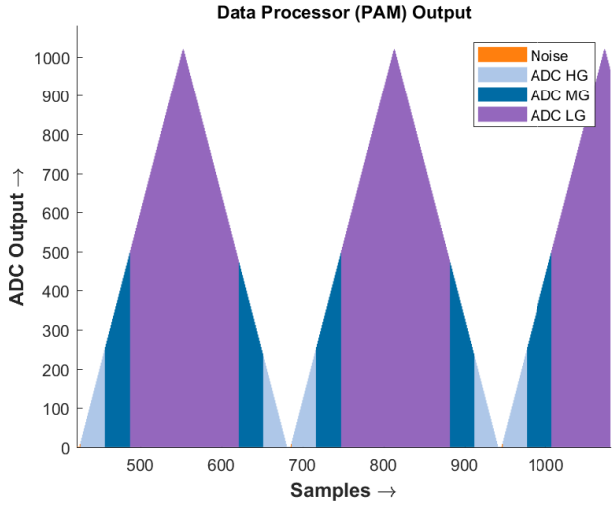


Figure 7.14: Reconstructed data processor output for continuous mode change input signal.

Although the internal ring buffer has been designed with a safety margin of 3 times the maximum expected event rate, it is essential to test whether the ring buffer generates the appropriate flags when it is 50 % and 80 % full and if the processor generates appropriate triggers. For the purpose of testing the overflow mode of ring buffer, patterns were generated such that the mode change is forced after every sample. This extreme artificially created mode

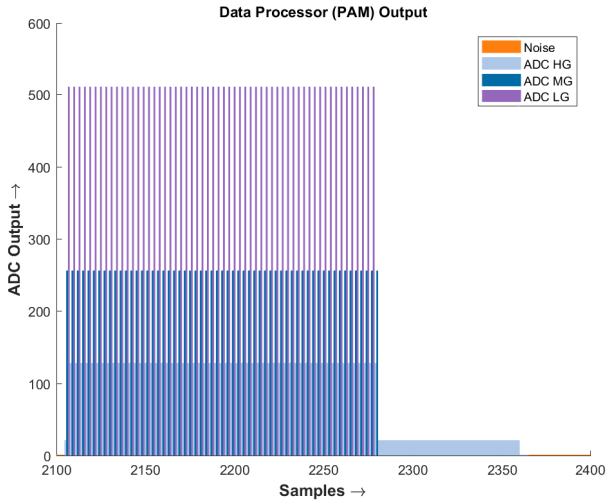


Figure 7.15: Reconstructed data processor output for continuous mode change input signal [60].

change causes lots of overhead since reset and header information has to be transmitted after every mode change. The data processor was expected to avoid bus mode change in accordance with the description in Section 5.3, Table 5.2 after 50 % and 80 % of its ring buffer occupancy.

The reconstructed waveform for verifying the processor functionality during overflow mode is shown in Figure 7.15. It can be noticed (by the varying colors) that the mode change is initially occurring frequently and in later stages, the mode is alternating between ADC HG and noise.

Based on the reconstructed waveform it is concluded that the data processor complies with the requirement specification of the data processor of the Vulcan chip.

7.4 Measurement Results of the ADC Baseline Regulator

An ADC regulator was developed to regulate the baseline of the signal by adjusting the ADC reference voltage as described in Section 4.10. A DC signal is fed as input to the Vulcan chip for testing the ADC regulator. The amplitude of the generated input DC signal was higher than the desired baseline to emulate the offset introduced by an inter-symbol interference. For the provided input signal the ADC regulator needs to attain the desired baseline after regulation as depicted in Figure 7.16.

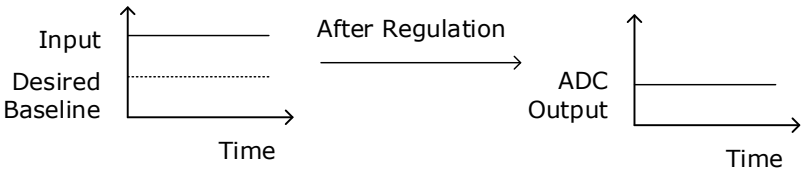


Figure 7.16: Illustration demonstrating the expected behavior of ADC baseline regulator.

The measurement results of the ADC baseline regulator are shown from Figure 7.17 to 7.19. The ADC baseline regulator has a coarse and a fine-tuning feature. The measurement of the course tuning feature is shown in Figure 7.17. A DC signal corresponding to ADC output value (i.e. 30) higher than the desired baseline was provided as input and the ADC regulator was required to bring the baseline corresponding to an ADC value of 10. During the measurement it was observed that the ADC regulator regulated the baseline as expected. The varying output shows the sigma-delta function of the baseline regulator. The average of the signal was measured around an ADC value of 10.

Figure 7.18 (Left) demonstrates the fine tuning feature of the ADC baseline regulator. It can be noticed that the toggling effect of the sigma-delta modulation of the regulator is smaller than the coarse tuning feature presented previously. Figure 7.18 (Right) shows the zoomed in image of the fine-tuning feature and it can be observed that the ADC value toggles within 1 LSB of the ADC.

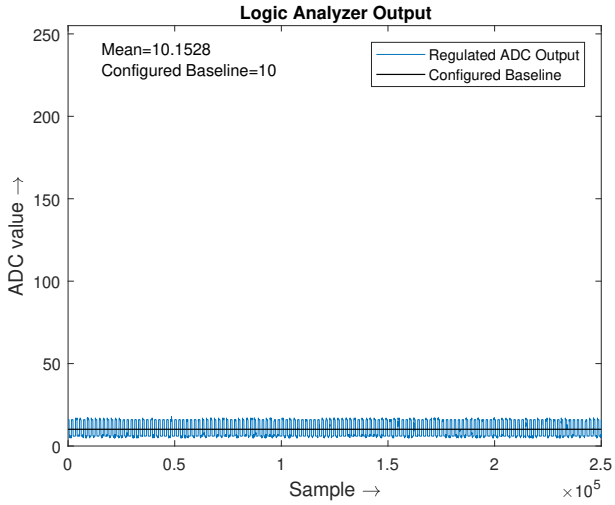


Figure 7.17: ADC regulator measurement result (coarse tuning). The required baseline is set at 10 and the regulated baseline measures an average of 10.1528.

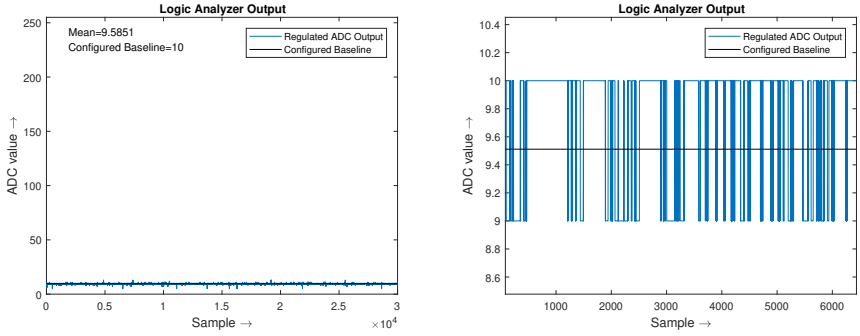


Figure 7.18: [Left] ADC baseline regulation measurement result (fine tuning). The required baseline is set at 10 and the regulated baseline measures an average of 9.5851. [Right] ADC baseline regulation measurement result - zoomed in (fine tuning).

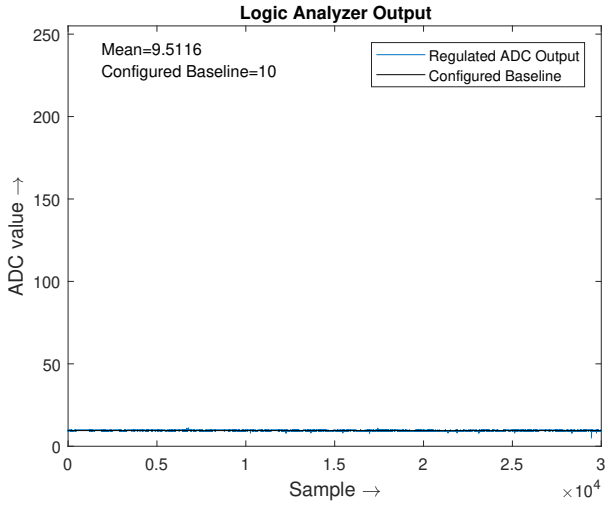


Figure 7.19: Baseline retained after regulation. ADC baseline for the signal range from 0 to 255.

Finally, Figure 7.19 shows the baseline retained at the configured level after the regulator is turned off. Based on the measurement result, the ADC regulator passed its specification.

Summary and Outlook 8

8.1 Summary

The goal of this thesis is three folds: First is to develop a system model to investigate further possible structures for regulation. Secondly, the design and development of digital signal processing units for a receiver suitable for particle physics applications. The third and final step is to design and implement structures to improve the reliability of the receiver.

The Vulcan receiver chip was specifically designed to process varying amplitude and aperiodic input pulse signals. Several transmission modes are possible depending upon the signal amplitude and the status of the internal modules. The internal data processor has to analyze the data stream and select a transmission mode based on the programmed predefined conditions.

The measurement results of the data processor from the two receiver prototypes were analyzed and the following conclusions were drawn:

- The data processor independently selects the mode of transmission.
- The data processor handles high data rates.
- The data processor efficiently formats data appropriate for reconstruction.
- The data processor successfully reduces the bandwidth of data during the absence of an input pulse

In essence, a data processor adhering to its specification was successfully developed, implemented and tested.

In the JUNO experiment, the shape of the input pulse carries vital information about the properties of sub-atomic particles. Utmost care has to be practiced to preserve the pulse shape. A new compensation method for the baseline shift, an effect that might impair the amplitude of the signal was discussed in this thesis. The measurement results presented in Chapter 7 proved that the baseline can be regulated to the desired level using the implemented ADC baseline

regulator. A model of the receiver chain was developed to understand the combined effect of the ADC baseline regulator and the overshoot compensator on the input pulse. The model was used to study the response of the system to component mismatches of the compensation circuit. The mismatches in the components of the compensation circuit leave a residue of the overshoot to propagate through the signal chain. An additional regulator to adjust the compensation circuit by estimating the mismatched is proposed in this thesis.

Owing to the complexity in the installation of the readout electronics and the "minimum duration of uninterrupted data acquisition" requirement of the experiment, a faulty receiver circuit cannot be replaced during the course of the experiment. Due to this reason, the decision to provide a thoroughly tested defect free circuits was made. The design for test structures (mainly the scan chain) introduced in the receiver was described in Chapter 6.

The implemented design for test structure proved to increase the test coverage of the design by providing test points which are accessed via the digital I/O pins. Complex input patterns were generated using EDA tools to test the design using the test structure. Test vectors were generated to detect manufacturing and delay-induced defects. The test vectors for the design were verified by simulation. The verified test vectors are now successfully converted into a suitable format that can be fed to an industrial scale test pattern generator.

8.2 Future Work

The system model described in Chapter 4 was developed with the intention to analyze the combined effect of the overshoot compensator and the ADC baseline regulator on the pulse shape of the signal. As a byproduct of this model, a possible concept for a new residual overshoot compensator was proposed in Chapter 4. A simple model was developed as a proof of concept for the implementation of the residual overshoot compensator. Further investigation is required in conjunction with the reference pulse. The optional residual overshoot compensator can be used to reduce the error generated due to a mismatch between external and on-chip resistors.

Appendix A

A.1 Cascading ADC

The quality of the signal reconstruction is greatly affected by the resolution of the ADC used for digitization. In Vulcan, a novel ADC system combining parallelization, cascading and level shifting of the input signal was designed. The concept of cascading ADCs and level splitting of signals for a higher resolution is demonstrated by the numerical example below.

For 1 V input range and an 8 bit ADC the step size can be calculated as shown in Equation A.1.

$$\text{Step size}_{(\text{8 bit ADC})} = \frac{1V - 0V}{256} = 3.9\,\text{mV} \tag{A.1}$$

If the input voltage range is divided evenly and one ADC is assigned for the upper half voltage range (1 V to 0.5 V) and another ADC is assigned to 0.5 V to 0 V then

$$\text{Step size}_{(\text{for half input range})} = \frac{1\,V - 0.5\,V}{256} = 1.9\,\text{mV} \tag{A.2}$$

Which would be the equivalent of having a 9 bit ADC

$$\text{Step size}_{(\text{9bit ADC})} = \frac{1\,V - 0\,V}{512} = 1.9\,\text{mV} \tag{A.3}$$

As shown in the above equations, two 8 bit ADCs can be combined to create a 9 bit ADC. Similarly, in Vulcan four 6-bit ADCs were combined to create an 8 bit ADC.

A.2 Simulink Model of the System

The Simulink implementation of the system described in Section 4.2 is presented here for reference. The overview of the system and reference generators can be seen in Figure 4.2 and Figure 4.3.

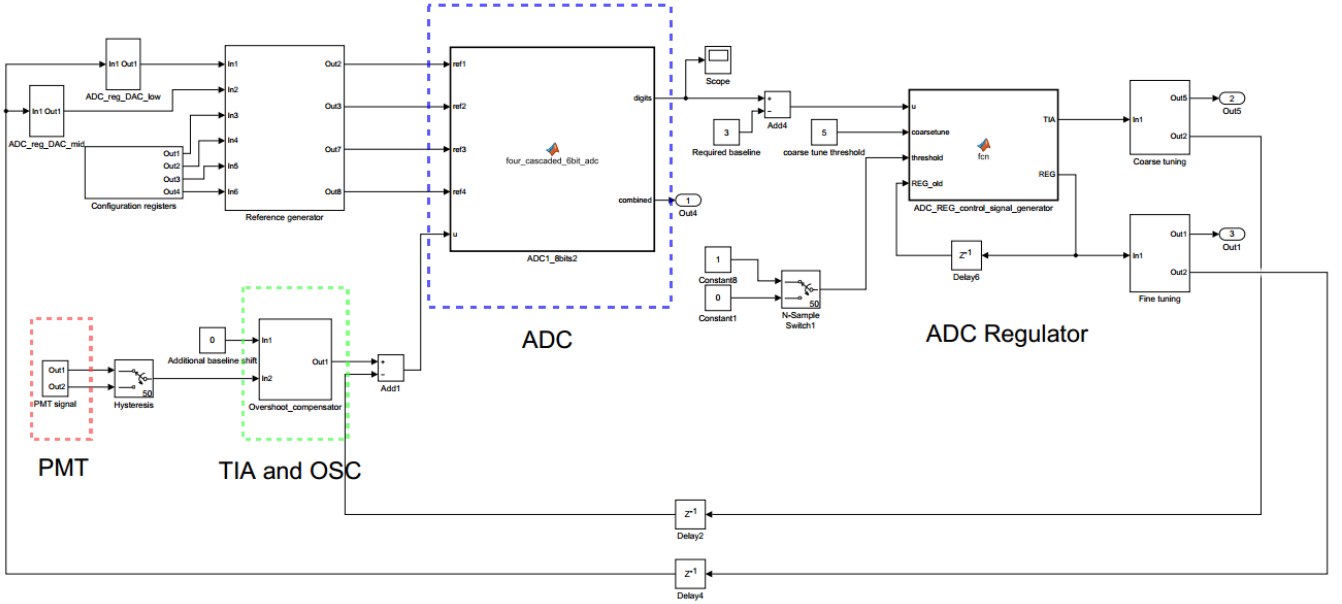


Figure A.1: A model of a system including a PMT (red), a high pass filter, an overshoot compensator, a transimpedance amplifier (green) an 8-bit ADC (blue), and a baseline regulator.

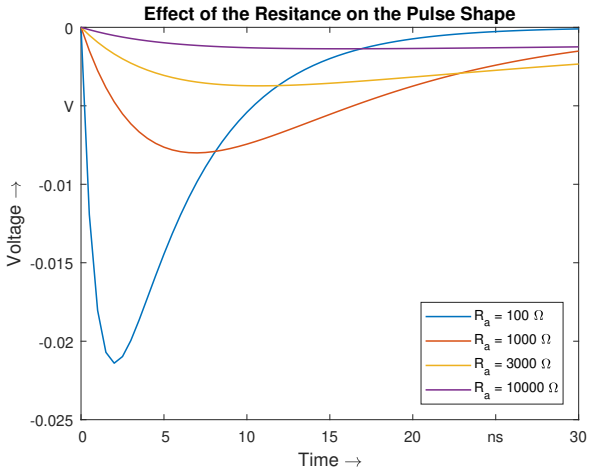


Figure A.2: The effect of the resistance R_a on the pulse shape.

A.3 Poles

Poles are roots of the transfer function (i.e. roots obtained when the denominator of the transfer function is set to zero). Roots can be real, imaginary or complex conjugate. Real parts of the roots produce exponentials signals, and imaginary parts produce sinusoidal values. When roots are complex conjugate pairs, with negative real values the poles produce signals that decay exponentially.

Depending on the value of the poles the response of the system changes. Poles highly determine the gain and stability of the system. When a system contains complex poles, the system tends to produce an overshoot in the response [30]. As a rule of thumb, second order systems tend to exhibit overshoot in the signal. The transfer function of the PMT and the high pass filter are individually first order systems. When the transfer function of the PMT and the high pass filter are combined the resulting system is a second order system.

The biasing resistor and the coupling capacitor placed between the PMT and the Vulcan chip forms a high pass filter. The effect of the biasing resistor value on the shape of the pulse is shown in Figure A.2.

A.4 Synchronization signal

As mentioned in Section 2.2.4, the data from the Vulcan chip is stored in the local DDR3 memory of the GCU. The local trigger of each PMT is sent to the data acquisition unit where the decision to issue a global trigger is made. On the issue of the local trigger, the data from the DDR3 memory is transmitted to the DAC otherwise it is discarded.

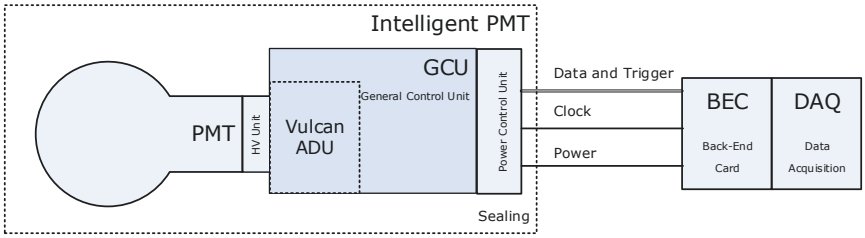


Figure A.3: Overview of the intelligent PMT for the underwater scheme for JUNO.

The Vulcan chip continuously transmits data. The data transfer between the Vulcan chip, memory and the data acquisition unit is controlled by the GCU. For synchronization purposes, the GCU may issue an asynchronous signal (SYNC) to the Vulcan chip. On arrival of the SYNC signal, the data processor captures the value of a 10-bit internal sync counter and transmits the counter value along with the data. This way the internal timing of the Vulcan chip can be synchronized to the GCU on the next rising edge of the clock, the data processor resets the internal sync counter.

A.5 Bubble Errors

Each 8-bit ADC contains 256 comparators. When the input signal crosses the reference voltage of a comparator, it produces a logic "1" else produces a logic "0". For every photoelectron generated by the PMT, each 8-bit ADCs produce 256-bit thermometer code where each bit corresponds to a comparator in the ADC. In thermometer coding, the number N is represented by repeating "1" N times. For example: In an 8-bit thermometer code the number 4 is represented by "0000 1111". Thermometer code increments sequentially from LSB to MSB.

In the entire thermometer code, the change of the logic from high to low (from logic "1" to logic "0") occurs only once. The presence of two logic level changes indicates an error. In Vulcan, a dedicated bubble error correction module is included and a bubble error flag is sent out through the data processor to indicate the existence of an error. In the bubble error correction block, each output is compared with "one output on the left and one on the right, the majority of the three is finally produced as output" [61]. For example: consider the three successive bits of the code A_{n-1}, A_n and A_{n+1}. The majority of the three is calculated by the following formula $(A_{n-1} \times A_n) + (A_n \times A_{n+1}) + (A_{n-1} \times A_{n+1})$. If the majority of three output and output of the thermometer code is different then a bubble error flag is generated. A first-order bubble error correction can be performed by simply flipping the bit on detection of a bubble error. In Vulcan, the bubble error correction feature can be enabled by configuration.

A.6 Gray Coding

When a comparator output does not hold to a constant value but varies between "0" and "1" during the setup and hold time, it becomes ambiguous of which of these two values are sampled. This ambiguity is called metastability.

Following the thermometer code output of the ADC, typically an encoder is placed to map the 256-bit thermometer code to 8-bit binary code resulting in fewer transmission lines for data transfer. As hardware description language compilers and logic synthesizers work with binary coded data, an additional stage to convert thermometer code to gray code and later gray code to binary code was opted to minimize the effect of metastability on multiple bits. Gray code differs from binary code with its property of "successive codes differ by only one bit" [62].

Appendix B

B.1 Measurement Tools

Oscilloscope: An equipment used for measuring varying voltage. An oscilloscope displays the amplitude of the voltage signal versus time. An oscilloscope allows to view fast changing waveforms. The oscilloscope has a high sample rate and bandwidth, permitting it to capture and display a greater number of data points over a longer time period. Compared to the logic analyzer, the oscilloscope can display amplitude and frequency can be displayed in greater detail and measure signals more accurately.

Spectrum Analyzer: An instrument used for the spectrum analysis of signals. It can plot the amplitude of the signal against frequency. Spectrum analyzer is used for testing the signal in the frequency domain as opposed to time domain analysis by the oscilloscope.

Network Analyzer: A tool used for characterization of linear behavior of the device. Mostly used for PLLs and transimpedance amplifier. The network here implies an electrical network.

Function Generator: An instrument used for generating square, triangle and sine waves. Frequency and duty cycle of the waveforms can be changed and DC offset can be added to the signals. Arbitrary waveform generators are used to produce different waveforms via programming.

Logic Analyzer: While the logic analyzer also plots the signal amplitude versus time, it is different from the oscilloscope as it can display the content of digital data streams. Logic analyzers have more channels compared to the standard oscilloscopes. Both digital oscilloscopes and logic analyzers sample the input signals. Rather than measuring analog signals in great detail like an oscilloscope, the logic analyzer uses threshold levels for detecting logic high and logic low.

Power Supplies and Multimeter: 3.3 V, 1.8 V power supplies were connected to the board. Sufficient multimeters were used to measure the current flowing to the Vulcan chip through I/O pins.

B.2 Pad Connections to the Digital Circuits of the Vulcan Chip

The Table B.1 gives the functional description of pads used by the digital circuits of the Vulcan chip. During testing, the JTAG pins JTAGTDI, JTAGTDO and JTAGCLK are used by the scan chain for input, output and clock respectively. The signal used for enabling shift operation in the scan chain and the test mode signal of scan chain are allocated individual pads.

Table B.1: Description of pads used by the digital circuits.

Pad Name	Pad Type	Pad Feature
JTAGTDO	Output.	Tri-State output pad with limited slew rate.
SYNC, JTAGTMS, JTAGTDI, JTAGTRST	Input.	Pads with high voltage tolerance.
JTAGTCK	Input.	Pads with high voltage tolerance and has Schmitt trigger.
RN	Input.	Input Pad with pull-up resistor.
SHIFT ENABLE, TEST MODE	Input.	Input Pad with pull-down resistor.
VDDCU	Power.	Dedicated power pad for digital circuits.
ESDGND	Ground.	Dedicated ground pad.

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Glossary

ADC Analog to Digital Converter
ADC HG ADC for the high gain track
ADC LG ADC for the low gain track
ADC MG ADC for the medium gain track
ADU Analog to Digital conversion Unit
ASIC Application-Specific Integrated Circuit
ATPG Automatic Test Pattern Generation
CAD computer-aided design
Cadence a computer aided design software for electronic circuit design
DAC Digital to Analog Converter
DAQ data acquisition
DC Direct Current
DDR Double Data Rate
DFT Design for Test
DRC Design Rule Check
DSP Digital Signal Processing
EDA Electronics design and automation tool used to manage the tedium and complexity of analysis and verification of an electronic design
FIFO First in First Out
FIT Failure in Time
GCU General Control Unit
GDSII GDSII stream format is a de facto standard used for the preparation of integrated circuit photomask. It is a binary file format representing planar geometric shapes, text labels, and other information about the layout in hierarchical form.
hard macro Hard macros are block level designs, which are optimized for area and power. Hard macro designs can be accessed only via the pins and cannot be manipulated.
HDL Hardware Description Language
I/O Input/Output
IDDQ supply current in the quiescent state
IP Intellectual property
iPMT intelligent PMT
JTAG Joint Test Action Group
JUNO Jiangmen Underground Neutrino Observatory
LIFO Last in First Out
LSB Least Significant Bit
LVDS Low Voltage Differential Signaling
LVS Layout Versus Schematic
MATLAB matrix laboratory, a software program for computations
ModelSim ModelSim is a multi-language HDL simulation environment by Mentor Graphics, for simulation of hardware description languages such as VHDL and Verilog
MSB most significant bit
netlist A netlist is a description of the connectivity of an electronic circuit. In its simplest form, a netlist consists of a list of the electronic components in a circuit and a list of the nodes they are connected to.
NOISE 50 Data below noise level and the ring buffer is 50% full.
NOISE 80 Data below noise level and the ring buffer is 80% full.
PAM Programmable Adaptive Memory
PC personal computer
PCB Printed Circuit Board

p.e. photoelectron
PLL Phase-Locked Loop
PMT Photo Multiplier Tube
RB 50 Ring buffer is 50% full.
RB 80 Ring buffer is 80% full.
RTL Register Transfer Logic
s-a-0 stuck at zero
s-a-1 stuck at one
Simulink Simulink is a graphical programming environment for modeling, simulating and analyzing multidomain dynamical systems
SNR Signal to Noise Ratio
SoC System-on-Chip
soft macro Soft macros are block level designs available in synthesizable RTL and can be manipulated to a certain degree.
TCK test clock
TDI test data in
TDO test data out
TIA transimpedance amplifier
TMS test mode select
TPG Test Pattern Generator
TRST test reset
VHDL Very High Speed Integrated Circuit Hardware Description Language
Vulcan The readout SoC related to this thesis
ZEA-2 Electronic Systems

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