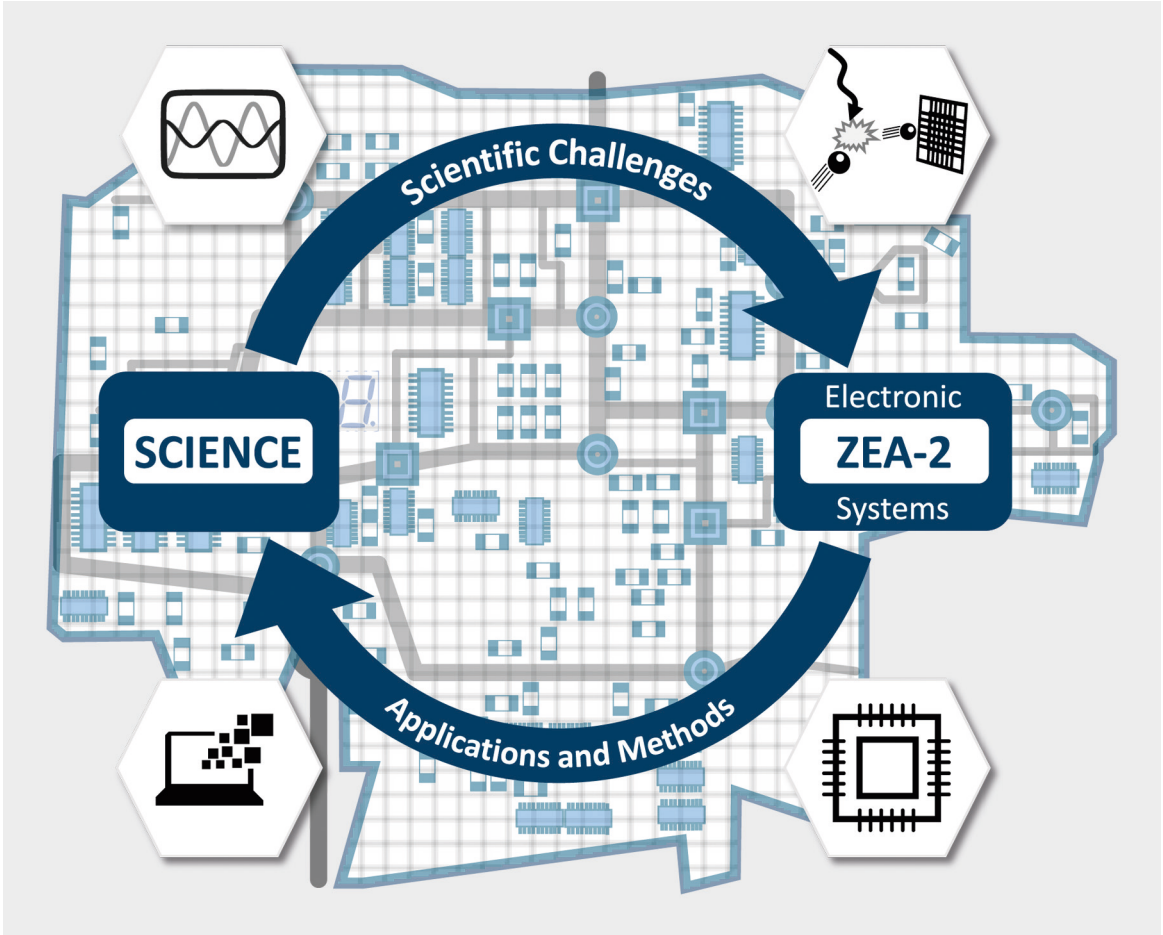

Configurable frequency synthesizer for large scale physics experiments

Nina Parkalian

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Abstract

This thesis describes the design and implementation of frequency synthesizers for the ”Jiangmen Underground Neutrino Observatory (JUNO)” project as a physical experiment. The fully integrated analog phase-locked loop (PLL) based frequency synthesizer is intended to generate the sampling clocks for the analog-to-digital converters (ADC) and digital signal processing (DSP) part. They are employed in the read-out electronics to be used in a neutrino experiment. The proposed design was fabricated in 65 nm CMOS technology. The design provides the best compromise between noise, power consumption and area for a highly reliable and configurable operation based on the application requirements. The design procedure for the PLL architecture and different sub-blocks are presented. A 4 GHz LC-based voltage-controlled oscillator (VCO) is suggested for the low noise operation while providing an optimum tuning range to increase the linearity and frequency coverage in case of process-voltage-temperature (PVT) changes. Furthermore, a novel technique for the amplitude regulation is suggested to detect amplitude errors at the outputs of the VCO and provide an optimized range for the amplitude for a low noise and reliable design.

In addition, a new approach for the charge pump is introduced that suppresses the associated current mismatch problem of conventional structures. This minimizes the static phase error at the input of the PLL that causes spurs at the output.

The measurement results of the analog PLL show very good performance of the structure based on the required specifications and confirm the simulations. The total power consumption for the PLL core equals to 18.5 mW at 1.8 V supply for the VCO and 1 V supply for the other blocks.

Furthermore, the high-level behavioral modeling for a digital PLL is implemented in Simulink/Matlab. The modeling provides a flexible design with fast simulation capability before the SPICE-based design to estimate the design parameters that are important in the digital PLL. A cost efficient design with improved phase noise is intended for this digital PLL. A new modeling approach for the ring type digital-controlled oscillator (DCO) as a critical sub-block of the digital PLL is introduced and its loop parameters are determined. The ring structure of the DCO without inductor maintains the correct performance of the digital PLL while involving in high magnetic fields. A topology for the time-to-digital converter (TDC) is proposed to improve its resolution. The topology applies noise shaping technique for the TDC to improve its effective resolution. Also, the TDC approach make it possible to integrate the ring DCO into the TDC design that leads to the reduction of the power and area consumption and improves reliability in case of variations in the process corner and temperature.

Zusammenfassung

Diese Arbeit beschreibt den Entwurf und die Implementierung eines integrierten Frequenzgenerators für das "Jiangmen Underground Neutrino Observatory (JUNO)" Projekt als physikalisches Experiment. Der vollständig integrierte, auf analoger Phasenregelschleife (PLL) basierende Frequenzsynthesizer, soll den Takt für den Analog-Digital-Wandler (ADC) und die digitale Signalverarbeitung (DSP) erzeugen. Sie werden in der Ausleseelektronik verwendet, um in einem Neutrinoexperiment verwendet zu werden. Das vorgeschlagene Design wurde in einer 65-nm-CMOS-Technologie hergestellt. Das Design bietet den besten Kompromiss zwischen Rauschen, Stromverbrauch und Flächenbedarfs für einen äußerst zuverlässigen und konfigurierbaren Betrieb, der auf den Anforderungen der Anwendung basiert. Das Design-Verfahren für die PLL-Architektur und verschiedene Baublöcke wird vorgestellt. Ein 4 GHz LC-basierter spannungsgesteuerter Oszillator (VCO) wird für den rauscharmen Betrieb vorgeschlagen, während ein optimaler Tuningbereich vorgesehen wird, um die Linearität und Frequenzabdeckung bei Änderungen der Prozessparameter und Temperatur (PVT) zu erhöhen. Weiterhin wird eine neuartige Technik zur Amplitudenregelung vorgeschlagen, um Amplitudenfehler an den Ausgängen des VCO zu erfassen und einen optimierten Bereich für die Amplitude für ein rauscharmes und zuverlässiges Design bereitzustellen.
Außerdem wird ein neuer Ansatz für die Ladungspumpe vorgestellt, der das damit verbundene Problem der Stromungleichheit herkömmlicher Strukturen unterdrückt. Dies minimiert den statischen Phasenfehler am Eingang der PLL, der unerwünschte Seitenbänder in der Ausgangsfrequenz verursacht.
Die Messergebnisse der analogen PLL zeigen eine sehr gute Leistungsfähigkeit

der Struktur basierend auf den erforderlichen Spezifikationen und bestätigen die Simulationen. Der Gesamtstromverbrauch für den PLL-Kern beträgt 18,5 mW bei 1,8 V Versorgungsspannung für den VCO und 1 V Versorgungsspannung für die anderen Blöcke.
Weiterhin wird ein High-Level-Verhaltensmodell für eine digitale PLL in Simulink/Matlab implementiert. Die Modellierung bietet ein flexibles Design mit schnellen Simulationsfähigkeiten vor dem SPICE-basierten Entwurf, um die Designparameter zu schätzen, die bei der digitalen PLL wichtig sind. Ein kostengünstiges Design mit verbessertem Phasenrauschen ist für diese digitale PLL vorgesehen. Ein vereinfachter Modellierungsansatz für den digital-gesteuerter Ringoszillator (DCO) des Ringtyps als kritischer Baublock der digitalen PLL wird eingeführt und seine Schleifenparameter werden bestimmt. Die Ringtopologie des DCO ohne Spule sichert die Funktionalität und Performance der digitalen PLL whärend sie in Umgebungen mit hohen Magnetfeldern arbeitet. Eine Topologie für den Zeit-Digital-Wandler (TDC) wird vorgeschlagen, um seine Auflösung zu verbessern. Diese Topologie benutzt Rauschformumg (noise shaping) für den TDC um die effektive Auflösung zu verbessern. Außerdem ermöglicht der TDC-Ansatz die Integration des Ring-DCO in das TDC-Design, was zu einer Reduzierung des Stroms- und Flächenverbrauchs führt und die Zuverlässigkeit bei Abweichungen in der Prozess und Temperatur verbessert.

Contents

List of abbreviations

JUNO Jiangmen Underground Neutrino Observatory

PLL phase-locked loop

VCO voltage-controlled oscillator

DCO digital-controlled oscillator

TDC time-to-digital converter

ADC analog-to-digital converter

DSP digital signal processing

PMT photo multiplier tubes

MH mass hierarchy

DAQ data acquisition system

pe photo-electrons

TIA transimpedance amplifier

GCU global control unit

SNR signal-to-noise ratio

PFD phase-frequency detector

CP charge pump

PD	phase detector
ISF	impulse sensitivity function
AM	amplitude modulation
FM	frequency modulation
PVT	process-voltage-temperature
HC	hot-carriers
BD	breakdown
AED	amplitude error detector
AMP	amplitude
DAC	digital-to-analog converter
TT	typical-typical
SS	slow-slow
FF	fast-fast
CML	current mode logic
MMD	multi-modulus divider
MUX	multiplexer
LDO	low drop out regulator
EMI	electromagnetic interference
FCW	frequency control word
TW	tuning word
OTW	oscillator tuning word
DLPF	digital loop filter
CW	control word

GRO gated ring oscillator

PI proportional-integral

IIR infinite impulse response

FIR finite impulse response

PM phase margin

DLL delay-locked loop

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Chapter 1

Introduction

Phase locking technology was introduced in 1930s and has been widely used in electronics and communications [1]. Frequency synthesis is a technique to generate low phase noise and stable frequencies that are extracted from a reference clock signal with a fixed frequency. PLL-based frequency synthesizers as necessary parts in many systems have various applications include providing clocks for the up and down frequency conversion in wireless transceivers [2] and high speed microprocessors [3]. Scaling in the CMOS technology allowed for the increase of the operating frequency of the PLLs and current PLLs are highly integrated on chip. For the comparison and selection of the PLL topology, some criteria as the following are considered.

Phase noise characteristic: The noise power of the PLL over frequency in phase domain is studied as phase noise and in time domain as jitter. It is important to detect the effect of different blocks and parameters on the phase noise performance and improve it.

Lock time: It refers to the time that is taken by the PLL to generate a clock signal with stable frequency. This parameter is especially important in dynamic systems with fast frequency changes (e.g. frequency hopping, receive-transmit changes).

Frequency tuning range: The determination of the frequency tuning range for the PLL should cover the intended frequency range in case of process-voltage-temperature (PVT) changes.

Power consumption and size on chip: Minimizing the power consumption of the design and its size on chip is important particularly by considering the production cost.
Reliability: A reliable design should guarantee its long term functionality.
There are many trade-offs in realizing the mentioned features based on the defined requirements for a design. As an example, reduction of the phase noise as an important design issue for the PLLs is a challenging task while staying with the limitations of the power consumption and area on chip [4]. The design approaches are suggested in this work to resolve the challenges under the specific conditions here.

1.1 Thesis objectives

This thesis focuses on the development of PLL-based frequency synthesizers for physical experiments. First, the design and fabrication of a highly reliable and configurable analog PLL is considered. This block is responsible to generate low noise sampling clocks for the analog-to-digital converters (ADC) and digital signal processing (DSP) parts of a front-end read-out chip. The read-out chips are intended to be applied at the receive chain of the neutrino detector of the Jiangmen Underground Neutrino Observatory (JUNO) experiment. The design of a high performance PLL is a challenging task and here its characteristics are determined by the requirements of the experiment. Primarily, a linear modeling is suggested to predict the noise and stability behaviors of the PLL. The main sub-blocks of the analog PLL include phase-frequency detector (PFD), charge pump (CP), loop filter, voltage-controlled oscillator (VCO) and frequency divider (DIVIDER). Each sub-block is investigated to propose novel methods to enhance their performance and configurability. Furthermore, there is an stringent need to keep the correct functionality of the design over 20 years. The LC-based VCO is recognized as a main source to be considered for these reliability considerations. Therefore, a new procedure is suggested to detect and regulate the output signals of the VCO to prevent the degradation phenomenon. The final implementation of the analog PLL and the results of the measurements approve the high performance of the design

based on the requirements and in comparison with some other reported works.
Later, the high-level modeling of a digital PLL is covered in this thesis. The application of this digital PLL is intended for the environments with high electromagnetic radiation. The main effect of electromagnetic interference is on the inductors in the oscillators that can result in the frequency shift and wrong function of the digital PLL. Thus, a digital-controlled oscillator (DCO) in a ring structure without inductor is considered for this digital PLL. Replacing the analog loop filter with the digital counterpart as well as the elimination of the inductor reduces significantly the area on chip. For compensation of the increased noise as the result of ring DCO, a novel time-to-digital converter (TDC) is presented that applies noise shaping. Therefore, a wide bandwidth digital PLL can be modeled with improved noise characteristics. Frequency and time domain analysis provide more insight about the operation and determination of the parameters. The final model is a new topology that integrates the output of the DCO into the TDC block to increase the precision of the design.
The following explains the thesis outline and configuration.

1.2 Thesis outline

Chapter 2 gives a comprehensive description about the JUNO experiment and the application of the PLL in this project. Chapter 3 presents the analog PLL-based frequency synthesizer for the JUNO project. In this chapter the single constituting blocks of the PLL-based frequency synthesizer including their detailed implementation are introduced. Different steps of the design that comprises requirement specification, modeling, implementation and simulation are explained. The measurement results for the analog frequency synthesizer are presented, which are in a good agreement with the simulation results and approve the performance and functionality of the structure based on the requirements.
In chapter 4, the digital PLL and its sub-blocks are introduced. Effective and novel methods are explored to optimize the digital PLL operation considering the precision, settling behavior and noise characteristic. The digital PLL is implemented in a high-level in Simulink/Matlab.
Finally, chapter 5 concludes the thesis and proposes suggestions for the future work.

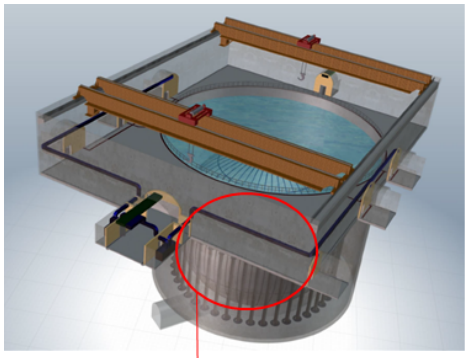
Chapter 2

Jiangmen Underground Neutrino Observatory

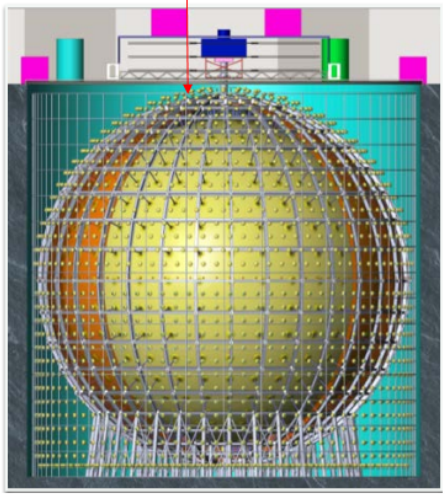
2.1 Introduction

The Jiangmen Underground Neutrino observatory (JUNO) is a multi-purpose neutrino experiment under construction in southern China. One major goal is the determination of the neutrino mass hierarchy using an underground liquid scintillator detector. Further science cases are in the investigations of important topics in neutrino and astro-particle physics such as neutrinos/anti-neutrinos from terrestrial and extra-terrestrial sources [5].

The conceptual drawing of the central detector is illustrated in Figure 2.1 [5] [6] [7]. The central detector is a spherical acrylic vessel and contains 20 kton of liquid scintillator. It will be installed in an underground water pool with an overburden of 700 m rock as shielding against unwanted particles and radiation sources [8]. At least 2 m water from any direction further shields the central detector against cosmic rays. The vessel is supported by a stainless steel truss as mechanical mounting to reduce its internal stress and frame for the detector elements. A cross-section of the JUNO detector is depicted in Figure 2.2 [5]. The inner diameter of the acrylic sphere is about 34.5 m and it will be produced of hundreds of acrylic sheets with thickness of



(a)



(b)

Figure 2.1: Conceptual drawing of (a) the whole detector surrounded by a water pool, and (b) the central detector [5] [6] [7].

12 cm. The main detector comprises 17,000 20-inch photo multiplier tubes (PMTs) to detect light generated in the central detector. Also, there are additional 25000 3-inch PMTs [8] to further increase the energy resolution of the detector [5]. The shielding water is converted into a Cherenkov detector instrumented with about 2000 additional PMTs to provide high efficient muon detection [6]. The system is

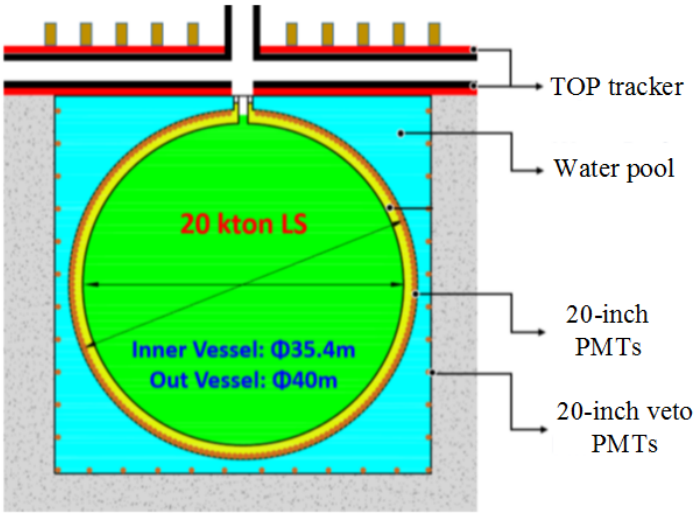


Figure 2.2: JUNO detector with more details [5].

part of the veto referred in [5]. The veto further includes a top tracker system at the top of the detector.

2.2 Neutrino mass hierarchy

The neutrino mass hierarchy (MH) information is important to realize the origin of neutrino mass generation [6]. JUNO is going to resolve the neutrino MH by applying precised spectral measurements of reactor antineutrino oscillations [6]. Figure 2.3 [6] shows the reactor neutrino spectra for different neutrino MHs. The oscillation phase in Figure 2.3 contains useful MH information. Uncertainty in the energy of events leads to the oscillation phase shifts. Therefore, a high energy resolution of 3% at 1 MeV is necessary to extract MH information from the spectral distortion [6].

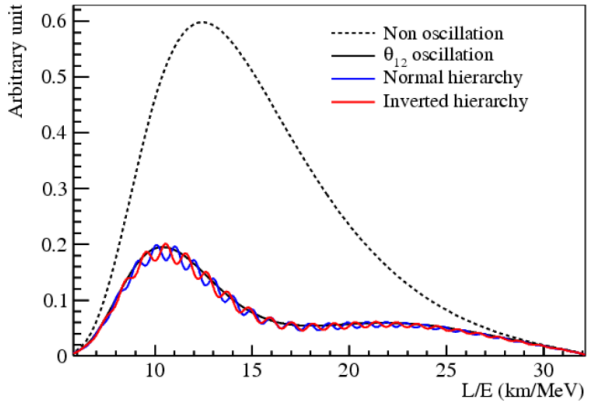


Figure 2.3: Reactor neutrino spectra [6].

2.3 JUNO electronics

The signals from the PMTs that are the central components of the detector are transferred to the read-out electronics. The principle of the operation is to read the output signals of the PMTs, pre-process them and transfer processing results to the data acquisition system (DAQ). The resolution for the average number of the photons that are detected by the PMTs vary from below one in case of low energy neutrino events to several thousands for showering muons. The counts of the photo-electrons as well as their arrival time profile must be determined as exact as possible for event reconstruction and identification. A trigger system preselects correlated photon incidents of relevant events to distinguish them from a huge number of random dark noise incidents. According to the arrival time and photo-electron pattern, the reconstruction of the energy, type and position of the event vertex is done by specially developed methods and corresponding software algorithms [5].

It was mentioned above that the installation of the detector is in water, therefore most of the electronic parts are put also in water to prevent the signal loss resulting from long distance analog signal transmission.

The following concepts are important to be considered for the realization of the

electronic systems [5].

Energy reconstruction: The goal is to optimize the energy measurement by the electronics. The energy resolution is basically limited due to the statistics of the detected photo-electrons. It is important that the electronics characteristics do not limit further the resolution. The required overall energy resolution of JUNO for the neutrino mass hierarchy determination was mentioned above as 3% at 1 MeV, which means a minimum of 1100 photo-electrons (pe) per MeV of deposited energy.

Reconstruction of the photon arrival time pattern: The reconstruction of the vertex position for neutrino events or particle track for muons needs the arrival time of the first photons at PMTs as early information. This is even more significant for the energy reconstruction of anti-neutrino events due to the position dependency of the effective pe yield. Highly accurate reconstruction of the vertex position helps for low systematic uncertainties [5].

Low dead time and dynamic acquisition rate: The minimum or zero dead time is needed to acquire all neutrino events from reactor, solar or geological origin [5]. There are showers of thousands of neutrino events in a period of 10 seconds depending on the distance. Thus, the read-out electronics must increase its acquisition rate to prevent data loss.

Based on the above discussions, Table 2.1 represent the required specifications that need to be fulfilled by the design of the electronic read-out system:

2.3.1 Read-out chip for JUNO

The principal high-level block diagram of the front-end read-out chip of the receive chain of the neutrino detector is shown in Figure 2.4 [9]. The PMTs convert photon hits to a flow of electrons (current pulses) with an approximate gain of 10^7. The transimpedance amplifier (TIA) converts the current pulses that are generated at

Parameters	JUNO specifications
Sampling rate	1 GS/s
Charge resolution	0.1 - 1 pe for signal range of 1 - 100 pe 1% of the signal range for signal range of 100 - 4000 pe
Dynamic range	1 - 4000 pe per channel
Approximation of the arrival time resolution	100 ps
Noise level	< 0.1 pe
Maximum acquisition rate	10^3 - 10^4 trigger/s

Table 2.1: The design specifications for JUNO.

the output of the PMTs into a voltage signal. The TIA gives low impedance to the PMT for high signal bandwidth and small voltage swing a the input. The low input impedance of TIA together with the large output capacitance of the PMT define the bandwidth. High bandwidth provides fast rise time of the pulse that define the

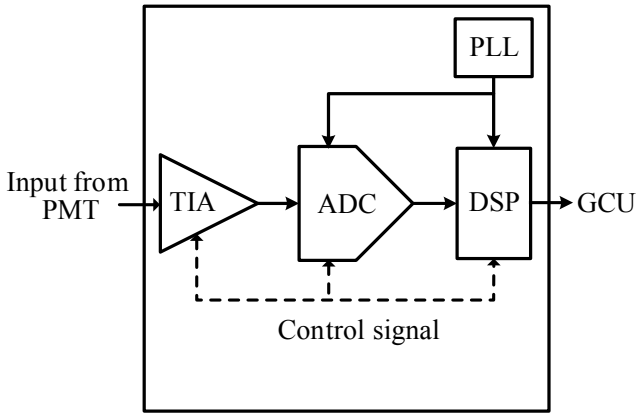


Figure 2.4: Principal high-level block diagram of the front-end read-out chip.

timing accuracy of the pulse, which should be limited by the PMT. Furthermore, high bandwidth has positive impact on the accuracy of pulse shape by separating the pulses. The analog-to-digital converter (ADC) receives the signal from TIA and digitizes the signal at its output to the digital signal processing (DSP) part. The output of the DSP part is given to the FPGA based global control unit (GCU) that has a low power hardware implementation [10]. Its numerous tasks include the selective read-out and data buffering, store and transmission of events via Ethernet link and control the remote peripherals [10].
One of the important aspects in JUNO is the design reliability. The failure rate for the electronic system should be less than 0.1 % per year of operation for detector targeting a long lifetime of operation over 20 years. In this time frame the system should be able to continue its work for the minimum of 10 years with the defined failure rate without maintenance and less than 5 % lost channels.
Besides, the impact of electronic noise on the system resolution as a critical parameter must be minimized. The ADC as a part of the electronic system is needed to have high performance and reliability. Also, the overall system and experiment cost impose strong limitations on the power consumption and design area for the read-out electronics.
Therefore, the clock system for the ADC and DSP part is based on a high performance, low power phase-locked loop (PLL) frequency synthesizer. The impact of the generated clock at the output of the PLL on the ADC functions will be explained in the following.

2.4 Impact of clock noise on ADC operation

One of the key elements that affect the performance and resolution of the ADCs is the jitter of the sampling clock. The PLL based frequency synthesizers are most common to generate the sampling clocks for the ADCs and it is important to keep their phase noise low to minimize the disturbances in the high speed ADCs. The main merits for the PLL's performance based on the JUNO requirements for ADC and DSP are jitter, power consumption, reliability and configurability.

2.4.1 Sampling clock specifications and requirements for the JUNO project

The PLL-based frequency synthesizer provides sampling clocks to the ADC in JUNO experiment as it was explained above. PLL phase noise is among the important metrics in the frequency domain that determine the design performance. Transferred to the time domain, the uncertainty in the clock edges with respect to the ideal clock is investigated as clock jitter as integrated phase noise.
At higher clock frequencies, the sampling clock jitter finds more importance due to its effect on the performance of the ADC. The total signal-to-noise ratio (SNR) for an ADC with sine wave input can be expressed as [11]:

$$\mathrm{SNR} = -20\log_{10}\left[\left(2\pi f_a t_{j,rms}\right)^2 + \frac{2}{3}\left(\frac{1+\epsilon}{2^N}\right)^2 + \left(\frac{2\sqrt{2}V_{n,rms}}{2^N}\right)^2\right]^{0.5}. \tag{2.1}$$

The first, second and third terms are the effects of sampling clock jitter, quantization noise and effective input noise on SNR, respectively. The parameter of $t_{\mathrm{j,rms}}$ in the SNR equation is the combined RMS jitter of the internal components of the ADC and the external sampling clock. The other terms include the analog input frequency of the full-scale input sine wave (f_a), number of bits (N), average differential non-linearity (ϵ) and effective input noise ($V_{\mathrm{n,rms}}$) of the ADC. Higher $t_{\mathrm{j,rms}}$ results in increased sampling time error and reduces the SNR that causes distorted digitized output signal at the output of the ADC.
It is useful to estimate the maximum tolerable jitter of the sampling clock for the ADC based on the specifications of the JUNO project as well as the actual signal shape. The simulations are done for an 8-bit ADC in JUNO experiment. A digital-to-analog converter (DAC) generates the DC reference voltage (V_{ref}) for the ADC in the range of 0 to 1 V. It is shown in Figure 2.5 that for values of $t_{\mathrm{j,rms}}$ below 10 ps, the ADC keeps its SNR and for $t_{\mathrm{j,rms}}$ values larger than 10 ps SNR significant degradation is already more than 0.5 dB [12].

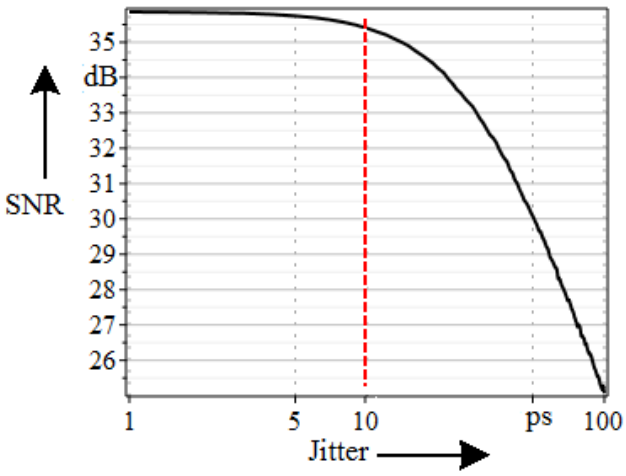


Figure 2.5: Effect of clock jitter on SNR.

Chapter 3

PLL-based frequency synthesizer design in 65 nm CMOS technology

In this chapter, a PLL-based frequency synthesizer is introduced. This PLL design generates the sampling clocks for the ADCs and DSP blocks in the JUNO experiment as explained in chapter 2. The basic operation of the PLL as well as the sub-blocks and the methods to improve their operation are discussed in following sections within the chapter. The design parameters and topology is based on the requirements for the sampling clocks in the JUNO experiment including reliability, configurability, jitter and power consumption.

3.1 Basics about PLL-based frequency synthesizer

The PLL-based frequency synthesizer is an important technique to generate clock signals with the frequency and stability specifications that are referred to a reference signal. A simple PLL design is known as type-I [13]. The open loop transfer function for this type of PLL includes one integrator that is from the VCO transfer function. This system has drawbacks of limited acquisition range and gives a solid trade-off between the stability and noise suppression [13]. Therefore, type-II PLL is considered

for this thesis that its open loop transfer function includes one more integrator in comparison with type-I PLL. A general block diagram of a type-II PLL is shown in Figure 3.1. Generally, its main blocks include phase-frequency detector (PFD), charge pump (CP), loop filter, voltage-controlled oscillator (VCO) and frequency divider (DIVIDER). The basic principle for the PLL operation is based on a negative feedback to synchronize the output clock of the divider (CK_{FB}) with the reference clock (CK_{REF}) in frequency and phase.

The PFD has benefit in comparison with phase detector (PD) since it detects phase and frequency at a time. PFD takes CK_{REF} and CK_{FB} as inputs and generates two output pulses, UP and DN. The width of these pulses indicate the phase and frequency error between the two inputs to the PFD. At the beginning of the PLL operation, the PFD performs as a frequency detector. Later, when the frequencies of two input clocks to the PFD are enough close, the PFD acts as a phase detector [13].

The charge pump is basically consists of two switched current sources. UP and DN signals from the PFD control these switches to convert the phase error information to proportional charging or discharging currents to the loop filter.

The loop filter extracts the control voltage for the VCO, V_{cnt}, from the output current of the charge pump. The VCO generates periodic signals with the frequency that is regulated by V_{cnt} to bring the system into lock state. The output angular frequency, ω_{out} of an ideal VCO is a linear function of V_{cnt} [1] and VCO gain, K_{VCO},

$$\omega_{out} = \omega_0 + K_{VCO} V_{cnt}. \tag{3.1}$$

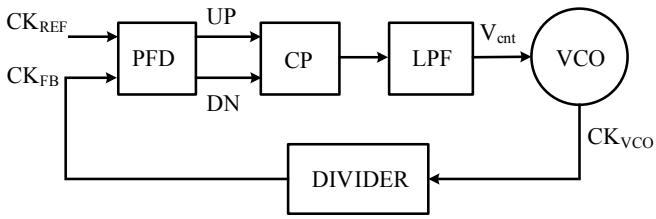


Figure 3.1: General block diagram of a PLL.

The frequency divider divides down the generated frequency at the output of the VCO to provide a signal (CK_{FB}) that can be compared with reference clock (CK_{REF}) at the input of the PFD.
The analysis of the PLL behavior as well as the design process for the single blocks will be discussed in details in the next sections of this chapter.

3.1.1 PLL behavioral characteristic in Matlab

The analytical modeling for PLL [14] is investigated to observe the behavior of each sub-block within the loop. It is to predict the transfer characteristics for stability investigations and noise behavior based on JUNO requirements. The prediction of the PLL loop dynamics and phase noise in behavioral simulators prior to transistor-level design is necessary to avoid time consuming simulations during parameter determination and help to get an overall view about the PLL characteristics. The focus of this work is on a type-II PLL with second order loop filter.
According to [1], the VCO model in frequency domain is extracted. The output signal of the VCO in time domain, $V_{out}(t)$, as a function of phase, $\phi(t)$, is expressed as

$$V_{out}(t) = A_m cos(\phi(t)), \tag{3.2}$$

where A_m is the oscillation amplitude. Regarding to the equation (3.1), $\phi(t)$ can be calculated as

$$\phi(t) = \phi_0 + \int_0^t \omega_{out}(t)dt, \tag{3.3}$$

where ϕ_0 is the initial phase. By replacing (3.1) and (3.3) into (3.2),

$$V_{out}(t) = A_m cos(\omega_0 t + K_{VCO} \int_0^t V_{cnt}dt + \phi_0), \tag{3.4}$$

in which the second term of the total phase is of interest when the VCO is in a PLL. This second term is called ϕ_{ex} and by transferring phase to the Laplace domain [1], the transfer function of the VCO in phase view as an ideal integrator is obtained,

$$\frac{\phi_{ex}}{V_{cnt}}(s) = \frac{K_{VCO}}{s}. \tag{3.5}$$

The Laplace domain representation of the PLL in phase view with sub-blocks is depicted in Figure 3.2. The loop parameters include VCO gain (K_{VCO}), PFD gain (K_{PD}), charge pump current (I_{CP}), division ratio (N) and loop filter components (R, C_0, C_1). These parameters are assessed to warrant a stable function while the intended phase noise and jitter behavior as given by the design requirements is achieved.

Despite the non-linearity of the PLL systems, their behavior can be approximated by a linear model during the steady state. The noise sources of the blocks are determined as:

- Reference noise,
- Charge pump noise associated with PFD,
- Loop filter noise,
- VCO noise,
- Frequency divider noise.

The linear model evaluates the noise contributions of single blocks by their shaped noise at the output of the PLL.

The open loop transfer function for the phase of the PLL is given as

$$H_{OL}(s) = \frac{K_{PD} I_{CP} K_{VCO} LF(s)}{Ns}, \tag{3.6}$$

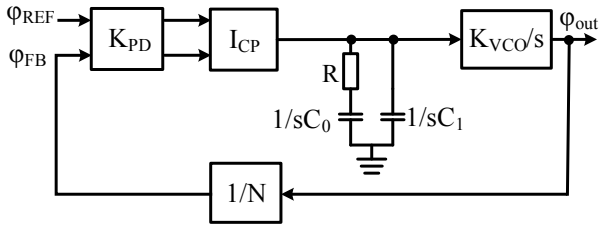


Figure 3.2: The Laplace domain representation of the PLL.

where LF(s) is the transimpedance of the loop filter including two poles and one zero

$$LF(s) = \frac{1 + RC_0 s}{s(C_0 + C_2 + RC_0C_1 s)}. \tag{3.7}$$

The closed-loop transfer function from each phase noise source to the PLL output and the type of their noise shaping are determined in Table 3.1.
The overall phase noise at the PLL output, $\mathcal{L}_{\text{PLL}}(s)$, is the superposition of each phase noise source within the loop, $\mathcal{L}_i(s)$, multiplied by its specific noise transfer function, $\text{NTF}_i(s)$, [14]

$$\mathcal{L}_{\text{PLL}}(s) = \sum \mathcal{L}_i(s) \left|\text{NTF}_i(s)\right|^2. \tag{3.8}$$

The RMS jitter, σ_{rms}, at the PLL output clock is calculated based on the overall PLL phase noise [15]

$$\sigma_{rms} = \frac{1}{2\pi f_{\text{out}}} \sqrt{2 \int_{f_1}^{f_2} \mathcal{L}_{\text{PLL}}(f) \mathrm{d}f}, \tag{3.9}$$

Noise source	Transfer function	Type
Reference	$\frac{NH_{\text{OL}}(s)}{1 + H_{\text{OL}}(s)}$	Low pass
Charge pump/PFD	$\frac{2\pi NH_{\text{OL}}(s)}{I_{\text{CP}}(1 + H_{\text{OL}}(s))}$	Low pass
Loop filter	$\frac{K_{\text{VCO}}}{s(1 + H_{\text{OL}}(s))}$	Band pass
VCO	$\frac{1}{1 + H_{\text{OL}}(s)}$	High pass
Frequency divider	$\frac{NH_{\text{OL}}(s)}{1 + H_{\text{OL}}(s)}$	Low pass

Table 3.1: The transfer functions of PLL blocks.

where f_{out} is the PLL output frequency and f_1 and f_2 are the frequency band limits for the integration.
In addition to the noise minimization techniques that must be applied to each block, the PLL loop bandwidth plays an important role in determining the overall noise behavior. As it was described in Table 3.1, the phase noise sources are shaped with different filtering types within the PLL. The phase noise originating from reference, charge pump and frequency divider is low pass filtered in the PLL and reducing the bandwidth helps to filter out more noise. On the other hand, higher bandwidth is needed to reduce the VCO noise contribution that is high pass filtered in the PLL. Thus, it is important to find out the optimum value for the bandwidth that results in the minimum phase noise at the output.
Furthermore, the PLL is a feedback system and stability analysis is necessary to guarantee the stable steady-state operation. The closed-loop stability analysis is done by analyzing the bode plots [16] extracted from the open-loop transfer function of the PLL to determine the phase margin as stability indicator. A typically design target for the phase margin is equal or higher than 45° to reach sufficient margin over tolerances.
The PLL jitter as well as the phase margin for different values of bandwidth are shown in Figure 3.3. The minimum RMS jitter around 0.72 ps and the phase margin around 45° occur for the bandwidth of 340 KHz. Therefore, for this design, the optimum loop bandwidth is considered around 340 KHz, which yields stable conditions with minimum jitter to satisfy JUNO requirements.

3.2 Oscillator structures

Oscillators are one of the key blocks in the PLL. Although they have non-linear characteristic, linear models can be used to predict their start-up conditions due to small signal values. The oscillator can be modeled as a negative feedback system [1] as is shown in the frequency domain in Figure 3.4. The transfer function of the system is considered as

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1 + A(s)}, \tag{3.10}$$

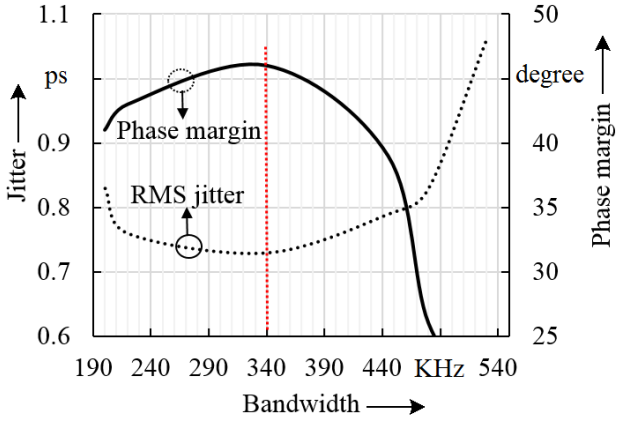


Figure 3.3: Phase margin and RMS jitter.

where $A(s)$ is the loop gain.
The Barkhausen criterion for loop gain and phase shift must be satisfied for a sustained oscillation at the frequency of ω_{osc}, [1]

$$|A(j\omega_{\text{osc}})| \geq 1, \tag{3.11}$$

$$\angle A(j\omega_{\text{osc}}) = 180^{\circ}. \tag{3.12}$$

The Barkhausen criterion is a necessary but not sufficient condition for a stable start-up of oscillation. For secure start-up, the loop gain should be reasonable larger than

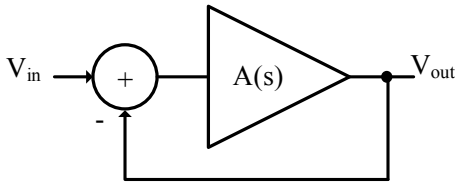


Figure 3.4: Negative feedback system.

unity. The LC-based VCO is considered based on the superior noise characteristics in accordance with JUNO requirements for jitter. One simple equivalent small signal representation of an LC-based VCO is shown in Figure 3.5 [17], where C_{eq} is the total capacitance of the tank circuit including varactors and parasitics. R_p represents the parasitic resistances of the tank circuit. The negative resistance is provided by the active devices to compensate the tank losses for a stable oscillation with the frequency of

$$\omega_{osc} = \frac{1}{\sqrt{LC_{eq}}}, \tag{3.13}$$

The sub-sections of 3.2.1 and 3.2.2 are dedicated to further investigate the phase noise and the design approach for the LC-based oscillator, respectively.

3.2.1 Phase noise analysis

There were discussions in chapter 2 about the negative effect of PLL noise on the ADC operation. The phase noise of the VCO has a significant role in determining the overall noise characteristics of the PLL. In this section, the phase noise of the VCO and its dependency on the design parameters is investigated.

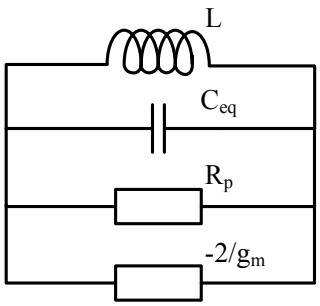


Figure 3.5: Small signal representation of LC-based VCO.

An ideal oscillator generates a periodic output in time domain, which corresponds to a single tone in frequency domain at the oscillation frequency. For the real oscillator with the oscillation frequency of ω_0, the output with the amplitude of $A_0(t)$ is expressed as [13]

$$V_{out}(t) = A_0(t)\cos(\omega_0 t + \phi(t)). \tag{3.14}$$

$\phi(t)$ signifies the phase fluctuations in the time domain, which appears as undesired sidebands around ω_0 in the output spectrum.
Some approaches for the phase noise modeling are introduced. Leeson's noise model proposed a linear time invariant analysis [18] for the phase noise in oscillators. The phase noise spectrum of an oscillator is shown in Figure 3.6 [18]. The $1/f$ flicker noise of electronic devices is up-converted to $1/\omega^3$ region. The thermal noise region, $1/\omega^2$, is caused by the white noise effects in the period of oscillation and finally the flat region for large offset frequencies is the thermal noise added externally to the oscillator [19]. The phase noise of VCO at an offset frequency of $\Delta\omega$ from the oscillation frequency of ω_0 is expressed according to the phase noise distribution as

$$\mathcal{L}(\Delta\omega) = 10\log\Big[\frac{2FKT}{P_{sig}}\Big(1+(\frac{\omega_0}{2Q_{tank}\Delta\omega})^2\Big)\Big(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\Big)\Big]. \tag{3.15}$$

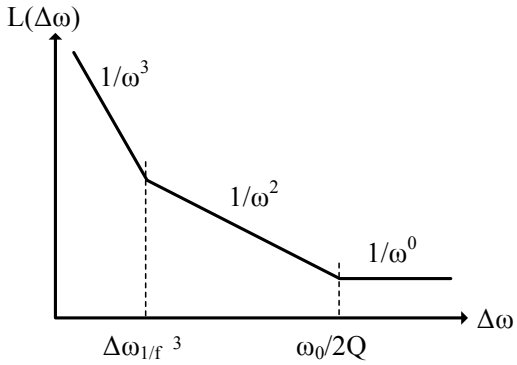


Figure 3.6: VCO noise spectrum.

F is an empirical fitting parameter that is determined from measurements. K, T and Q_{tank} are Boltzmann constant, temperature and LC-tank quality factor, respectively. P_{sig} is the signal power and $\Delta\omega_{1/f^3}$ is the flicker noise corner frequency. Although the Leeson model determines the dependency of the phase noise on the oscillator parameters but there are some problems in predicting the phase noise using its formula. In the model, F and $\Delta\omega_{1/f^3}$ must be determined empirically. Also, the noise flattening frequency is not always $\omega_0/2Q$ and can deviate from this point [20]. On the other hand, Hajimiri and Lee 's noise model proposed a more precise analysis that is a linear time-variant model for the phase noise [21]. In the model an impulse sensitivity function (ISF) response is defined to describe the impact of current disturbance on oscillator noise. According to this method, injecting a current impulse into the oscillation cycle can change the oscillating phase or amplitude depending on the injection time within the oscillation cycle. If the current impulse is injected at the maximum of the oscillation amplitude, the oscillation amplitude disturbs but there is no phase shift. Applying the current impulses at zero crossings causes phase shift but no amplitude disturbance. Based on the model, by applying a white cyclostationary noise source, the phase noise can be expressed as

$$\mathcal{L}\{\Delta\omega\} = 10\log\left[\frac{1}{2}\frac{KT}{V_{max}^2}\frac{1}{R_p(C\omega_0)^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right], \tag{3.16}$$

where V_{max} is the maximum voltage swing across the tank, R_p is the parallel resistor and C is the tank capacitor.

3.2.2 Proposed voltage-controlled oscillator

The LC-based VCO is designed to fulfill the realization of the noise and reliability requirements of JUNO due to the key role of the VCO characteristics in the PLL. The LC-based VCO topology developed in this thesis is presented in Figure 3.7. A symmetric center-tapped inductor and PMOS voltage-controlled varactors constitute the LC-tank circuit. Two cross coupled NMOS transistors (M_5, M_6) provide the negative resistance to compensate the LC-tank resistive losses.
The use of a symmetric center-tapped inductor between the VCO outputs is advan-

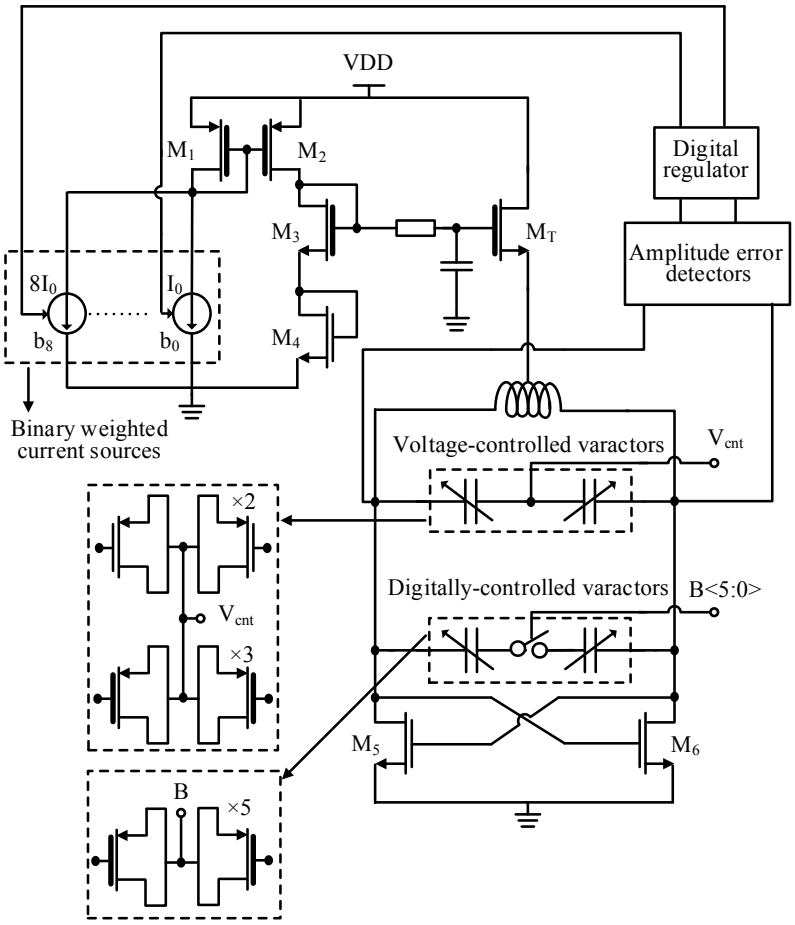


Figure 3.7: VCO architecture.

tageous over a tank circuit with two uncoupled inductors [22]. In comparison with two uncoupled inductors, the symmetric inductor is excited differentially while the current flows in the same direction. This increases the total inductance per unit area by amplifying the magnetic field [23]. For the oscillator design with two uncoupled

inductors, they must be located far apart to reduce the negative effects of unwanted coupling. Thus, the symmetric inductor is beneficial in saving chip area [23].
The quality factor of inductors are limited by the conductor losses resulting from the metal resistance including skin effect and substrate parasitic capacitances [23]. Differential excitation for the symmetric inductor reduces the substrate parasitic effects and leads to an improvement in the quality factor up to 50% [23], [24].
The varactors convert amplitude modulation (AM) noise from supply voltage fluctuations to the frequency modulation (FM) noise, which deteriorates the phase noise characteristics. Therefore, to reduce the supply noise effects, a thick gate oxide NMOS source follower, M_T, acts as a top voltage regulator and isolates the center tap of the inductor from the power supply.
The oscillator is supplied with 1.8 V to ensure enough bias voltage for stable operation.
Binary weighted current sources with their current feature from I_0 to $8I_0$ are shown in Figure 3.7. They are regulated by applying the differential outputs of the VCO to amplitude error detectors. Their structure will be more in detail described in sub-section 3.3.4. The regulated currents are mirrored through M_1 and M_2 to two diode-connected NMOS transistor, M_3 and M_4, which also form a current mirror with M_T and the cross coupled transistors. Therefore by regulating the gate voltage of M_T, the biasing voltage at the center tap of the inductor is adjusted.
The oscillator design includes two varactor banks of voltage-controlled and digitally-controlled to tune the oscillation frequency. MOS-based varactor for the capacitor bank of the LC-based VCO is preferred over reverse biased diodes because of wider tuning range and better quality factor [25]. In the MOS-based varactor, the connected drain and source forms one capacitor terminal and gate is the other terminal. The MOS-based varactor has nonlinear capacitance behavior with the operation regions of inversion, depletion and accumulation that are classified according to the biasing conditions [26]. The characteristic of the varactor affects the linearity of the VCO tuning range that is important to determine the settling performance of the PLL. For guarantee of an almost linear capacitance characteristic for the MOS varactor over the tuning range of the oscillator, the transistor should only work in accumulation or inversion mode, which inversion mode varactors are selected for this design.
The maximum value for MOS capacitance that can be obtained in accumulation and

inversion for a transistor with the channel area of S and the oxide thickness of t_{ox} is approximated by C_{ox} [26]

$$C_{ox} = \frac{\epsilon_{ox} S}{t_{ox}}. \tag{3.17}$$

One of the important parameters in the design of VCO is the tuning range. It should cover the required frequency range that is needed for the PLL to get the lock-state in case of process and temperature changes.

On the other hand, a high gain VCO is more sensitive to noise [27]. Thus, decreasing the VCO gain, K_{VCO}, can help to improve the phase noise characteristics.

Some methods apply discrete tuning such as switched capacitor array that takes large area on chip [28]. This method needs an extra calibration circuit to select the right tuning band during the locking process of the PLL, which increases the complexity of the design [29].

In this design, a hybrid structure from thin and thick gate oxide transistors is used for the voltage-controlled varactors. Thick gate oxide varactors provide higher quality factor and good linearity over the tuning range in comparison with thin gate oxide varactors [30]. But, the ratio between the maximum and minimum capacitance ($C_{\mathrm{max}}/C_{\mathrm{min}}$) is lower for thick gate oxide varactors due to smaller C_{ox}. Applying just thick gate oxide varactors cannot provide the required tuning range for the VCO in an area efficient way to cover the process and temperature variations.

The PMOS thin gate oxide varactors give more capacitance changes with limited linear range for the gate-source voltage,V_{GS}, around the threshold voltage. Figure 3.8 depicts the characteristics of the PMOS varactor using thin and thick gate oxide transistors. The wide linearity and the limited capacitance of thick gate oxide varactors as well as the limited linearity and large capacitance value of thin gate oxide varactors can be seen. Consequently, the proposed hybrid design takes advantage of thick gate oxide varactor to improve linearity, especially for the V_{GS} far from the threshold voltage, and thin gate oxide varactor to supply the necessary tuning range without extra circuitry.

Using equation 3.13, the gain of the proposed VCO that determines the output frequency (f_{osc}) variation with respect to tuning voltage (V_{cnt}) changes can be derived as,

$$\frac{\partial f_{\mathrm{osc}}}{\partial V_{\mathrm{cnt}}} = \frac{1}{4\pi\sqrt{L}(C_{\mathrm{vTK}} + C_{\mathrm{vTN}})^{1.5}} \frac{\partial (C_{\mathrm{vTK}} + C_{\mathrm{vTN}})}{\partial V_{\mathrm{cnt}}}, \tag{3.18}$$

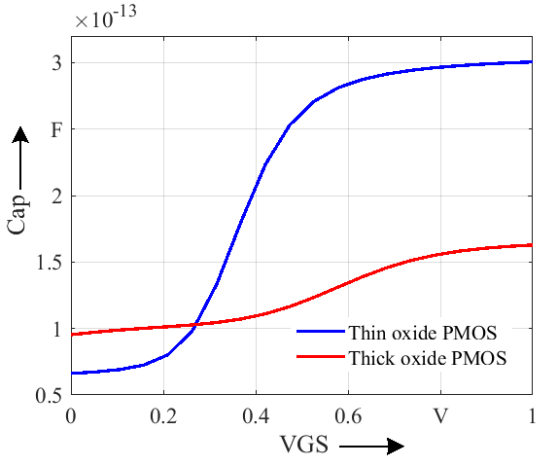


Figure 3.8: Comparison of PMOS varactors formed by thin and thick gate oxide transistors.

where C_{vTK} and C_{vTN} are the equivalent capacitance for the thick and thin gate oxide varactors including their parasitics, respectively. The dependency of the VCO gain to the design parameters is extracted from the equation. The simulation result for the tuning range of the proposed VCO is shown in Figure 3.9 while all bits of the digitally-controlled varactors are set to one. The gain of the VCO covers different process corners and temperatures to generate 4 GHz as the intended oscillation frequency for this design. This is important for the design to reach the correct frequency to guarantee the operation for the JUNO experiment. The VCO in the nominal case generates 4 GHz for the control voltage of 0.5 V as the preferred value. Furthermore, the linearity of the tuning range suppresses more the noise impacts of nonlinear characteristics.

The digitally-controlled varactors are controlled by the binary bits and are predicted to shift the VCO tuning range in case of extreme process-voltage-temperature (PVT) changes. This coarse tuning can extend the VCO gain by 20%.

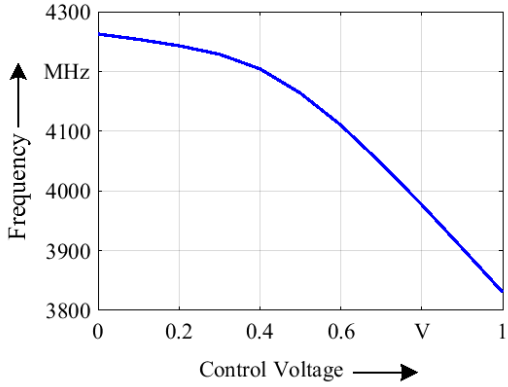


Figure 3.9: Simulation result for the proposed VCO tuning range.

3.3 Regulated amplitude for the VCO in the PLL

The optimized range for the VCO output amplitude is needed to provide the reliable and low noise operation of the PLL for JUNO experiment. In the LC-based VCO, the output voltage amplitude can exceed the power supply limits due to the inductive loading. For the proposed VCO with the supply voltage of 1.8 V, it is important to prevent the amplitude growth at the output of VCO beyond 1 V. The reason is the PLL core blocks that are connected to 1 V power supply. Applying a high swing to thin gate oxide transistors violates the reliability and performance specifications of the PLL in JUNO that its importance was explained in chapter 2.
On the other hand, reduction of VCO output amplitude restricts the signal power and deteriorates phase noise of the VCO. Furthermore, the output amplitude should be enough to guarantee the driving capability of the VCO for the following block, i.e. frequency divider. In the following, the effect of VCO output amplitude on the reliability is investigated and a circuit approach is suggested to achieve the regulated amplitude.

3.3.1 The impact of degradation phenomenon on circuit performance

As CMOS feature size scales down, the channel electric fields in short channel length MOSFETs increase by applying large drain-source voltage. The energy of carriers may increase within their moving in the channel. These high-energy carriers that are known as hot-carriers (HC) can create trap states at the gate-oxide interface or trapped charge carriers at the bulk-oxide [31].
In addition, the breakdown (BD) phenomenon is more likely to happen by applying a high gate-voltage across the thin gate oxide of a transistor for a prolonged time [32]. This effect develops conducting paths through the gate-oxide that increase the leakage current and may cause failure in the operation of the MOS devices. The HC and BD effects may degrade the long-term performance of the devices by reduction of mobility and transconductance and increase of threshold voltage over time [33].
For more investigation about the HC and BD phenomenon, the impact of large VCO amplitude on the MOS varactor is considered. The quality factor of MOS varactors in strong inversion is expressed as [34]

$$Q_{\text{var}} = \frac{1}{2\pi f R_s C}, \tag{3.19}$$

where f is the oscillation frequency of the VCO and C is the varactor capacitance. R_s is the parasitic series resistance associated with the PMOS varactor in strong inversion with the width and length of W and L, respectively, and is given by [34]

$$R_s = \frac{L}{12\mu_p C_{ox} W(V_{GS} - V_{tp})}, \tag{3.20}$$

where μ_p is the mobility of holes, C_{ox} is the oxide capacitance, and V_{GS} and V_{tp} are the gate-(drain/source) voltage and the threshold voltage of the PMOS varactors. R_s increases as the result of the gate-oxide BD that raises the threshold voltage and reduces the mobility. Thus, the quality factor of the varactor degrades.
The total quality factor of the LC-tank is calculated as [35]

$$Q_{tank} = \frac{1}{\frac{1}{Q_{var}} + \frac{1}{Q_{ind}}}, \tag{3.21}$$

where Q_{ind} is the inductor quality factor. Although the inductor mostly determines the quality factor of LC-tank, the design of a low quality varactor can significantly degrade the overall quality factor of the LC-tank. The dependency of phase noise, $\mathcal{L}(\Delta\omega)$, on Q_{tank} reveals the adverse effect of Q_{var} reduction on VCO phase noise characteristics.
Further, HC and BD reduces the transconductance of the cross-coupled NMOS. Its dependency on the mobility and threshold voltage is expressed as

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{tn}). \tag{3.22}$$

With regard to the equivalent circuit of the LC-based oscillator in Figure 3.5, the degraded g_m degrades the condition of,

$$g_m \geq \frac{2}{R_p}, \tag{3.23}$$

which is needed for a sustainable oscillation start-up.
In the PLL architecture, the frequency divider follows the VCO. The outputs of the VCO are applied to two NMOS input transistors of the frequency divider that the structure will be explained in sub-section 3.5.1. The prolonged BD effect on the transconductance of the input transistors can violate the operation condition of the frequency divider.

3.3.2 Modeling the degradation phenomenon

Modeling approach is considered to estimate the negative effect of the oxide BD on MOSFET. The leakage current between gate and drain/source as the result of degradation appears in the form of a voltage dependent current sources as given in [36],

$$I = K(V_{gd})^P. \tag{3.24}$$

Where K and P are scaling factors for the gate leakage current and the exponent of the gate current [37], respectively. They are obtained from the device characterization for the applied stress. Although this nonlinear model gives a good estimation on the BD

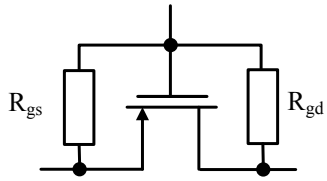


Figure 3.10: Linear model for oxide BD.

effect, calibration against measurement is needed to get the adequate accuracy [38]. In [38], a linear model is developed to show the changes in circuit performance when the BD occurs. It is depicted in Figure 3.10 that linear resistors, R_{gs} and R_{gd}, are placed between gate and drain/source for the modeling.
In this set of simulations, the equivalent resistors R_{gs}/R_{gd} are approximated with a value of 100 KΩ to monitor the effects of oxide BD on proposed VCO phase noise. The BD effect on the VCO is assessed by the modification of the transistor model through inserting the R_{gs}/R_{gd} to the NMOS cross-coupled pairs and thin oxide PMOS varactors. The phase noise characteristic of the VCO for two cases, with and without BD modeling, is shown in Figure 3.11. For this comparison, the same setting of the bits for the binary weighted current sources is considered. There is 4 dB difference between the phase noise results at 1 MHz offset frequency from 4 GHz carrier frequency. Therefore, the adverse effect of degradation on the noise performance of the PLL can be clearly observed.

3.3.3 Digital control loop procedure to regulate the VCO amplitude

The previous discussions explained the importance of the regulated amplitude at the output of VCO to have a reliable and low noise design based on JUNO requirements. Thus, a digital control loop approach is proposed to provide the regulation for VCO amplitude. The digital control loop consists of the amplitude error detectors (AEDs) and a digital regulator block that are shown in the Figure 3.7. It is intended to detect the deviation of amplitude against a nominal window with upper and lower limit at the differential outputs of the VCO and to regulate the amplitude through the binary

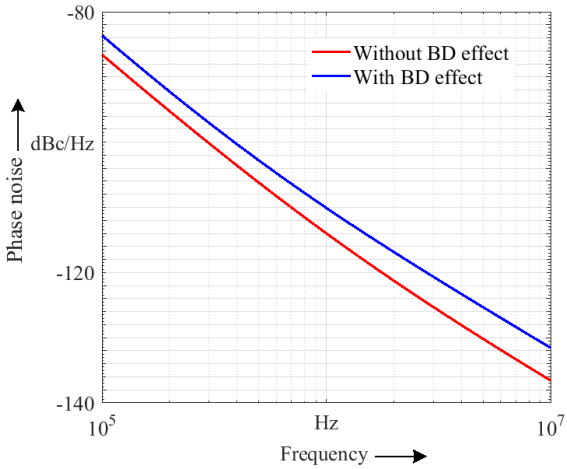


Figure 3.11: Phase noise comparison with and without BD effect.

weighted current sources. The digital regulator block includes a digital counter. Two AEDs composed of UP-AED and DOWN-AED are used with different DC reference levels of REF_U and REF_D, respectively.

The UP-AED specifies the maximum and the DOWN-AED determines the minimum limit for the VCO output amplitude. The outputs of the AEDs are fed into the digital counter, which generates a control word with eight bits to adjust the VCO amplitude through the binary weighted current sources. Figure 3.12 illustrates the control flow of the digital control loop. Initially, a default value is assigned to the control word to start the regulation. When the VCO amplitude (AMP) exceeds the REF_U, the output of UP-AED generates Zero binary signal. Therefore, the digital counter generates a new control word to reduce the overall currents through the binary weighted current sources in order to lower the VCO bias voltage at the center tap of the inductor to reduce the output amplitude. Otherwise, the UP-AED doesn't signal an error and no amplitude reduction is needed. The output of the Down-AED provides One as binary signal to the digital counter when the VCO amplitude falls below the REF_D. The digital control loop responds to this amplitude reduction by setting the control word bits to increase the bias voltage and the VCO output amplitude.

The digital control loop is a feedback system that is only active during the amplitude

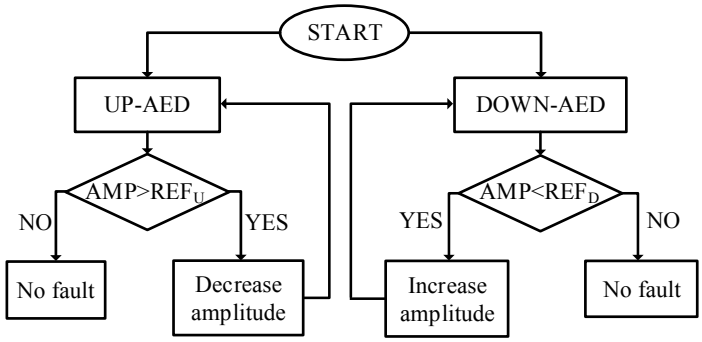


Figure 3.12: Digital control loop algorithm.

regulation time and is deactivated otherwise. This removes the stability concerns that is generally associated with feedback systems.

3.3.4 Amplitude error detector design

The AEDs are included in the digital control loop to recognize the amplitude errors at the output of VCO. The schematic of the AED is shown in Figure 3.13 [39]. The input transistors of M_1 and M_2 receive the differential output signals of the VCO. They provide a symmetrical loading for the VCO. M_3 takes a DC reference voltage, REF_U or REF_D, from a digital-to-analog converter (DAC) as input. A feedback amplifier, which takes its inputs from the drain voltage of M_7, V_{D7}, and a constant voltage, V_{amp}, provides the gate voltage, V_{GP}, to two PMOS loads, M_4 and M_5.
The error detection procedure for the UP-AED will be described as follows. In the fault free mode of operation, in which the amplitude is below the REF_U , the total current of the tail source, M_0, passes through M_3 and M_1/M_2 have no currents. The current of M_3 is subtracted from the current of M_5 and the result enters to M_9. This subtraction reduces the current through M_9 and M_7, so V_{D7} drops. For compensation of the V_{D7} drop, the feedback amplifier reduces V_{GP}. Therefore, the drain currents of M_4 and M_5 increase that raise the drain voltage of M_6, V_{D6}, which is used as the

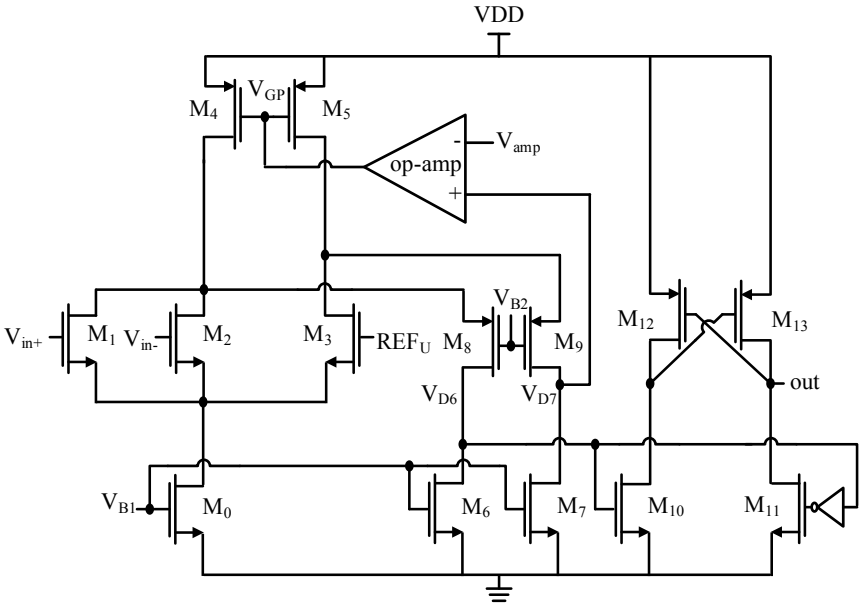


Figure 3.13: Schematic of amplitude error detector.

error indicator.

In the opposite case, when the VCO amplitude is higher than REF_U, M_1 and M_2 start to conduct currents while the current of M_3 is reduced. A very small fraction of current is subtracted from the current of M_5 and V_{D7} increases. The feedback amplifier in consequence of this rise increases V_{GP}. The reduction of the current through M_6 decreases V_{D6}, which means the VCO amplitude, is higher than the maximum limit. V_{D6} is directly connected to a level shifter based on cross-coupled PMOS transistors [40]. The level shifter converts V_{D6} to 0 or 1, i.e. supply voltages, to represent them as binary signals for the digital counter.

In Figure 3.14 the simulation results of UP-AED is shown when the digital control loop is open. The VCO output amplitude, $V_{in+/}$, and REF_U, which is 1 V are compared. At the start of oscillation, the VCO amplitude is lower than REF_U. So, the output of the UP-AED tends to one as in Figure 3.14 and by increasing the amplitude further than REF_U, the output of UP-AED goes to zero. The compatibility of V_{D7}

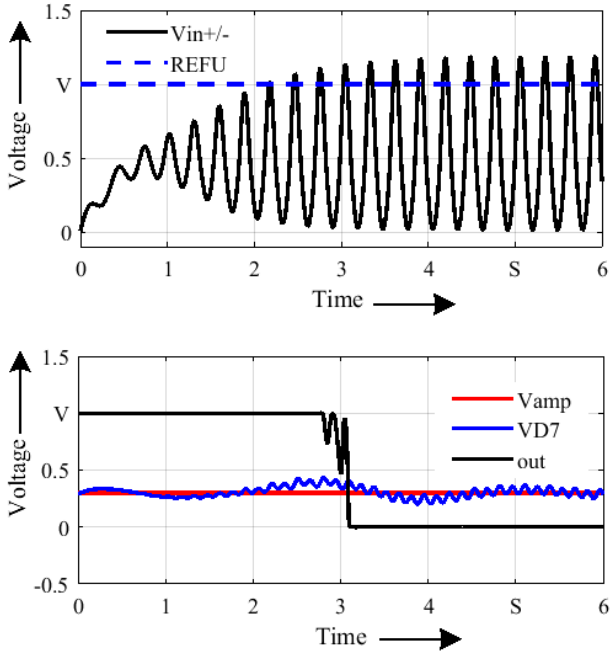


Figure 3.14: Simulation results of UP-AED.

to V_{amp} approves the operation of the feedback amplifier in tracking the voltage changes in V_{D7}. The same procedure occurs for DOWN-AED with REF_D of 0.85 V. Therefore, the regulated output amplitude for the VCO between 0.85 V and 1 V is achieved that guarantees a reliable and low phase noise operation.

3.4 Phase frequency detector/charge pump

3.4.1 Phase frequency detector architecture

The PFD detects the phase and frequency difference between its inputs, CK_{REF} and CK_{FB}. The proportional signals, UP and DN, are generated at its outputs

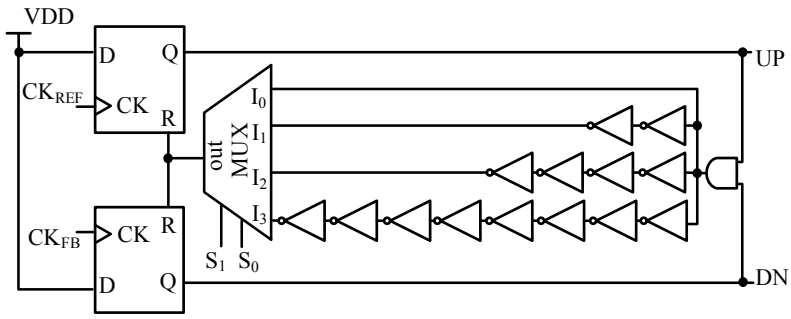


Figure 3.15: Phase frequency detector.

to represent the phase and frequency difference between CK_{REF} and CK_{FB}. The structure of a tri-state PFD [41] is shown in Figure 3.15. It consists of two edge-triggered asynchronous resettable D-type flip-flops that are clocked by CK_{REF} and CK_{FB}. Their inputs are connected to logic 1 (VDD). The AND gate receives UP and DN signals as inputs to reset the flip-flops. The dead-zone is defined as one of the non-ideal effects in the PFD that makes the range of phase error detection lower than 2π [42]. Therefore, the control voltage of the PLL cannot get to the correct value during the dead-zone and this increases the jitter of the system [43]. Inserting a delay in the reset path of the PFD is suggested as a solution for the dead-zone problem [44]. The presented PFD offers a programmable reset path with different delays provided by inverters. The dead-zone conditions vary by PVT changes and the programmable reset path is to ensure the minimum dead-zone in case of PVT variations.

3.4.2 Charge pump design

Non-idealities in the conventional charge pumps cause problems for the PLL performance. The mismatches between the charging, I_{UP}, and discharging, I_{DN}, currents at the output node of the charge pump introduce ripples on the control voltage of the oscillator. This causes static phase error at the input of the PFD that appears as increased reference spurs [45].

The ratio of the spur amplitude, A_{spur}, to the carrier amplitude, A_{carrier} is expressed as [46]

$$\frac{A_{\text{spur}}}{A_{\text{carrier}}} = \frac{1}{2}\frac{K_{\text{VCO}} \cdot V_{\text{ripple}}}{2\pi f_{\text{REF}}}, \tag{3.25}$$

where V_{ripple} is the ripple amplitude. The formula shows that a higher ripple amplitude increases the reference spurs.

The effects of charge pump's non-idealities on the phase error are approximated by [47], [48]

$$\begin{aligned}\Delta\Phi_{\text{tot}} &= \Delta\Phi_{\text{leakage}} + \Delta\Phi_{\text{mismatch}} + \Delta\Phi_{\text{timing}}, \\ &= 2\pi\left(\frac{I_{\text{leakage}}}{I_{\text{CP}}} + \frac{\Delta I}{I_{\text{CP}}} \cdot \frac{t_{\text{on}}}{T_{\text{REF}}} + \frac{\Delta I}{I_{\text{CP}}} \cdot \frac{\Delta t_{\text{delay}} \cdot t_{\text{on}}}{T_{\text{REF}}^2}\right),\end{aligned} \tag{3.26}$$

where I_{CP} and I_{leakage} are the charge pump and the leakage current, respectively. ΔI represents the current mismatch, t_{on} is the on-time of the PFD, T_{REF} is the reference clock period and Δt_{delay} is the timing mismatch. System considerations like transistor sizing, dead-zone removal and minimizing the layout mismatch can reduce I_{leakage}, t_{on} and Δt_{delay}. Circuit techniques are used to reduce the current mismatch as a major factor of influence.

Some approaches were proposed in previous works to reduce the charge pump non-linearity. For example, one technique in [49] limits the operation of the charge pump to only I_{UP} or I_{DN}, which increases the output resistance variation. The design of a novel charge pump employing an error amplifier is presented here that detects the mismatches between I_{UP} and I_{DN} and corrects their mismatch.

The proposed charge pump design is shown in Figure 3.16. The main current path includes the transistors, M_1, M_3, M_5 and M_7. It is in parallel with the auxiliary path that consists of M_0, M_2, M_4 and M_6. These two paths are based on cascode configuration, which increases the output impedance of the charge pump and boosts the current matching. The reference current, I_{ref} enters to the up current mirror to generate I_{UP}.

Both UP and DN current mirrors are on the basis of Sooch cascode current mirror [50]. It is a low power structure to minimize I_{UP}/I_{DN} variations in case of control voltage changes at the output node of the charge pump (V_{out}).

The calibration part of the charge pump consists of control logics and a feedback

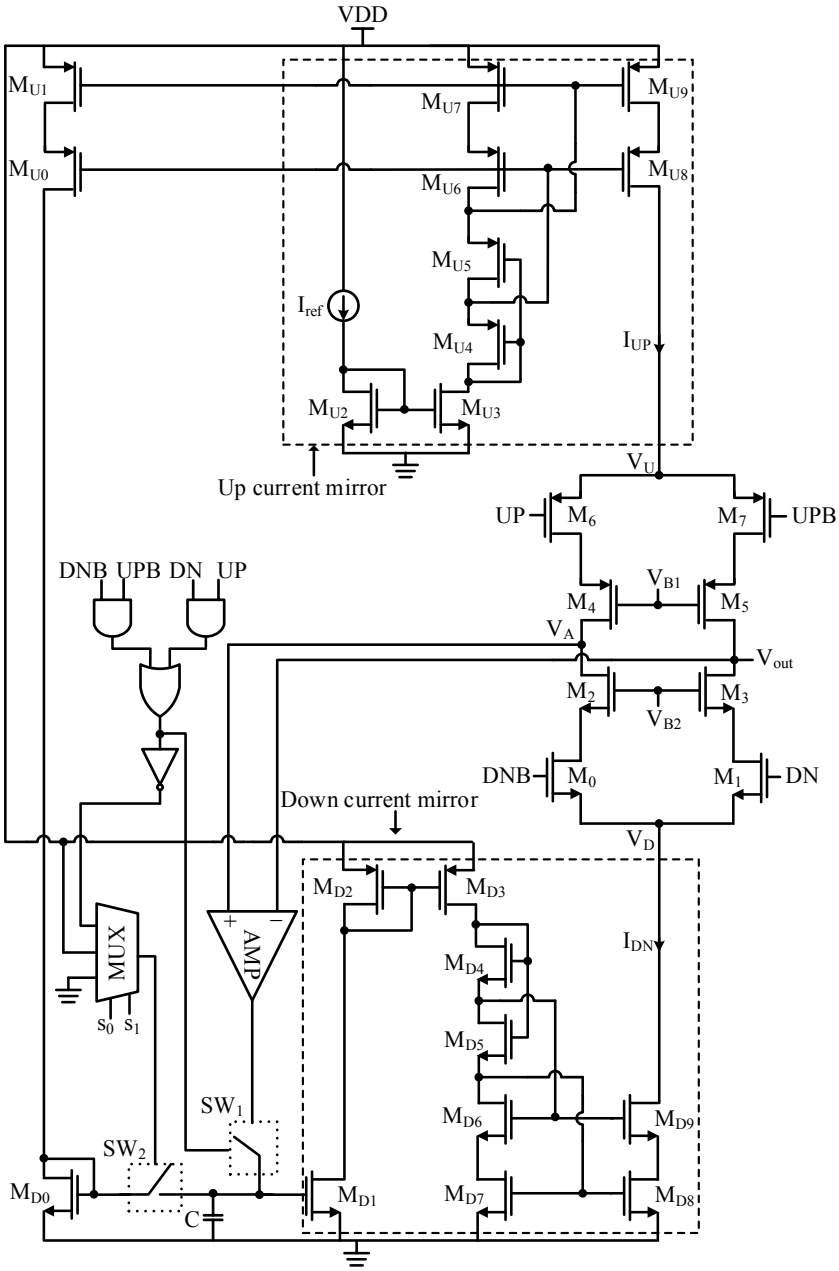


Figure 3.16: Proposed charge pump design.

amplifier. DN/DN_B and UP/UP_B are anti-phase signals that control the inputs of two AND logics. When both UP and DN signals are high (VDD) or low (gnd), the SW_1 switch is on and the feedback loop is activated. The mechanism of the feedback loop is to correct the current mismatches within the lock state of the PLL.
The loop filter at the output of the charge pump is charged by the output current and the output voltage of the charge pump, V_{out}, settles to an approximately constant value over some clock cycles.
The auxiliary path is activated during the time when both UP and DN signals are low. The output voltage of the auxiliary path, V_A is compared with the held V_{out} by the feedback amplifier. The gate voltage of M_{D1} is set to a value that V_A matches V_{out} that means mismatch between I_{UP} and I_{DN} is removed.
For investigation of the correction method for the current mismatch, the PLL during the locking acquisition process is considered.
The periods of UP and DN signals are equal to the T_{REF} that can be divided into two time spans of T_E and T_{NE},

$$T_{REF} = T_E + T_{NE}. \tag{3.27}$$

T_E stands for the time span that UP and DN signals have the same signal level and T_{NE} represents the time span that UP and DN signals have opposite signal levels. At the start-up of the PLL's operation, there are phase and frequency differences between CK_{REF} and CK_{FB} and T_{NE} is longer than the other operation times of the PLL. During T_{NE}, SW_2 is on and I_{UP} is mirrored to the down current mirror via M_{D0}, M_{U0} and M_{U1}. As soon as the PFD resets, UP and DN pulses have the same signal level for the duration of T_E and the calibration mode is activated by turning on SW_1. The discussed process repeats until the PLL locks, which means UP and DN are almost identical

$$T_{REF} = T_E. \tag{3.28}$$

The calibration mode and the feedback loop is activated most of the time. When both UP and DN are high, the feedback amplifier is also active but its impact is negligible for two reasons. First, the time duration of the high level is short compared to the duration of the low level. Second, the large capacitive loading given by the loop filter at V_{out} causes a slow slew rate.
The simulation results show the operation of the proposed charge pump to match

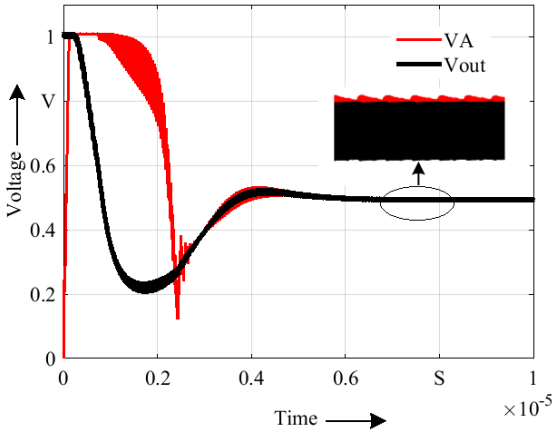


Figure 3.17: Simulation results of V_A and V_{out} of the charge pump.

I_{UP} and I_{DN}. In Figure 3.17 the convergence of V_A towards V_{out} during the locking process is shown. There are very small ripples (about 3.4 mV) on V_{out} during the locking process of the PLL. This approves the good matching between I_{UP} and I_{DN}. In addition, a comparison of current mismatch with and without the activation of the calibration loop is done. Three process corners of typical-typical (TT), slow-slow (SS) and fast-fast (FF) are considered for the comparison in Figure 3.18. Without the calibration loop, the huge current mismatch between 3% to 19% is observed. Also the current mismatch varies over the process corners. The advantage of the calibrated mode in the reduction of the mismatch is observed.

The current mismatches for control voltages close to the low and high supply rails are below 1.7% and for control voltages around the middle of the 1 V supply voltage (the desired control voltage at the lock state of the PLL) is below 0.3%. Therefore, the reference spurs resulting from the charge pump current mismatches are highly suppressed and the overall jitter of the PLL is improved.

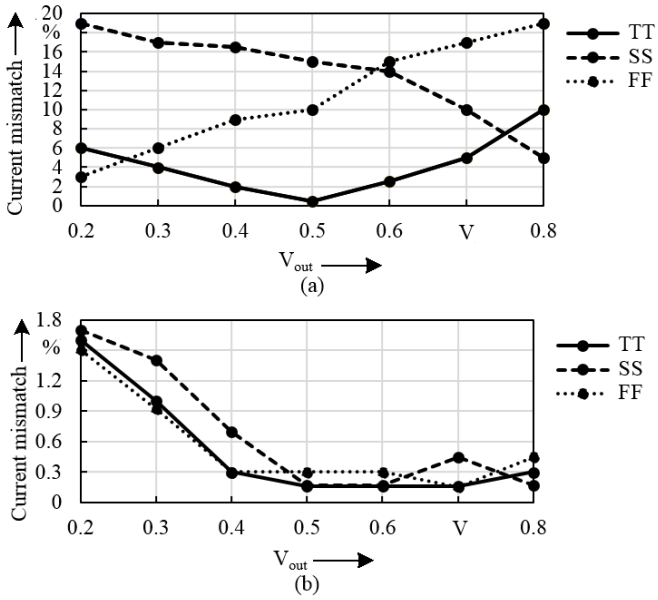


Figure 3.18: Current mismatch comparison: (a) without and (b) with calibration loop.

3.5 Frequency dividers

Frequency divider divides down the output frequency of the VCO with a ratio to make the output frequency of the divider equal to the reference frequency in the lock state of the PLL. The selection of frequency dividers, divider-by-two or multi-modulus, for the PLLs are based on the required division ratio. The following sub-sections introduce these two types of the frequency dividers, which both are combined during this thesis work.

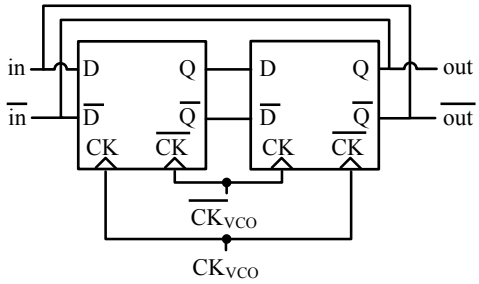


Figure 3.19: Divider-by-two block diagram.

3.5.1 Frequency divider by two

The block diagram of a divider-by-two is shown in Figure 3.19. It consists of two D-latches connected in a negative feedback configuration from differential outputs to the differential inputs [51]. A current mode logic (CML) topology [52] is selected for the implementation of the D-latches because of its high speed operation. Furthermore, the differential structure of the CML rejects substrate and power supply disturbances originating from other blocks at the output.
The schematic of the D-latch is depicted in Figure 3.20. Differential clock signals at the output of the VCO, CK_{VCO} and $\overline{CK}_{VCO}$, drive the transistors, M_{C1} and M_{C2}, as switches. When CK_{VCO} is high, the differential transistors, M_{N1} and M_{N2}, track the signals at their inputs and transfer the result to the output nodes. When CK_{VCO} is low, the cross-coupled regenerative pairs, M_{R1} and M_{R2} store the logic states at the outputs. Setting the appropriate size for the transistors is important to get the optimum operation considering the power consumption and latch speed.
The self-oscillation [53] criterion is brought up in the design of the divider to guarantee the proper operation in case of low amplitude driving clocks and is expressed as

$$g_{mR} R_L > 1. \tag{3.29}$$

g_{mR} and R_L are the transconductance of the cross-coupled pair and the resistive loading at the output nodes, respectively. By cascading N divider-by-two, a frequency division ratio of 2^N will be obtained. Considering C_L as the capacitive loading at

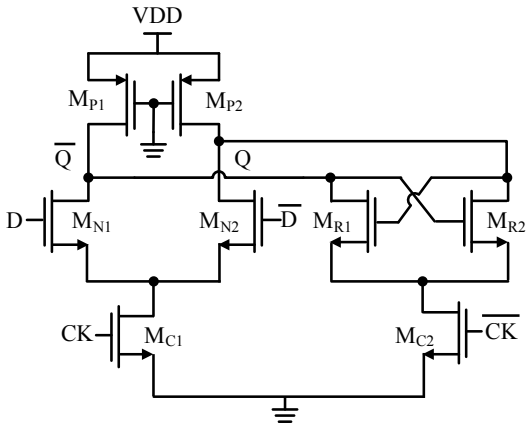


Figure 3.20: CML D-latch schematic.

the output node, the self-oscillation frequency is approximated by $1/R_L C_L$ [54]. By tuning the self-oscillation frequency to the intended frequency at which the divider should work, the phase noise can be significantly reduced [55].

3.5.2 Multi-modulus frequency divider

The multi-modulus divider (MMD) performs the frequency division over a continuous range. The programmable structure consisting of n cascaded 2/3 divider cells is introduced in Figure 3.21 [56].
The operation of the design is explained according to [56]. Once in a division period, the signal, $mod_{(n-1)}$, is generated in the last cell of the multi-modulus divider and is propagated up in the cascaded design. If the programmable input bit, P, is logic '1', and the mod signal is active, then the 2/3 cell divides by three once in a division cycle. Otherwise, the 2/3 cell divides by two for the rest of division cycle. By the programmable input bits, P, the division ratios of two and three are dithered to get the intended division ratio. The output frequency of the divider, f_{out}, is defined

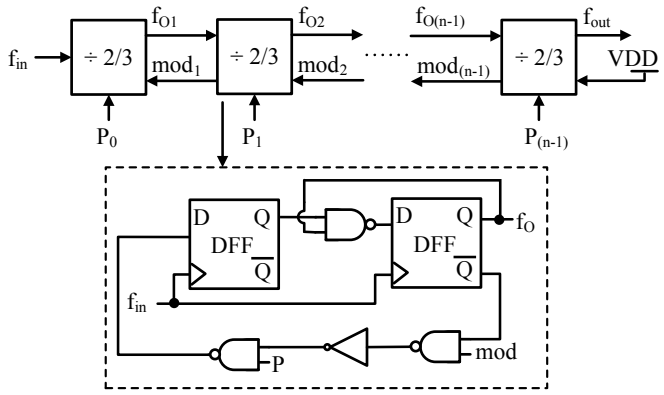


Figure 3.21: Multi-modulus frequency divider block diagram.

based on the final division ratio and the input frequency, f_{in} [56]

$$f_{out} = (2^n + 2^{n-1}P_{n-1} + ... + 2P_1 + P_0)^{-1} \times f_{in}. \tag{3.30}$$

The transient simulation in Figure 3.22 clarifies more the operation of the multi-modulus divider. In this set of simulations, a five bit structure is selected and the simulation results for f_{in} and the outputs of 2/3 divider cells are shown. This design is able to divide down the input frequency in the range of 32 to 63. Here, f_{in} is 1 GHz and by activating P_0, the final frequency at f_{out} resulting from division by 33 is obtained.

3.5.3 The frequency division approach for the considered PLL

The frequency division architecture in the feedback path of the PLL is shown in Figure 3.23. It is a combination of two divider-by-two and a multi-modulus divider. Two divider-by-two at the output of VCO as the first stages of division allow a high frequency operation and consume the highest amount of power compared to the other frequency dividers in the design. They are followed by the MMD block to divide down the feedback frequency to the reference frequency. The reason for the

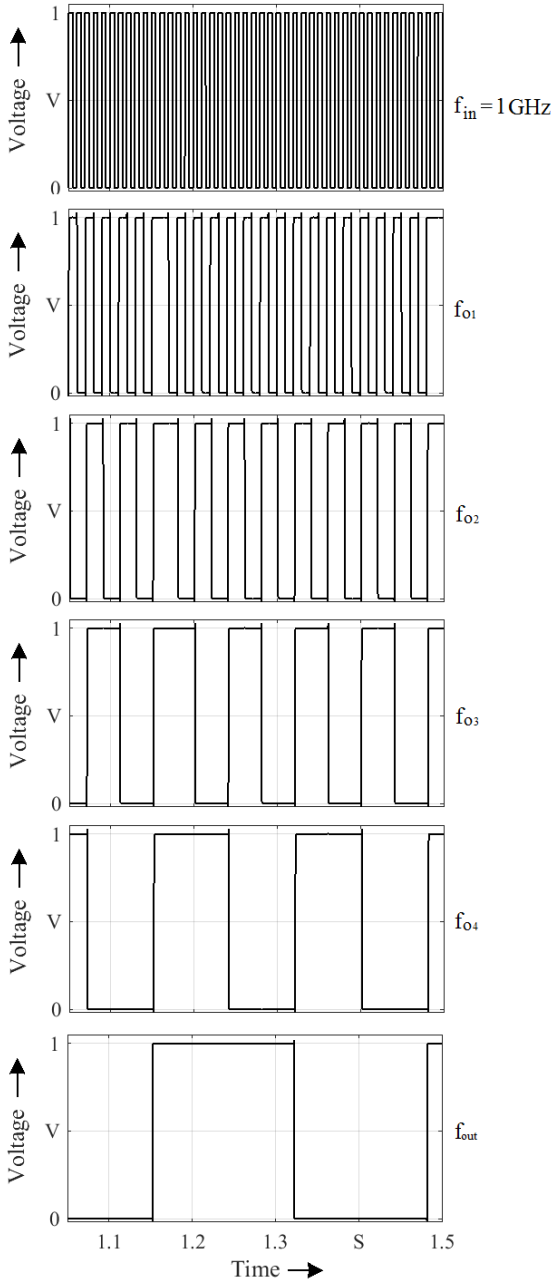


Figure 3.22: Transient simulation of five bit multi-modulus divider.

MMD block is to allow a continuous division ratio of the PLL to cover the case of changing the reference frequency.
A 5 bit MMD is employed for the PLL that can generate division ratios in the range of 32 to 63 using the generated control bits from the control register. The control block consists of a set of two cascaded D-flip flops that are clocked by the output of the MMD to synchronize the generated control bits from the delta-sigma ($\Delta\Sigma$) modulator [57] that is used for the fractional operation.

3.6 Design implementation and measurement results

In the previous sections, the design approaches for the PLL and its sub-blocks were explained. In this section, the implementation and the measurement results are provided to show the functionality of the structure based on JUNO requirements. The overall top view of the PLL core and the clocking system to distribute the sampling clocks to the ADCs and the DSP block is shown in Figure 3.24.
The typical reference frequency, f_{REF}, for JUNO is 31.25 MHz. It is provided by a signal generator to the PLL for measurement purposes, but the functionality of the design for the input frequencies with the ratios of half or a quarter of f_{REF}, $f_{REF}/2$ and $f_{REF}/4$, was also required.
One of the important requirements was a configurable design. It means a flexible design that functions properly in case of a modified reference frequency or a modi-

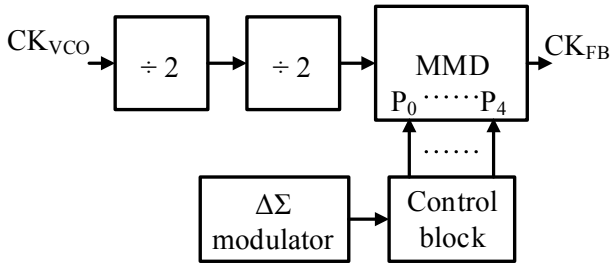


Figure 3.23: Frequency division approach block diagram of the PLL.

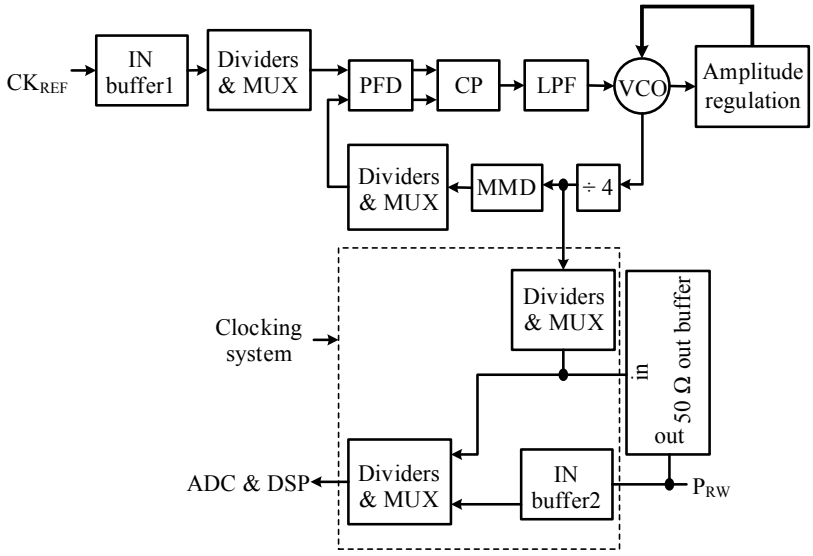


Figure 3.24: Top view of the PLL core and clocking system.

fied driving frequency of the ADC and the DSP blocks. This flexibility is possible by making the input path from f_{REF} and the clocking path to the ADC and digital circuitry configurable by applying frequency dividers and multiplexer (MUX) blocks. The frequency dividers and MUXs that are shown in Figure 3.24 provide three options of: No frequency division, a division ratio by two or four. For example, they can give frequencies of 62.5 MHz, 125 MHz, 250 MHz, 500MHz and 1 GHz to the ADCs derived from a 4 GHz oscillation frequency of the VCO.

The input and output buffers are predicted for test and measurement purposes. Two input buffers, one is at the input of the PLL (IN buffer1) receives CK_{REF} and the other (IN buffer2) is to feed an external clock from the P_{RW} node to the ADC and the DSP block for test purposes.

The measurement result for an oscillation frequency of 1 GHz was obtained at the output of the 50 Ω output buffer. The architecture of this buffer is shown in Figure 3.25. The frequency of 1 GHz was chosen as the typical frequency for the

measurements based on the JUNO requirements for the ADC sampling frequency. The measurement of the PLL output clock is also done through the P_{RW} node.
If an external clock is injected through P_{RW}, the 50 Ω output buffer must be switched off. Thus, two control bits B_0 and B_1 are placed to give the possibility of on or off mode for the 50 Ω output buffer. The SW_{B0} is closed for the PLL output clock measurements while SW_{B1} is open. If the external clock is injected, the SW_{B0} is open while SW_{B1} is closed. The level shifter on the right side converts the control bit levels since SW_{B0} and SW_{B1} are thick gate oxide switches.
The PLL except the VCO and 50 Ω output buffer is powered by a low drop out regulator (LDO) that provides 1 V supply voltage. A power supply of 1.8 V is given externally to the VCO and a second regulator on chip supplies the output buffer with 1.8 V.
The PLL has been fabricated in TSMC 65 nm standard CMOS GP technology. The chip micrograph and the PLL layout with the approximate positions of the constituting blocks is shown in Figure 3.26. The total area of the PLL on chip corresponds to

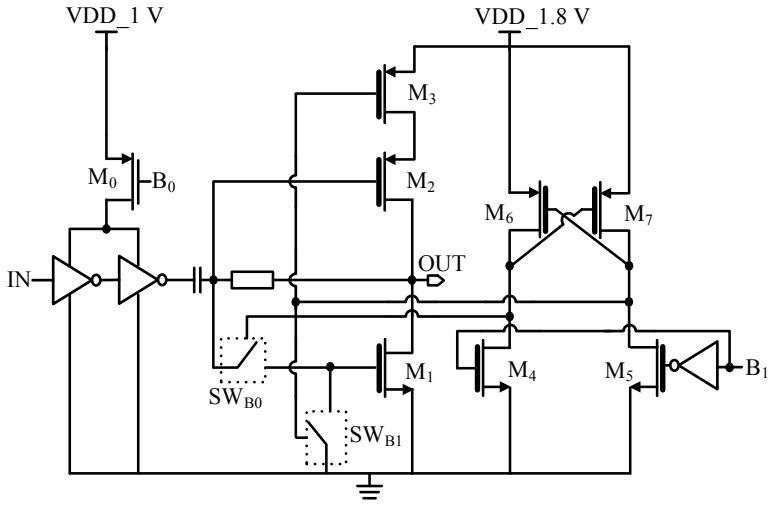


Figure 3.25: 50 Ω output buffer.

0.36 mm^2, of which 0.3 mm^2 is related to the PLL core and 0.06 mm^2 to the clocking system.

The phase noise of the PLL is measured by a Keysight PXA signal analyzer. Figure 3.27 shows the simulated and measured phase noise spectrum of the PLL. The simulated result is obtained based on the discussions for the PLL modeling in Matlab in sub-section 3.1.1. The measurement results for the phase noise at 1 MHz offset from 1 GHz carrier frequency indicates -111 dBc/Hz and the RMS jitter corresponds to 1.4 ps. There is some difference between the phase noise results from the simulation and measurement, e.g. 9dB difference at 1 MHz offset frequency. The reason for this difference can be explained as follows:

The substrates of the thin oxide varactors in the VCO are connected to 1 V from the LDO. The bandgap circuit as a part of the LDO generates the reference voltage for the LDO. Hence, noise of the bandgap can be injected to the VCO through the thin gate oxide varactors. The LDO was designed to supply the 1 V domain of the whole chip that the PLL is a part of it. Therefore, it is not possible to suppress the effect of noise from the LDO by optimizing its bandwidth. Also, a low pass filter could not be applied to the output of the bandgap circuit due to the large area

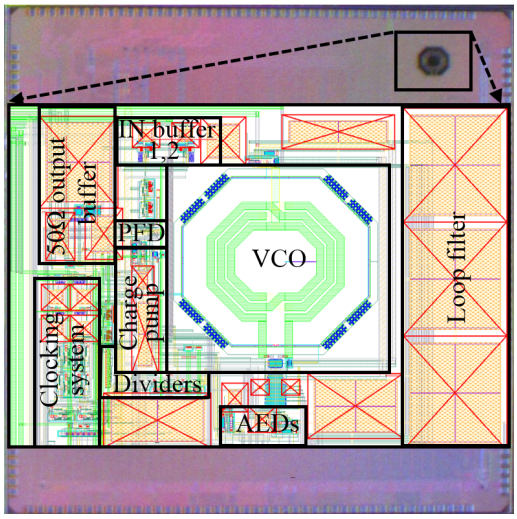


Figure 3.26: The chip micrograph and layout.

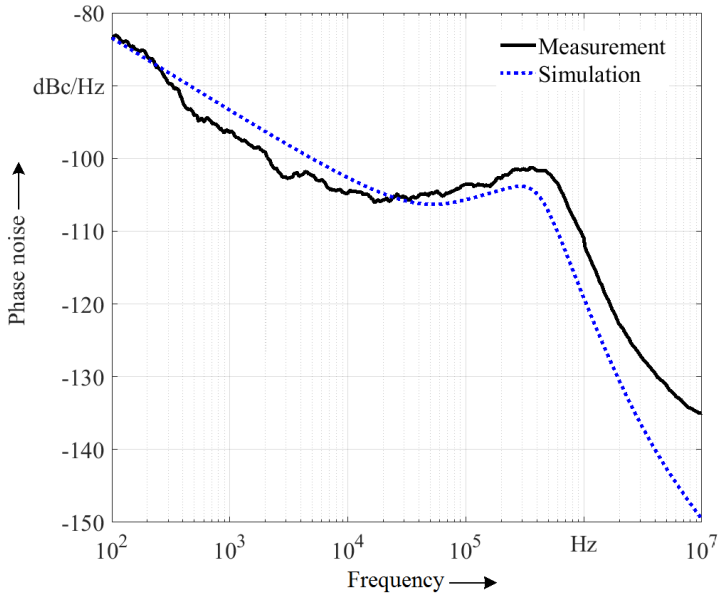


Figure 3.27: PLL phase noise.

consumption of the capacitor. According to the simulation result, the best case phase noise characteristics of the PLL could get to -120 dBc/Hz at 1 MHz offset from the 1 GHz carrier frequency, if the noise from the LDO could be reduced by the design of a separate LDO for the VCO.

The tuning range of the VCO presents the oscillation frequency changes by the variation of the control voltage (V_{cnt}). The tuning range at 1 GHz at temperatures of $-60°$C, 20°C and 80°C is shown in Figure 3.28. At the temperature of 20°C, the tuning range for 1 GHz carrier is 112 MHz, which is in a good agreement with the simulation result that was reported in section 3.2.2. Furthermore, it is observed that by the temperatures variations, e.g. $-60°$C to 80°C, the tuning range easily covers 1 GHz as the target frequency.

Furthermore, the measurements result for the control voltage of the VCO is reported in Figure 3.29. The control voltage settles close to 0.5 V, which is the favorable range by considering the 1 V supply of the PLL.

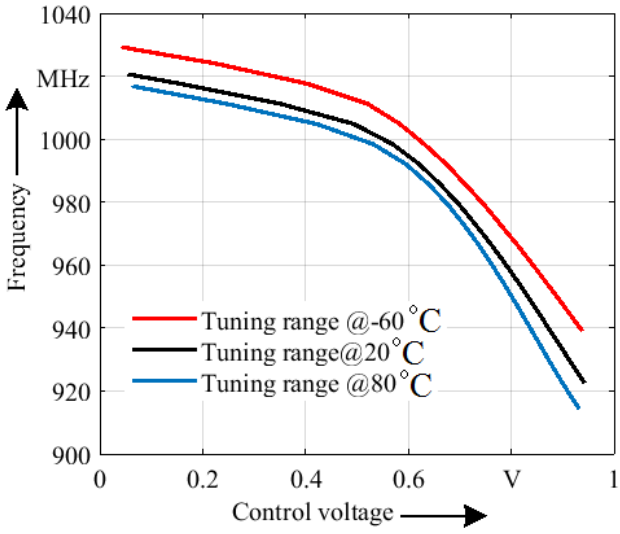


Figure 3.28: PLL tuning range at different temperatures.

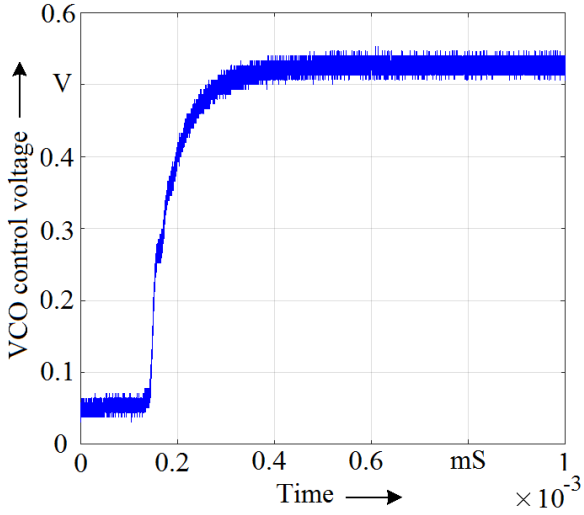


Figure 3.29: VCO control voltage.

The total power consumption of the PLL including the output buffer and excluding the clocking path to the ADC and DSP block is around 18.5 mW that the details of the current consumption and the related power supply are notified in the pie diagram in Figure 3.30. The performance of the proposed design and the comparison with some previous data from the literature is summarized in Table 3.2. Normalized power consumption, P_{NOM}, and normalized phase noise, $\mathcal{L}(\Delta f)_{\mathrm{NOM}}$, are defined by [58] to have a fair comparison between the structures with different carrier frequencies, f_{out},

$$P_{NOM} = \frac{P_{con}}{f_{VCO}}, \tag{3.31}$$

$$\mathcal{L}(\Delta f)_{NOM} = \mathcal{L}(\Delta f) - 20\log\left(\frac{f_{out}}{\Delta f}\right). \tag{3.32}$$

In the above equations, P_{con} and Δf refers to the power consumption and the offset frequency from f_{out}, respectively.
The reported results for P_{NOM}, $\mathcal{L}(\Delta f)_{\mathrm{NOM}}$ and area shows the superior performance of the presented design in comparison with other published works.

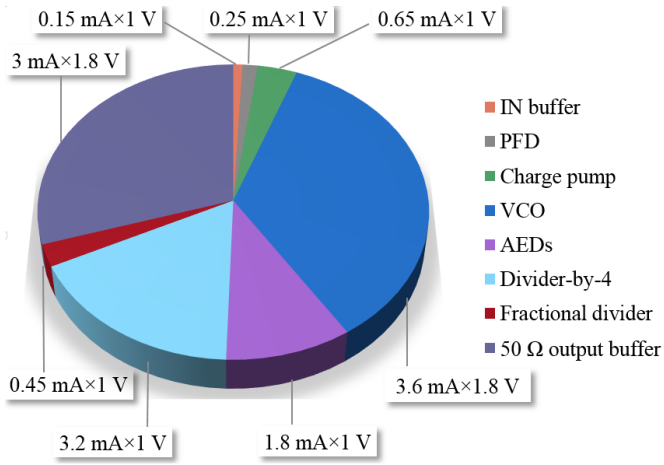


Figure 3.30: Power consumption of PLL's blocks.

	This work	[59]	[60]	[61]
Technology (nm)	65	130	130	65
f_{REF} (MHz)	31.25	60	16	50
f_{VCO} (GHz)	4	2.4	4.2	1
f_{measured} (GHz)	1	2.4	1.2	1
Power supply (V)	1.8: VCO and 50 Ω output buffer 1.0: other blocks	-	1.5	1.2
VCO type	LC	LC	LC	Ring
Division ratio	128	40.64	-	20
Bandwidth (kHz)	340	2000	80	-
$\mathcal{L}(\Delta f)$(dBc/Hz) @ 1 MHz	Measurrement: -111 Simulation*: -120	-99.6	-116.4	-97
Power (mW)	18.5	9.6	48	8.4
RMS jitter (ps)	Measurement: 1.4 @ 1 GHz Simulation*: 0.85 @ 1 GHz	-	-	4.54 @ 1 GHz
Area (mm^2)	0.3	0.46	1.5	0.32
$\mathcal{L}(\Delta f)_{NOM}$ (dBc/Hz)	Measurrement: -171 Simulation*: -180	-167.2	-182.4	-157
P_{NOM} (mW/GHz)	4.625	4	11.4	8.4

* w/o LDO noise.

Table 3.2: Performance summary and comparison with other designs.

Chapter 4

Digital phase-locked loop

4.1 Motivation for the implementation of a digital PLL

Electromagnetic compatibility (EMC) concepts have taken many attentions in integrated circuit design. The EMC determines the ability of the systems to perform their operation without degradation in electromagnetic loaded environment [62]. EMC concerns for integrated circuits can be generally classified into two main groups including intra-chip or externally-coupled [63]. Intra-chip EMC is considered as the result of the interferences between the signals or noises from different blocks on the same chip. On the other hand, the consideration for externally-coupled EMC as the name implies comes from the interferences with circuits or devices off-chip [63]. By scaling down the technology, reducing the power supply and designs with higher switching speed, the immunity of the circuits to the radio frequency interference generally decreases [64].
Various studies investigate the effect of electromagnetic interference (EMI) on the PLLs [65] [66]. In a PLL circuit, electromagnetic radiation with sufficient power level can affect the oscillator. This effect may lead to a frequency shift of the oscillator and degrades the output spectrum by adding spurious tones [65]. If the frequency of the EMI is close to the oscillation frequency of the VCO, the VCO frequency may be controlled by the frequency of the interference signal [67]. In a LC-based

VCO, the magnetic field around the inductor may couple with the surrounding magnetic fields from the external sources and result in undesired changes of the effective inductance value [68]. Besides, the integration of the inductors on chip takes large area and raises the cost. Therefore, ring oscillators are preferred over LC-based oscillators for the digital PLL in this thesis due to the target application in high magnetic field environments and the strong project requirement for low area consumption.
A digital PLL provides the benefits of smaller area as well as configurability and scalability with technology scaling. Therefore, it is an appropriate clock generator for area sensitive applications [69]. The goal of the digital PLL for this thesis is to present a structure with optimized power and area consumption. The noise characteristic of a digital PLL is worse in comparison with the analog correspondence, particularly when it is integrated with a ring oscillator [69]. The design for this thesis aims at a bandwidth optimization to present a high bandwidth design for higher suppression of the ring oscillator phase noise.

4.2 Introduction to the digital PLL

A digital PLL as an alternative for an analog PLL avoids the non-idealities of analog parts such as the charge pump and reduces the large die area by replacing the analog loop filter with a digital counterpart. In comparison with an analog PLL, the digital PLL provides scalability, portability and a high degree of programmability to cover the PVT variations [70] [71].
This chapter contains a detailed overview to the digital PLL design, its constituting blocks and their function. A high level modeling approach as well as some new methods to improve the digital PLL operation are presented. The simulation results in Simulink/Matlab which agree to the theoretical concepts are provided in both time and frequency domain.

4.3 Simulink and Matlab as modeling tools

During the SPICE-based design, several parameters should be changed to achieve the required characteristics. This is very time consuming especially for complex systems such as PLLs. Behavioral modeling is a beneficial method to estimate the design parameters and operation in a more time-efficient way.
Modeling in Simulink/Matlab gives high flexibility for the system design. In Matlab, mathematical expressions describe the design and in Simulink, the build-in blocks existing in its library represent the equations. It is tried to propose a realistic modeling for the high-level architecture implemented in Simulink/Matlab environment to estimate the design parameters close to the SPICE-based structure. The goal is to determine the design parameters and specifications like settling behavior, stability and noise behavior before the transistor level design.

4.4 Digital PLL architectures

Two common implementations of digital PLLs include divider-based [72] and accumulator-based [73] architectures. The structure of a divider-based digital PLL is shown in Figure 4.1 [74]. This design imitates the topology of the conventional analog PLLs. The time-to-digital converter (TDC) replaces the PFD/CP in analog PLLs. The TDC digitizes the phase difference between the reference clock and the

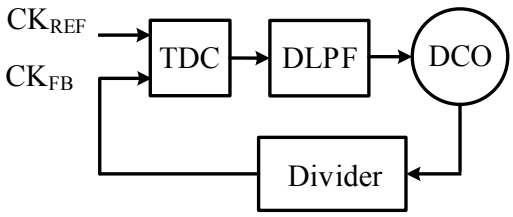


Figure 4.1: Divider-based digital PLL block diagram.

feedback clock. DCO and digital loop filter (DLPF) in the block diagram stand for digital-controlled oscillator and digital loop filter, respectively. The only practical implementation of a divider-based digital PLL is a type-II system to provide zero phase error between the reference and feedback clocks. It can hardly tolerate an unknown constant phase error resulting from a type-I operation [75].
On the other hand, the accumulator-based digital PLL can operate in type-I mode to accelerate the frequency locking [75] for high-speed applications.
In this thesis, an accumulator-based digital PLL is considered and its general behavior will be explained in the following sub-section.

4.4.1 Accumulator-based digital PLL

Figure 4.2 [73] shows a top-level block diagram of an accumulator-based digital PLL that has been implemented in Simulink.
The structure includes four main blocks, TDC, phase detector, DLPF and DCO. A D-flip flop is used as a re-timer, where the output clocks of the DCO, CK_{DCO}, sample CK_{REF} to generate the re-timed clocks, CK_R, to synchronize all sub-blocks.
The DCO as a critical block in the digital PLL generates the signal at output frequency, f_{out}, that in the locked state is given by the product of frequency control word (FCW) and reference frequency, f_{REF},

$$f_{out} = FCW \times f_{REF}. \tag{4.1}$$

During one CK_R period, the reference phase accumulator generates the reference phase, $R_R[k]$, by accumulating the FCW

$$R_R[k] = \sum_{l=0}^{k} FCW, \tag{4.2}$$

where the index number of k is the k-th transition of the CK_{REF}. The DCO phase accumulator provides the DCO's phase, $R_{DCO}[k]$, by counting the rising transitions of CK_{DCO},

$$R_{DCO}[k] = \sum_{l=0}^{i} 1 \Bigg|_{iT_{DCO}=kT_R}, \tag{4.3}$$

with i as the index number for the i-th transition of CK_{DCO}. T_{DCO} and T_R are the time period of the CK_{DCO} and CK_R, respectively.
The $\epsilon[k]$ at the output of the fractional error compensation part is based on the TDC operation, which measures the fractional delay difference between CK_{REF} and CK_{DCO}.
The phase detector performs an arithmetic subtraction of the phase information from the accumulators and the TDC to get the phase error information, $\varphi_e[k]$,

$$\varphi_e[k] = R_R[k] - R_{DCO}[k] + \epsilon[k]. \tag{4.4}$$

The phase error from the phase detector is transferred to the DLPF to produce the tuning word (TW). The TW is multiplied by the DCO gain normalization (GN) to prepare the oscillator tuning word (OTW) for the frequency adjustment of the DCO. The detailed description of the sub-blocks of the accumulator-based digital PLL and

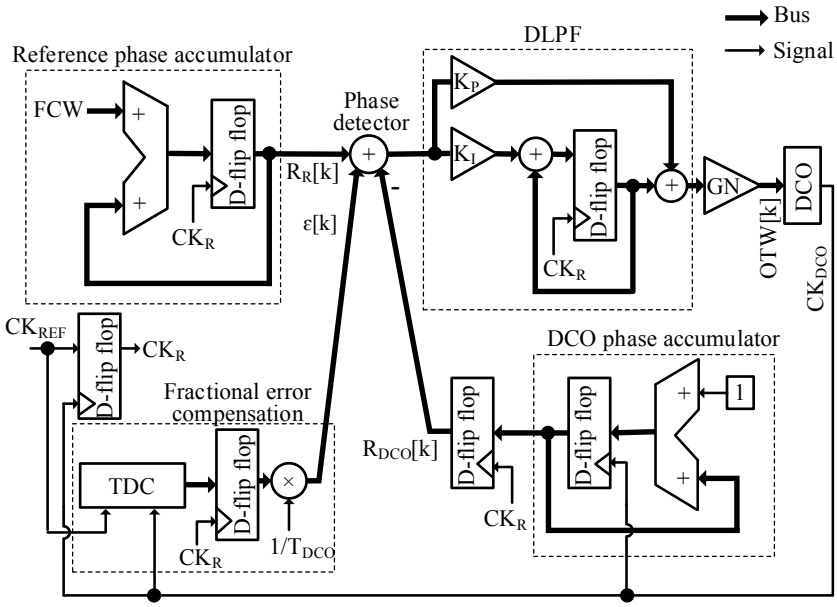


Figure 4.2: Accumulator-based digital PLL block diagram in Simulink.

their modeling procedure as well as the design parameters determination will be presented in the next sections.

4.5 Digitally-controlled oscillator

Basically, the difference between DCO and VCO exists in the way that the output frequency of the oscillator is tuned. The control of the DCO is implemented in a digital manner that is in contrast with the VCO that has an analog control voltage. The ring type oscillator without LC-tank is advantageous as it generates multi-phase clocks inherently without extra circuitry, consumes less area on chip and its power consumption reduces with scaling [76]. The ring type DCO is selected for the implementation of the digital PLL in this thesis based on the discussions in section 4.1. It is known that the ring DCO has poorer phase noise characteristics than LC-based DCO. Therefore, design techniques in the determination of the digital PLL bandwidth are used to alleviate the DCO's phase noise effect on the digital PLL phase noise behavior.
For characterization and comparison of the function of oscillators, some performance metrics are defined. The definition of some of them such as tuning range, phase noise, power consumption, tuning range linearity and monotonicity are common between VCO and DCO. The monotonicity with tuning word and frequency resolution as a characteristics specified for the DCO structure are among the important characteristics that will be introduced next:
Monotonicity with tuning word: Monotonicity of the tuning range is defined for both VCO and DCO. It is important that the output frequency of the DCO changes monotonically by increasing or decreasing the oscillator tuning word. Non-monotonic behavior increases jitter and may bring the digital PLL into unlock situation [77].
Frequency resolution: It refers to the minimum frequency step that can be obtained at the output of DCO.

4.5.1 Oscillation frequency of the ring oscillator

A ring oscillator system that consists of a number of delay stages connected in a feedback topology is shown in Figure 4.3.
It is simply assumed that every delay component is an inverter with C_L and R_L as the loading capacitance and resistance, respectively, at the output. The oscillation frequency of this structure with N delay block is defined as

$$f_{osc} = \frac{1}{2N\tau_d}, \tag{4.5}$$

where τ_d is the delay of each inverter and depends on the C_L and R_L ($\tau_d \propto C_L R_L$). The determined proportionality for τ_d can be written also as ($\tau_d \propto C_L \Delta V / I_D$), [78] where I_D is the current drive of the load and ΔV is the voltage swing at the output node.
Based on the equation for the oscillation frequency of the ring oscillator, the parameters of N, C_L and R_L can be used to build a controllable design. A variety of designs for the frequency tuning in the ring DCO namely capacitive loading, tri-state buffers and current starving are introduced.
The capacitive loading method [79] adjusts the frequency by tuning the capacitive loading at the output of every delay stage. This method leads to a design that occupies large area on chip and its power consumption is not scalable [80]. Also the tuning range with this method is limited. For the DCO using tri-state buffers, a set of tri-state buffers are connected in parallel with every delay element to tune the output frequency [81]. In the current starving approach, the driving strength of the

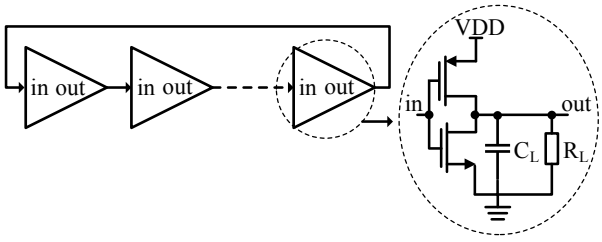


Figure 4.3: A model of the ring oscillator structure.

delay stages are changed by controlling their current drive [82]. In the following sections, tri-state buffer and current starving based ring DCOs will be introduced in more details and a final approach will be presented to improve the DCO frequency resolution.

4.5.2 Ring DCO based on parallel tri-state buffers

The schematic in Figure 4.4 is considered to find out the oscillation frequency changes using tri-state inverters. The inverter-based delay component in the main path is in parallel with a tri-state inverter that is activated or deactivated by applying a control bit (CB). When CB is high, which means the tri-state buffer is activated, the output currents of both paths are added at the output and the voltage swing increases while the capacitive loading stays approximately constant [83]. Therefore, the ring DCO can oscillate with a higher frequency if the tri-state inverter is activated. The overall design of the N-stage ring DCO using the tri-state inverters is depicted in Figure 4.5. Each column consists of one inverter in parallel with m tri-state inverters. Matching between the columns is necessary for multi-phase applications if all generated phases at the outputs of the delay stages are required. The sizes of the tri-state inverters are scaled within each column. The number of

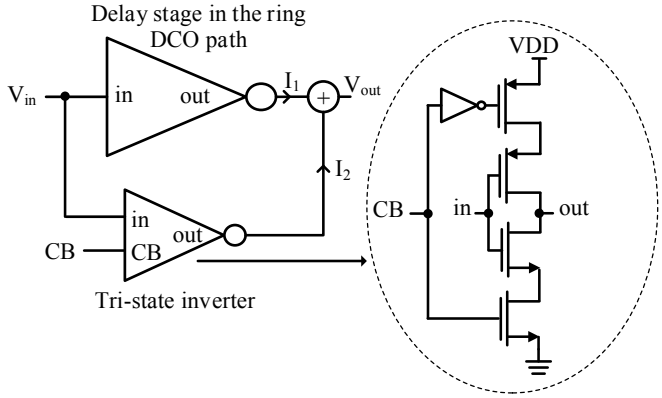


Figure 4.4: Schematic of inverter delay in parallel with a tri-state inverter.

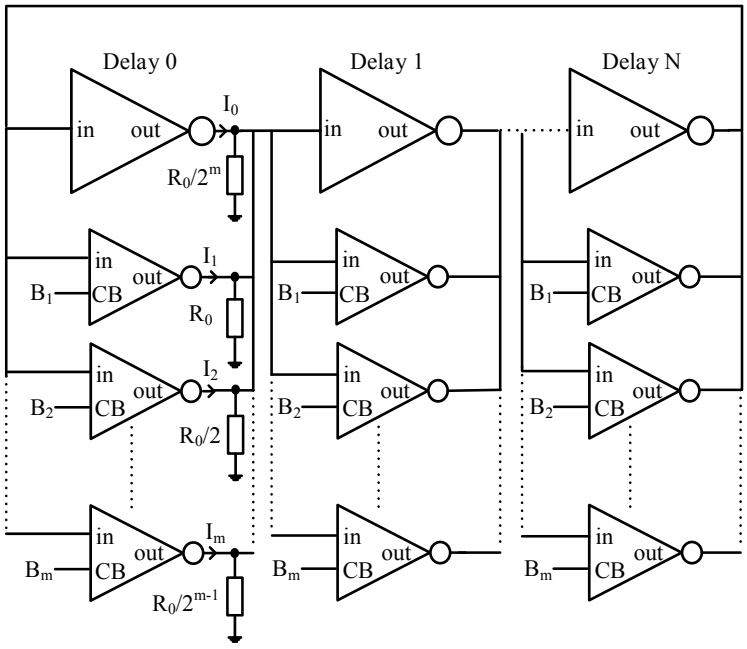


Figure 4.5: Ring DCO using tri-state inverters.

tri-state inverters in the column as well as their size are important to determine the frequency resolution, tuning range and the linearity of the frequency changes in the ring DCO.

Pseudo-thermometer code is one of the control approaches for the tri-state inverters in the ring DCO [83]. In comparison with Pseudo-thermometer code, if weighted binary codes are employed, for a specified frequency tuning range and resolution, smaller number of tri-state inverters is needed and the complexity and area consumption is reduced. In this method, the sizes of the tri-state inverters are determined on the basis of weighted scaling to keep the frequency changes monotonic and linear within the tuning range. The ratio of the voltage swing at the output of each inverter or tri-state inverter to the related driving current is represented as a resistor at their outputs as it can be observed in Figure 4.5.

When all tri-state buffers are deactivated the oscillation frequency is defined as

$$f_{osc} = \frac{2^m}{2NCR_0} = 2^m f_0. \tag{4.6}$$

For getting a monotonic and linear design by activating the tri-state inverters using the weighted binary code, the resistances at the outputs of stages is necessary to be scaled with increasing powers of 2 through scaling the size of tri-state inverters. The scaled values of the output resistances are also included in Figure 4.5.
The ring DCO frequency versus the control word is plotted in Figure 4.6, in which f_0 is the frequency resolution. The delay elements in the ring DCO using tri-state buffers can be implemented with the standard cells to enhance the portability but the resolution may be insufficient [84].

4.5.3 Ring DCO based on current starving

The current starving technique considers the current of the delay element in the ring DCO as a variable and enables the frequency tuning by controlling the supply current of the delay cell.
For the design of the DCO using this method, the delay component is implemented by two inverters [85]. The first inverter is based on current starving while the other inverter is a standard transistor configuration. The ring DCO based on current

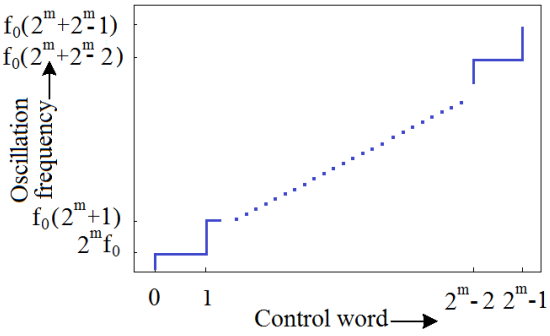


Figure 4.6: Variation of oscillation frequency in a ring DCO using tri-state inverters.

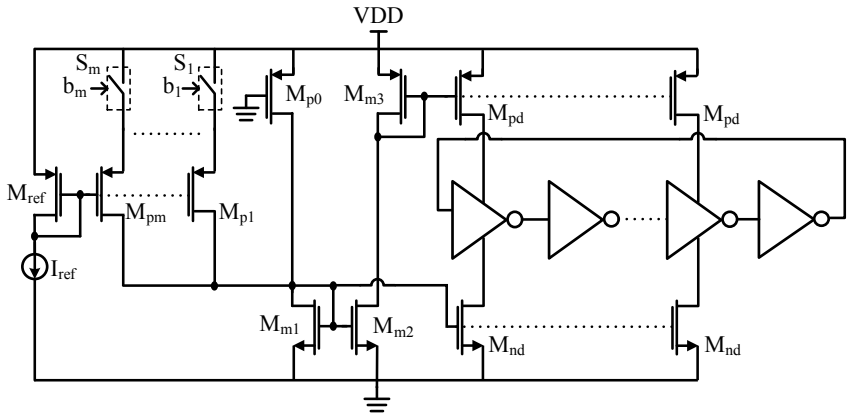


Figure 4.7: Ring DCO using current starving.

starving is shown in Figure 4.7. The top PMOS transistor, M_{pd}, changes the charging current at the output node of the delay components according to the control bits and the NMOS transistor, M_{nd}, varies the discharging current. Binary weighted coding is used to control the switches, S_1 to S_m, and so the sizes of PMOS current sources, M_{p1} to M_{pm}, should be binary weighted to ensure monotonicity for the topology. The transistors, M_{m1} to M_{m3}, mirror the tuned current to the delay elements through M_{nd} and M_{pd} and M_{p0} is intended to maintain the minimum oscillation frequency when the control word is zero.
One important benefit of this structure over the tri-state based DCO is its higher resolution but the static power can increase due to the static current source [84].

4.5.4 Proposed approach for the DCO

According to previous discussions about DCO structures, a final design is proposed. The proposed DCO combines the previous introduced designs to provide the best trade-off between their advantages and disadvantages. The aim is to meet a high resolution design with linear, monotonic and wide tuning range to cover the required oscillation frequency in case of process and temperature variations. Figure 4.8 shows the final approach for the DCO. The frequency control is partitioned into

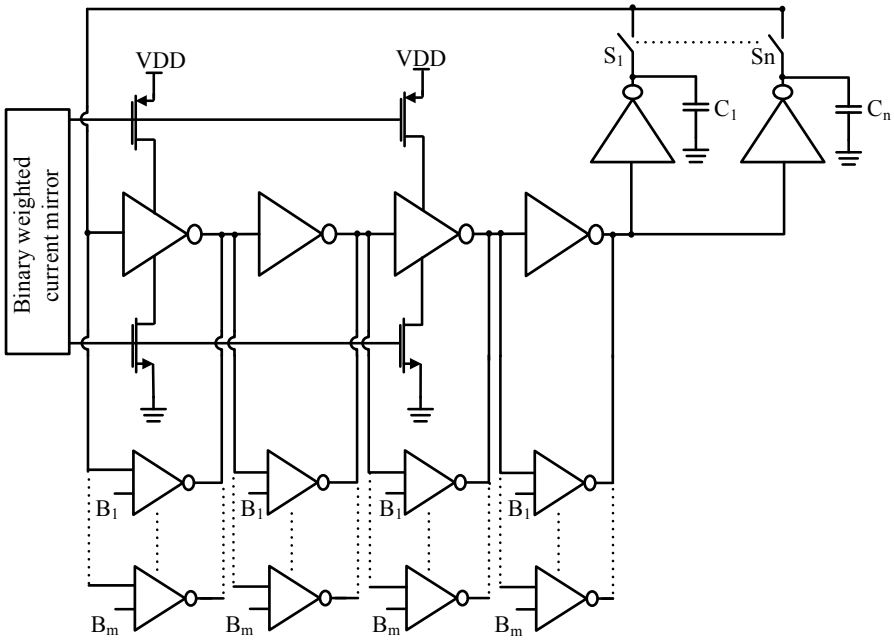


Figure 4.8: Proposed approach for the DCO.

three modes according to Figure 4.9 with separate tuning settings.
The frequency of the DCO is coarse tuned by changing the loading capacitor of the last delay component in the ring structure. Each capacitor gives the loading for the last delay component by activating the related switch (S_1 to S_n). One-hot coding is applied to the switches, which means the activation of just one of the switches at a time. The highest frequency is obtained when the switch to the minimum loading capacitor is activated in the ring, which means S_1 is on. The capacitor values are selected on the basis of the minimum and maximum limits for the total tuning range of the DCO and also the required frequency steps Δf_{S1} to $\Delta f_{S(n-1)}$ within the coarse tuning range.
The fine tuning is performed within two separated modes using tri-state buffers and current starving methods. First, m stages of tri-state buffers in parallel with

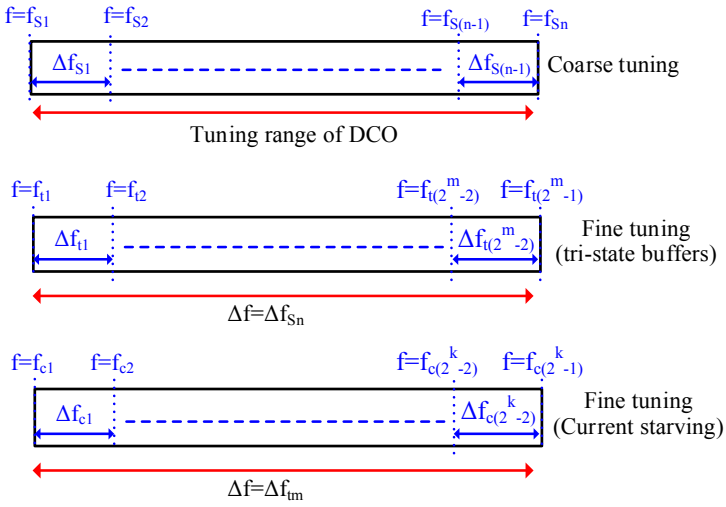


Figure 4.9: Frequency tuning concept for the proposed DCO.

delay components create '$2^m - 1$' frequency values for each Δf_{sn} as is depicted in Figure 4.9.

The final mode determines the frequency resolution of the DCO using the current starving method. The current starving topology divides down Δf_{tm} to '$2^k - 1$'frequencies. The designation of the number of control bits in each mode depends on the required resolution and tuning range of the DCO.

4.5.5 Proposed DCO design in Simulink

In the previous section, an approach for the DCO to realize the design requirements was introduced. In this section, a model for the DCO in Simulink is proposed. The suggested model is depicted in Figure 4.10 [86]. The design consists of the delay components, loop gain and saturation blocks.
The generated oscillator tuning word (*OTW*) is given to a Bit-to-Integer converter block that converts the *OTW* bit vector to integer values. This removs the need for the complicated signal routing through the decoders and multiplexers in Simulink especially when the number of *OTW* bits increase. The integer values at the output of the Bit-to-Integer converter are used as control word (*CW*) for the delay components in the DCO loop to tune the the output frequency of the DCO.
Initial conditions are necessary to force a high or low state at the start of oscillation. Therefore, a narrow pulse is injected to the DCO to start-up the oscillation.
The satuartion block limits the high and low levels of its input signal based on the defined values of the block parameters. Otherwise, the oscillation amplitude grows continuously in the loop.
The loop gain, K_L, must be selected in a way to realize the oscillation conditions based on the Barkhausen criterion as explained in section 3.2. The model of the delay components includes the design parameters such as DCO gain, oscillation frequency and resolution.
Figure 4.11 introduces the linear model of delay elements in s-domain.

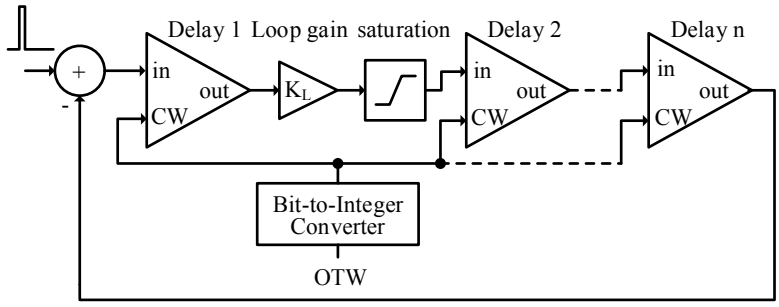


Figure 4.10: Proposed DCO model in Simulink.

The transfer function from the input to the output of the delay element corresponds to the transfer function of a transistor based delay element considering the dominant poles and zeros. The transfer function of each delay component, $H(s)$, evaluated at $s = j\omega$, is used to obtain the total loop gain, $H_T(j\omega)$, for n delay stages.
Accordingly,

$$H(j\omega) = \frac{1}{1 + \frac{j\omega}{\alpha\omega_f}}, \tag{4.7}$$

$$H_T(j\omega) = K_L(H(j\omega))^n. \tag{4.8}$$

Corresponding to the Barkhausen criterion, a phase shift of π is needed in the feedback loop to start the oscillation with the frequency of ω_{osc},

$$tan^{-1}\left(\frac{\omega_{osc}}{\alpha\omega_f}\right) = \frac{\pi}{n}. \tag{4.9}$$

It is intended in the frequency domain model to have $\omega_f = \omega_{osc}$, thus

$$\alpha = \frac{1}{tan\left(\frac{\pi}{n}\right)}. \tag{4.10}$$

For an stable oscillation,

$$|K_L(H(j\omega))^n| \geq 1, \tag{4.11}$$

which gives the K_L value as

$$K_L \geq \left[1 + tan^2\left(\frac{\pi}{n}\right)\right]^{n/2}. \tag{4.12}$$

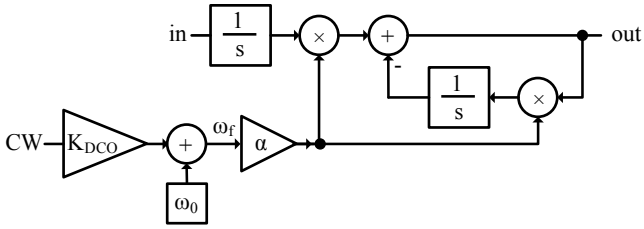


Figure 4.11: The delay component model in s-domain.

K_{DCO} in equidistant steps determines the DCO gain that is defined by the output frequency changes, Δf_{DCO}, in response to one LSB change of the OTW, [87]

$$K_{DCO} = \frac{\Delta f_{DCO}}{2^b}, \tag{4.13}$$

where b refers to the number of bits of the OTW. Finally, the oscillator runs with the frequency of

$$\omega_{osc} = \omega_0 + (CW \cdot K_{DCO}), \tag{4.14}$$

in which the free running frequency, ω_0 and K_{DCO} are determined based on the design specifications to maintain functionality in case of temperature and process changes in the transistor-based implementations.

4.6 Time-to-digital converter

4.6.1 General considerations

A time-to-digital converter converts time as an analog quantity to the digital domain. The concept of TDC operation can be described based on Figure 4.12 [88], which is used to clarify the performance parameters of the TDC.
The start and stop signals with their rising edges at times, T_{start} and T_{stop}, respectively, are the input signals to the TDC. The basic procedure to quantize a time interval ($T_{in} = T_{start} - T_{stop}$) is based on a counter to count the cycles of a reference clock with the period of T_{res} within T_{in}. T_{in} can be defined as [88]

$$\begin{aligned} T_{in} &= NT_{res} + (T_{res} - \Delta T_{stop}) - (T_{res} - \Delta T_{start}) \\ &= NT_{res} + \Delta T_{start} - \Delta T_{stop} \\ &= NT_{res} + q_{error}, \end{aligned} \tag{4.15}$$

where N is the counted value.
The quantization error, q_{error}, occurs at the beginning and the end of the measurement interval. ΔT_{start} is the time interval between the rising edge of the start signal and the next rising edge of the reference clock. The same explanation applies to ΔT_{stop}

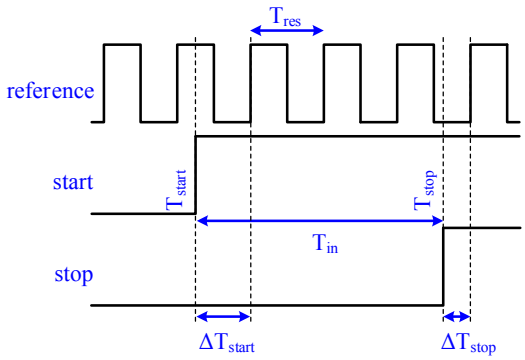


Figure 4.12: TDC conceptual waveforms.

for the stop signal. The quantization error happens as the result of a limited number of reference clocks, i.e. limited resolution (T_{res}). The resolution of a TDC, which is referred to as the minimum time variable that can be quantized by the TDC [89], is an important parameter to be considered in the design of the TDC. The TDC resolution impacts the performance of the digital PLL and mainly determines the in-band noise of the digital PLL [72].

4.6.2 An overview of TDC architectures

The need for high resolution TDCs increases as CMOS technology is scaled. It is important to a have a review over some of the basic designs for TDC and introduce their pros and cons. At the end a new design for the TDC is proposed to realize the requirements for the considered application.

4.6.2.1 TDC with gate and sub-gate delay resolution

Delay-line TDC: This is a classical approach [90] in which the start signal propagates through a delay chain as in Figure 4.13. The state of the start signal at the output of each delay element is sampled by a stop signal through the sampling ele-

ments (D-flip flops). The outputs of the sampling elements result in a thermometer code. The position of the high-low transition in this code indicates the time interval between the start and stop signals.
The simple structure and the high speed operation are the strength points of the design but the limited time resolution due to the CMOS gate delay is a negative aspect that causes limited time resolution [76].
Vernier TDC: The idea of the Vernier TDC [91], [92] is to improve the time resolution of the delay-line TDC. It is capable of measuring time intervals with a resolution of sub-gate delay [93]. The Vernier TDC consists of two delay chains with the same number of delay elements for the start and stop signal as shown in Figure 4.14. The start signal propagates through the first delay chain with a delay per element of τ_1 and the stop signal goes through the second delay line with a delay of τ_2 per element. The stop signal follows the start signal and the time interval between the rising edges of the start and stop signals is detected and kept by the D-flip flops. It is assumed that τ_1 is larger than τ_2 and the effective resolution is given by

$$\Delta = \tau_1 - \tau_2. \tag{4.16}$$

The structure can provide high resolution especially when τ_1 is close to τ_2. The dynamic range of a TDC is defined as the maximum time interval that can be quantized while the performance specifications [89] are kept. For the Vernier TDC,

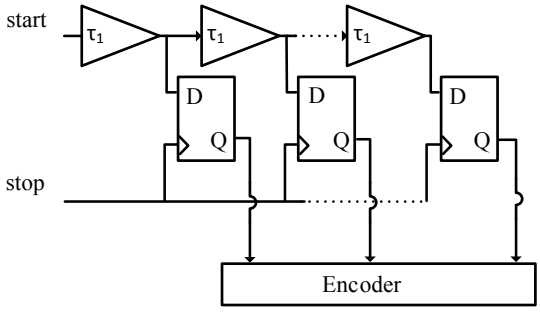


Figure 4.13: Block diagram of delay-line TDC.

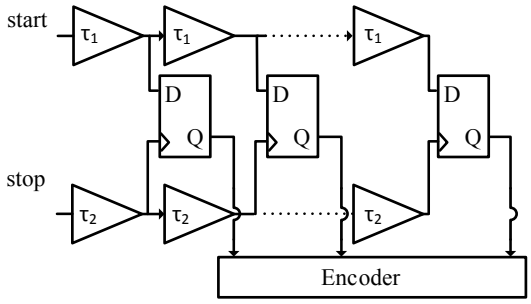


Figure 4.14: Block diagram of Vernier TDC.

a large number of delay elements are required to cover a large dynamic range, which increases the area and power consumption for this structure as well as the conversion time [94] that is needed by the TDC to quantize the time interval.

4.6.3 Gated ring oscillator TDC as a case of oversampling and noise shaping TDCs

Oversampling and noise shaping are among the techniques to improve greatly the effective resolution of the TDC [95].
In the oversampling method, a slowly varying signal is sampled with a higher frequency than the Nyquist rate to distribute in-band quantization noise over the oversampling frequency range.
Noise shaping is complementary technique to increase the resolution. The concept is to transfer the quantization noise at low frequencies towards the high frequencies that later will be filtered out by the loop filter in the digital PLL structure.
The gated ring oscillator TDC (GRO-TDC) [96], [97] applies oversampling and noise shaping to increase the resolution. Figure 4.15 (a) shows the block diagram of the GRO-TDC with a ring oscillator as its core [97], in which the delay elements are gated by a control signal (Enable).
The operation is explained based on the quantization process in Figure 4.15 (b). The

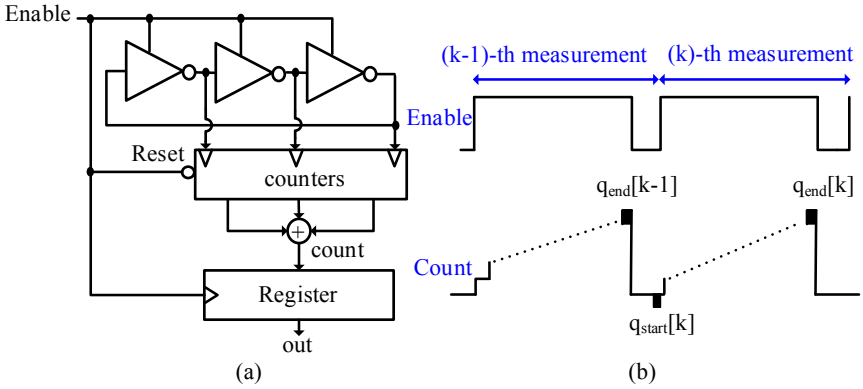


Figure 4.15: (a) Block diagram of the GRO-TDC, (b) quantization process.

Enable signal, which its generation is explained in sub-section 4.6.4 is extracted from two inputs to the TDC. Its pulse width is the time that must be converted to digital domain. While Enable signal is active, i.e. during the measurement interval, the ring oscillator is active and the transitions of the ring oscillator are counted. As soon as the Enable signal falls into inactivity, which happens at the end of the measurement interval, the ring oscillator is deactivated and its phase state is kept. Therefore, the quantization error at the end of a measurement interval (i.e. (k-1)-th measurement), $q_{end}[k-1]$, is preserved and carried over to the start of the next measurement interval (i.e. (k)-th measurement), $q_{start}[k]$. This gives the first order noise shaping that is further examined by the mathematical relation for the overall quantization noise [97], $q_{error}[k]$.

$$q_{error}[k] = q_{end}[k] - q_{start}[k], \tag{4.17}$$

in which, $q_{start}[k] = q_{end}[k-1] = q[k-1]$, due to the quantization error transfer. Thus

$$q_{error}[k] = q[k] - q[k-1]. \tag{4.18}$$

By transferring (4.18) to the frequency domain, the equivalent noise transfer function can be determined as

$$NTF(z) = 1 - z^{-1}. \tag{4.19}$$

The noise spectral density gets multiplied by this noise transfer function. Therefore, low frequency noise components are transferred to higher frequencies.
Along with the high resolution that the GRO-TDC gives, there are some imperfections for the structure. The ring oscillator is stopped during the inactivation time of the Enable signal and its output nodes are floating. The floating nodes are vulnerable to external disturbances [98] and they are exposed to the leakage and charge redistribution [99] that also increase with technology scaling. The errors prevent the output phase to be completely preserved and cause the variation of the output phase during the inactivity of the Enable signal that is referred to as skew error [100]. Furthermore, the gating delay, which means the incapability to start or stop the GRO immediately, causes skew error [95]. This kind of errors are not shaped and degrade the noise characteristics.
The suggested design for the TDC in this thesis will mitigate the shortcomings of the GRO-TDC defects.

4.6.4 Proposed design of the TDC

Based on the prior explanations, a novel structure for the TDC is proposed to suppress the errors associated with GRO-TDC. Figure 4.16 shows the implemented design of the TDC in Simulink and Figure 4.17 depicts its operation.
The ring oscillator generates M clock phases at a frequency to realize the oversampling condition. The pulse generator provides CK_{EN}. Its pulse width is the time interval between the rising edges of the inputs to the TDC, CK_{REF} and CK_{DCO}. This time interval will be converted to a digital word by the TDC operation. A counter accumulates the clock transitions at the output of the ring oscillator within the CK_{EN} period and the rising edge of CK_{EN} resets the counter's output. The multiplication by $2M$ at the output of the counter is to consider both rising and falling edge transitions in the ring oscillator. This provides the coarse quantization of the time interval. M registers that are implemented using D-flip flops take their inputs from the outputs of the ring oscillator. They are triggered by the rising edge of the CK_{EN} and track the phase information of the ring oscillator's outputs within one CK_{EN} period. This means fine quantization information.

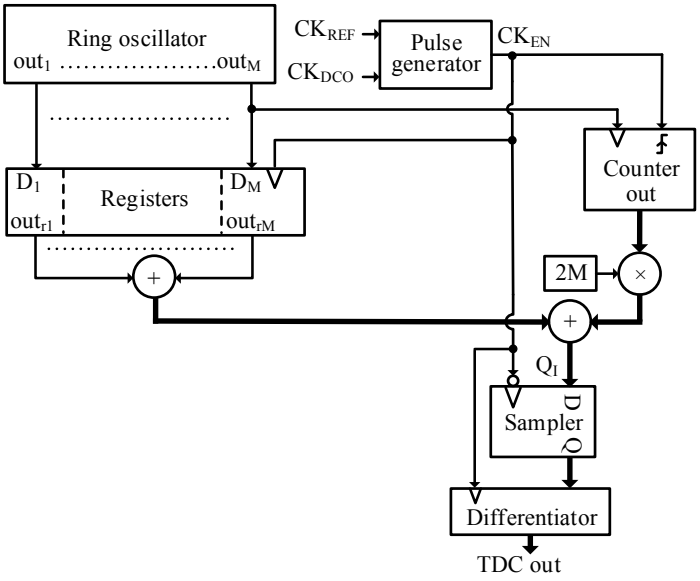


Figure 4.16: Proposed TDC design in Simulink.

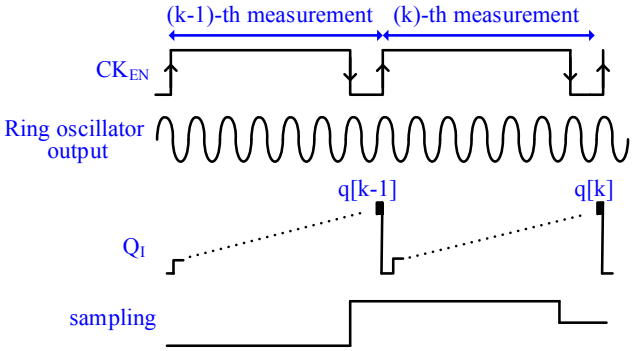


Figure 4.17: Operation of the proposed TDC by its waveforms.

In this proposed design, the ring oscillator is not deactivated and generates clocks continuously during one CK_{EN} period to remove the gating problems associated with GRO-TDC. The continuity of the quantization within the CK_{EN} period im-

plements the concept of the quantization noise transfer at the end of the current measurement interval to the start of the next measurement that is needed for the first order noise shaping. The quantized information at the outputs of the counter and the registers (Q_I) are going through a sampler block. This sampler block samples Q_I with the falling edge of CK_{EN} to give the quantized time interval between the rising edges of CK_{REF} and CK_{DCO}. The final results are obtained at the output of the differentiator.

4.7 Digital loop filter

The digital loop filter (DLPF) is an important block due to the role of the filter factors in the determination of the digital PLL loop dynamics, including stability, settling time and noise performance. The binary information from the phase detector, $\varphi_e[k]$, is given to the DLPF in the digital PLL. The generated control bits, $TW[k]$, at the output of the DLPF, specify the DCO tuning word after normalization.
There are different architectures for the DLPF. Their selection depends on the design specification and noise suppression requirements. A proportional-integral (PI) loop filter is a common used approach for digital PLL design [87].
The time-domain implementation of this topology in Simulink was included in Figure 4.2. The proportional path with the coefficient of K_P connects directly the output of the phase detector to the DCO. The loop filter with only the proportional path results in a type-I digital PLL. A type-I PLL shows faster dynamics in lock acquisition [87], but its noise attenuation is poor. Adding the integral path with the coefficient of K_I leads to a type-II loop with better noise performance.
The DLPF z-domain model is shown in Figure 4.18, in which the delay block with the transfer function of z^{-1} corresponds to the register (D-flip flop) in the time domain implementation of the DLPF.
The discrete-time domain description of the PI-DLPF is given by

$$TW[k] = K_P \cdot \varphi_e[k] - K_P \cdot \varphi_e[k-1] + K_I \cdot \varphi_e[k-1] + TW[k-1], \tag{4.20}$$

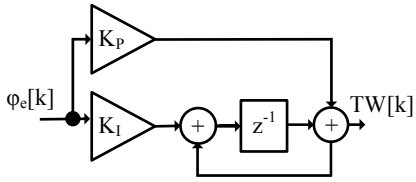


Figure 4.18: DLPF z-domain model.

which results in the following z-domain transfer function,

$$\frac{TW(z)}{\varphi(z)} = K_P + \frac{K_I z^{-1}}{1 - z^{-1}}. \tag{4.21}$$

For the improvement of the noise suppression, higher order loops can be employed by cascading infinite impulse response (IIR) or finite impulse response (FIR) filters [101] with the PI-filter but this is likely to create stability challenges for the digital PLL. For the type-II loop, the value of K_P determines the speed of the loop response to the phase difference at the filter input and its value is normally larger than K_I [87].
An extensive analysis to find out the optimum value for the loop filter coefficients will be conducted in section 4.10.

4.8 Digital PLL in frequency domain

The functionality of the sub-blocks of digital PLL in the time domain were investigated. In order to explore the loop dynamics and characteristics of the digital PLL, a frequency domain analysis is needed.

4.8.1 Digital PLL in z-domain

The frequency domain model of the digital PLL based on the transfer function between the input and the output of the building blocks is a useful tool for the linear

analysis of the digital PLL.
Regarding the discrete structure of the digital PLL, the z-domain analysis is the most accurate modeling as is shown in Figure 4.19 [73], that is compatible with the time domain model of the digital PLL in Figure 4.2. Each block in the time-domain model is replaced with its z-domain representation.
The open loop transfer function of the digital PLL in Figure 4.19 is extracted as

$$H_{ol}(z) = \frac{K_P(z-1)+K_I}{(z-1)^2}, \tag{4.22}$$

which is used to obtain the closed loop transfer function for the type-II loop,

$$H_{cl}(z) = \frac{K_P(z-1)+K_I}{(z-1)^2+K_P(z-1)+K_I}. \tag{4.23}$$

Although the z-domain model is the exact method to describe the digital PLL, it is easier and more common to estimate the digital PLL behavior with a continuous time model in s-domain [102]. The validity of this model depends on the digital PLL loop bandwidth. It is defined in [103] that the sampling frequency, which is the reference frequency here (f_{REF}) must be at least ten times more than the PLL bandwidth to apply the estimation. Therefore, for the z-operator

$$z = e^{j\omega/f_{REF}}, \tag{4.24}$$

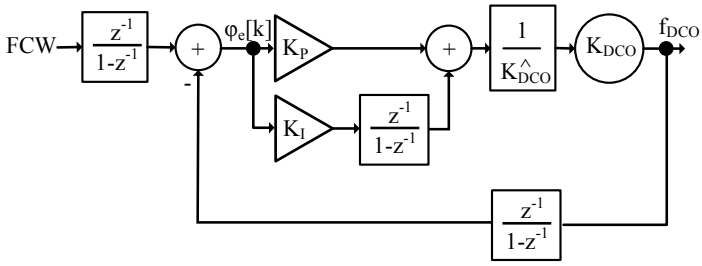


Figure 4.19: z-domain model of digital PLL.

the following approximation is valid [104],

$$z \approx 1 + j\omega / f_{REF} = 1 + s / f_{REF}. \tag{4.25}$$

4.8.2 Digital PLL in s-domain

Placing equation (4.25) in $H_{ol}(z)$ and $H_{cl}(z)$ will give the continuous time approximation of the open loop and closed loop transfer functions in s-domain,

$$H_{ol}(s) = \frac{K_P f_{REF} s + K_I f_{REF}^2}{s^2}, \tag{4.26}$$

$$H_{cl}(s) = FCW \frac{K_P f_{REF} s + K_I f_{REF}^2}{s^2 + K_P f_{REF} s + K_I f_{REF}^2}. \tag{4.27}$$

Figure 4.20 is the block diagram implementation of $H_{ol}(s)$ and $H_{cl}(s)$ for a type-II digital PLL.
Equation (4.27) can be written as the conventional two-pole system [73], [13],

$$H_{cl}(s) = FCW \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{4.28}$$

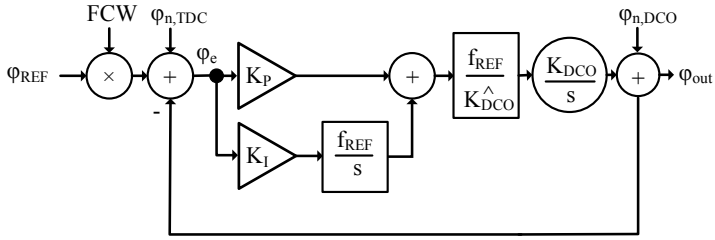


Figure 4.20: s-domain model of digital PLL.

ζ and ω_n are the damping factor and the natural frequency of the system, which are related to the digital PLL parameters as

$$\omega_n = f_{REF}\sqrt{K_I}, \tag{4.29}$$

$$\zeta = \frac{K_P}{2\sqrt{K_I}}. \tag{4.30}$$

For values of $\zeta < 0.5$, severe ringing will be observed in the step response of the system that is referred to as under-damped response. For prevention of extreme ringing $\zeta \geq \sqrt{2}/2$ is selected [105]. Furthermore, it is stated in [13] that for $\zeta \geq \sqrt{2}/2$, the loop bandwidth, ω_{3dB}, can be approximated as

$$\omega_{3dB} \approx 2\zeta\omega_n. \tag{4.31}$$

Therefore, the dependency of ω_{3dB} on the PI-filter coefficients is found,

$$\omega_{3dB} \approx f_{REF}K_P, \tag{4.32}$$

which approves the importance of K_P in determining ω_{3dB}. Therefore, the dependency of ζ and ω_{3dB} on the coefficients of the digital loop filter are determined and the simulation results illustrate their relations in the following sections. The parameters of ζ and ω_{3dB} are important to determine stability, settling behavior and noise characteristics of the digital PLL.

4.8.3 Digital PLL implementation and simulation results in Simulink

The same reference frequency as for the PLL in chapter 3 is given to the digital PLL, i.e. 31.25 MHz. The DCO is developed to generate the output clocks with the frequency of 1 GHz. Hence, FCW is set to as 32.
For the investigation of the step response of the system, the transfer function from the TDC to the output of the digital PLL, $H_{TDC}(s)$, is calculated,

$$H_{TDC}(s) = \frac{K_P f_{REF} s + K_I f_{REF}^2}{s^2 + K_P f_{REF} s + K_I f_{REF}^2}. \tag{4.33}$$

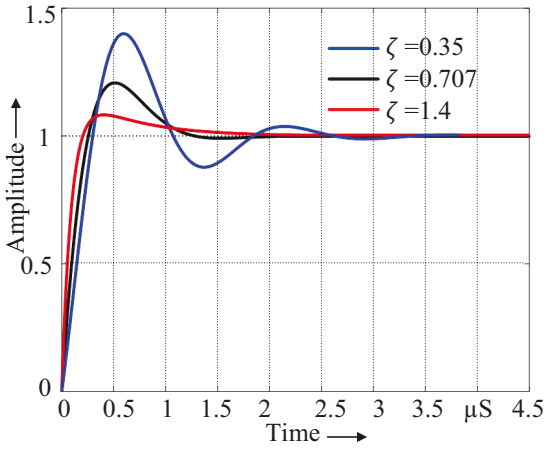


Figure 4.21: Step response for $H_{TDC}(s)$.

The simulation results of the step response of $H_{TDC}(s)$ for various values of ζ are shown in Figure 4.21. In the underdamped case (ζ=0.35), a big overshoot and ringing of the step response is observed before the settling. This causes a peaking in the noise transfer function and raises the jitter of the digital PLL [106]. Thus, $\zeta \geq 0.707$, is an appropriate range for this design.

The phase margin is an indicator for the stability of the system. Therefore, the parameters that affect the phase margin are examined. First, a constant $\zeta = \sqrt{2}/2$ is assumed while ω_{3dB} is changed. For the condition of a constant ζ, K_P and K_I must change simultaneously. It can be seen in Figure 4.22 that for a constant ζ, changing the loop filter coefficients varies the loop bandwidth while the phase margin (PM) stays the same and here is equal to 65°.

In addition, the simulation results extracted from the bode plots confirm the approximate linear relation of ω_{3dB} and K_P. This relation is depicted in Figure 4.23.

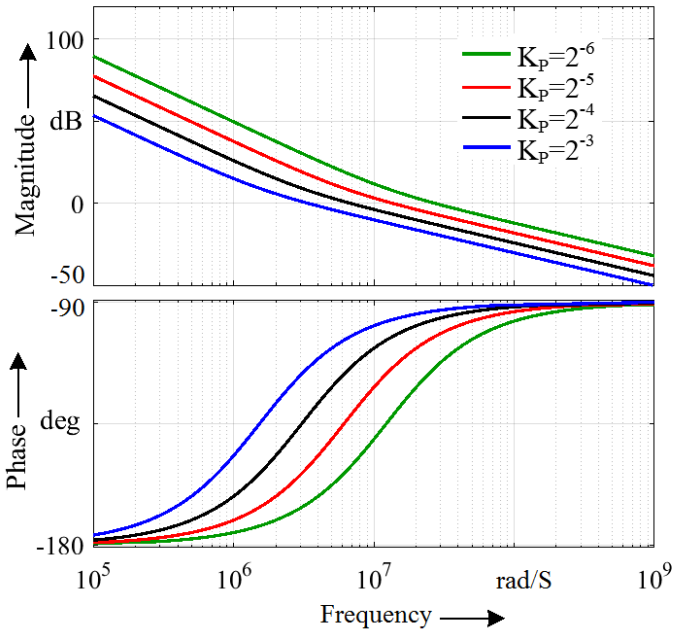


Figure 4.22: Bode plot of $H_{ol}(s)$ for $\zeta = \sqrt{2}/2$.

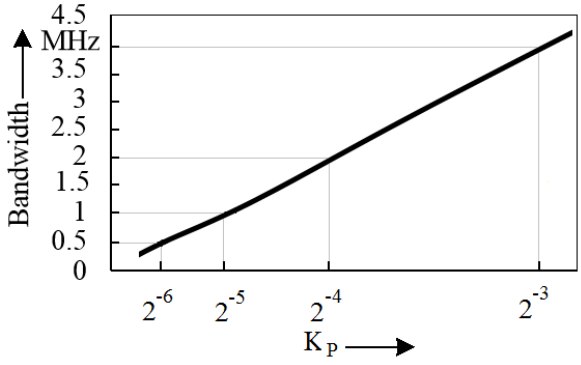


Figure 4.23: Dependency of loop bandwidth on K_P.

In the next step, ζ is varied by changing K_P. Increasing K_P and ζ shows positive effect on the phase margin as is examined in Figure 4.24. On the other hand, an

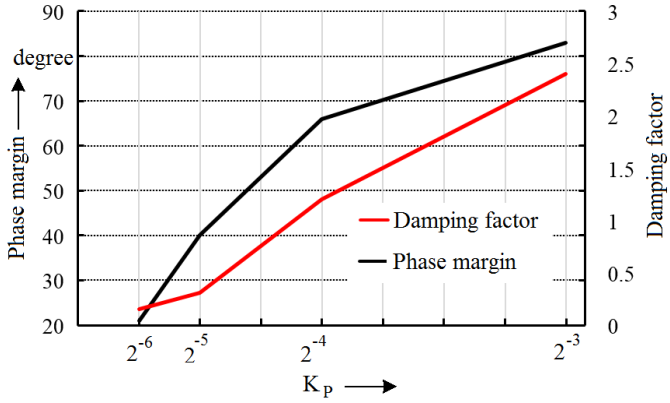


Figure 4.24: Variation of phase margin with K_P and ζ changes.

increase of K_P widens the bandwidth, which determines the settling time and noise behavior of the system. The settling time of the PLL is a performance metric related to the required time for the loop to get into the locking range. Thus, finding the optimum value for the loop filter coefficients depends strongly also on the noise and settling time of the system.
The s-domain simulations for the digital PLL were implemented using transfer functions in Matlab and also the corresponding blocks in Simulink by applying the control design library. The final results using these two approaches were totally compatible.

4.9 Noise analysis for the digital PLL

The phase noise of the DCO and the quantization noise of the TDC are known as the main contributors to the output phase noise of the digital PLL [72].

4.9.1 DCO noise model

Phase noise of DCO can be modeled using jitter ($1/\omega^0$) and wander ($1/\omega^2$) constructs [107]. For modeling the jitter noise, it is assumed that for an oscillator with the frequency of $f_0 = 1/T_0$, the oscillation events occur at integer factors of T_0 (i.e. $T_0, T_1, ...$) as in Figure 4.25. The random fluctuations cause delay in the oscillation occurrence time (time-stamp). Therefore, the real time-stamps, $t_j[k]$, for k oscillation cycles is expressed as [107]

$$t_j[k] = kT_0 + \Delta t[k], \tag{4.34}$$

where the second term is the timing deviation from the ideal time-stamp. The time deviations are independent and identically distributed. This create the noise floor of $\mathcal{L}$ that is independent of the offset frequency.
The following equation is used to extract the RMS jitter, $\sigma_{\Delta t}$, for non-accumulated jitter [107]

$$\sigma_{\Delta t} = \frac{T_0}{2\pi}\sqrt{\mathcal{L}f_0}. \tag{4.35}$$

In addition, the modeling of accumulative jitter (wander noise) is considered, in which the deviation in each time-stamp depends on the previous oscillator period fluctuations as shown in Figure 4.26. In this case, the actual time-stamp is declared as [107]

$$t_w[k] = kT_0 + \sum_{l=1}^{k} \Delta T[l]. \tag{4.36}$$

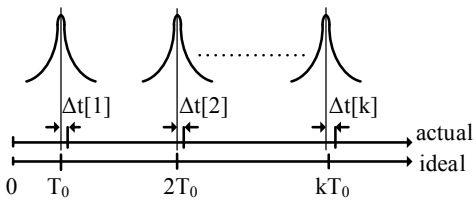


Figure 4.25: Development of timing jitter.

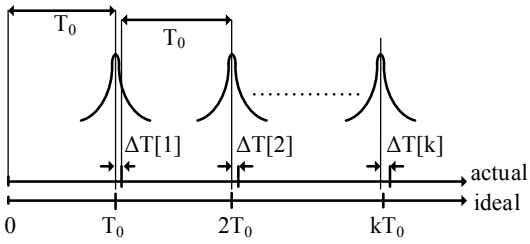


Figure 4.26: Development of accumulative jitter.

The $\sigma_{\Delta t}$ for this kind of jitter with the phase noise of $\mathcal{L}(\Delta\omega)$ at the offset frequency of $\Delta\omega$ is extracted as [107]

$$\sigma_{\Delta t=} = T_0 \Delta\omega \sqrt{\frac{\mathcal{L}(\Delta\omega)}{2\pi\omega_0}}. \tag{4.37}$$

It is assumed that the $1/\omega^3$ corner frequency is inside the loop bandwidth of the digital PLL with the negligible contribution.
The transfer function from the digital PLL output to the DCO noise, $\varphi_{n,DCO}$, is introduced to analyze the DCO noise contribution to the digital PLL noise profile,

$$H_{DCO}(s) = \frac{s^2}{s^2 + K_P f_{REF} s + K_I f_{REF}^2}. \tag{4.38}$$

The noise shaping of the DCO at the output of digital PLL, $\mathcal{L}_{out,DCO}(f)$ for the single side band noise power spectral density of the DCO, $\mathcal{L}_{DCO}(f)$, is given as

$$\mathcal{L}_{out,DCO}(f) = \mathcal{L}_{DCO}(f)|H_{DCO}(j2\pi f)|^2. \tag{4.39}$$

The DCO noise shows a high-pass characteristic within the digital PLL that means extending the loop bandwidth helps further to filter out the DCO noise.

4.9.2 TDC noise model

The limited resolution of the TDC leads to quantization noise that affects the phase noise of the digital PLL and was added into digital PLL model as $\varphi_{n,TDC}$ in Figure 4.20. The TDC resolution determines the in-band phase noise of the digital PLL [100].

For a TDC with the time resolution of T_{res}, the variance of the timing error is calculated as [108]

$$\sigma_t^2 = \frac{T_{res}^2}{12}, \tag{4.40}$$

As in [108], the phase noise is calculated by normalizing σ_t to the unit interval and multiplying by 2π,

$$\sigma_\varphi = \frac{2\pi\sigma_t}{T_{DCO}}. \tag{4.41}$$

The total phase noise has uniform distribution over the range from dc to Nyquist frequency [108]. Therefore, the phase noise spectrum as the result of TDC quantization noise at the output of the digital PLL is,

$$\mathcal{L}_{TDC} = 10\log\Big[\frac{(2\pi FCW)^2}{T_{REF}}\frac{T_{res}^2}{12}\Big]. \tag{4.42}$$

Considering equation (4.33), the output noise resulting from the TDC is

$$\mathcal{L}_{out,TDC}(f) = \mathcal{L}_{TDC}|H_{TDC}(j2\pi f)|^2, \tag{4.43}$$

which shows that the noise of a conventional TDC is low pass filtered in the digital PLL.

Therefore, lowering the loop bandwidth for a conventional TDC suppresses the noise. A TDC structure with noise-shaping was introduced in section 4.6.4 to carry the TDC noise at low frequencies to higher frequencies. Equation (4.43) is changed by taking into account the noise transfer function (4.19) to apply noise-shaping,

$$\begin{aligned}\mathcal{L}_{out,TDC}(f) &= \mathcal{L}_{TDC}|H_{TDC}(j2\pi f)|^2|1-e^{-j\omega/f_{REF}}|^2,\\ &\approx \mathcal{L}_{TDC}|H_{TDC}(j2\pi f)|^2\left[\frac{(2\pi f)^2}{f_{REF}^2+(2\pi f)^2}\right].\end{aligned} \tag{4.44}$$

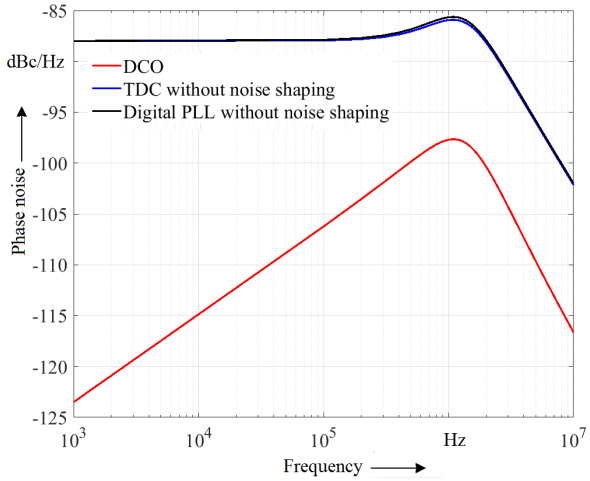


Figure 4.27: Phase noise characteristic without noise shaping.

The $\mathcal{L}_{out,TDC}(f)$ with noise shaping removes the need for a low bandwidth to improve the noise behavior. This combination allows to raise the loop bandwidth to reduce the effect of DCO noise in the digital PLL and as a result the overall noise characteristic of the digital PLL gets better. Higher bandwidth can help also in the reduction of power consumption for the DCO [109].

4.10 Optimum loop bandwidth for the digital PLL

The focus of this work is to get a high bandwidth digital PLL with low jitter. This is achieved with the assistance of the noise shaping technique for the TDC. Besides the advantage of the DCO noise suppression, the wide bandwidth reduces the settling time of the digital PLL and speeds up the locking process. The phase noise behavior of the DCO, the TDC and the digital PLL without noise shaping is shown in Figure 4.27. It can be seen that the digital PLL phase noise corresponds closely to the TDC noise as the limiting factor for noise reduction at low frequency offsets.
On the other hand, Figure 4.28 depicts the advantage of noise shaping in the TDC to

improve the digital PLL noise. It is important to determine the optimum bandwidth. For the simulations, $\zeta = \sqrt{2}/2$ is considered for a stable operation. Accordingly, the phase margin is about 66°. A loop bandwidth around 2 MHz gives the minimum jitter for this digital PLL with the values for f_{REF}, f_{DCO} and FCW as mentioned before. Therefore, the DLPF coefficients are obtained as $K_P = 2^{-4}$ and $K_I = 2^{-9}$.

4.11 Time-domain simulations for the digital PLL

The complete digital PLL is simulated in Simulink with the goal of generating 1 GHz clocks at the output of the DCO in the lock state as is shown in Figure 4.29. For this set of simulations, the ring oscillator in the TDC has four stages with the oscillation frequency of 1 GHz that provides a resolution of 125 ps in the conventional operation without noise shaping. By including the noise shaping effect for the TDC, the effective resolution will improve to 4.9 ps. It should be mentioned that by applying a higher frequency ring oscillator in the TDC, the effective resolution gets better.
In correspondence with equation (4.14), the design parameters for the DCO are extracted from a SPICE-based model with concentrate on a preserved oscillation at

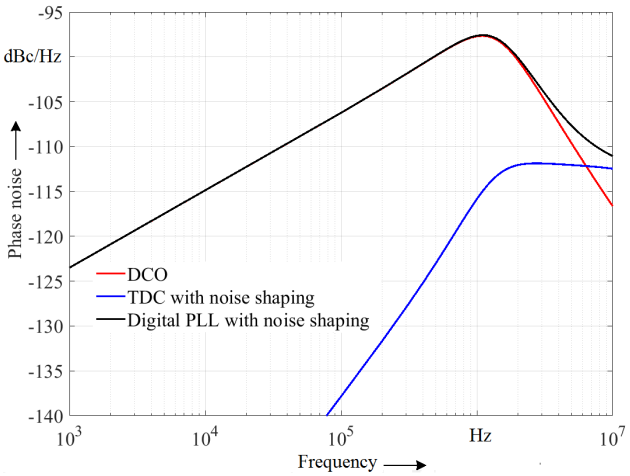


Figure 4.28: Phase noise characteristic with noise shaping.

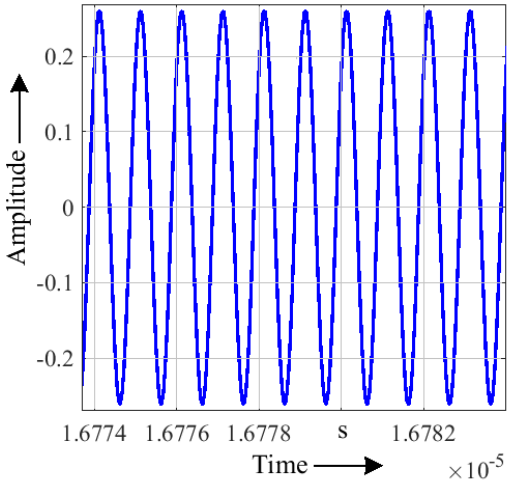


Figure 4.29: Output of the ring DCO at 1 GHz.

the required frequency in case of changes in temperature and process corners. By considering four delay stages in the modeled DCO in Simulink, for $\omega_0 = 800$MHz and $K_{DCO} = 819.2\text{MHz}/2^{13}$, Figure 4.30 illustrates the locking process of the digital PLL through the settling behavior of the *CW*. The *CW* starts with the lower limits of its range. Later, it increases until it gets to the locking range and steady-state value, which is 2000 to generate 1 GHz frequency at the output of the DCO.

4.11.1 Frequency monitoring of the digital PLL in Simulink

Getting the frequency information during the locking process of the digital PLL is necessary to verify the digital PLL behavior in frequency locking. A frequency monitoring system is developed in Simulink that measures the output frequency of the DCO. The operation of the system is explained based on Figure 4.31. The idea is to count the transitions of CK_{DCO} within a pulse, CK_{P}. CK_{P} is extracted from CK_{REF} and its pulse width is equal to T_{REF}. CK_{P} is given to the Enable block. The Enable block resets when enabling. The counter counts CK_{DCO} transitions within the pulse width of CK_{P} and stops counting with the falling edge of CK_{P}. A sampler

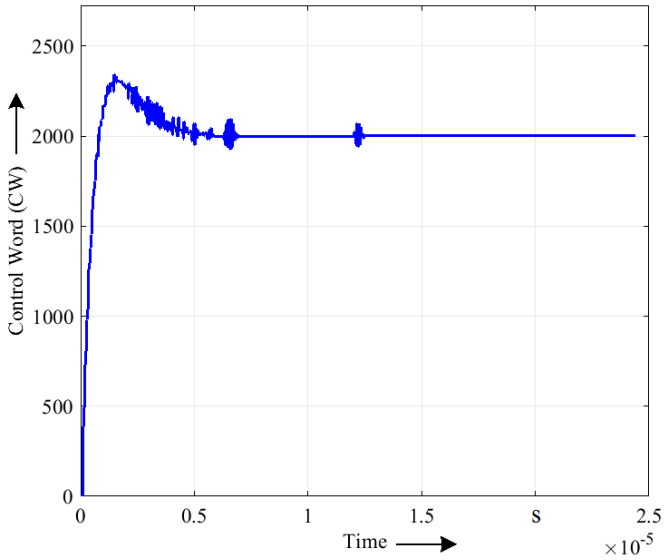


Figure 4.30: Control word of the DCO in the digital PLL.

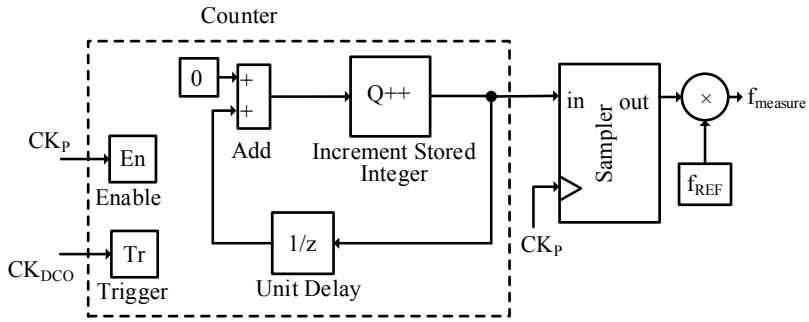


Figure 4.31: Frequency monitoring of the digital PLL in Simulink.

block at the output of the counter is clocked with CK_P and samples the counting values. Finally, the output of the sampler is multiplied by f_{REF} to obtain f_{DCO}. The frequency information and locking to 1 GHz for the considered digital PLL is shown in Figure 4.32.

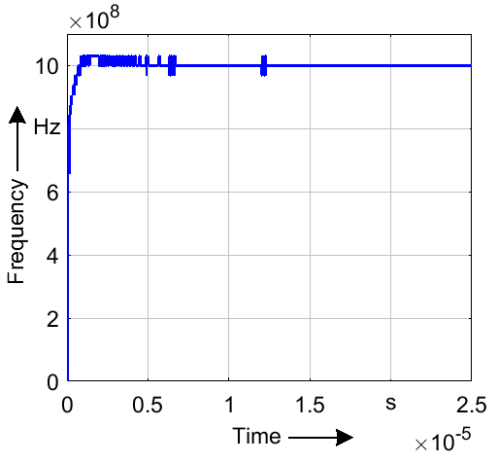


Figure 4.32: Measured frequency of the DCO.

The performance summary of the high-level model of the digital PLL is presented in Table 4.1.

4.12 Digital PLL with reduced area and power consumption

In this thesis, two ring oscillators have been used. The first ring oscillator is the DCO. The second one is in the TDC, which was implemented to improve the resolution with the noise shaping technique. For the reported TDC, a separate ring oscillator was designed to generate a fixed oscillation frequency. This frequency can change by variations in temperature and process corners. Therefore, the TDC characteristics including the resolution are influenced by this phenomenon which creates challenges in predicting the design performance parameters such as resolution.
For other applications of the TDC such as measurement devices (oscilloscope, logic analyzer) and pulsed laser time-of-flight measurements [110], it will be a good idea to generate the multiphase clocks with a fixed frequency for the TDC operation using a PLL or delay-locked loop (DLL). However, this increases the complexity and power consumption as the result of PLL or DLL insertion to the TDC.

	This work
Simulation tool	Simulink/Matlab
DCO type	Ring
TDC type	Ring oscillator based
Loop filter type	P-I filter
f_{REF}	31.25 MHz
F_{DCO}	1 GHz
FCW	32
Loop bandwidth	2 MHz
TDC effective resolution	4.9 ps
K_{DCO}	819.2 MHz/2^{13}

Table 4.1: The performance summary of the digital PLL.

The idea for this thesis is to remove the second ring oscillator in the TDC and feed the multiphase clocks that are generated at the output of the DCO to the TDC as is shown in the Simulink top level design in Figure 4.33. The retimed clock (CK_R) is generated at the output of a Re-timer block (D Flip-Flop) to synchronize all sub-blocks. Bit-to-Integer Converter following the reference/DCO phase accumulator is to simplify the signal routing in the top level modeling. A sampler block (D Flip-Flop) samples the output of digital loop filter after normalization to generate a fixed control word for the DCO during the period of retimed clock. The TDC design in Figure 4.16 used the pulse width of CK_{EN} as a variable to measure the time interval between CK_{REF} and CK_{DCO}. For the TDC design proposed here that applies the output clocks of the DCO, the frequency of the ring oscillator (DCO in the digital PLL) is changing during the lock process. Keeping CK_{EN} as before imposes two variables to the TDC and may result into incorrect time to digital conversion. Therefore, the need for the pulse generator is eliminated and the CK_{REF} is used also as CK_{EN}. This means, within this TDC, the coarse information by counting the DCO clock transitions is generated during the period of CK_{REF} and the registers are triggered by the rising edge of CK_{REF}.

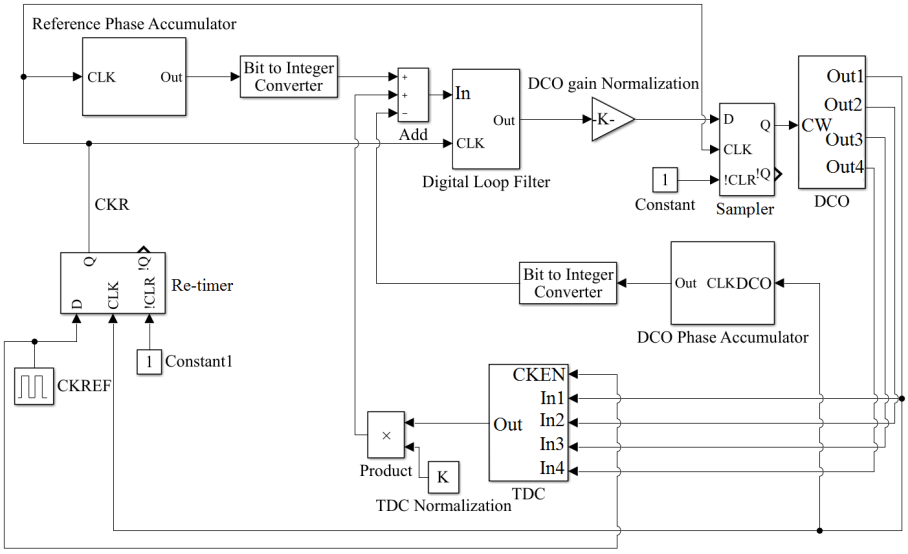


Figure 4.33: Digital PLL with reduced area and power consumption.

If the digital PLL with this TDC and the previous structure in Figure 4.2 are compared, no noticeable differences in settling behavior or stability conditions appear but the digital PLL implementation with the second TDC is superior in terms of precision as well as area and power consumption.

Chapter 5

Summary and future work

5.1 Summary

In this thesis the development of a PLL-based frequency synthesizer in 65 nm CMOS technology was studied. The application of the design was to generate sampling clocks for the ADCs and DSP block. There are stringent requirements for the jitter, configurability, power, area consumption, and especially reliability of the design regarding its application as clock source in the read-out electronics of the JUNO central detector. It was tried in the PLL design and its sub-blocks to get high performance results based on the requirements. The PLL behavioral modeling was performed to analyze the loop dynamics. This included the assessment of the loop bandwidth and phase margin that are needed to predict the optimized jitter and stability of the system, respectively. A topology was proposed for the low noise VCO that provides a novel varactor array to achieve the optimized tuning range considering the linearity and gain to cover 4 GHz oscillation frequency for all process corners and extensive range of temperatures. The long life-time of the project requires strong requiremnts on reliability and enforces detailed investigations and simulations on corresponding solutions. The impacts of hot carrier and gate oxide breakdwon on the operation of VCO was examined. Correspondingly, a new architecture for an amplitude error detector was presented to track the amplitude level at the outputs of

the VCO to address the reliability and especially corresponding noise degradation. Furthermore, the non-idealities and challenges that exist for the conventional charge pumps were investigated. A novel design for the charge pump was suggested to solve the current mismatch as one of the important problems to reduce the spur rejection at the input of the PLL. The programmability of the frequency dividers made the optimum functionality of the PLL possible in case of changes in the reference frequency. Besides, the configurable frequency dividers with the multiplexer blocks provide a wide range of sampling frequency for the ADCs and DSP block. The measurement results for the fabricated PLL showed a very good agreement with the simulated expectations and approve the optimized operation of the PLL.
The second part of the thesis was devoted to the high-level behavioral modeling of a digital PLL in Simulink and Matlab. This gives the flexible and fast estimation of the design parameters prior to SPICE-based simulations. A low area with reduced power consumption for improved noise characteristic was intended. The ring oscillator was preferred to prevent the use of inductor due to the possible application of the design in high magnetic field environments. Variety of methods such as tri-state buffers and current-starving were studied to control the output frequency of the DCO in a monotonic way. Additionally a simplified high level model for the DCO was implemented. The delay components were defined based on a linear s-domain model and mathematical expressions were used to extract its design parameters. The TDC concept with different approaches and resolutions were introduced. A novel model for the TDC was declared that could improve the resolution using noise shaping technique. The frequency domain analysis for the digital PLL helped to estimate the loop filter parameters that are involved in determination of the loop bandwidth, phase noise and stability conditions for the design. A wide bandwidth architecture was proposed to decrease the noise of the DCO within the loop and at the same time by employing the noise shaping for the TDC, the overall noise of a ring oscillator based digital PLL was improved.
A second proposed digital PLL integrates the multiphase clocks generated at the outputs of the DCO with the TDC design and removes the designed ring oscillator in the TDC. Replacing the ring oscillator in the TDC with DCO clocks helped in the area and power reduction. Furthermore, the injection of DCO clocks instead of the extra ring oscillator in the TDC results in a constant resolution for the TDC independent

of the process and temperature changes. In the other words, the operating range of the design was enhanced.

5.2 Future work

As further steps for future implementations of the work some additional steps can be included.
Regarding the analog PLL, a detailed analysis on the circuit operation under the aging and stress conditions employing the special simulators is beneficial. This can give a more precise insight over the reliability involved parameters in the design process.
The next step for the presented digital PLL can be transistor-based implementations. The extracted parameters and behavior from the high-level modeling accelerates greatly the transistor-based design. Furthermore, there is the possibility of the co-simulation of the Simulink with Cadence. Therefore, the transistor-based results can be integrated into the high-level modeling to acquire more precise parameters for the design and make the high-level modeling more compatible with the transistor-based implementation. This co-simulation also allows simply to include the effects of the process and temperature changes in the modeling.

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