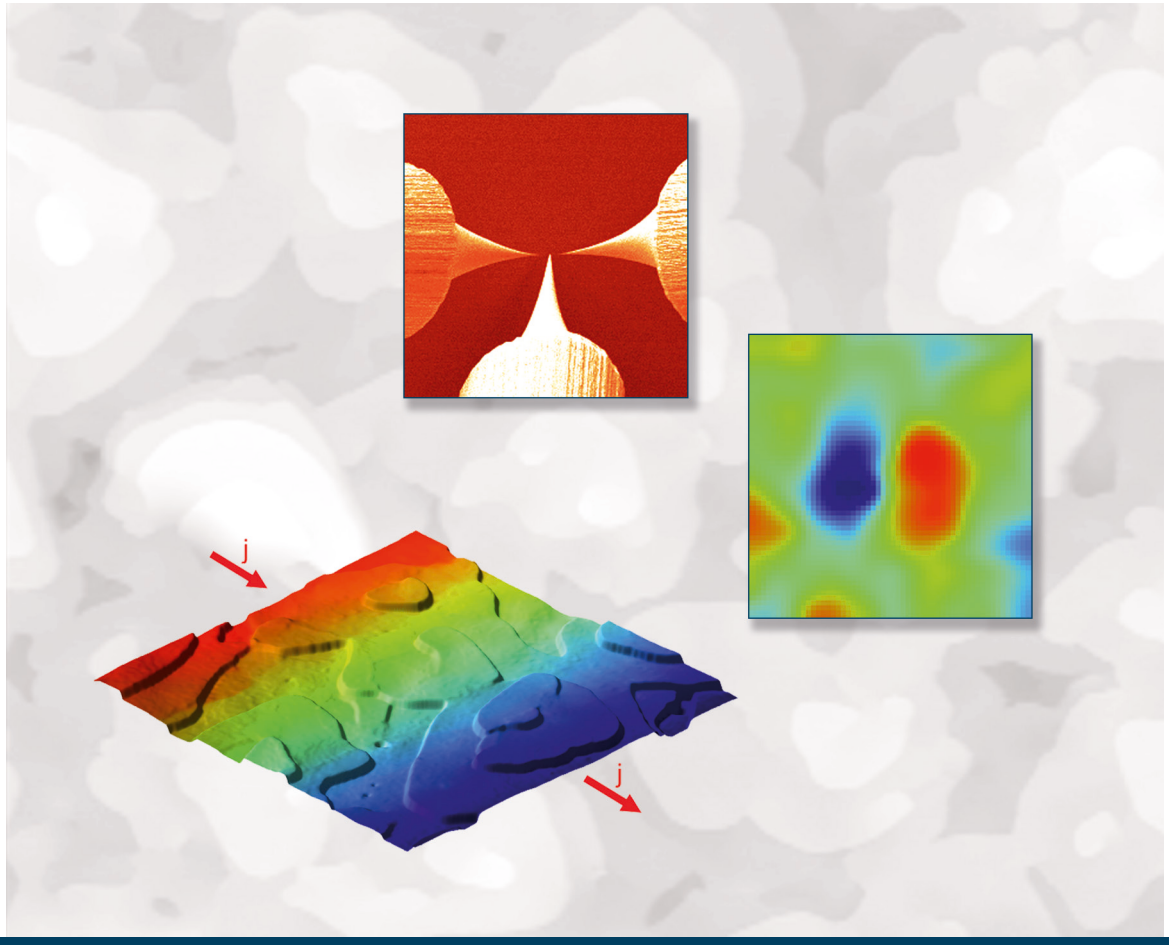

Scanning tunneling potentiometry at nanoscale defects in thin films

Felix Lüpke

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In theory, there is no difference between theory and practice. But, in practice, there is.

Jan L. A. van de Snepscheut

Contents

Introduction

The continuous miniaturization of electronics has led to smaller and more powerful devices in our everyday life, such as smart phones and tablet computers. This process is substantiated by Moore's law, which predicts shrinking of electronic devices by a factor of two every two years [1]. While this model described the development over the last decades astonishingly well, it has come clear that it will break down in the near future [2, 3, 4, 5], which results from technical challenges in the fabrication of such small devices. However, even if the fabrication technology would not be the limiting factor, it is clear that at some point a fundamental size-limit for a classical transistor is reached – a single-atom transistor [6].

Generally, transistors consist of areas of differently doped semiconductors, mainly silicon (Si). The doping is the result of atomic defects within this host lattice of Si atoms. The positioning of the dopants in the Si lattice is a random process, such that for ultra-small devices, in the limit where the doping of the Si is determined by only a few doping atoms, small variations in the local dopant configuration can have large effects on the resulting device properties. The same is true for unintentional lattice defects, such as lattice vacancies, interstitial atoms, domain boundaries and step edges on the sample surface. In large devices, the exact number of such defects often is not too critical because the device properties are average over a large volume. In a device consisting of only few atoms however, e.g. an unintended atomic vacancy almost certainly leads to a failure of the device. As a result, the search for alternative concepts for future electronics is flourishing. Recent developments show that spintronics (spin-based electronics) [7] and quantum computing [8] could be a next big step in computer technology. At the forefront of these two topics are three-dimensional topological insulators (3D TIs), which have been first proposed in 2005 [9] by C. L. Kane and E. J. Mele. What makes these materials promising candidates for future electronic devices are their two-dimensional surface states, where the spin of the charge carriers is locked to their momentum. Furthermore, the corresponding dispersion relation has the form of a linear dependence of the energy on the impulse, resulting in the so-called Dirac cone [10]. As a result, new pathways for the realization of spintronics are opened, where the spin polarization of a current can be controlled simply its current direction. Furthermore, it has been shown that TIs in combination with superconductors can lead to the formation of Majorana fermions [11], which are theoretically predicted to be suitable for the preparation of quantum bits [12, 13]. The combination of multiple of such quantum bits into quantum computers has the potential to solve certain problems much faster than any classical computers [14]. However, for these new materials to find their ways into applications, a miniaturization of the corresponding devices is required. Here, again the fabrication of ultra-small devices depends crucially on the behavior of defects in such systems. Due to this ultimate importance, the fundamental properties of defects under current flow have acquired an increasing interest in the research community and also electronics industry [15, 16, 17, 18, 19].

On a macroscopic level, inducing defects into a sample material in general changes the conductivity of the sample under investigation. A widely used method to experimentally determine the electrical conductivity of a sample with high accuracy is a four-probe measurement [20]. Hereby, two contacts are used to drive a current through the sample and two contacts are used to measure the voltage drop across the sample. The resulting electrical conductivity is $\sigma \sim I/V$ according to Ohm's law. Performing such conductivity measurements under the influence of an external electric or magnetic field gives access to further sample properties due to a different response of the defect conductivity on the external field than the

host lattice. Hereby, the resulting effect of the defects on the sample conductivity is typically expressed in terms of the charge carrier mobility μ, which is a measure of 'how easy can the charge carriers in the sample move'. Such transport measurements, like Hall measurements and measurement of universal conductance fluctuations, however access the properties of the ensemble of defects in the sample, averaged over the entire sample volume under investigation. The influence of individual defects in a sample can be better accessed by locally resolved transport measurement, such as scanning tunneling potentiometry (STP), which allows to perform nano-scale transport measurements [17, 21]. STP is based on the working principle of a scanning tunneling microscope (STM), which allows highly resolved lateral profiling of a conducting sample surface, down to atomic scale. STP maps the local potential of the sample under investigation and thereby allows a direct correlation of the sample surface structure, i.e. its topography, and transport properties, such as local conductivity. As a result, this method is well suited for the investigation of the influence of individual defects with sizes ranging from the atomic scale up to microns.
Depending on the samples and types of defects, due the large span of defect sizes which can be investigated by the STP technique, one can investigate classical transport effects, as well as quantum mechanical effects at defects [19].
In order to fully understand the observed features, in STP generally a rigorous analysis of the sample system under investigation is of importance. For example, in many samples several parallel conduction channels can participate in electrical transport, not only the surface which is investigated by STP. Hereby, especially the transport through the sample bulk has also to be considered. The disentanglement of the different conduction channels is therefore generally a prerequisite for a detailed analysis of a sample under investigation. For TI samples this problem becomes rather complex, because of a multitude of possible parallel conduction channels [22].
The use of a four-tip STM [23] allows to combine the macroscopic measurement of the sample properties by four-probe measurements, as well as STP measurement on the nanoscale in a single measurement setup. A further advantage of transport measurements performed with a multi-tip STM is that the measurements can be performed under ultra-high vacuum (UHV) conditions, directly after the preparation of samples. Hereby, the contacting of the sample is controlled e.g. via a scanning electron microscope and allows flexible positioning of the individual tips with high accuracy. As a result, in contrast to usual transport measurements, no lithographic patterning under ambient conditions is required, which results in the contamination of the sample surface [24, 25].

The present thesis describes the implementation of STP and a newly developed method for four-probe measurements into a four-tip STM setup in chapter 1 and 2. These methods are then used to analyze the electrical resistance of individual defects in a TI ultra-thin film as described in chapter 3. Chapter 4 describes the superposition of the multiple conduction channels in TI ultra-thin films in detail, where it is possible to disentangle the contributions of the individual channels by gate dependent transport measurements. Another parallel conduction channel in such sample is given by the interface layer which is formed between the TI film and the Si(111) substrate during the sample growth. The conductivity of this interface layer and resulting influence in the transport in TI films is analyzed in chapter 5. The STP method was further applied to Bi ultra-thin films which prove to be a promising candidate for the investigation of the transition between the diffusive and ballistic transport regime due to their large mean free path at room temperature, as described in chapter 6. Finally, chapter 7 describes details of the resistor network models which have been a crucial theoretical tool throughout this thesis for the analysis of the STP data.

Chapter 1 Scanning tunneling potentiometry implemented into a multi-tip setup by software

1.1 Introduction

Scanning tunneling potentiometry (STP) is an intriguing tool when it comes to investigating the fundamentals of charge transport in real space. It provides direct access to the local electrochemical potential in a sample surface which allows to analyze transport phenomena such as Ohm's law on a nanoscopic scale. STP is based on scanning tunneling microscopy, in which an atomically sharp metal tip is scanned across the sample surface point-by-point. The tip-sample distance is kept constant by application of a voltage difference between tip and sample and maintaining a constant tunneling current by adjusting the tip height. The resulting measurement signal is the topography of the sample – a map of the tip height in which the current set point is met. In addition to this topography measurement, STP allows to measure the local electrochemical potential quasi-simultaneously. The result is a map of the electrochemical potential at the sample surface. By application of a lateral current through the sample, the electric potential has a slope according to the voltage drop across the sample, the so-called transport field. STP allows to analyze the local potential variations with respect to the topographic features.

In principle two different STP implementations have been reported in literature which are based on two possibilities to separate the topography and potential feedback loops – either temporal, by performing the individual feedbacks after each other [21], or by use of an AC signal for topography feedback and DC signal for potential feedback [26]. In general, the voltage measured by STP is the superposition of the local electrochemical potential, thermovoltage and photovoltage, where the latter can be excluded in typical experimental setups. Thermovoltage effects between the tip and sample however can be a large parasitic signal. Here small temperature differences of tip and sample can be sufficient to result in large relative signals and therefore have to be controlled carefully when performing local transport measurements where one is interested in the transport field.

We report here the implementation of the STP technique into a four-tip STM setup by use of a temporal separation of the topography and potential feedback which allows an implementation into existing setups only by software changes. The resulting setup allows flexible *in situ* contacting of the sample under investigation in order to inject a lateral current such that also molecular beam epitaxy grown films and nanostructures can be analyzed without additional sample processing as shown in the following article. In detail, locally resolved transport measurements on $\mathrm{Ag/Si}(111)-(\sqrt{3}\times\sqrt{3})$ and $\mathrm{Si}(111)-(7\times7)$ surfaces are demonstrated. Here, the resistivity of steps and terraces on the sample surfaces could be determined and the results are in agreement with literature and prove the functionality of the present implementation. After verification of the setup, further local transport experiments were performed on a variety of samples, addressing intricate problems on the atomic and mesoscopic scale as shown in the following chapters.

1.2 Scanning tunneling potentiometry implemented into a multi-tip setup by software

The following article has been published in the journal **Review of Scientific Instruments**:

- **F. Lüpke**, S. Korte, V. Cherepanov, and B. Voigtländer, Scanning tunneling potentiometry implemented into a multi-tip setup by software, *Rev. Sci. Instrum.* 86, 123701 (2015)

Author contributions:
F.L., S.K., V.C. and B.V. conceived the experiments**. F.L.** performed the measurements and analyzed the experimental data. **F.L.**, S.K., V.C. and B. V. wrote the paper. All authors discussed and commented on the manuscript.

Note that parts of the material contained in the article *Scanning tunneling potentiometry implemented into a multi-tip setup by software* in combination with additional measurements were presented also in the following review articles:

- B. Voigtländer, V. Cherepanov, and P. Coenen, The Multimeter at the Nanoscale, Vakuum in Forschung und Praxis 28, 38–42 (2016)
- B. Voigtländer, The Multimeter at the Nanoscale, Imaging and Microscopy 18, 31-33 (2016)

REVIEW OF SCIENTIFIC INSTRUMENTS **86**, 123701 (2015)

Scanning tunneling potentiometry implemented into a multi-tip setup by software

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We present a multi-tip scanning tunneling potentiometry technique that can be implemented into existing multi-tip scanning tunneling microscopes without installation of additional hardware. The resulting setup allows flexible *in situ* contacting of samples under UHV conditions and subsequent measurement of the sample topography and local electric potential with resolution down to Å and μV, respectively. The performance of the potentiometry feedback is demonstrated by thermovoltage measurements on the Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30° surface by resolving a standing wave pattern. Subsequently, the ability to map the local transport field as a result of a lateral current through the sample surface is shown on Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30° and Si(111) – (7×7) surfaces. © *2015 AIP Publishing LLC.* [http://dx.doi.org/10.1063/1.4936079]

I. INTRODUCTION

In recent years, multi-tip scanning tunneling microscopes (STMs) have become popular instruments.[1–4] The most common experiments reported in the literature using those instruments are multi-probe measurements that allow to determine the microscopic electrical properties of the samples under investigation. However, such devices can be further extended with scanning tunneling potentiometry (STP) techniques which allow to map the electric potential on the nanoscale with spatial and potential resolution of few Å and μV, respectively.[4–6] Combination of STP with multi-probe point measurements creates a powerful tool for the electrical sample characterization capable to give insight into fundamental transport properties, such as the influence of defects on the local electric transport. This applies especially for surface dominated transport as present, e.g., in topological insulators and allows the investigation of transport phenomena such as the Landauer dipole.[7,8]

Since the invention of STP by Murlat and Pohl,[9] several different technical implementations of STP have been reported mostly in single-tip STM setups[6,10] for which the transport field is usually applied to macroscopic sample contacts up to several mm away from each other. As a result, the current density in the region of measurement can be low, resulting in a bad signal-to-noise ratio of the measured electric potential distribution throughout the sample surface. To circumvent this problem, patterning metallic contacts on the sample surface was reported to increase the current density across the structure under investigation.[8,11] However, the patterning process often results in contamination of the sample surface.

In contrast, multi-tip STM setups have the advantage of flexible *in situ* contacting the sample with several electrodes, e.g., molecular beam epitaxy grown films and nanostructures without additional sample processing.[1,2,4] As a result, by variation of the spacing of the electrodes, the current density in the surface and also through the bulk can be measured and controlled.[12] Furthermore, the direction of injected current can be varied by repositioning of the electrodes enabling the quantification of transport anisotropies.[13]

Multi-tip STP implementations have been reported that facilitate the above mentioned advantages over single-tip setups.[4] However, these implementations are based on additional hardware such as external power sources and feedback electronics that need to be added to existing setups in order to enable potentiometry measurements.[4,6] In contrast, we present here a software based multi-tip STP technique that can be readily implemented into existing multi-tip setups without installation of additional hardware.

II. EXPERIMENTAL SETUP

We use a home-built room temperature four-tip STM in Besocke/Beetle-based design with electrochemically etched tungsten tips. Each tip has an individual ring for xy-motion and a tube piezo for z-motion.[14,15] Atomic resolution on Si(111) – (7×7) is achieved with each tip. The STM is equipped with a scanning electron microscope (SEM) for precise positioning of the individual tips.

Each of the four tips is connected to one of the four instances of equivalent electronics which can be switched between current and voltage measurement, as also done in other four-tip STM setups.[1] For current measurement, the voltage applied at each tip can be set individually. Furthermore, the sample can be either on floating or ground potential. In STP measurements, three of the four tips are in current probe mode, two current injection tips (tips 1 and 2), and the scanning tip (tip 3). The fourth probe is operated in voltage probe mode and is used as a reference voltage probe (tip 4). This tip is optional such that the presented implementation is also applicable for three-tip STM setups. A schematic of the setup is shown in Fig. 1.

The four biasing electronics units are connected to a commercial multi-tip STM controller with individual

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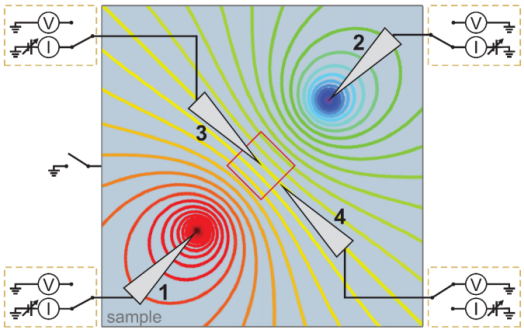

FIG. 1. Schematic of the four-tip STP setup. Tips 1 and 2 are in contact to the sample surface and inject a lateral current represented by the colored equipotential lines. Tip 3 is in tunneling contact and is scanned across the surface. The scan area is indicated as red square (largely exaggerated). Tip 4 is in contact to the sample surface close to the scanning area and serves as reference voltage probe.

digital-to-analog converter (DAC) outputs to address the bias voltage for each tip and analog-to-digital converters (ADCs) to read out the current or voltage at each tip.

III. BIASING ELECTRONICS

Figure 2 shows a schematic of the biasing electronics which is typical for a multi-tip setup.[1] The present setup is based on a FEMTO DLPCA-200 current amplifier[16] and allows variable-gain current measurement or voltage measurement. For current measurement, the tip is connected to the input of the current amplifier which is floating on bias potential V_{tip}. From the output of the current amplifier, the bias voltage is subtracted before the signal is fed to the output I_{out}. For voltage measurement, the tip is connected to a high input impedance (10 TΩ) voltage follower with its output connected to the V_{out} output of the electronics.

In high resolution STP measurements, the control of V_{tip} of the scanning tip in the range of μV is required. This can be achieved by a voltage divider (e.g., 1:100) which is applied just in front of the V_{tip} input of the scanning tip biasing electronics. This decreases the dynamic range of the voltage which can be applied to this tip accordingly. Not to be limited by this, the topography tip-sample tunneling bias voltage is applied to the sample rather than the tip as described below.

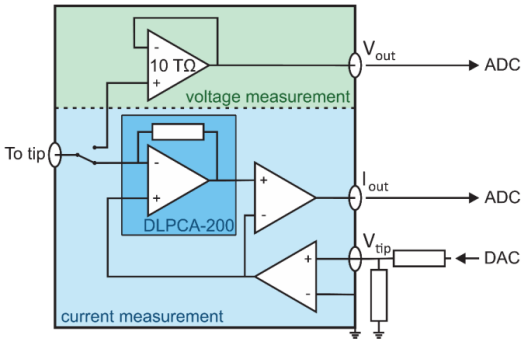

FIG. 2. Schematic of the biasing electronics for each tip. In the upper part, the voltage measurement is performed by a voltage follower circuit. In the lower part, the current measurement schematic is shown. The bias voltage V_{tip} is applied via the differential input in front of which the optional voltage divider for the scanning tip is located.

IV. SOFTWARE IMPLEMENTATION

The multi-tip STP implementation presented here is based on the interrupted feedback loop single-tip STP implementation reported in Ref. 6. In this technique, the surface is scanned point-by-point as in regular STM measurements. However, at each scanning point after the topography value $z(x, y)$ is acquired, the tip is held at constant height and the bias voltage between scanning tip and sample is shifted. Now, the potentiometry feedback is run for a time $t_{pot} \approx 1$–50 ms. The final value of the potentiometry feedback is saved as the sample potential at the momentary position of the scan $V_{lateral}(x, y)$. After restoring the topography bias voltage, the topography feedback is re-enabled and the scan is continued by moving to the next scan position.[17] The flow chart of the measurement procedure is shown in Fig. 3. In this way, topography and potentiometry signals are acquired point-by-point across the sample surface. Depending on the feedback time t_{pot} and the number of scan points, a whole scan takes up to several hours.

The potentiometry feedback is a PI-feedback algorithm just like the one used for the topography feedback. However, it adjusts the tip voltage as control variable instead of the tip height (in topography feedback), and the process variable set point (i.e., the tunneling current) is set to $I_t = 0$ nA during the potentiometry feedback. The corresponding feedback constants determine the bandwidth of the potentiometry feedback and have to be adjusted for each measurement.

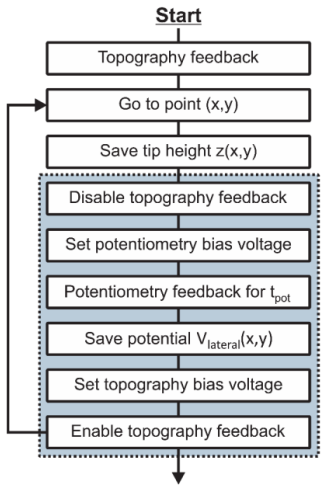

FIG. 3. Potentiometry measurement flow chart. Highlighted by the dotted rectangle is the additional procedure needed to acquire the sample potential in comparison to conventional STM.

V. MEASUREMENT PROCEDURE

In order to perform a potentiometry measurement, first the sample (connected to ground) needs to be contacted by the two current injecting tips (tips 1 and 2). After coarse approaching all four tips to the sample surface, the current injecting tips are brought into contact to the surface under tunneling conditions of, e.g., $V_{tip} = 1$ V, $I_t = 10$ pA. One after the other, the current injection tips are advanced further by a few nm with disabled topography feedback until a stable current ($\lesssim$1% variation per minute) of up to several μA is measured between that tip and the sample. Typically, there is a sharp increase of the current as the tips come into contact to the surface after which the tips should not be advanced further to prevent damage to the tips or the sample surface. However, if at this point the resulting current is unstable, advancing the tips a bit further can help to stabilize the contact.

Next, the optional reference voltage probe (tip 4) is brought into contact to the sample surface in the same way (in current measurement mode). When a stable contact is achieved, the electronics of this tip is switched to voltage measurement. This tip serves to measure the reference voltage which can be used during the measurement preparations as described below and also to compensate small fluctuations in the current injecting contacts during measurements:[4] Changes of the contact resistance in the current injecting contacts result in a change of the sample potential at the point of current injection. This will directly influence the measured potential at the position of the scanning tip and can be compensated by subtracting the potential of a static reference voltage probe from the measured potential of the scanning tip.

Now, the sample backside contact is disconnected such that the electric potential of the sample depends only on the potential of the two current injecting tips.

To approach the scanning tip (tip 3), the voltage of both injection tips is set to 0 V, while that of the scanning tip is set to, e.g., $V_{tip} = 1$ V. Then, the tip is approached to the sample surface until it is in tunneling contact ($I_t \sim 10$ pA). Subsequently, a topography scan should be performed to check if the scan area is suitable for potentiometry measurements.

To apply a transport field, first the scanning tip (tip 3) is retracted and its voltage is set to $V_{tip} = 0$ V. Now, the voltage of the injection tips is set such that a lateral current $I_t \gtrsim 1$ μA results in a potential distribution $V_{lateral}(x, y)$ over the sample surface. Subsequently, $V_{lateral}(x, y)$ is shifted until the sample potential under the scanning tip is approximately 0 V. This can be done using the information of the voltage probe. In order to adapt $V_{lateral}(x, y)$ at the position below the scanning tip, the voltage of both current injecting tips is shifted identically, maintaining the injected current.[18] Next, the bias voltage for the topography measurement V_{offset} is added to the voltage of the current injecting tips. For high resolution measurements, the voltage divider is now applied to V_{tip} of the scanning tip. Following the described preparations, the tunneling contact of tip 3 is re-engaged and the STP scan can be started. Figure 4 shows a schematic of the potentiometry measurement setup with the voltages applied to the tip and sample indicated, respectively.

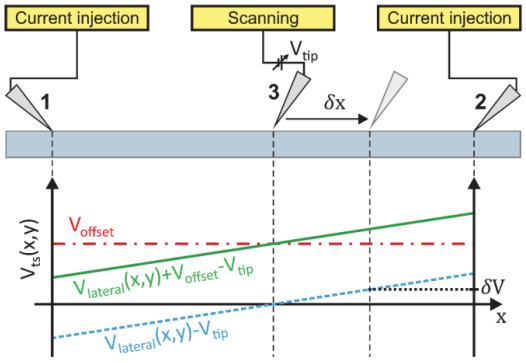

FIG. 4. Schematic of the potentiometry measurement. Tips 1 and 2 are in contact to the sample injecting a current. Tip 3 is in tunneling contact and is scanned across the sample surface. The dashed vertical lines indicate the position of the tips, respectively. In the line graph, the tip-sample voltage V_{ts} is plotted as a function of the lateral coordinate x. During topography feedback, the solid green line holds. For potentiometry feedback, V_{ts} is shifted by V_{offset} resulting in the dashed blue line. Moving the scanning tip by an amount, δx results in a change of the potential under the tip by δV. Note: The movement of the scanning tip is largely exaggerated in this graph.

In STP, the voltage difference between the scanning tip and sample, $V_{ts}(x, y)$, usually referred to as bias voltage at the scan position (x, y), is the superposition of the lateral transport field, the offset voltage, and the momentary voltage applied to the tip during topography feedback $V_{ts}(x, y) = V_{lateral}(x, y) + V_{offset} - V_{tip}$ (solid green line in Fig. 4). When starting the STP scan, after acquiring the topography at the momentary scan position, the topography feedback is deactivated and the injection tip voltages are shifted by $-V_{offset}$ leaving only $V_{lateral}(x, y)$ applied to the sample resulting in $V_{ts}(x, y) = V_{lateral}(x, y) - V_{tip}$ (dashed blue line in Fig. 4). Subsequently, the potentiometry feedback loop is activated and adjusts V_{tip} to the local sample potential under the tip $V_{tip} = V_{lateral}(x, y)$. After the feedback time t_{pot}, the potentiometry feedback is deactivated. V_{tip} is recorded as the sample potential at this scan position and is maintained until the next activation of the potentiometry feedback loop. After restoring the topography bias voltage $V_{ts}(x, y) = V_{lateral}(x, y) + V_{offset} - V_{tip}$, the topography feedback is re-activated and the tip is moved to the next scan position.

Note that, for neighboring scan positions $(x \to x + \delta x)$, the local sample potential varies by an amount of δV during the topography feedback. In detail, during the topography feedback, it holds $V_{ts}(x + \delta x, y) = V_{offset} + \delta V$. However, in usual measurements, $\delta V \ll V_{offset}$ such that the change in V_{ts} for neighboring scan positions can be neglected.[6]

For the potentiometry feedback to work in an optimal way, it is recommended that the tunneling I–V curve of the scanning tip is linear, such that a change in the control variable (tunneling voltage) will have a linear effect on the process variable (tunneling current).[19] Furthermore, due to the fundamental noise limit of the potential measurement which is the sum of thermal (Johnson) noise and the amplifier noise, the limit of the potentiometry resolution is[10]

$$V_{Limit} = \sqrt{V_{Johnson}^2 + V_{Detector}^2}, \quad (1)$$

TABLE I. Noise limit for transport measurements in the present setup at three different tunneling junction resistances and a bandwidth of $\Delta f < 50$ Hz.

V_{ts}/I_t	V_{Limit} (μV)
10 GΩ	<300
1 GΩ	<40
100 MΩ	<10

with

$$V_{Johnson} = \sqrt{4k_B T \Delta f V_{ts}/I_t} \quad (2)$$

and

$$V_{Detector} = N_{Detector}\sqrt{\Delta f} V_{ts}/I_t. \quad (3)$$

Here, $N_{Detector} = 4$ fA/$\sqrt{\text{Hz}}$ is the noise level of the current amplifier.[16] Low tunneling voltages and high tunneling current setpoint depending on the bandwidth Δf of the setup are necessary for low noise potentiometry measurement.[10] For transport measurements with several mV of voltage drop across the scan area, we determine $\Delta f < 50$ Hz as the feedback loop speed for which a good signal-to-noise ratio is achieved while a relatively high scanning speed is maintained. For this bandwidth, the noise limit for three different tunneling resistances is given in Table I.

VI. RESULTS

A. Thermovoltage on Ag/Si(111) – ($\sqrt{3} \times \sqrt{3}$)R30°

The Ag/Si(111) – ($\sqrt{3} \times \sqrt{3}$)R30° reconstruction is a well-studied sample system when it comes to scanning tunneling microscopy, spectroscopy, and also potentiometry.[4,6] Therefore, this system can be used as a benchmark system to test the performance of the presented STP implementation. For the preparation of the Ag/Si(111) – ($\sqrt{3} \times \sqrt{3}$)R30° surface, n-Si(111) 700 Ωcm wafers were flash annealed and an equivalent amount of 10 nm of Ag was deposited at 470 °C following the procedure outlined in Ref. 4. The surface of the prepared sample is known to have a high 2D conductivity, while the bulk of the sample is almost insulating compared to the surface.[4,6]

As a first test, the performance of the potentiometry feedback is demonstrated by measurement of thermoelectric effects. The thermovoltage between the scanning tip and the sample surface is usually undesired in transport measurements and the identification and reduction of these effects give a good first insight into the investigated sample system and hinder unwanted effects in later transport measurements.

To measure the thermovoltage, a potentiometry scan is performed during which the sample is on ground potential and no transport field, i.e., lateral current is applied. The result of such a scan is shown in Figs. 5(a) and 5(b) as topography and potential map, respectively. In the topography, we observe a one atomic layer high island and domain boundaries between different domains of the Ag/Si(111) – ($\sqrt{3} \times \sqrt{3}$)R30° reconstruction on the otherwise flat surface. The corresponding potential map shows an increased potentiometry signal located at the step edges of the island and the domain boundaries, in agreement with the literature.[6]

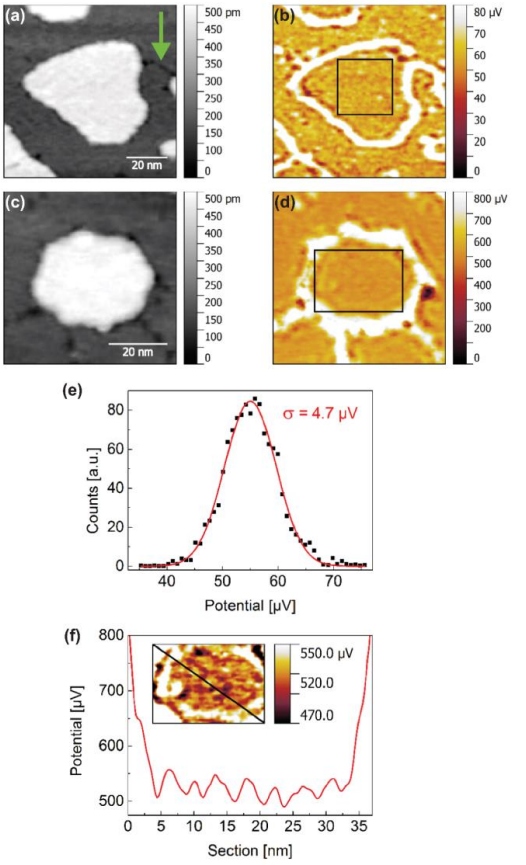

FIG. 5. Thermovoltage measurements on Ag/Si(111) – ($\sqrt{3} \times \sqrt{3}$)R30°. (a) Topography of an island on the Ag/Si(111) – ($\sqrt{3} \times \sqrt{3}$)R30° surface at $V_{offset} = 10$ mV and $I_t = 0.1$ nA with a domain boundary indicated by the green arrow. (b) The corresponding potential map shows an enhanced potentiometry signal at the edges of the islands and domain boundaries. The potentiometry feedback time is 20 ms at a bandwidth of $\Delta f = 2$ Hz. (c) Topography of an island with the scanning tip under laser irradiation. (d) Corresponding potential map of (c). The amplitude of the potentiometry signal is increased by a factor of around 10 compared to (b). (e) Potential distribution of a featureless surface area (black square in (b)). The standard deviation is $\sigma = 4.7$ μV. (f) Section along the black line in the inset that corresponds to the black rectangle in (d). A standing wave pattern with a periodicity of 4.29(14) nm is observed. The section is averaged over 3 lines.

The minimum resolution of the potentiometry is determined as the standard deviation of the measured potential of a featureless surface area (square in Fig. 5(b) and respective histogram in Fig. 5(e)); in this case, $\sigma = 4.7$ μV. Note that for this measurement, a low bandwidth of $\Delta f = 2$ Hz was used resulting in a fundamental noise limit to $V_{Limit}(2\text{ Hz}) = 1.9$ μV. In the next step, to verify the observation of the thermovoltage features, the tip was heated by a laser ($\lambda = 532$ nm, P = 20 mW) and the measurement was repeated. A strong increase in the potentiometry signal by a factor of around 10 is observed, confirming its nature to be due to thermoelectric effects as seen

in the topography and potential map in Figs. 5(c) and 5(d), respectively.[20] In the potential map (Fig. 5(d)), oscillations in the sample potential can be observed. These oscillations appear pronounced in Fig. 5(f) and can be identified as a standing wave pattern which can be explained by thermoelectric effects.[6]

When two materials are in tunneling contact, the thermovoltage present at the tunneling junction is proportional to the difference of the squared temperatures of the two materials.[21] The leading term of the local thermovoltage is given by

$$V_{\mathrm{th}}(x,y) \propto (T_{\mathrm{t}}^2 - T_{\mathrm{s}}^2)\left(\frac{1}{\rho_{\mathrm{s}}(x,y,E)} \cdot \frac{\partial \rho_{\mathrm{s}}(x,y,E)}{\partial E}\right)\Bigg|_{E=E_{\mathrm{F}}},$$

where T_{t} and T_{s} are the temperature of the tip and sample, respectively. The observed standing wave pattern results from modulations of the local density of states in the sample $\rho_{\mathrm{s}}(x,y)$ and is below the resolution of the setup without laser heating of the tip.[6] The resolution of a standing wave pattern confirms the proper function of the potentiometry feedback.

VII. DETERMINATION OF STEP AND TERRACE RESISTIVITY

A. Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30°

To perform transport measurements, a lateral current is applied through the sample surface. A peculiarity of the Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30° surface prepared as described above is the 3D bulk Ag islands visible in the SEM images (Fig. 6(a)).[4] The bulk Ag island thickness is much larger than that of the actual Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30° reconstruction

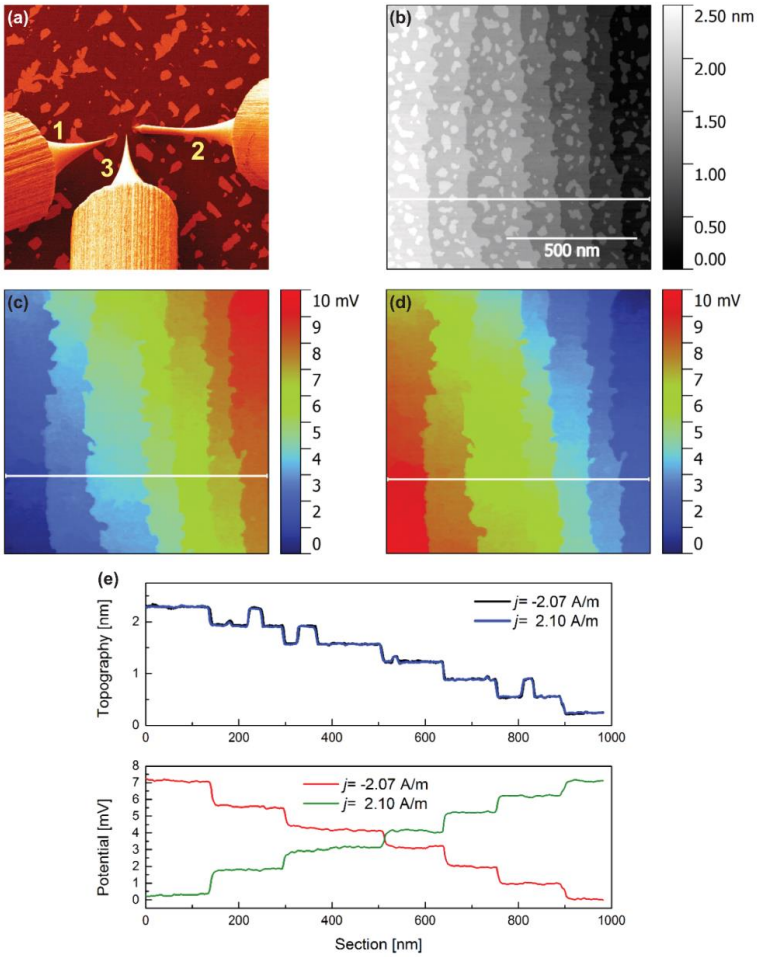

FIG. 6. Transport measurements on Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30°. (a) SEM image of the measurement setup with tips 1 and 2 contacting two 3D Ag islands on the sample surface and tip 3 scanning in between. The distance between the two contacted islands is $d = 30(1)$ μm. (b) Topography of the Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30° surface. Parallel steps with islands on the terraces can be observed. (c) and (d) Corresponding potential maps for two opposite current directions. The current densities are $j = 2.10(8)$ A/m and $j = -2.07(8)$ A/m, respectively. Large voltage drops at the step edges can be observed, while there is only a small voltage gradient across the terraces. The one atomic layer high islands show no direct effect on the surrounding potential landscape. (e) The line profiles indicated in (b)-(d) are each averaged over 3 lines. The average voltage drop at the steps is determined to be $\Delta V_{\mathrm{step}} = 1.08(3)$ mV. The average slope on the terraces is $E = 0.67(8)$ mV/μm. Tunneling conditions $V_{\mathrm{offset}} = 500$ mV and $I_{\mathrm{t}} = 0.5$ nA. The STP scans each took 4.5 h to perform.

and can be easily contacted allowing a stable injection of a lateral current. As a result, for this measurement, the optional voltage reference probe is not used. To contact the islands, the current injecting tips are approached into tunneling contact and then advanced by few tens of nm with the tunneling feedback deactivated pressing the tips into the islands. Subsequently, the scanning tip is approached to the sample surface as described above and a potentiometry scan is performed. The results of the STP measurements for two opposing directions of the injected current are shown in Figs. 6(b)-6(e).

The topography of the Ag/Si(111) – $(\sqrt{3}\times\sqrt{3})$R30° surface (Fig. 6(b)) is dominated by approximately parallel monoatomic substrate steps ($h \approx 3.1$ Å) with an average terrace width of 170 nm. One atomic layer high islands are observed on the terraces. The cross sections in Fig. 6(e) show large voltage drops at positions of steps in the topography. Across the terraces, an almost linear voltage gradient can be observed with no direct influence of the ad-islands on the voltage drop. A detailed analysis shows that domain boundaries between different domains of the $(\sqrt{3}\times\sqrt{3})$R30° reconstruction provide the largest contribution to the voltage drop across the terraces besides the gradient resulting from the undisturbed surface. This observation is in agreement with the literature.[4] For reverse current directions, we observe an inverted voltage drop indicating a symmetric current response.

The given sample topography of a parallel step array allows a direct evaluation of the step resistivity and terrace resistivity which was not the case in previous STP studies of the Ag/Si(111) – $(\sqrt{3}\times\sqrt{3})$R30° system.[4,6]

From the potential cross sections (averaged over 3 lines), the average voltage drop located at the topographic steps is determined to be $\Delta V_{\text{step}} = 1.08(3)$ mV. The current density at the position of the scanning tip is $j = \frac{2I}{\pi d} = 2.10(8)$ A/m which is determined from the measurement geometry where $d = 30(1)$ μm is the distance of the injection tips and I is the absolute current injected into the sample.[22] From this, the step resistivity can be determined to be $\rho_{\text{step}} = \Delta V_{\text{step}}/j = 514(23)$ $\mu\Omega$m. The voltage drop across the terraces is determined from the residual resistance after subtracting the sum of the step resistances from the total resistance and gives $E = 0.67(8)$ mV/μm corresponding to a resistance of $\rho_{\text{terrace}} = E/j = 319(39)$ Ω/□. These values are in agreement with previous values from the literature.[4,6] For the present sample, the steps contribute 91% of the voltage drop across the Ag/Si(111) – $(\sqrt{3}\times\sqrt{3})$R30° surface, while the terraces contribute only to 9%.

B. Si(111) – (7 × 7)

The Si(111) – (7 × 7) reconstruction is frequently reported in the literature since the beginning of STM studies but is still subject of current investigations.[12,23] Up to now, there are no STP transport studies on this surface reported in the literature. For the measurements, we have used the same n-Si(111) 700 Ωcm substrates as above. The two current injecting tips were brought carefully into direct contact with the freshly prepared Si(111) – (7 × 7) reconstructed surface (flash annealed to 1230 °C) in order to keep the Si(111) – (7 × 7) terminated surface as intact as possible. As a result, the reference voltage probe is again not necessary.

In contrast to the Ag/Si(111) – $(\sqrt{3}\times\sqrt{3})$R30°, the Si(111) – (7 × 7) reconstruction on n-Si(111) 700 Ωcm cannot be regarded as a purely 2D conducting material: The bulk and space charge layer of the underlying substrate can have a significant contribution to the measured conductivity.[12] In order to achieve accurate results using STP, a detailed analysis of the conduction through the surface and bulk is mandatory. Such an analysis can be performed by variable distance four-probe measurements as shown recently.[12] A combined analysis of the sample (four-probe measurements + STP) can be performed with the setup presented. For a current injection tip distance of $d = 65(1)$ μm, at the position of the scanning tip,

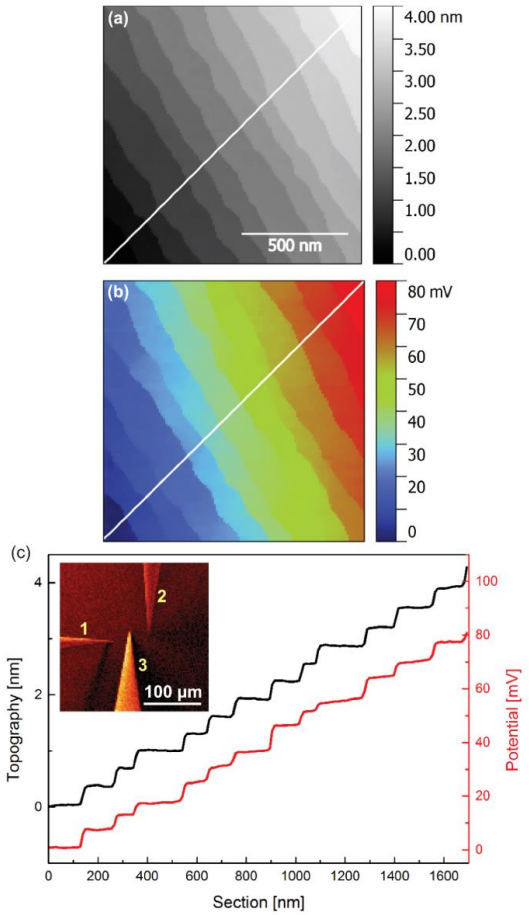

FIG. 7. Transport measurements on Si(111) – (7 × 7). (a) Topography of the surface showing parallel steps with an average terraces width of 130 nm. (b) Corresponding potential image. A sharp voltage drop is observed at the step edges and a small voltage drop across the terraces. (c) Line profiles indicated in (a) and (b). The average voltage drop at the steps is $\Delta V_{\text{step}} = 5.67(1.72)$ mV. The average slope of the terraces is $E = 8.33(45)$ mV/μm. The inset shows the SEM image of the tip setup on the Si(111) – (7 × 7) surface. The distance between the current injecting tips 1 and 2 is 65 μm. Tunneling conditions are $V_{\text{offset}} = 100$ mV and $I_t = 0.01$ nA.

an amount of 69(6)% of the lateral current is transmitted by the surface conductivity associated with the (7×7) reconstructed sample surface.[12] The resulting current density at the position of the scanning tip is $j_{\text{surf}} = \frac{2I}{\pi d} \cdot 0.69(6) = 0.056(4)$ A/m.

Next, the step and terrace conductivities can be determined as before for the Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30° sample. The corresponding measurements are shown in Fig. 7. In the case of Si(111) – (7×7), we observe a variation of the voltage drop at different steps. We attribute this to variations in the shapes and sizes of the terraces and also domain boundaries, which results in changes of the current flow paths. The average voltage drop at the steps is determined to be $\Delta V_{\text{step}} = 5.67(1.72)$ mV and across the terraces $E = 8.33(45)$ mV/μm. The resulting resistivity is $\rho_{\text{step}} = 0.101(32)\,\Omega$m and $\rho_{\text{terrace}} = 149(14) \cdot 10^3\,\Omega/\square$, respectively, while the average step distance in the measurement is 130 nm. These results are in agreement with previously reported results.[12,23] For this surface, the steps contribute 82% of the measured surface resistance, while the terraces contribute 18%.

VIII. SUMMARY

We present a multi-tip scanning tunneling potentiometry realization which can be implemented into present multi-tip scanning tunneling microscopes without hardware changes. The resulting setup allows *in situ* contacting and STP measurements with flexible positioning of two current injecting electrodes such that the current density in the sample surface and the current direction with respect to the sample under investigation can be controlled with no need of contact patterning.

To map the local potential of the sample on the nanoscale, a third tip is scanning the sample surface between the current injecting electrodes by an interrupted feedback technique, recording the local topography and electric potential. A fourth tip is optional and can be used as a reference voltage probe.

Thermovoltage measurements on the Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30° surface demonstrate the performance of the potentiometry feedback by resolving a standing wave pattern. The resolution of the presented setup is determined to be $\sigma = 4.7\ \mu$V.

The ability to map the local transport field is shown on Ag/Si(111) – $(\sqrt{3} \times \sqrt{3})$R30°, where sharp voltage drops located at step edges and symmetrical potential characteristics are observed for reverse current directions. From the investigated sample geometry of a 2D conductor with a parallel step array, conductivities of the terraces and steps can be extracted easily. This straightforward method can further be applied to samples with similar geometry.

For mixed systems of 2D and 3D conduction, a combination of four-probe measurements together with STP allows to first disentangle the bulk and surface conductivity and then determine the contribution of the terraces and steps on the sample surface to the measured conductivity. This approach is demonstrated and gives a comprehensive view of the conduction in Si(111) – (7×7) on the micro and nanoscale and can be further applied to a wide range of samples that are not limited to pure 2D conductors on an insulating bulk as the case in previous STP studies.

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Chapter 2 Four-probe measurements using current probes with voltage feedback to measure electric potentials

2.1 Introduction

In this chapter a newly developed multi-probe measurement method is presented which allows a non-invasive sample characterization. This new measurement method is a further development based on the previous STP implementation which utilizes the multiple tips of the present setup to perform four-point measurements in combination with a potential feedback loop for the voltage sensing tips. In addition to the advantages of previous four-probe measurement implementations in multi-tip STMs, such as flexible positioning of the tips and *in situ* measurement, the resulting setup simplifies the required measurement electronics and allows non-invasive multi-probe measurements.

In general, independent from scanning probe measurement capabilities multi-probe measurements setups, such as commercially available parameter analyzers have two current injecting tips to which a bias voltage is applied and the resulting lateral current through the sample is measured. Two further tips are then used for the measurement of the potential drop across the sample which is typically performed by a voltage follower circuit [27]. In the implementation presented here however, we use the potential feedback as described in the previous chapter of this thesis instead of voltage follower circuits. The most striking advantage is that the new implementation allows the measurement of the voltage drop across the sample non-invasively which means the sample is not damaged in the course of the measurement, because all measurement contacts can be realized with tunneling contacts. The potential measurement is hereby performed as described in chapter 1, with the measurement tips a few tenths of nanometers above the sample surface, while current injection takes place in tunneling contact as in usual constant-current STM experiments.

Non-invasive *in situ* four-probe measurements in combination with scanning tunneling potentiometry make the here reported four-tip STM a powerful tool for the characterization of fragile materials which are of interest for electronic applications. Transport measurements which span the length scale from millimeter to nanometer without changes in the experimental setup – even the same set of tips can be used for all the different measurements. As a result, the same setup can be used for macroscopic transport measurements, but also for the characterization of nanoscale defects.

Furthermore, the technique is also combinable with magnetic fields and low temperatures which, in combination with the gating, allows to perform the whole spectrum of classical transport measurements *in situ* and non-invasive.

2.2 Four-probe measurements using current probes with voltage feedback to measure electric potentials

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- **F. Lüpke**, D. Cuma, S. Korte, V. Cherepanov, and B. Voigtländer, Four-probe measurements using current probes with voltage feedback to measure electric potentials.

Author contributions:
F.L., S.K., V.C. and B.V. conceived the experiments**. F.L.** and D.C. performed the measurements and analyzed the experimental data. **F.L.**, D.C., S.K., V.C. and B. V. wrote the paper. All authors discussed and commented on the manuscript.

Four-point probe measurements using current probes with voltage feedback to measure electric potentials

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(Dated: January 3, 2018)

We present a four-point probe resistance measurement technique which uses four equivalent current measuring units, resulting in minimal hardware requirements and corresponding sources of noise. Local sample potentials are measured by a software feedback loop which adjusts the corresponding tip voltage such that no current flows to the sample. The resulting tip voltage is then equivalent to the sample potential at the tip position. We implement this measurement method into a multi-tip scanning tunneling microscope setup such that potentials can also be measured in tunneling contact, allowing in principle truly non-invasive four-probe measurements. The resulting measurement capabilities are demonstrated for $BiSbTe_3$ and $Si(111) - (7 \times 7)$ samples.

I. INTRODUCTION

Four-terminal sensing and four-point probe methods are widely used measurement techniques which allow to determine the electrical resistance of a sample [1]. In contrast to classical two-terminal measurements, this technique eliminates lead and contact resistances from measurements and thereby allows the precise measurement of resistances with high accuracy. Originally proposed by F. Wenner for application in geophysics [2], today four-probe measurements can be found in a wide range of applications including semiconductor characterization [1]. Due to their high accuracy, four-probe measurements are often used in fundamental research such as (low temperature) transport measurements where the sample under investigation is typically contacted by lithographic contacts [3], monolithic four-point probes [4–7] or a multi-tip scanning tunneling microscope (STM) [8–13]. In general, the four-probe measurement setup consists of two biased contacts which inject a current into the sample and two contacts which measure the resulting voltage drop across the sample, e.g. by high ohmic volt meters [1, 8, 10]. The four-probe resistance of the sample is then determined from the slope of the resulting four-probe I/V curve [8].

Previously reported implementations of four-probe measurements into a multi-tip STM require two different kinds of electronics for current and voltage sensing, respectively [8]. As a result, in order to approach the tips to the sample surface and to exchange contacts during four-probe measurements, the tips have to be rewired to the different electronics in between measurements. One approach to simplify this process is to use four instances of identical electronics which can perform both, voltage and current measurements [8, 11] as shown in Fig. 1 (left). The switching between the two measurement modes is then performed e.g. by a relay [8, 11]. A drawback of this approach is, that it leads to bulky, complex electronics and introduces additional noise to the measurements due to the additional circuitry.

An alternative way to measure local sample potentials in a STM is the scanning tunneling potentiometry method [11, 14, 15]. In this method, the voltage applied to the tip is controlled by a feedback loop, such that the current to the sample vanishes, i.e. the electrical potential of the tip and the sample at the position of the tip are identical. The voltage resulting in a vanishing current is then recorded as the local electric potential of the sample.

Here, we present a four-probe measurement implementation where voltage measurements are performed by means of current measurement in combination with a software voltage feedback loop. This approach requires only four identical, minimalistic, biased current measurement units, as hardware voltage measurement circuitry and relays are redundant. In the resulting setup, shown in Fig.

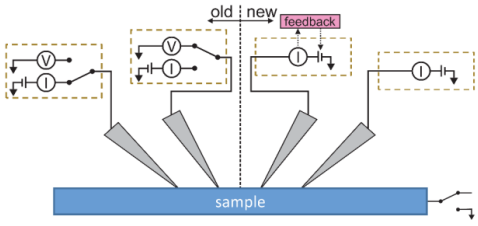

FIG. 1. Schematic of a four-point measurement with tips of a multi-tip STM forming the contacts on the sample surface. (left) A measurement setup, where each tip is connected to identical electronics which can be switched between voltage and current measurement mode by a relay. (right) A setup, where each tip is connected to identical biased current measurement electronics and voltage measurements are performed via feedback loops. The complete four-probe measurement setup results by mirroring at the central vertical dashed line, respectively. In both realizations, the sample ground contact is connected to approach the tips to the sample and is disconnected during the four-probe measurements.

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1 (right), current and voltage probes can be flexibly exchanged without any rewiring. Furthermore, the voltage sensing can be performed in tunneling contact such that truly non-invasive four-probe measurements become possible which is advantageous e.g. for the characterization of fragile samples. This paper organizes as follows. In Sec. II, we focus on one of the voltage probes where we discuss different kinds of realizations of the voltage measurement. In Sec. III, we determine the theoretical noise levels of the different voltage measurement realizations and subsequently the entire four-probe measurement setup. In Sec. IV, we demonstrate four-probe measurement capabilities on $BiSbTe_3$ and Si(111)$-(7\times7)$ samples under ultra-high vacuum conditions. In Sec. V, further applications and improvements of the present setup are discussed.

II. METHODS

The experimental setup used here is a home-built room temperature four-tip STM with electrochemically etched tungsten tips. Further details on the experimental setup can be found in Refs. 16 and 17. In this setup, we compare different four-probe measurement methods in which the voltage measurement is realized in three different ways (A) to (C).

A. Voltage follower

In this voltage measurement method, the voltage sensing tip is connected to a typical voltage follower circuit, as used in previous setups [8] and as shown schematically in Fig. 2 (a). The tip is brought into direct contact to the sample by approaching it towards the sample surface by a few nm out of the tunneling contact as described elsewhere [8, 18]. The resulting junction resistance between the tip and the sample typically is in the range of kΩ to MΩ. The local sample voltage at the position of the tip V_{local} is measured by a high input-impedance buffer circuit before the signal is read into the measurement software via an analog-to-digital converter (ADC). Between the voltage follower circuit and the ADC a low-pass filter can be used to adjust the measurement bandwidth Δf in order to reduce the measurement noise.

B. Voltage feedback

This approach is based on the measurement of the voltage by nulling the current flowing between the tip and sample, similar to standard methods for measuring voltages with high precision [19]. As in the voltage follower application, the voltage sensing tip is in direct contact to the sample surface but is only connected to a biased transimpedance (current) amplifier. A schematic of the setup is shown in Fig. 2 (b). The voltage sensing is performed by a proportional-integral software feedback loop, similar to the topography feedback loop typically used in STM. For this purpose, the amount of current through the tip at a certain tip bias voltage V_{bias} is read into the measurement software via an ADC converter and the feedback loop nulls the tip-sample current by continuously adjusting V_{bias} via a digital-to-analog converter (DAC) connected to the V_{bias} input of that tip, until $V_{\mathrm{bias}} = V_{\mathrm{local}}$ [11, 15]. The measurement noise bandwidth in this implementation is given by the bandwidth of the feedback loop, which we determine as the time interval $\tau = 1/(2\pi\Delta f)$ in which the difference between currently applied tip voltage and target local sample voltage $V_{\mathrm{bias}} - V_{\mathrm{local}}$ decreases by $1 - e^{-1} \approx 63.2\%$, similar to an RC circuit (Fig. 2 (c)). Δf can be determined by applying a sine signal to the input of the closed feedback loop and tuning its frequency until a damping of $-3\,\mathrm{dB}$ is observed. At this point the sine frequency corresponds to Δf. Note that the resulting feedback duration t_{fb} which is required for the feedback loop to converge below the noise threshold is typically larger than τ and depends on the initial difference of the two signals $V_{\mathrm{bias}} - V_{\mathrm{local}}$.

C. Tunneling voltage feedback

This method is a special case of (B), where the voltage sensing tip is in tunneling contact rather than direct contact. A challenge in the measurement of the local sample voltage in tunneling contact is that, both the topography feedback and voltage measurement are entangled by their concurrent use of the tunneling current as the process variable [11]. One solution for this problem is the temporary stopping the topography feedback during the measurement of the local sample potential. However, a deactivation of the topography feedback results in the tip drifting towards or away from the sample on the time scale of less than a second (at room temperature), resulting in a significant change of the junction resistance, as the tunneling current depends exponentially on the tip-sample distance. Therefore, for typical four-probe measurement durations of up to several minutes it is difficult to hold the tip in tunneling contact throughout the measurement. For this reason, also the measurement of the local sample potential in tunneling contact with a voltage follower is impractical.

The alternating feedback technique [11, 15] overcomes this problem. In this method, the STM control software performs alternatingly topography and voltage feedback on the timescale of ms. The corresponding schematic setup is shown in Fig. 2 (d). In detail, the tip height in tunneling contact is controlled such that a current set point I_{set} is maintained at a fixed tunneling voltage $V_{\mathrm{bias}} = V_{\mathrm{t}}$. Then, for a time t_{fb}, the topography feedback is stopped (the tip is held at fixed height above the sample), while the tip voltage V_{bias} is adjusted such that the tunneling current vanishes as described in the voltage feedback method and shown in Fig. 2 (c). Afterwards the

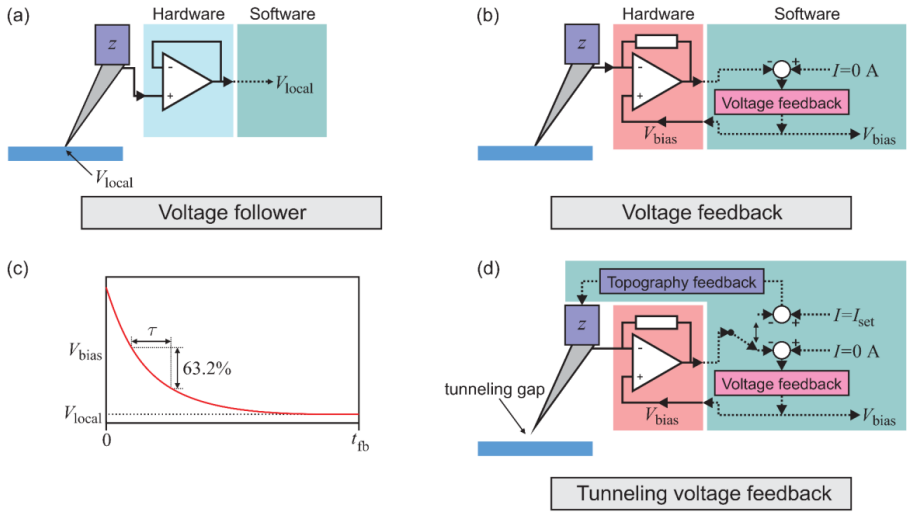

FIG. 2. Schematic of the three voltage measurement techniques. Solid lines correspond to hardware connections and dashed lines to software implementations. At the interfaces of hardware and software realizations, analog-to-digital and digital-to-analog converters transform the signals accordingly (not shown). (a) Schematic of the voltage follower implementation with the tip in direct contact with the sample surface. The local sample potential V_{local} is directly passed to the output of the voltage follower circuit and into the software. (b) Schematic of the software voltage feedback implementation which continuously adjusts the current through the tip to 0 A (such that $V_{\mathrm{bias}} = V_{\mathrm{local}}$) in direct contact to the sample surface. (c) Schematic of the working principle of the voltage feedback. The tip voltage V_{bias} is adjusted to the local sample potential V_{local} for a feedback duration t_{fb}. The bandwidth of the feedback loop is Δf, which we determine as the decrease of $V_{\mathrm{bias}} - V_{\mathrm{local}}$ by $1 - e^{-1} \approx 63.2\%$ in the time interval $\tau = 1/(2\pi\Delta f)$. (d) Schematic of the tunneling voltage feedback implementation in which the software alternatingly performs topography feedback (setpoint $I = I_{\mathrm{set}}$) and voltage feedback (setpoint $I = 0\,\mathrm{A}$) on the timescale of ms.

tunneling voltage $V_{\mathrm{bias}} = V_{\mathrm{t}}$ is restored, the topography feedback is re-enabled and the procedure is repeated. A drawback of this method is that the switching between the two feedback loops takes up additional time in comparison to methods (A) and (B). As a result, the fundamental noise level for the same measurement duration increases in comparison to a measurement without alternating feedback. However, the striking advantage of this method over previous methods is that the local sample potentials can be measured non-invasively and with the same minimalistic electronics as in the voltage feedback implementation (B).

An alternative way to disentangle the topography and potential feedback in tunneling contact include the use of a DC current component and an AC current component and use them individually for the voltage and topography feedback, respectively [14, 20, 21]. However, this method requires additional circuitry and is reported to be prone to cross-talk between the AC and DC signal [22]. For this reason, we focus here only on the performance of the voltage follower and alternating feedback techniques.

For comparison of the different measurement techniques (A) through (C) we connect each of the four tips to one of four instances of equivalent electronics including a relay which can switch between a voltage follower circuitry (based on OPA111) and a biased commercial FEMTO DLPCA-200 variable gain transimpedance amplifier [23] to measure the currents with adjustable measurement range. Typically, the gain of the current injecting tips is $10^6\,\mathrm{V/A}$, while that of the voltage sensing tips in the voltage feedback techniques is $10^9\,\mathrm{V/A}$. For the voltage feedback techniques, we further use voltage dividers of up to 1/1000 in front of the bias voltage connector of the voltage sensing tip's electronics, in order to increase the voltage feedback accuracy which can otherwise be limited by the minimum step size of the DAC and noise in the V_{bias} signal. The resulting voltage feedback resolution of the present setup is readily in the µV range [11, 12].

III. NOISE ANALYSIS

To compare the individual voltage measurement methods, we use in the following a measurement bandwidth of $\Delta f = 275\,\mathrm{Hz}$, which is smaller than the bandwidth of the used current amplifier and voltage follower circuits,

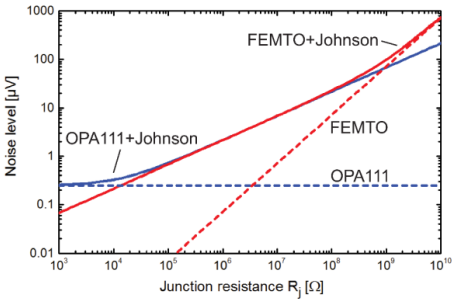

FIG. 3. Detector noise V_{detector} of voltage follower (dashed blue line) and voltage feedback (dashed red line) circuitry and resulting respective noise limit V_{limit} (solid lines) in combination with Johnson noise, as a function of the junction resistance R_{j} for detector bandwidths of $\Delta f = 275\,\text{Hz}$. For large junction resistances $R_{\text{j}} \gtrsim 1\,\text{G}\Omega$ the noise level of both, the voltage follower and voltage feedback method, is too large for typical four-probe measurements $V \gtrsim 100\,\mu\text{V}$. At intermediate junction resistances $100\,\text{k}\Omega \lesssim \text{R}_{\text{j}} \lesssim 1\,\text{G}\Omega$ the noise performance of both implementations is dominated by the Johnson noise resulting in approximately the same noise level. For small junction resistances $R_{\text{j}} \lesssim 100\,\text{k}\Omega$ the noise level of the voltage follower circuit converges to the fundamental input noise level of the used opamp (dashed blue line). For the voltage feedback, the noise level continuously decreases as the junction resistance is further lowered resulting in a lower noise level compared to the voltage follower.

respectively. A general limitation of the voltage measurement accuracy is given by the junction resistance R_{j} between the probes and the sample. On the one hand, the thermal (Johnson) noise of the tip-sample junction is given by [24]

$$V_{\text{Johnson}} = \sqrt{4k_{\text{B}}T\Delta f R_{\text{j}}},$$

where k_{B} is the Boltzmann constant and $T = 300\,\text{K}$ is the junction temperature. Additionally, large junction resistances result in a smaller lateral current injected into the sample which decreases the signal-to-noise ratio with respect to the detector noise floor. In the case of the voltage follower circuit (A), the detector noise is given by [24]

$$V_{\text{detector}} = \widetilde{V}_{\text{detector}}\sqrt{\Delta f},$$

where $\widetilde{V}_{\text{detector}} = 15\,\text{nV}/\sqrt{\text{Hz}}$ is the input noise density of the OPA111. The resulting total voltage noise at the tip-sample junction is given by

$$V_{\text{limit}} = \sqrt{V_{\text{Johnson}}^2 + V_{\text{detector}}^2}.$$

On the other hand, the detector noise limit of the voltage feedback techniques (B) and (C) is limited by the input current noise of the current amplifier $\widetilde{I}_{\text{detector}}(\text{gain} = 10^9\,\text{V/A}) = 4.3\,\text{fA}/\sqrt{\text{Hz}}$. Resulting from the current noise in combination with the junction resistance follows a corresponding voltage noise of [24]

$$V_{\text{detector}} = \underbrace{\widetilde{I}_{\text{detector}}R_{\text{j}}}_{\widetilde{V}_{\text{detector}}}\sqrt{\Delta f}.$$

In contrast to the voltage follower circuit, this noise limit depends also on the junction resistance R_{j}, which means that for vanishing junction resistance, the voltage noise V_{limit} goes to zero.

Figure 3 shows a plot of the theoretical noise limit of the present voltage follower and voltage feedback circuitry as a function of the junction resistance R_{j} and at $\Delta f = 275\,\text{Hz}$. As evident in the graph, for large junction resistances $R_{\text{j}} \gtrsim 1\,\text{G}\Omega$ the noise level of both, the voltage follower and feedback method, is too large for typical four-probe measurements $V_{\text{limit}} \gtrsim 100\,\mu\text{V}$. At intermediate junction resistances $100\,\text{k}\Omega \lesssim R_{\text{j}} \lesssim 1\,\text{G}\Omega$ the noise level of both implementations is almost identical as it is dominated by the Johnson noise and is in an acceptable range for most applications. For small junction resistances $R_{\text{j}} \lesssim 100\,\text{k}\Omega$, the voltage follower approaches the constant noise limit of the OPA111, while the noise level of the voltage feedback technique further decreases. We conclude that for high accuracy measurements, the voltage feedback technique is superior to the voltage follower implementation.

A way to further increase the measurement accuracy is an averaging of the measurement signals over a time interval larger than the measurement bandwidth. Hereby, the statistical noise decreases as $\sim 1/\sqrt{t}$ with the measurement duration t. However, this is only true if the measurement setup itself is stable. In real measurements, thermal drift and fluctuations in the contacts, e.g. due to electromigration, can have significant influence on R_{j} and thus on the noise in the four-probe measurement. As a result, for $t > 1/(2\pi\Delta f)$ it can be expected that the noise will first go down with $1/\sqrt{t}$ due to the increased averaging of the statistical noise before it starts to deviate from this behavior as the measurement time becomes longer than the time constant on which the measurement setup is stable. The latter can largely depend on the sample under investigation, the exact measurement setup, the tip material and the voltage measurement method used. In typical four-tip setups, the tips are mounted under 45° angle with respect to the sample surface, such that contacting the tip to the sample surface results in a flexible junction between the sample and the elastic tip. As a result, in direct contact, drift does not have such a significant effect on the four-probe measurement as the junction resistance does not change significantly during typical measurement durations. In the alternating feedback technique, on the other hand, the separation between voltage sensing tip and sample is continuously controlled by the alternating feedback, such that the drift for all of the present techniques should be comparable.

To determine the noise level of the full four-probe I/V measurement, in principle both the noise of the measured injected current I and the voltage drop V have to be considered. However, the Johnson noise occurring at the current injecting contacts correspond to fluctuations in the contact resistances which do not play a role in four-probe measurements. As a result, the error in the measurement of the injected current is only determined by the detector noise which in the present setup is below

$$I_{\mathrm{detector}} = \widetilde{I}_{\mathrm{detector}}(\mathrm{gain} = 10^6\,\mathrm{V/A}) \cdot \sqrt{\Delta \mathrm{f}} \approx 2.2\,\mathrm{pA}.$$

As typical injected currents are at least $\sim$ nA, the voltage measurement noise is the dominant source of noise in the four-probe measurements.

IV. FOUR-PROBE MEASUREMENTS

In the four-probe measurements, we record a fixed number of data points (e.g. 1000) for each I/V curve and record the voltage drop for each increment of injected current. The resulting four-probe resistance $R_{4\mathrm{P}}$ is determined by a linear fit to the data around 0 A and for a two-dimensional conductor is independent of the tip spacing when measured with an equidistant tip-tip separation [1]. The corresponding sample sheet conductivity is

$$\sigma_{2\mathrm{D}} = \frac{\ln(2)}{R_{4\mathrm{P}}\pi}.$$

As errors in the positioning of the tips can have a large influence on the measured conductivity [25], for the comparison of the different techniques we have performed each measurement without repositioning the tips between the individual measurements on each sample. As a result, positioning errors can be excluded from the comparison of the different measurements as they only influence the absolute resistance measured but not the relative errors which we will compare in the following.

A. $BiSbTe_3$

We first demonstrate four-probe measurements using the different voltage measurement techniques on a 10 nm thin film of $BiSbTe_3$. The sample was grown on Si(111) by molecular-beam epitaxy and was exposed to air prior to the analysis in the four-tip STM chamber [12]. The result of an equidistant four-probe measurement on the $BiSbTe_3$ film using the tunneling voltage feedback technique and a measurement duration $t = 15\,\mathrm{s}$ is shown in Fig. 4 (a). The linear fit results in $R_{4\mathrm{P}} = 1210(2)\,\Omega$ and therefore $\sigma_{2\mathrm{D}} = 0.1823(3)\,\mathrm{mS}/\square$, corresponding to a relative error of 0.17%. The comparison of the relative errors for the different measurement durations and techniques is shown in Fig. 4 (b). We find that the data of the tunneling voltage feedback measurements shows

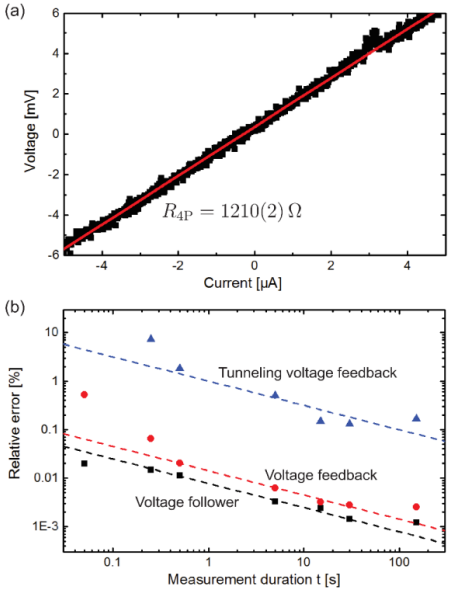

FIG. 4. (a) Equidistant four-probe I/V of $BiSbTe_3$ measured by tunneling voltage feedback (measurement duration $t = 15\,\mathrm{s}$) with a linear fit. (b) Error of the resistance measurement relative to the measured resistance for the three different measurement techniques and for different measuring durations on $BiSbTe_3$. The dashed lines correspond to the expected behavior of statistical noise $\sim 1/\sqrt{t}$. For shorter measurement durations, the voltage feedback does not fully converge, resulting in additional measurement errors while for longer measuring durations ($> 30\,\mathrm{s}$) variations in the tip contacts increase the error in the data.

generally a higher noise level compared to the other two methods, which have comparable noise levels. We attribute this finding to the larger junction resistance of the tunneling contact in comparison to the other measurement methods in combination with smaller averaging duration during the measurement as result of the alternating feedback. In the same graph, we have also plotted dashed lines corresponding to $a \sim 1/\sqrt{t}$ behavior for each of the three methods which represents the theoretical dependence of statistical noise on the tunneling resistance and which describe the data quite well. We attribute this observation to the fact that the sample is quite soft and therefore the contacts of the tips with the sample are rather stable such that the combined Johnson and amplifier noise is the dominant source of noise for $0.5\,\mathrm{s} \leq \mathrm{t} \leq 30\,\mathrm{s}$. For $t < 0.5\,\mathrm{s}$, the data points of the voltage feedback measurement deviate from the graph of the statistical noise. In this range, due to the short measurement duration the voltage feedback loop does not fully converge to each new value of V_{local} as the lateral current is swept,

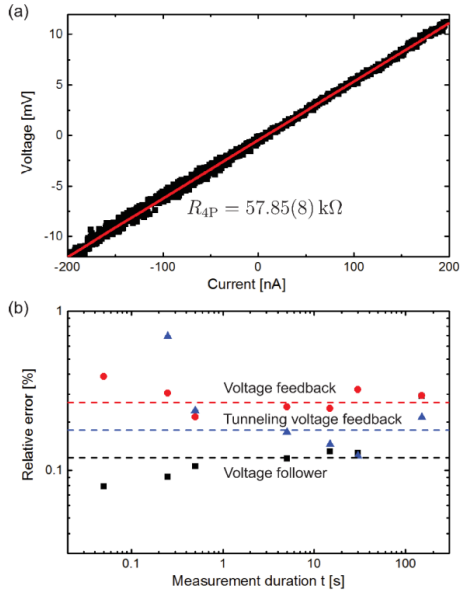

FIG. 5. (a) Equidistant four-probe I/V of Si(111) $-$ (7×7) measured by tunneling voltage feedback (measurement duration $t = 15\,\mathrm{s}$) with a linear fit. (b) Relative noise of the different measurement techniques for different measuring durations t on Si(111) $-$ (7×7). The dashed lines correspond to the average constant noise levels of the three measurement techniques. For shorter measurement durations the limited bandwidth of the voltage feedback based techniques increases the measurement error.

resulting in additional errors in the measurements. For $t > 30\,\mathrm{s}$, we find that measurement instabilities begin to increase the measurement errors above the expected statistical error behavior. We estimate the junction resistances of the current injecting tips from the difference of the measured 2D sheet conductivity in comparison to the current/voltage characteristics at the current injecting tips to be $R_\mathrm{j} \approx 9\,\mathrm{k\Omega}$. The junction resistance for the tunneling voltage feedback is $R_\mathrm{j} \approx 40\,\mathrm{M\Omega}$

B. Si(111) $-$ (7×7)

We further applied the different four-probe measurement techniques to the Si(111) $-$ (7×7) surface. The transport properties of this surface have been under recent discussion because earlier results on its surface conductivity varied largely as a result of numerous different measurement and sample preparation procedures [4]. One way to measure the surface conductivity is to determine the two-dimensional contribution in distance-dependent four-probe measurements [5, 9, 11, 26]. Fig. 5 (a) shows a typical four-probe measurement on this surface in tunneling voltage feedback mode. The linear fit results in $R_{4P} = 57.85(8)\,\mathrm{k\Omega}$ corresponding to $\sigma_{2D} = 3.814(5) \cdot 10^{-6}\,\mathrm{S/\square}$. This result is in general agreement with previous measurements on the same samples which used the voltage follower method [10]. For a more detailed comparison, Fig. 5 (b) shows the noise levels for the three different techniques and at varying measurement duration on the same sample without repositioning the tips. While there are deviations for short measurement durations $t < 0.5\,\mathrm{s}$ which are again the result of the voltage feedback loop not fully converging, especially in tunneling contact, we find that noise level of the three different techniques approximately coincide for measurement durations $t \geq 0.5\,\mathrm{s}$. In this range, the data shows rather constant noise levels for all three techniques, which means that the larger amount of noise resulting from the tunneling contact of the voltage probe in contrast to the voltage measurement in direct contact is insignificant under the present measurement conditions. We explain this finding to be due to large fluctuations in the tip contacts during the measurements resulting from the hard sample surface and non-linearities in the four-probe I/V curves which dominate the noise in the measurements. We estimate the junction resistance of the current injecting tips in contact to be $R_\mathrm{j} \approx 200\,\mathrm{k\Omega}$. In comparison, the junction resistance of the tunneling tip in the present case is $R_\mathrm{j} \approx 20\,\mathrm{M\Omega}$.

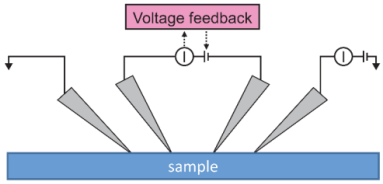

FIG. 6. Schematic of the most simple four-point probe measurement setup using the voltage feedback technique. The current through the sample is injected between a tip connected to a biased current sensor and a tip on ground potential. The voltage drop across the sample is determined by the two inner tips which are connected to a biased current sensor which nulls the current between the voltage sensing tips. The voltage required to compensate the current through the tips corresponds to the voltage drop across the sample surface between the two contact points of the voltage sensing tips.

V. DISCUSSION

The most simple measurement setup of a four-point measurement resulting from the voltage feedback method is shown in Fig. 6. Here, only two current measurement units are required, one to inject the lateral current to another tip on ground potential and the other to null the current between the two voltage sensing tips. The resulting voltage at which no current flows through

the voltage sensing tips corresponds to the voltage drop across the sample surface between the respective contact points of the voltage sensing tips.

The present approach further allows to have all four tips required for the four-probe measurement in tunneling contact to the sample, which enables truly non-invasive four-probe measurements. For this application the only additional requirement is that the sample needs to be on floating potential during the potential measurement and on fixed potential for the topography feedbacks of the tips. While we have not yet implemented this approach into the present setup, yet, it can be realized e.g. by switching of a relay connecting the sample to ground synchronous with the topography feedback. Note that this relay would not result in much additional noise in the actual four-probe measurement because it is not located in any of the current paths of the actual measurement. An alternative would again be the use of an AC component for the topography feedback and a DC component for the actual four-probe measurement. In this realization, to decouple the DC conductivity measurement, the sample could be connected via a capacitor to a sine generator, which provides the AC signal. We further propose that it is also possible to use a different mechanism for the topography feedback, e.g. atomic force microscopy (AFM) based feedback, to maintain a constant tip-sample distance while the potential measurement is continuously performed via the tunneling current. The advantage of an AFM feedback to control the tip heights is that the sample can be on floating potential throughout the entire measurement[27].

A general advantage of non-invasive four-probe measurements is that the damaging of the samples and tips is greatly reduced compared to conventional four-probe measurements. This is important because a change in the sample surface structure can significantly alter its transport properties. While for the measurements shown in the present manuscript the influence of tip contacting on the measured conductivity is negligible because of the spatial extent of the samples, this aspect becomes more important for smaller and more fragile nanostructures, e.g. monoatomic wires. Furthermore, for samples in the ballistic transport regime especially the invasiveness of the voltage probes can have a significant influence on the measured transport properties [28]. Using the tunneling voltage feedback technique one can precisely control the invasiveness of these probes. Concerning the tip wear, conventional four-probe measurements lead to a blunting and bending of the tips such that they have to be exchanged regularly. In contrast, four-probe measurements in tunneling contact prevent much of this wear and increase the tip lifetime significantly.

VI. CONCLUSION

We have demonstrated a multi-point probe implementation which uses equivalent minimalistic current sensors at each probe and where voltage measurements are performed by a software voltage feedback loop. The resulting setup performance, under typical experimental conditions, is comparable to previous voltage follower setups, but with less complicated electronics. As we have used here the same electronics for the comparison of the different measurement methods, in the final application the noise level of the voltage feedback techniques will be even lower than demonstrated here, when the electronics are reduced to only the required biased current amplifiers. Nevertheless, we find that all of the above measurement errors are small ($\leq 1\%$) compared to other typical error sources in four-probe measurements, especially the positioning errors of the tips which result in relative errors in the measured conductivity of $\sim$ 10% [10, 25]. The implemented tunneling voltage feedback technique further allows the non-invasive characterization of sample transport properties, compatible with vacuum conditions, low temperatures, gating and magnetic fields which makes it a powerful tool for future studies.

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Chapter 3 Electrical resistance of individual defects at a topological insulator surface

3.1 Introduction

Topological insulators host surface states with properties that make them promising candidates for the application in electronic devices. Here, we will focus on the three-dimensional (3D) TIs, which have a two-dimensional topological surface state at its surface in combination with a bulk band gap.

The theoretical prediction of 3D TIs [9] led to experimental efforts in form of a search for materials showing the predicted properties with the first reported 3D TI being the alloy $Bi_{1-x}Sb_x$ found by Hsieh et al. in 2008 [28]. Shortly thereafter, further promising materials with band gaps of up to 300 meV were reported in form of Bi_2Se_3, Bi_2Te_3 and Sb_2Te_3 [29].

TI are characterized by an inverted band gap which is typically the result of a large spin-orbit coupling (SOC) [29]. The result is an inverted band gap which at the boundary to a 'regular' material (with a regular, non-inverted, band gap) leads to a band crossing at the surface of the TI.

The special property of the band crossing is that it has a spin polarized linear dispersion as shown in Fig. 3.1. The spin-polarized linear dispersion results on the one hand that elastic 180° backscattering is suppressed in these materials. On the other hand, the linear dispersion corresponds in theory to that of massless charge carriers and therefore high carrier mobility, potentially leading to low power electronics.

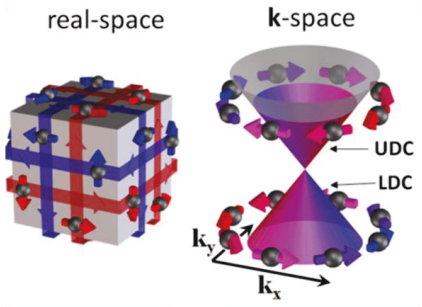

Figure 3.1. Schematic of the topological surface state of a three-dimensional topological insulator in real-space and momentum-space. The spin-polarization is indicated by colored arrows. [10]

In sum, these properties make TIs promising candidates for application in devices and as a result the transport through the TSS is of great interest.

It has however become clear that unintentional defects, such as vacancies and anti-site defects can undermine the electric transport through the TSS by shifting the Fermi level intro the bulk bands. This effect can be compensated by alloying different TIs into ternary and quaternary materials.

In the following the ternary material $(Bi_{1-x}Sb_x)_2Te_3$ with $x \sim 0.5$ is investigated. This compound is optimized for low bulk conductivity such that an electrical current through the sample is mainly transmitted by the TSS. As a result, the current flow through the TSS at the sample surface can be assessed in real space by STP in order to understand the implications resulting from the band structure in experiments and ultimately in devices.

We present in the following a detailed analysis of the influence of different kinds of defects (step edges, domain boundaries, void defects) on an electric current transmitted through a $(Bi_{1-x}Sb_x)_2Te_3$ thin film sample. For these transport measurements, we used the methods reported in chapter 1 and 2 of this thesis.

3.2 Electrical resistance of individual defects at a topological insulator surface

The following article has been published in the journal **Nature Communications**:

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Author contributions:
F.L., M.E., T.H., M.L. and N.v.d.D. performed the experiments. **F.L.**, V.C. and B.V. designed the STP experiment. M.E., T.H., L.P. and C.M.S. designed the photoemission experiment. M.L., P.S., D.R., N.v.d.D., G.M. and D.G. developed and fabricated the samples. The manuscript was written by **F.L.**, M.E., T.H., M.L. and B.V. All authors discussed and commented on the manuscript.

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Electrical resistance of individual defects at a topological insulator surface

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Three-dimensional topological insulators host surface states with linear dispersion, which manifest as a Dirac cone. Nanoscale transport measurements provide direct access to the transport properties of the Dirac cone in real space and allow the detailed investigation of charge carrier scattering. Here we use scanning tunnelling potentiometry to analyse the resistance of different kinds of defects at the surface of a $(Bi_{0.53}Sb_{0.47})_2Te_3$ topological insulator thin film. We find the largest localized voltage drop to be located at domain boundaries in the topological insulator film, with a resistivity about four times higher than that of a step edge. Furthermore, we resolve resistivity dipoles located around nanoscale voids in the sample surface. The influence of such defects on the resistance of the topological surface state is analysed by means of a resistor network model. The effect resulting from the voids is found to be small compared with the other defects.

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It has recently become clear that three-dimensional topological insulators (TIs) with their unique electronic properties are prime candidate materials for spintronic devices and quantum computing[1]. Prohibited 180° backscattering is ascribed to the topological surface states (TSSs) of these materials, which potentially leads to low power dissipation and high-efficiency devices[1,2]. Although research on these materials is still in an early stage, especially the compounds Bi_2Se_3, Bi_2Te_3 and Sb_2Te_3 have the potential to result in a disruptive technology due to their applicability at room temperature resulting from a pronounced band gap of up to 300 meV (refs 1,3).

Although strict 180° backscattering is prohibited in the TSS, it has become clear that phonon scattering and scattering at defects at different angles can significantly contribute to the resistance of the TSS[4,5]. Such backscattering at the surface of a TI has first been analysed by quasiparticle interference at steps and atomic defects[2,6–8]. Only recently, the electrical resistivity of single steps at the surface of Bi_2Se_3 was measured in locally resolved transport measurements[9]. However, when describing the nanoscopic resistance in a TI, steps are only one part of the whole picture and further defects such as domain boundaries and voids at the TI surface may have an important influence on the total sample resistance, as we will show in the following.

Here we use a combination of *in situ* surface analysis tools, angle-resolved photoemission spectroscopy (ARPES) and four-tip scanning tunnelling microscopy (STM), to achieve a detailed electronic and charge transport analysis of pristine $(Bi_{0.53}Sb_{0.47})_2Te_3$ thin films, respectively. For this compound, it has recently been shown that it has low bulk conductivity, whereas on its surface the Fermi energy cuts only through the TSS[10–13]. As a result, a current through the sample is expected to be transmitted predominantly by the TSS, which makes $(Bi_{0.53}Sb_{0.47})_2Te_3$ a promising candidate material for application in devices. Furthermore, it allows us to directly measure the nanoscopic resistance of individual defects, which we find at the TI surface. Consequently, we are able to determine the contribution of each type of nanoscale defects to the overall TI film resistivity. In particular, we find that domain boundaries result in the largest localized resistance, which is four times higher than that of a step edge. Furthermore, the resistance due to nanoscale voids in the TI surface is miniscule compared with these defects.

Results

Macroscopic sample characterization. We investigate in the following a 10.5(5) nm film of $(Bi_{0.53}Sb_{0.47})_2Te_3$ prepared on a Si(111) substrate by molecular beam epitaxy[10,14]. We used the same sample for STM and ARPES measurements, which was kept under ultra high vacuum (UHV) conditions at all times to avoid any contamination of the TI surface throughout the measurements. The topography of the film measured by STM is shown in Fig. 1a. Here we find screw dislocations and step heights of 1 nm corresponding to quintuple layer (QL) steps as the dominant features in accordance with the literature[14]. Step heights different than 1 nm are only observed within a few nanometres away from the dislocation cores. From the average thickness of the TI film and the observed surface structure, we conclude that the TI film consists of 9 QL (the ninth layer is ~97% closed), with additional material distributed in form of islands in three open layers on top of the ninth QL. ARPES results of the surface obtained at $h\nu = 8.4$ eV are shown in Fig. 1b. Here, the TSS can be unambiguously identified as Dirac cone with the Dirac point located just above the valence band edge. By varying the photon energy to $h\nu = 21.2$ eV, we further find some contributions from the bulk conduction band minimum at the Fermi energy due to its higher relative cross-section at this photon energy[15]. From this measurement, we determine the band gap at the TI surface to be 260(20) meV (see Supplementary Note 1 and Supplementary Fig. 1). The observed inherent *n*-doping of the TI surface we attribute to a downward band bending with respect to its bulk[16,17]. Spin-resolved energy distribution curves further reveal a high spin polarization of the Dirac cone, confirming the topological nature of the observed surface state (Supplementary Note 1 and Supplementary Fig. 1).

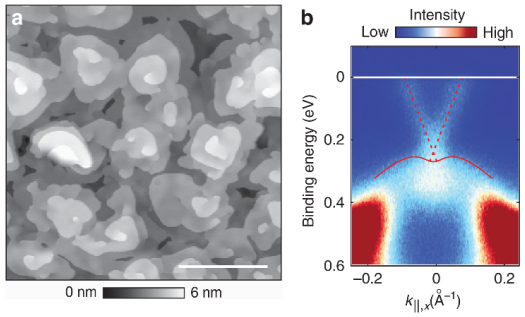

Figure 1 | Overview of the sample topographic and electronic structure. (**a**) STM image of the sample surface, showing that screw dislocations and QL steps are the dominant features. Scale bar, 200 nm. (**b**) ARPES measurement of the same sample along $k_{\|,x}$ direction (in-plane, corresponding to $\bar{K} - \bar{\Gamma} - \bar{K}$). The Fermi energy is indicated by the solid white line. The Dirac cone of the TSS is indicated by dashed red lines intersecting at the Dirac point just above the valence band edge (solid red curve).

The macroscopic sample conductivity at room temperature is measured *in situ* in a four-probe geometry with a home-built four-tip STM[18]. Using equidistant tip spacing $s = 5$–$100\,\mu$m, we find linear four-probe *I*/*V* curves and constant four-probe conductance as a function of the tip spacing, as expected for a two-dimensional conductor[5]. The resulting sheet conductivity of the TI film is $\sigma_{4P} = 0.44(5)\,\mathrm{mS}\square^{-1}$. Furthermore, we determine the carrier concentration in the TSS from the ARPES measurements to be $n_{surface} = 4(1) \times 10^{12}\,\mathrm{cm}^{-2}$ (see Supplementary Note 1). A measurement of the electron mobility results in $\mu_{surface} \approx 500\,\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$, which is in agreement with previously reported values in $(Bi_{1-x}Sb_x)_2Te_3$ with $x \sim 0.5$ (refs 11,12). From the above values we estimate the surface channel conductivity to be $\sigma_{surface} = en_{surface}\mu_{surface} = 0.32(11)\,\mathrm{mS}\square^{-1}$, which is also in agreement with recent transport measurements[9]. Compared with the total conductance of the entire TI film, this results in an estimated amount of $\sigma_{surface}/\sigma_{4P} \simeq 73$ % of the total current through the TI film to be transmitted by the TSS channel at the sample surface. The remaining part of the current we expect to be transmitted by the TSS channel at the substrate interface along with possible bulk contributions[11,12,19].

Nanoscale transport measurements. In the following, we use scanning tunnelling potentiometry (STP) implemented into the four-tip STM, to determine the resistance of individual defects at the TI surface[20]. Hereby, a lateral current injected into the sample by two STM tips gives rise to a local current density *j* and results in a voltage drop across the sample. A third STM tip is then scanned across the sample surface and simultaneously records topography and potential maps. Details on the present STP method can be found in ref. 20, Supplementary Note 2 and Supplementary Fig. 2. Figure 2a shows the result of a STP measurement at the TI surface. The dominant contributions to

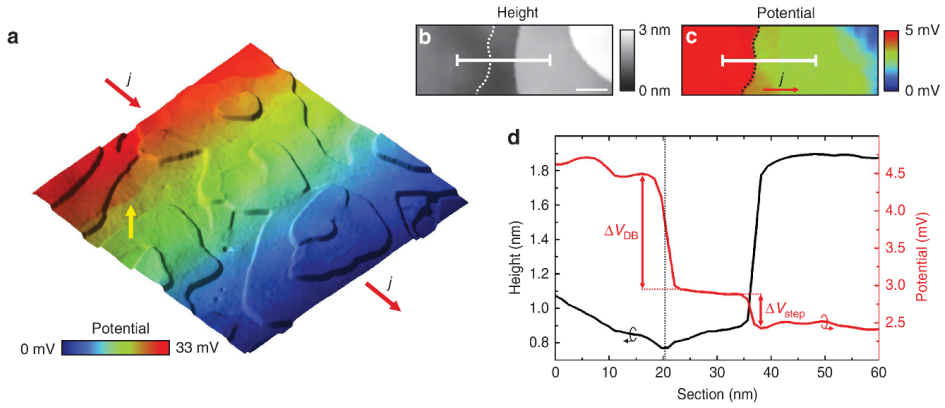

Figure 2 | Nanoscale transport measurements at the sample surface. (**a**) Overlay of topography as terrain and potential distribution as colour code. The current density j through the sample is indicated by the red arrows. The topography is dominated by QL steps while in the potential we observe an overall linear voltage slope on the terraces and additional voltage jumps located along lines at the sample surface, for example, the one highlighted by the yellow arrow. Scan size: 300 nm. (**b**) Topography showing two steps at the sample surface. The section indicated by the solid white line is shown in **d**. Scale bar, 20 nm. (**c**) Corresponding potential map with subtracted linear background. Sharp voltage drops are located at the position of topographic steps and along the dotted line which we explain as a domain boundary in the TI film. The corresponding potential section indicated by the solid white line is shown in **d**. (**d**) Black line graph: height profile from **b**. Red line graph: potential section from **c**. The voltage drops are $\Delta V_{step} = 0.46(5)$ mV at the step edge and $\Delta V_{DB} = 1.54(5)$ mV at the position of the domain boundary (indicated by the vertical dotted line).

the voltage drop are an overall linear voltage slope on the terraces and voltage jumps along lines at the sample surface. A more detailed topography scan is shown in Fig. 2b, centred at a QL step. Figure 2c shows the corresponding potential map from which we subtracted the average slope on the terraces to reveal the defect induced fine structure in the voltage drop[9,20]. We observe a voltage drop at the position of the QL step but also an even more pronounced voltage drop at the indicated dotted line. In the corresponding height profile in Fig. 2d, we observe a minimum in the topography at the position of the dotted line, while the QL step can be identified by its height of $\sim$1 nm. This finding at the position of the dotted line we explain to be due to a domain boundary between neighbouring domains of the TI film. The nucleation in islands, with two different rotational domains of the crystal structure[14], gives rise to in-plane stacking fault domain boundaries in the TI film upon coalescence of the islands[21]. In the corresponding potential section in Fig. 2d, the voltage drop located at the position of the domain boundary ΔV_{DB} is almost four times larger than that at the step edge ΔV_{step}, which equals to a significantly lower conductivity of the domain boundary in comparison to the QL step edge.

To determine the absolute value of the conductivity of the defects, we use the above estimate that a fraction of 73% of the total current is transmitted by the surface channel: $I_{surface} = 73\% \cdot I_{total} = 653(11)\,\mu$A with I_{total} being the current injected by the outer tips. For a distance between the current injecting tips of $d = 10(2)\,\mu$m, the local current density at the surface in the middle between the outer tips, where the potentiometry measurement is performed, is $j = 2I_{surface}/\pi d = 42(9)\,\mathrm{Am}^{-1}$ (refs 20,22). The resulting conductivity of the two above line defects then is $\sigma_{step} = j/\Delta V_{step} = 907(250)\,\mathrm{Scm}^{-1}$ and $\sigma_{DB} = j/\Delta V_{DB} = 272(60)\,\mathrm{Scm}^{-1}$. Although the conductivity of the step is in agreement with the literature[9], the much lower conductivity of a domain boundary was not reported to this point. We explain this finding by the vertical extension of the domain boundary into the TI film beyond the first QL[21], in contrast to the step that is located exclusively at the first QL. Owing to the vertical extension of the TSS into the film[10], the resulting scattering cross-section is larger for the domain boundary than for the step edge.

The terrace conductivity which we determine from the average voltage slope on the terraces E_0 is $\sigma_{terrace} = j/E_0 = 0.76(17)\,\mathrm{mS}\square^{-1}$. In total, we find that the line defects amount to 44% of the total observed surface channel resistance, in comparison with the voltage slope on the terraces, which contributes 56%. Hereby, the absolute voltage drops upon reversal of the lateral current are identical within the measurement errors (for further details, see Supplementary Note 3 and Supplementary Fig. 3). It is also noteworthy that possible bulk contributions to the transport would imply that defects have an even higher effect on pure TSS transport due to the resulting lower current density transmitted by the TSS.

Transport dipoles around void defects. Besides the above line defects, we further observe variations of the local electric potential in the form of resistivity dipoles around nanoscale voids at the sample surface. Resistivity dipoles result from a current flowing around a localized region of increased resistance[23,24]. Such an observation is of special interest in a TI due to the peculiar TSS properties, which prohibit 180° backscattering from such defects[4,5]. The topography of a typical void with a diameter of $\sim$5 nm on a terrace of the TI film is shown in Fig. 3a. Figure 3b shows the corresponding potential map, where the potential slope of the surrounding terrace has been subtracted. The dipole is found to be centred at the defect and its lobes are aligned with the overall orientation of the current.

This observation qualitatively agrees with the classical analytic description of resistivity dipoles in diffusive transport, where the amplitude of the dipole depends only on the diameter of the void and the electric field on the surrounding terrace[23]. However, the analytic description considers only circular defects and deviations in shape can have significant impact on the observed dipole amplitude. For a detailed analysis of resistivity dipoles around arbitrarily shaped defects, we therefore use a resistor network model[25,26], to analyse the potential distribution around the voids (for details, see Supplementary Note 4 and Supplementary Fig. 4).

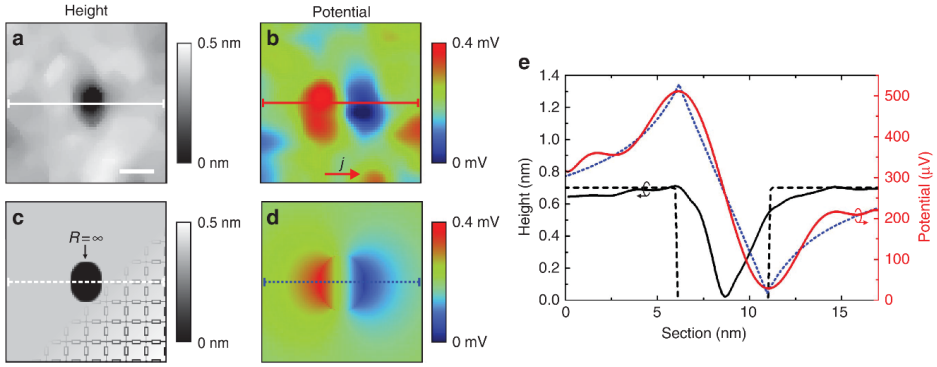

Figure 3 | Resistivity dipoles around nanoscale voids. (**a**) STM image of a typical void in the sample surface. Scale bar, 5 nm. (**b**) Corresponding potential map showing a dipole shaped feature centred at the defect. The lobes of the dipole are aligned with the macroscopic current direction. (**c**) Resistor network model mask with indicated schematic of the resistors. (**d**) Calculated potential distribution around the defect resulting from the resistor network model shown in **c**, after background subtraction. (**e**) Sections indicated in **a**–**d**. Solid black line: experimental height profile section from **a**. Solid red line: experimental potential section from **b**. Dashed black line: section of the model system shown in **c**. Dotted blue line: calculated potential section from **d**.

In this model too, only the dimensions of the void and the voltage slope on the terrace surrounding the defect, which is well defined in the experimental data, are parameters.

Figure 3c shows a plot of the resistor distribution mask corresponding to the experimentally observed defect geometry from Fig. 3a. Shown is a 80×80 nodal point excerpt from a total resistor network size of 200×200 nodal points. Hereby, the grey area corresponds to the conductivity of the surface channel, whereas black indicates an area of infinite resistance corresponding to a void in the sample surface. From this, the resulting potential distribution around the defect under static current flow is shown in Fig. 3d. For a comparison of theoretical and experimental results, Fig. 3e shows sections of the experimental (solid black line) and simulated (dashed black line) topography, and corresponding potential sections (red: experimental and blue dotted: simulated). In the experimental height profile, we find that the size of the void is smeared out laterally, which we attribute to the finite radius of the tunnelling tip. However, we observe larger voids to be 1 QL in depth, from which we conclude that the depth of the void shown in Fig. 3a is also 1 QL. The expected defect geometry is indicated by the dashed line. The section of the experimental potential map shows a pronounced dipole feature with a clear position of the dipole minimum and maximum. We find that the simulated potential distribution is in excellent agreement with the experimental data without any further parameters involved to fit the amplitude or shape of the defect. Furthermore, we conclude from the fact that we can explain the experimental data by means of a resistor network that we are in the diffusive transport regime[25,26]. In a next step, we will analyse the effect of voids on the overall resistance of the surface channel.

Calculation of the void defect resistance. In an infinitely wide conductor a single finite defect does not contribute to the resistance, because the relative area of increased resistance associated with the defect vanishes in comparison with the infinite conductor. Resistivity dipoles in this case can be described by the classical analytic description[23]. However, if a certain defect density is present, the conductor can be approximated by virtual parts (for example, squares for a two-dimensional conductor), each with a volume corresponding to the inverse of the defect density and with one defect residing in it (Fig. 4a). In each constrained virtual part of the conductor, the single finite defect then results in an increased resistance compared with the defect-free conductor. This can be made clear in a simplified model shown in Fig. 4b where the conductor is modelled by a small number of parallel resistors and the defect in the conductor corresponds to a resistor of infinite resistance. Here, a current j through the conductor has to be redistributed as it passed around the defect. At the position of the defect, this leads to a higher voltage drop due to the lower number of parallel resistors. The voltage drop amounts to $\Delta V = jR/2$ across the defect, whereas it is $\Delta V = jR/3$ elsewhere. The additional voltage drop caused by the defect results in a constant offset $\Delta V_{\mathrm{defect}}$ in comparison with the undisturbed system and can be detected far away from the actual position of the defect. The increase in resistance resulting from the defect is then $\Delta R_{\mathrm{defect}} = \Delta V_{\mathrm{defect}}/j$. For the present example, this means that a current of 1A passing through such a virtual domain with resistors of $R = 1\,\Omega$ will result in a total voltage drop across the system of 1 V in the defect free case. With the defect replacing one of the resistors, the same current results in a voltage drop of $\sim$1.17 V, which corresponds to an increase of the resistance due to the defect by 17%.

After introducing the effect of a defect on the resistance in the simplified, quasi one-dimensional model in Fig. 4b (no resistors in the vertical direction), we turn now to the full two-dimensional resistor network, which includes also resistors in the vertical direction as shown in Fig. 4c. This is the actual model we use to analyse the experimental data. Here, a void corresponds to a finite area with all resistors in this area having infinite resistance. Figure 4d shows the calculated potential resulting upon current flow through the model in Fig. 4c. A section through the centre of the dipole and parallel to the overall current direction is shown in Fig. 4e. Here, the minimum and maximum of the dipole feature are located at the boundary of the void (indicated as shaded area). Further away from the defect, the section approaches the indicated dashed lines corresponding to a persistent voltage drop of $\Delta V_{\mathrm{defect}}$. Figure 4f shows sections perpendicular to the overall current direction. Here we find a bell-shaped potential distribution with decaying amplitude as the distance from the defect increases. It can be shown from the current conservation that the average value of each curve in Fig. 4f is the same. As a result, $\Delta V_{\mathrm{defect}}$ is equal to the difference of the average voltage perpendicular to the overall current direction between any points along the x direction before and after passing the defect.

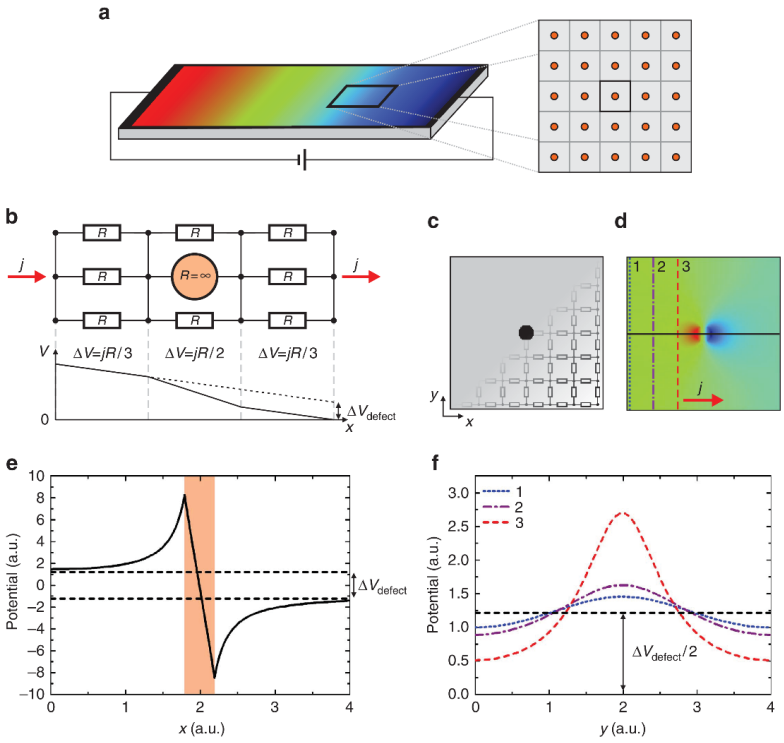

Figure 4 | Resistor network analysis of the void defects. (**a**) Schematic of a current carrying two-dimensional conductor. The conductor can be approximated by dividing it into virtual parts (squares) where each square corresponds to the inverse of the defect density in size and has one defect (orange circle) residing in it. (**b**) Simplified resistor network model of one virtual part of the conductor indicated in **a**. An incoming current j is initially transmitted by the three parallel resistors left from the defect. However, at the position of the defect the current has to flow via smaller number of parallel resistors (two) before it can flow again via three resistors after it passed the defect. The resulting potential distribution shows a higher local voltage drop ΔV located at the position of the defect. The result is a voltage offset $\Delta V_{\mathrm{defect}}$ compared with the voltage drop across a defect-free conductor, which results in a voltage drop corresponding to the dotted line. (**c**) Full resistor network model of a void in a conductor. Size: 200 × 200 pixel, with each pixel corresponding to a nodal point of the resistor network. (**d**) Background-subtracted potential distribution resulting from **c** upon current flow. (**e**) Section of the transport dipole along the solid black line in **d**. The position of the void is indicated by the shaded area. The persistent voltage drop $\Delta V_{\mathrm{defect}}$ after the current passed the defect is indicated by the dashed lines. (**f**) Sections perpendicular to the current along the lines labelled as 1, 2 and 3 in **d** and with the corresponding line styles. The amplitude of the lateral potential distribution decays with increasing distance to the defect. The constant black dashed line corresponds to the average value of each section and equals to $\Delta V_{\mathrm{defect}}/2$.

In the next step, we use the previous results to analyse the resistance arising from a density of voids at the TI surface corresponding to the experimentally found defect density and size. Therefore, we analyse a quadratic resistor network corresponding to one virtual domain of area $1/\rho$, where $\rho \approx 1/(150\,\mathrm{nm})^2$ is the experimentally observed defect density, with a single defect of diameter 5 nm in it. The resulting additional resistance associated with this defect density and size is $\Delta R_{\mathrm{defect}} = \frac{\Delta V_{\mathrm{defect}}}{j} = 2\,\Omega\square^{-1}$. In comparison, the experimental data results in $R_{\mathrm{terrace}} = \frac{1}{\sigma_{\mathrm{terrace}}} = 1315\,\Omega\square^{-1}$. This means that the experimentally observed void defect density and size results in an increase in the terrace resistance of only about 0.2% in comparison with the defect-free terrace.

Discussion

Because of the small effect of the observed defect density and sizes on the sample resistance, we are not able to resolve $\Delta V_{\mathrm{defect}}$ directly in the experiments. However, we show here that the knowledge of the geometrical arrangement of the defects (size and defect density) is sufficient to calculate their influence on the resistance of the conductor. The above described increase in resistance due to a certain defect distribution becomes larger for increasing defect sizes and higher defect densities such that we expect that in a suitable sample this effect can be directly observed in the experimental data. Furthermore, this means that the terrace conductivity, which contributes to 56% of the total resistance of the surface channel, is dominated by phonon scattering and scattering at defects, which are smaller than the defects we report here, such as atomic vacancies or anti-site defects[5,13]. Owing to the influence of scattering at such small defects being still below our resolution, we only measure their influence on a larger scale, which manifests as an increased overall resistance on the terraces.

Tip jumping artefacts[27,28] can be excluded from playing a role in our STP measurements. The voltage drop features at steps are precisely located at their topographic signature and in agreement with the literature[9]. At domain boundaries, there is no significant change in the sample topography that could lead to tip jumping. Concerning the voids, the relevant signature of the resistivity

dipoles is the decay of the dipole outside of the actual void, namely on the surrounding flat terrace where also no significant change in the sample topography is present, which could lead to tip jumping. The influence of thermovoltage between tip and sample in the present measurements is insignificant: by measurement at zero transverse current we find the largest thermovoltage signal to be located directly at step edges where it is below 50 μV in comparison with voltage drops of ∼mV resulting from the transport measurements.

In conclusion, we determined the resistance of several types of nanoscale defects at the surface of a $(Bi_{0.53}Sb_{0.47})_2Te_3$ thin film. We find that significant amounts of resistance are present at surface step edges and domain boundaries of the TI film, which result in a fundamental limit of the resistivity of the TI film and therefore need to be carefully controlled for future application in electronic devices. By evaluation of voids in the sample surface, we further present a generic method how quasi 0D defects such as atomic vacancies and anti-sites defects can be evaluated in future local transport measurements. A way to further increase the resolution of the transport measurements, possibly enabling to resolve potential maps around single-atomic defects, would be the measurement at low temperatures[20]. Local transport measurements at atomic defects, below the carrier mean free path, should also enable to clarify quantum mechanical contributions to the electrical surface state transport.

Methods

Sample preparation. Before the deposition by molecular beam epitaxy (MBE), a $10 \times 10\,mm^2$ Si(111) sample was cleaned by a RCA/hydrofluoric acid (HF) process to remove organic contaminations and the native oxide. The hydrofluoric acid passivates the Si surfaces with a hydrogen termination during the transfer into the MBE chamber (base pressure 1×10^{-10} mbar). In the MBE chamber, the sample was first heated to 700 °C for 10 min, to desorb the hydrogen termination from the Si surface and then cooled to 275 °C for the TI film growth. The Te deposition was started for several seconds before the Bi and Sb evaporators were opened simultaneously. Co-evaporation of Te, Bi and Sb from effusion cells took place at $T_{Sb} = 408$ °C, $T_{Bi} = 470$ °C and $T_{Te} = 330$ °C. After deposition, the sample was cooled to room temperature and transferred to the four-tip STM and ARPES under UHV conditions for which a movable UHV chamber was used. For all results compared in the manuscript, the exact same sample was used. After the STM/ARPES measurements, the sample was characterized *ex situ* by X-ray reflectivity and Rutherford backscattering, to determine the TI film thickness and the chemical composition. Further details can be found in ref. 14.

Angle-resolved photoemission spectroscopy. ARPES measurements took place at ∼30 K using a MBS A-1 hemispherical energy analyser, which was set to 40 meV energy resolution. We used monochromatic vacuum ultraviolet light with $h\nu = 8.4$ eV from a microwave-driven Xe discharge lamp and light with a photon energy of $h\nu = 21.2$ eV from a standard He discharge source.

Four-probe measurement. Four-probe measurements were performed at room temperature. To measure the macroscopic sample resistance, two of the four STM tips inject a lateral current through the TI layer, while the remaining two tips are used to measure the voltage drop at the surface resulting from the lateral current. Hereby, the tip positioning is monitored by a scanning electron microscope. Details on the home-built four-tip STM setup can be found in ref. 18. For all STM experiments, we used electrochemically etched tungsten tips.

Scanning tunnelling potentiometry. STP measurements were performed at room temperature. Hereby, a lateral current is injected into the sample using two STM tips, while the resulting voltage drop is mapped using a third tip in tunnelling contact. The technique was recently implemented into our four-tip STM as reported in ref. 20 and is based on the interrupted feedback technique. To map the sample topography and potential quasi-simultaneously, a software feedback loop alternatingly performs first topography and then potential measurement at each scan pixel. In detail, to measure the local sample potential, the tip is held at constant height while the tip voltage is adjusted by a feedback loop until the tunnelling current vanishes. At this voltage the electric potential of the tip is identical to that of the sample at the momentary scan position. The spatial and potential resolution are as low as Å and μV, respectively. Typical tunnelling parameters are $V_{tip} = -5$ mV, $I_t = 10$ pA. Further details on the potential measurement can be found in Supplementary Note 2 and Supplementary Fig. 2.

Resistor network calculations. The resistor network calculations solve Ohm's law $I = SV$ in the form of a linear equation system. Hereby, S is the matrix of conductivities in which the resistance of each resistor enters inversely, V is the vector of the voltage at each nodal point of the network and I is the vector with the sums of incoming an outgoing currents at each nodal point. The latter, after Kirchhoff's law, is zero at each nodal point, except at the boundaries where current is injected. In the data shown here, these are the two boundaries left and right of the network, whereas across the boundaries at the top and bottom no current is allowed to flow in our out of the system. To solve the linear equation system, S is inverted numerically $V = S^{-1}I$ such that V contains the electric potential at each nodal point corresponding to the voltage drop across the system.

Computer code availability. Computer code used within the manuscript and its Supplementary Information are available from the corresponding author upon reasonable request.

Data availability. Data within the manuscript and its Supplementary Information are available from the corresponding author upon reasonable request.

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Author contributions

F.L., M.E., T.H., M.I. and N.v.d.V. performed the experiments. F.L., V.C. and B.V. designed the STP experiment. M.E., T.H., L.P. and C.M.S. designed the photoemission experiment. M.I., P.S., D.R., N.v.d.V., G.M. and D.G. developed and fabricated the samples. The manuscript was written by F.L., M.E., T.H., M.L. and B.V. All authors discussed and commented on the manuscript.

Additional information

Supplementary Information accompanies this paper at http://www.nature.com/naturecommunications

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3.3 Electrical resistance of individual defects at a topological insulator surface – supplemental material

The following supplementary information has been published alongside the article *Electrical resistance of individual defects at a topological insulator surface* in the journal **Nature Communications**:

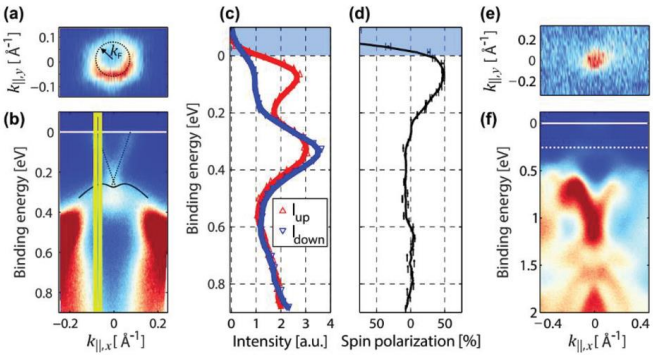
- **F. Lüpke**, M. Eschbach, T. Heider, M. Lanius, P. Schüffelgen, D. Rosenbach, N. von den Driesch, V. Cherepanov, G. Mussler, L. Plucinski, D. Grützmacher, C. M. Schneider and B. Voigtländer, Electrical resistance of individual defects at a topological insulator surface, *Nat. Commun.* 8, 15704 (2017)

Supplementary Note 1: Angle resolved photoemission spectroscopy

A cut in the $k_{\parallel,x}/k_{\parallel,y}$ plane at the Fermi energy and $h\nu = 8.4$ eV is shown in Supplementary Fig. 1 (a). We observe a small amount of warping of the Dirac cone and an average Fermi wave vector of $k_{\mathrm{F}} = 0.07(1) \cdot 10^{10}\ \mathrm{m}^{-1}$ which we determined by fitting a circle to the Fermi surface. Note: The asymmetry of the Fermi surface stems from the geometrical arrangement of the ARPES measurement setup. Hereby, the k_y direction is scanned by rotation of the sample with respect to the photon source. Due to the analyzer sitting in a fixed 45° angle with respect to the photon source, the resulting intensity in $-\mathrm{k}_y$ direction is higher than in $+\mathrm{k}_y$ direction. The corresponding dispersion in $k_{\parallel,x}$ is shown in Supplementary Fig. 1 (b). Supplementary Fig. 1 (c) shows spin-resolved energy distribution curves measured with a FeO-based spin detector (FERRUM, Focus GmbH) along the yellow box indicated in Supplementary Fig. 1 (b). The resulting in-plane spin polarization shown in Supplementary Fig. 1 (d) is as high as 50% in the Dirac cone indicating the topological nature of the surface state. Supplementary Fig. 1 (e) shows a cut in the $k_{\parallel,x}/k_{\parallel,y}$ plane at the Fermi energy measured at $h\nu = 21.2$ eV. At this photon energy, the relative intensity of the TSS is smaller while that of the bulk bands is higher in comparison to measurements at $h\nu = 8.4$ eV[1]. Here, we observe a small contribution from the bulk conduction band at the Fermi energy from which we conclude that the Fermi energy lies just at the conduction band edge. The corresponding dispersion in $k_{\parallel,x}$ is shown in Supplementary Fig. 1 (f) where the TSS is also not visible due to its low photoemission cross section. From this measurement, we extract the band gap to be 260(20) meV. The carrier concentration in the TSS can be determined from k_{F} after Supplementary Ref. [2]

$$n_{\mathrm{surf}}(E_{\mathrm{F}}) = \frac{k_{\mathrm{F}}^2}{4\pi} = \frac{(0.07(1) \cdot 10^{10}\ \mathrm{m}^{-1})^2}{4\pi} = 4(1) \cdot 10^{12}\ \mathrm{cm}^{-2}, \qquad (1)$$

where k_F is taken from the $k_{\parallel,x}/k_{\parallel,y}$ plane measurement in Supplementary Fig. 1 (a).

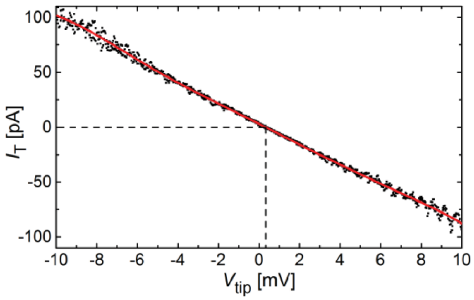


Supplementary Figure 1. Angle resolved photoemission spectroscopy. (a) Cut in the $k_{\parallel,x}/k_{\parallel,y}$ plane at the Fermi Energy ($h\nu = 8.4$ eV). (b) Corresponding dispersion in $k_{\parallel,x}$ direction with the Dirac cone indicated by dotted lines. (c) Spin-resolved energy distribution along the yellow box in (b). (d) Relative spin polarization resulting from (c). (e) Cut in the $k_{\parallel,x}/k_{\parallel,y}$ plane at the Fermi energy ($h\nu = 21.2$ eV). (f) Corresponding dispersion in $k_{\parallel,x}$ direction with valence band edge indicated by the dotted line.

Supplementary Note 2: Potentiometry voltage feedback

Shown in Supplementary Fig. 2 is the I/V curve of the tunneling tip around $V_{tip} = 0$ V where we find an almost linear dependence with finite slope. In this example, the stabilization parameters for the topography feedback were $V_{tip} = -10$ mV and $I_T = 100$ pA. During the potentiometry feedback, the tip is held at constant height above the sample surface and the tip voltage is adjusted, resulting in a change of the tunneling current corresponding to the shown I/V curve. The tip voltage is adjusted by the feedback loop until a current $I_T = 0$ A is reached such that the tip

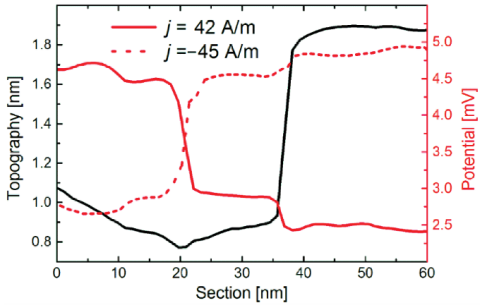
potential is the same as the underlying sample. More details on the method can be found in Supplementary Ref. [3].



Supplementary Figure 2. Current voltage characteristics of the tunneling tip. The I/V curve around $V_{\mathrm{tip}} = 0\,\mathrm{V}$ shows an almost linear slope across the voltage range. At $I_{\mathrm{T}} = 0\,\mathrm{A}$ a finite voltage is observed corresponding to the local sample potential under the tip.

Supplementary Note 3: Voltage drop upon reversal of the current direction.

Supplementary Fig. 3 shows a potentiometry section for reverse current directions resulting in the reverse voltage drop. We do not observe a dependence of the absolute voltage drops at steps, domain boundaries and across terraces on the current direction within the measurement errors.



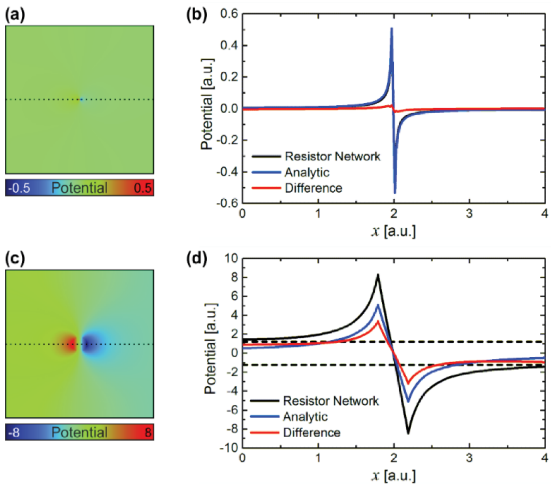
Supplementary Figure 3. Comparison of voltage drop for reverse current directions. The current densities are $j = 42(9)\,\mathrm{A\,m^{-1}}$ and $j = -45(9)\,\mathrm{A\,m^{-1}}$, respectively. Only small differences in the absolute voltage drops for both current directions are visible which we attribute to uncertainties within the measurement such as the exact position of the tips and small variations in the current density.

Supplementary Note 4: Resistor network calculations.

In order to validate the results from the resistor network calculations, we compare the two-dimensional analytic solution around a circular defect after Supplementary Ref. [4] to the results obtained from the resistor network calculations. Hereby, the resistor network should lead to the same result as the classical analytic description for a large enough system compared to the defect size and fine enough mesh of resistors.

For a small defect size compared to the system size (10 nm defect diameter compared to 1 µm system size with 200×200 nodal points) the potential distribution resulting from the resistor network is shown in Supplementary Fig. 4 (a). The corresponding analytic solution and resistor network voltage curves, shown in Supplementary Fig. 4 (b), almost coincide with only a notable difference of below 5% very close to the defect. We conclude that the analytic solution and resistor network give the same results for a large enough system and that the number of resistors in the

system is sufficient. On the other hand, Supplementary Fig. 4 (c) shows the potential distribution resulting from the resistor network for a larger defect (100 nm diameter compared to 1 µm system size again with 200 × 200 nodal points). In this case, a significant difference between the analytic solution and the resistor network curve is evident as shown in Supplementary Fig. 4 (d). Here, in the vicinity of the defect the difference of the two curves is about 40% of the dipole amplitude which is a direct result of the finite size of the resistor network which cannot be described by the analytic solution. In conclusion, large resistor networks, compared to the size of the defect, can be used to reproduce the results of the analytic solution while small resistor networks can be used to evaluate finite size effects. Furthermore, resistor networks can describe the potential distribution around arbitrarily shape defects, which makes them even more versatile concerning the analysis of experimental data.



Supplementary Figure 4. Resistor network calculations compared to analytic theory. (a) Potential distribution around a small defect resulting from the resistor network (linear background subtracted). (b) Plot of the section indicated in (a), analytic potential curve and difference between

resistor network and analytic curve. (c) Potential distribution around a larger defect in a resistor network of the same size as in (a) (linear background subtracted). (d) Plot of the section indicated in (c), analytic potential curve and difference between resistor network and analytic curve.

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Chapter 4 Disentangling *in situ* top and bottom surface state transport of a topological insulator ultra-thin film by gating

4.1 Introduction

Three-dimensional topological insulators (3D-TI), due to the unique electronic properties of their topological surface states (TSS), are prime candidates for application in future electronic devices [30, 31]. Among the most promising materials for applicability at room temperature due to their pronounced band gap of up to 300 meV are the compounds Bi_2Se_3, Bi_2Te_3 and Sb_2Te_3 [30, 32].

It has become clear though that the aforementioned binary materials often suffer from unintentional doping by crystal lattice defects such as vacancies and anti-site defects [30, 33, 34]. This doping can shift the Fermi energy into the bulk conduction/valence bands and result in highly conductive bulk transport channels, bypassing the auspicious TSS [35]. One way to reduce such bulk conductivity is to alloy different binary TIs into ternary or even quaternary compounds [35, 36, 37]. The underlying mechanism is the compensation of the unintentional defects which allows to shift the Fermi energy back into the bulk band gap [38]. However, the electronic bands on the surface of the TI are typically shifted with respect to the bulk due to surface band bending [24, 37]. This effect renders it difficult to achieve both, a low conducting bulk and a surface electronic configuration, where the Fermi energy only cuts the TSS, simultaneously. On the other hand, the use of thin films reduces the influence of bulk conduction and due to the large dielectric constant of TIs [39, 40, 41], can result in a large screening length in comparison to the film thickness, which means that the bands throughout such ultra-thin films are rather flat [42, 43]. The ternary compound $(Bi_{1-x}Sb_x)_2Te_3$ with $x \sim 0.5$ has proven to have low bulk conductivity while on its surface the Fermi energy is cutting only the TSS [22, 36, 44]. Furthermore, possible conduction channels at the substrate interface can be excluded [45], which makes $BiSbTe_3$ a promising candidate material for further application, as a lateral current through the sample is expected to be transmitted predominantly by the TSS.

The characterization of samples by transport measurements typically requires sample processing under ambient conditions, such as lithography to apply electric contacts prior to the measurements. However, the exposure of TI samples to air is reported to alter their electronic properties [24, 25, 46, 47, 48]. As a result, the comparison of *in situ* sample characterization, for instance by photoemission experiments, and subsequent *ex situ* transport measurements of the same sample needs to be taken with a grain of salt because the samples are altered in between the measurements. Recent *in situ* investigations [17, 32, 49, 50, 51, 52] overcome this general limitation by transport measurements, where the sample is under UHV conditions at all times allowing direct comparison of the different characterization methods.

Especially ultra-thin films close to the thickness limit of TIs (~5 QL), where the TSS at the top and bottom surface begin to overlap and hybridize [34, 53], are of particular interest for applications due to their strongly suppressed bulk conductance. In such ultra-thin films, the capacitive coupling of the TSS at the top and bottom surface via the TI film bulk, acting as a

dielectric, is reported to become significant when gating the TI film [39, 40, 41] and results in a simultaneous gating of the TSS on both surfaces with a single gate electrode. This finding is however in discrepancy with recent reports which have shown that the filling of the TSS changes only on one surface of the film upon application of a gate voltage, while on the other surface it remains unchanged [22, 44].

In the present work we use a combination of the *in situ* surface analysis tools, angle resolved photoemission spectroscopy (ARPES) and four-tip scanning tunneling microscopy (STM), for the analysis of pristine $BiSbTe_3$ ultra-thin films. We interpret gate-dependent four-probe measurements by use of a generic multi-channel transport model which allows us to disentangle the conduction through the TSS on the top and bottom surface and evaluate the amount of bulk conduction in the TI film. The model further gives access to the carrier concentrations and carrier mobility in each of the transport channels and a generic explanation for the different findings reported in literature. The sample used in this chapter is the same as in chapter 3 of this thesis.

4.2 Sample preparation

We prepared a $d = 10.5(5)$ nm films of $(Bi_{0.53}Sb_{0.47})_2Te_3$ on a silicon-on-insulator (SOI) wafer by means of molecular beam epitaxy (MBE). Contacting the TI thin film with the tips of a four-tip STM results in the sample geometry shown in Fig. 4.1, resembling an *in situ* realization of a TI field-effect transistor. The Si(111) SOI substrate hereby consists of a 70 nm thick Si(111) device-layer on top of a 300 nm thick buried oxide layer which is comprised of amorphous SiO_2, whereas 700 µm of Si(001) act as the handle wafer.

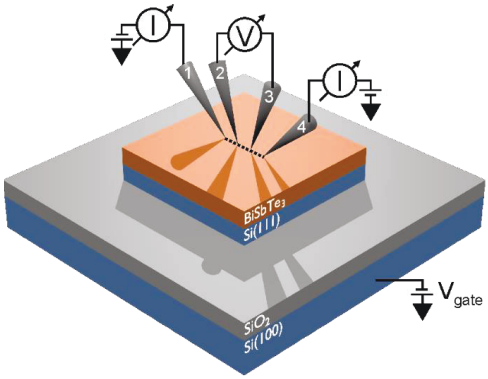

Figure 4.1. Schematic of the transport measurement setup. A $BiSbTe_3$ ultra-thin film is grown on a silicon-on-insulator substrate. The tips of a four-tip STM contact the TI thin film for transport measurements while the gate voltage V_{gate} is applied to the back side of the substrate.

In order to perform *in situ* gate-dependent transport measurements, due to the design of the sample holder, a pre-structuring of the sample substrate was required in order to be able to control the electric potential of the Si(001) handle wafer and TI film separately. The corresponding mesa structure was transferred to the SOI substrate by employing photolithography and reactive ion etching (RIE) prior to the growth. AZ5214 was used as

photoresist and the etching was performed by applying a standard SF_6-process to remove the 70nm thick silicon layer on top of the SiO_2. The resulting square Si(111) mesa structure ($5 \times 5\ mm^2$) is located in the center of the $10 \times 10\ mm^2$ SOI substrate and provides a suitable substrate for selective area growth. The substrate pre-structuring procedure is shown in Fig. 4.2 (a)-(d) and is followed by the TI film growth (Fig. 4.2 (e)), with the details of the growth procedure described in the following.

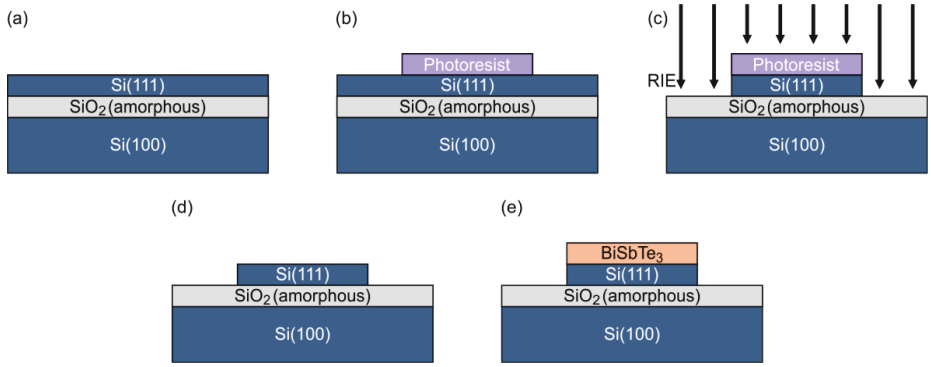

Figure 4.2. Preparation of the sample substrates (a) Silicon-on-insulator (SOI) wafer before patterning. The thickness of the individual layers are Si(111) – 70 nm, SiO_2 – 300 nm, Si(100) – 700 µm. (b) Resist mask after photolithography. (c) Reactive ion etching to remove Si(111) layer. (d) The mesa structure as it is introduced into the MBE system. (e) Selective-area growth of $BiSbTe_3$ on the remaining Si(111) mesa.

In a first step, the pre-structured substrate was cleaned using a RCA/HF procedure in order to remove contaminations and the oxide from the sample surface. As a result, the Si(111) surface is H-terminated when the sample is introduced into the MBE chamber ($p \leq 1 \cdot 10^{-10}$ mbar). The sample was then heated to 700°C for 10 min to desorb the hydrogen before it was cooled to 275°C for the TI growth. First, the sample was flushed with Te for several seconds, before the Bi ($T_{\mathrm{Bi}} = 470$ °C) and Sb ($T_{\mathrm{Sb}} = 408$ °C) evaporators were opened simultaneously. After the deposition, the samples were cooled to room temperature and transferred to the 4-tip STM/ARPES under UHV conditions. The resulting angle-resolved photoemission spectra are shown in chapter 3.3 of this thesis.

4.3 Transport measurements

For the transport measurements, we use a home-built room temperature four-tip STM [23] which allows individual positioning of the tips under scanning electron microscope monitoring. Due to the floating potential of the TI film, which denies regular contacting with the STM tip for transport measurements, we used a special tip-approaching technique. Hereby, we apply an AC voltage to the handle wafer which is readily contacted when the sample is mounted into the STM. Due to the capacitive coupling between the handle wafer, forming the back gate, and the device layer with the TI film grown on top, the electric potential of the device layer oscillates as a result of the AC voltage.

In order to safely approach the tips, the AC voltage frequency needs to be in a suitable range to be detected by the current amplifiers connected to the STM tips, below 1 kHz for the present current amplifiers (DLPCA-200). Furthermore, the AC amplitude has to be in a range such that the increase in current due to engagement of the tunneling contact with the tips results in a suitable auto-approach cancelling criterion. Useful parameters for the present STM and sample setup were $f = 500$ Hz and a peak to peak voltage amplitude $V_p = 200$ mV. After safely approaching all four tips to the sample surface in this way, the AC voltage is disconnected we perform four-probe measurements with Fig. 4.3 (a) showing a four-probe I/V of the TI film at $V_{\mathrm{gate}} = 0$ V. Here, we find a linear current voltage characteristic, indicating ohmic contacts between the tips and the TI film. The four-probe resistance resulting from a linear fit to the measurement is $R_{4\mathrm{P}} = 500(1)\ \Omega$ which corresponds to a sheet conductivity of $\sigma_{\mathrm{total}} = \ln(2)\,/\pi R_{4\mathrm{P}} = 0.44(5)$ mS $\square^{-1}$, including the positioning errors of the tips [54]. The two-dimensional character of the conductivity of the sample we confirmed by additional four-probe measurements at different tip spacing which result in a constant four-probe resistivity (not shown). The inset in Fig. 4.3 (a) shows a scanning electron microscopy image of the four tips contacting the sample surface with a mutual tip distance $s = 100(5)$ µm.

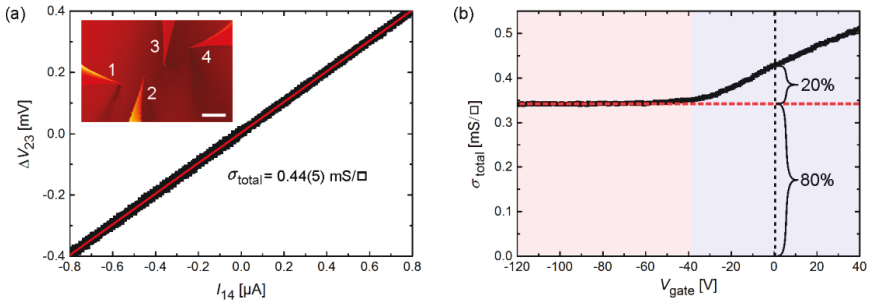

Figure 4.3. Gate dependent four-probe measurements. (a) Experimental four-probe I/V measurement of the TI film at $V_{\mathrm{gate}} = 0$ V (black dots) and linear fit (red line) resulting in a sheet conductivity of $\sigma_{\mathrm{total}} = 0.44(5)$ mS/□. Inset: Scanning electron microscopy image of the four-probe setup. Scale bar: 100 µm. (b) Experimental gate dependent TI film sheet conductivity σ_{total} (black points) and linear guide to the eye (red dashed line). The two gating regimes are indicated as shaded areas left and right of $V_{\mathrm{gate}} = -38$ V. The amount of conductivity at $V_{\mathrm{gate}} = 0$ V distributes to 80% below the red dashed line and 20% above.

In the next step, we determine the TI film conductivity as a function of the gate voltage as shown in Fig. 4.3 (b). In this graph, we find two distinctly different gating regimes: For gate voltages larger than $V_{\mathrm{gate}} = -38$ V we find an almost linear increase in the TI sheet conductivity, while for gate voltages below $V_{\mathrm{gate}} = -60$ V we find that the conductivity forms a plateau at $\sigma_{\mathrm{total}} = 0.34(1)$ mS $\square^{-1}$. Hereby, the voltage applied between the outer current injecting tips ΔV_{14} is a few mV such that in general $\Delta V_{14} \ll V_{\mathrm{gate}}$. In order to analyze this gate-dependent transport behavior, we employ in the following a multi-channel transport model.

4.4 Transport Model

The conduction in a TI thin film is described in general by three parallel conduction channels – one channel for the TSS on each side of the film and one channel resembling the interior (bulk) of the film (in the following referred to as 'film bulk'). To disentangle these parallel conduction channels is typically a difficult task because transport measurements in general measure the superposition of all parallel channels σ_{total} such that information about the individual channels can only be extracted from their different response to an external stimulation, e.g. by a magnetic field, or as in the present case, an electric field. The analysis of the resulting dependence of σ_{total} on the external electric field requires a suitable transport model to conclude about the properties of the individual channels.

Here, we will use in a first step a simple two channel transport model, where we assume only gating of the TSS closest to the back gate in order to get a basic understanding of the present system. Subsequently, we perform a more detailed analysis in form of a three channel transport model where we consider the gating throughout the film in a detailed model, including the capacitive coupling of the TSS on the top and bottom of the film.

The sample conductivity is measured by means of a four-probe measurement with a tip spacing of 50 µm for which we used a home-built four-tip STM at room temperature. Two of the four STM tips inject a lateral current through the conductive TI layer while the remaining two tips are used to measure the voltage drop across the surface resulting from the current. The resulting four-point conductivity is an average conductivity of the sample surface in the region of measurement. Positioning of the electro-chemically etched tungsten tips is monitored by an SEM.

4.4.1 Two channel model

In the two channel model, we assume that only the TSS closest to the gate electrode is affected by the application of a gate voltage, while the conductivity of the other channel remains constant, as also found in the literature [44, 55]. In the present sample geometry, the channel influenced by the gate is the TSS channel at the bottom of the film with a corresponding conductivity σ_{bot}, while the conductivity of the constant channel $\sigma_{\mathrm{background}}$ is a superposition of TI film bulk conductivity σ_{film} and the top TSS channel conductivity σ_{top}. The resulting total conductivity is $\sigma_{\mathrm{total}} = \sigma_{\mathrm{bot}} + \sigma_{\mathrm{background}}$, where we determine $\sigma_{\mathrm{background}} = \sigma_{\mathrm{film}} + \sigma_{\mathrm{top}} = 0.34\ \mathrm{mS}\,\square^{-1}$ directly from the plateau in the conductivity in the experimental data below $V_{\mathrm{gate}} = -60\ \mathrm{V}$.

The bottom channel at zero gate voltage has a conductivity $\sigma_{\mathrm{bot}}\left(V_{\mathrm{gate}} = 0\ \mathrm{V}\right) = \sigma_{\mathrm{bot}}^{0}$ as a result of a carrier concentration n_{bot}^{0}. The additional gate induced charge carriers in the bottom channel n_{bot} are determined by a plate capacitor model with the gate induced charge carrier concentration

$$n_{\mathrm{gate}} = \frac{C_{\mathrm{gate}} V_{\mathrm{gate}}}{e}. \tag{4.1}$$

Hereby, the gate capacitance C_{gate} we calculate from the sample geometry after

$$C_{\text{gate}} = \left(\left(\frac{3.9\varepsilon_0}{300\ \text{nm}} \right)^{-1} + \left(\frac{11.7\varepsilon_0}{70\ \text{nm}} \right)^{-1} \right)^{-1} = 11\ \text{nF/cm}^2.$$

The resulting conductivity of the bottom channel, after Drude, is $\sigma_{\text{bot}} = \mu_{\text{bot}}\left(en^0_{\text{bot}} + C_{\text{gate}}V_{\text{gate}}\right)$. Hereby, μ_{bot} is the mobility of charge carriers in the bottom channel. Fitting eq. (4.1) to the experimentally observed increase of the conductivity $\sigma_{\text{bot}}(V_{\text{gate}})$ via $n_{\text{bot}} = n_{\text{gate}}$ around zero gate voltage results in $\mu_{\text{bot}} = 210\ \text{cm}^2/\text{Vs}$ and $n^0_{\text{bot}} = 2.5 \cdot 10^{12}\ \text{cm}^{-2}$. The corresponding charge carriers are electrons as a result of the positive slope of the graph.

From the fit, it results that at a gate voltage of $V_{\text{gate}} = -38\ \text{V}$ the charge carrier density in the bottom TSS in minimized. We interpret this voltage to be the point where the Fermi energy in the bottom channel is located at the Dirac point of the TSS. Further gating of the bottom channel below $V_{\text{gate}} = -38\ \text{V}$ results in the generation of holes in the bottom channel. While it has been reported that Dirac holes have approximately the same mobility as the corresponding Dirac electrons [37], we find from ARPES that the Dirac point is located directly at the valence band edge and due to the large number of available states in the valence band, the generated holes are predominantly of bulk character such that we cannot address Dirac holes in the present transport experiments.

From the experimentally observed plateau in the total TI film conductivity we can only estimate the mobility of the generated holes in the bottom channel below $V_{\text{gate}} = -38\ \text{V}$ to be $< 2\ \text{cm}^2/\text{Vs}$, which is lower than the corresponding TSS mobility by two orders of magnitude. While the mobility of bulk holes in $BiSbTe_3$ was reported earlier to be one order of magnitude lower than the corresponding TSS mobility [55] we explain the finding by the bulk mobility in the present measurements to be further decreased due to the phonon scattering at room temperature.

Owing to this low bulk carrier mobility, in combination with typical carrier concentrations $\sim 10^{13}\ \text{cm}^{-2}$ in similar films [44], results in a low conductivity of the interior of the TI film, as we also show in the following. We conclude that $\sigma_{\text{background}}$ is dominated by the conductivity of the top TSS. As a result, at $V_{\text{gate}} = 0\ \text{V}$ the fraction of the total current transmitted by the top TSS we find to be $\sigma_{\text{background}}/\sigma_{\text{total}} \approx 80\%$, as indicated in Fig. 4.3 (b). In combination with the carrier concentration in the top TSS n^0_{t}, obtained from ARPES, the mobility of the top TSS can be determined to be $\mu_{\text{top}} = \sigma_{\text{background}}/(n^0_{\text{t}}e) = 534\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$, which is in good agreement with literature values [22, 56].

Although the above simple two channel model already gives a conclusive result of the TI properties of the present sample, in agreement with earlier literature reports [22, 44], it has to be taken with a grain of salt, because this model has several limitations. On the one hand, in the ultra-thin film limit the capacitive coupling between top and bottom TSS can generally not be neglected [39, 40, 41]. On the other hand, the TI bulk can in principle contribute significantly to the conduction, especially at room temperature [57] such that it has to be analyzed in general with more detail.

We therefore introduce in the following a more general gating and transport model which includes the capacitive coupling of the TSS at the top and bottom surface of the thin film.

Furthermore, this refined transport model includes a separate conduction channel for the film bulk for which we perform band bending calculations in order to get a better understanding of the band configuration throughout the film.

4.4.2 Three channel model

In the three channel transport model, the total TI sheet conductivity is given by $\sigma_{\mathrm{total}} = \sigma_{\mathrm{top}} + \sigma_{\mathrm{bot}} + \sigma_{\mathrm{film}}$. No longer assuming that the gate affects only the bottom TSS channel and inclusion of the capacitive coupling between the TSS at the top and the bottom results in a gate dependent carrier concentration in the top TSS channel and furthermore in the film bulk. The total film conductivity results as

$$\sigma_{\mathrm{total}}(V_{\mathrm{gate}}) = \left(n^0_{\mathrm{top}} + n_{\mathrm{top}}(V_{\mathrm{gate}})\right) e\mu_{\mathrm{top}} + \left(n^0_{\mathrm{bot}} + n_{\mathrm{bot}}(V_{\mathrm{gate}})\right) e\mu_{\mathrm{bot}} + \sigma_{\mathrm{film}}(V_{\mathrm{gate}}), \tag{4.2}$$

where μ_{top} (μ_{bot}) is the mobility of charge carriers, n^0_{top} (n^0_{bot}) is the initial carrier concentration in the top (bottom) TSS channel without gating, and n_{top} (n_{bot}) is the corresponding gate induced charge carrier concentration.

The initial carrier concentrations n^0_{top} and n^0_{bot} are *a priori* unknown. For an ideal topological insulator, the position of the Fermi level relative to the Dirac point and therefore charge carrier concentration in both top and bottom TSS channel, should be identical. However, it has become clear that this is typically not the case in experiments [22, 56], due to the different environments the top and bottom TSS are exposed to and which result in different amounts of unintentional doping on either surface. Hereby, the TSS channel at the interface to the substrate is expected to be more pristine than that at the top of the TI film due to the susceptibility of surface adsorbates and evaporation of material there.

Here, again the ARPES measurement determines n^0_{top} which decreases the number of free parameters in eq. (4.2) when fitting it to the experimental data. In contrast, n^0_{bot} is difficult to access experimentally and is typically determined from theoretical models. The same applies for the gate induced charge carrier concentrations n_{top} and n_{bot}.

4.4.3 Quantum capacitance

Quantum capacitance effects occurs in capacitors when at least one of the capacitor plates, e.g. in a parallel-plate capacitor with corresponding geometric capacitance

$$C_{\mathrm{geom}} = \varepsilon/d,$$

has a low density of states ρ. Hereby, ε is the dielectric constant of the material between the plates and d is the plate distance. This case is observed e.g. in field effect transistors, where a gate voltage V_{gate} is used to control the charge concentration in the channel of the device. As a result of the low density of states, the application of a voltage V_{gate} to the device leads not to the typical charging behavior $Q = C_{\mathrm{geom}} V_{\mathrm{gate}}$, but the amount of induced charges is attenuated. The reason is that due to the low density of states, the induced charge carriers need to be lifted into higher energy levels, for which additional energy is required. This correction to the

geometric capacitance corresponds to another capacitor connected in series, which due to the quantum mechanical nature of the density of states is called the quantum capacitance.

In general, moving a number of electrons N, corresponding to a charge $Q = Ne$, from one plate of a capacitor to the other corresponds to a change in the electric potential in the capacitor of $\Delta V = Q/C_{\mathrm{geom}}$ corresponding to the typical behavior one expects without quantum capacitance effects. However, due to the limited amount of states available in one of the plates, the filling level of the plate has to change from its initial configuration (Fig. 4.4 (a)) to

$$N = \rho \times e\Delta V_{\mathrm{qc}}$$
$$\Leftrightarrow\ \Delta V_{\mathrm{qc}} = Q/\rho e^2$$

as is depicted in Fig. 4.4 (b).

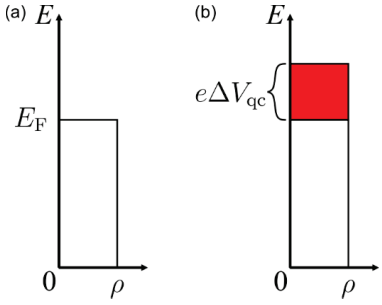

Figure 4.4. Origin of the quantum capacitance. (a) Schematic of the filling level of a capacitor plate made of a material with a constant low density of states ρ, filled up to the Fermi energy E_{F}. (b) Introducing an additional amount of charge carriers into the system results in an increase in the filling level by an amount $e\Delta V_{\mathrm{qc}}$, corresponding to $N = \rho \times e\Delta V_{\mathrm{qc}}$. The voltage required to lift the charge carriers to higher energies $\Delta V_{\mathrm{qc}} = Q/\rho e^2$ results in a lower capacitance of the system.

This filling of higher energy levels results total in a voltage change across the capacitor as

$$V_{\mathrm{gate}} = \Delta V_{\mathrm{geom}} + \Delta V_{\mathrm{qc}} = \frac{Q}{C_{\mathrm{geom}}} + \frac{Q}{\rho e^2} = \frac{Q}{C_{\mathrm{geom}}} + \frac{Q}{C_{\mathrm{qc}}}.$$

This expression corresponds to a series circuit of two capacitances, C_{geom} and C_{qc}, and results in a lower capacitance in comparison to C_{geom} without the quantum capacitance effects. For $\rho \to \infty$ the system approaches the classical model dominated by C_{geom}. The corresponding equivalent circuit diagram is depicted in Fig. 4.5.

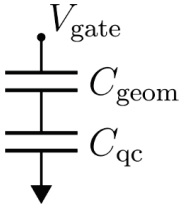

Figure 4.5. Equivalent circuit diagram of a capacitor including quantum capacitance effects. The amount of charge carriers induced in the system by the voltage V_{gate} is reduced by

the quantum capacitance C_{qc} in comparison to the case when the capacitance is given only by C_{geom}.

When investigating gate-dependent transport properties of samples with only one transport channel, this circuit diagram can be directly used to determine the gate-dependent charge carrier concentrations in the channel [58]. However, topological insulator thin films are a sample system where two parallel transport channels can both be subject to quantum capacitance effects resulting from a single gate electrode, such that the analysis of gate-dependent carrier concentrations in the individual transport channels becomes a more complex task. In the following, we therefore deduce the corresponding equivalent circuit diagram from a basic parallel-plate capacitor, in order to give a fundamental understanding of the system.

In a simple parallel plate capacitor with metallic plates having high ρ, as shown in Fig. 4.6 (a), a negative voltage applied to the bottom plate via the gate contact results in the polarization of the dielectric ε between the capacitor plates and induces the same amount of positive and negative charge on the top and bottom capacitor plates, respectively. The resulting polarity of the induced charges on the respective capacitor plates is indicated by '+' and '-'. The capacitance for the shown geometry calculates after the geometric capacitance $C_{\mathrm{geom}} = \varepsilon/d$.

With an additional metal plate inserted in the parallel-plate capacitor, as shown in Fig. 4.6 (b), and the distance between the capacitor plates increased corresponding to the thickness of the metal plate in order to compensate its effect on the geometrical capacitance, results in the same capacitance as in Fig. 4.6 (a). The explanation is that as a result of the electric field charges are accumulated at the surface of the intermediate plate which counteract the electric field in the capacitor plate such that it vanishes inside of the metal. Hereby, the intermediate plate does not acquire a net charge.

In contrast to this behavior, when the intermediate metal plate is connected to ground, a net positive charge is induced on the bottom side of the intermediate plate corresponding to the charge on the bottom capacitor plate (Fig. 4.6 (c)). As a result, the electric field above the bottom of the intermediate plate is fully screened, such that no charges are induced in the top capacitor plate. The resulting capacitance between the bottom capacitor plate and the intermediate metal plate is double the value as in the previous models (Fig. 4.6 (a) and (b)).

When the intermediate plate is conducting but with low ρ and is connected to ground via the corresponding quantum capacitance C_{bq} (Fig. 4.6 (d)), the electric field between the top and bottom capacitor plates is only partially screened, resulting in a net positive charge of the intermediate plate, however lower than the case depicted in Fig. 4.6 (c). In detail, the exact amount of net charges on the capacitor plates and intermediate metal plate depends on the capacitances of the individual capacitors and can be calculated via the respective equivalent circuit diagram. In the limit of $C_{\mathrm{bq}} \gg C_{\mathrm{geom}}$ the behavior approaches the case as if the metal plate is directly connected to ground, corresponding to Fig. 4.6 (c), while for C_{bq} vanishing, the behavior is as if there was no connection of the intermediate plate to ground as in the case depicted in Fig. 4.6 (b).

Figure 4.6 (e) shows the schematic which includes quantum capacitance effects of the intermediate metal plate, C_{bq}, as well as the top plate C_{tq}, which further reduces the amount of charge carriers induced in the top plate as function of the gate voltage in comparison to the previous geometry. This schematic corresponds to the experimental setup of the gated TI thin

film and results in the equivalent circuit diagram shown in Fig. 4.7 (a). Hereby, the two dielectrics, above and below the intermediate plate, correspond to the gate dielectric C_{gate} and TI film bulk C_{TI}, respectively. Note that in the corresponding experimental realization the intermediate plate is practically infinitesimally thin, resulting in its top surface, bottom surface and top plate of C_{bq} in Fig. 4.6 (e) to practically coincide spatially. Nevertheless, the corresponding equivalent circuit diagram is still valid.

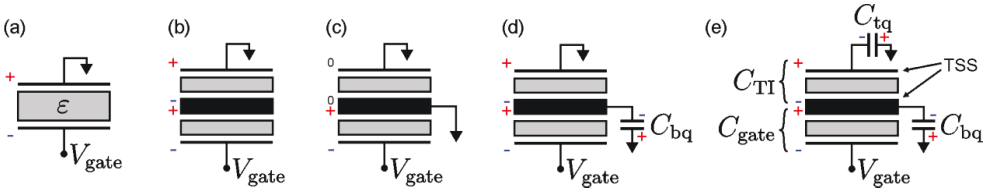

Figure 4.6. Schematic of a parallel plate capacitor with different electric connections. (a) Typical parallel plate capacitor with metallic plates and a negative voltage V_{gate} applied to the bottom plate and a dielectric indicated by ε. The resulting polarity of induced charges is indicated as '+' and '-', respectively. (b) Parallel-plate capacitor with an intermediate metal plate, which has no electrical connections. The dielectric is separated into two parts of equal size. (c) The same capacitor as in (b) but with the intermediate plate connected to ground. (d) Same as in (c), but the intermediate plate is connected to ground via a capacitance C_{bq}. (e) The same setup as in (d) but with the top capacitor plate connected to ground via an additional capacitance C_{tq}.

According to the equivalent circuit diagram in Fig. 4.7 (a), it follows

$$V_{\mathrm{gate}} = Q\left[\frac{1}{C_{\mathrm{gate}}} + \frac{1}{C_{\mathrm{bq}} + \left(\frac{1}{C_{\mathrm{tq}}} + \frac{1}{C_{\mathrm{TI}}}\right)^{-1}}\right].$$

In the sample investigated in this thesis $C_{\mathrm{gate}} = 11\ \mathrm{nF/cm^2}$ which is much smaller than C_{bq}, C_{tq} and C_{TI}, which are typically on the order of $\mu\mathrm{F/cm^2}$ as shown in the following. As a result, the amount of charges induced in the system is given by

$$Q \simeq V_{\mathrm{gate}} C_{\mathrm{gate}}.$$

On the other hand, the distribution of these charges into the top and bottom channel, respectively, is given by the ratio

$$\frac{Q_{\mathrm{bq}}}{Q_{\mathrm{tq}}} = \frac{C_{\mathrm{bq}}}{\left(\frac{1}{C_{\mathrm{tq}}} + \frac{1}{C_{\mathrm{TI}}}\right)^{-1}} = C_{\mathrm{bq}}\left(\frac{1}{C_{\mathrm{tq}}} + \frac{1}{C_{\mathrm{TI}}}\right).$$

It follows, that when the TI film is very thin ($C_{\mathrm{TI}} \to \infty$) and the filling level of the top and bottom channel are the same ($n_{\mathrm{tq}} = n_{\mathrm{bq}} \Leftrightarrow C_{\mathrm{tq}} = C_{\mathrm{bq}}$) that $Q_{\mathrm{bq}} = Q_{\mathrm{tq}}$, which means that both channels are influenced by V_{gate} in the same way. On the other hand, if ($C_{\mathrm{TI}} \to 0$), as the case for a very thick film, only the channel closest to the gate electrode is affected by V_{gate}. This behavior is consistent with our previous considerations.

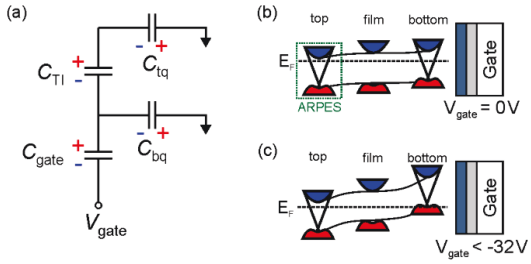

Figure 4.7. Gating model and band schematics of the TI film. (a) Equivalent circuit diagram of the sample geometry including the quantum capacitances C_{tq} and C_{bq}. (b) Band schematic in the TI film at $V_{\mathrm{gate}} = 0$ V. The film conduction band and valence band are indicated in blue and red, respectively. The relative position of the bands with respect to the Fermi energy in the top channel is known from ARPES. (c) Band schematic of the TI film under negative gate voltage $V_{\mathrm{gate}} \leq -32$ V. In this case, the Fermi energy at the bottom TSS is pinned at the edge of the film valence band.

In the simple two channel model, we assumed that all gate induced charge carriers are induced in the bottom TSS. However, for the TSS generally the effect of quantum capacitance has to be taken into account. The quantum capacitance manifests as an additional energy required to introduce more charge carriers into a capacitor due to a small density of states on one or both of the capacitor plates. As a result, the gate effect and thereby the number of charge carriers induced in such a capacitor is attenuated [59]. In the corresponding equivalent circuit diagram this effect can be described by an additional capacitance C_{Q} in series to the gate electrode [59]. Due to a generally small density of states in the TSS, especially close to the Dirac point, the quantum capacitance can have a large effect in gating of such devices. The quantum capacitance further results in the electric field of the gate to be not perfectly screened by the TSS closest to the gate [59]. A result of the penetrating electric filed to the TSS further away from the gate is the capacitive coupling of the two TSS at the top and bottom of the TI film, where the TI film bulk acts as a dielectric which mediates the coupling of the two surface states. This capacitive coupling becomes large for thin films and depends on the dielectric constant of the TI bulk, which typically is on the order of $\varepsilon_{\mathrm{TI}} = 100\varepsilon_0$ [39], for the present sample resulting in $C_{\mathrm{TI}} = \frac{\varepsilon_{\mathrm{TI}}}{d} \approx 8\,\frac{\mu\mathrm{F}}{\mathrm{cm}^2}$ after Ref. [40].

The resulting equivalent circuit diagram including the quantum capacitance for each of the surface channels C_{bq} and C_{tq}, the coupling capacitance via the TI film bulk C_{TI} and the coupling of the gate electrode via C_{gate} is shown in Fig. 4.7 (a) (after Ref. [39, 40, 41]). This equivalent circuit model results in the following set of equations describing the gate induced carrier concentrations in the top and bottom TSS channel [39, 40, 41]:

$$n_{\mathrm{bot}} = -n_{\mathrm{gate}} - n_{\mathrm{TI}}$$
$$n_{\mathrm{top}} = n_{\mathrm{TI}} \tag{4.3}$$

with

$$n_{\mathrm{gate}} = \frac{C_{\mathrm{gate}}\left(eV_{\mathrm{gate}} - \Delta E_{\mathrm{bot}}\right)}{e^2}$$
$$n_{\mathrm{TI}} = \frac{C_{\mathrm{TI}}\left(\Delta E_{\mathrm{top}} - \Delta E_{\mathrm{bot}}\right)}{e^2} \tag{4.4}$$

and

$$\Delta E_{\mathrm{bot}} = -e^2 n_{\mathrm{bot}}/C_{\mathrm{bq}}$$
$$\Delta E_{\mathrm{top}} = -e^2 n_{\mathrm{top}}/C_{\mathrm{tq}} \tag{4.5}$$

The quantum capacitances however generally are a function of the carrier concentrations themselves $C_{\mathrm{tq}}(n_{\mathrm{top}})$ and $C_{\mathrm{BQ}}(n_{\mathrm{bot}})$. A rigorous analysis of the effect of gating on the system therefore requires a more detailed description. For the case of the linear dispersion of the TSS, the charge carrier density in the TSS is well defined as a function of the energy level with respect to the Dirac point [33]

$$E_{\mathrm{top}} = \sqrt{n_{\mathrm{top}} 4\pi\hbar^2 v_{\mathrm{F}}^2} \equiv a\sqrt{n_{\mathrm{top}}}, \tag{4.6}$$

and in the same way $E_{\mathrm{bot}} = a\sqrt{n_{\mathrm{bot}}}$. The general formulation of the quantum capacitance is [39] $C_{\mathrm{Q}} = e^2 n/E$, which result with eq. (4.6) in $C_{\mathrm{tq}} = \frac{e^2\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}}}{a}$ under the presence of initial charge carriers n_{top}^0 prior to gating and accordingly for C_{bq}. This formulation of the quantum capacitance is consistent with eq. (4.5) and (4.6). Note that for the case of the Dirac cone this expression differs by a factor of two from the approximation of the quantum capacitance $C_Q \approx e^2 \frac{\partial n}{\partial E}$, which is also commonly used [39, 40], typically when one expects only small changes in E.

The initial energy level of the top TSS (without an applied gate voltage) is $E_{\mathrm{top}}^0 = a\sqrt{n_{\mathrm{top}}^0}$. A change in the carrier concentration $n_{\mathrm{top}}^0 \rightarrow n_{\mathrm{top}}^0 + n_{\mathrm{top}}$ will therefore result in a change of the energy level by ΔE_{top} according to $E_{\mathrm{top}}^0 + \Delta E_{\mathrm{top}} = a\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}}$, where we find that

$$\Delta E_{\mathrm{top}} = a\left(\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}} - \sqrt{n_{\mathrm{top}}^0}\right). \tag{4.7}$$

Note that this term significantly differs from eq. (4.5), which shows a linear dependence between E and n in contrast to a square root dependence. Combining equations (4.3) - (4.7) we find the explicit equations

$$n_{\mathrm{top}} \simeq \left(\left(\frac{C_{\mathrm{TI}} a}{e^2} \right)^{-1} \left(-n_{\mathrm{bot}} + \frac{C_{\mathrm{TI}} a}{e^2} \left(\sqrt{n_{\mathrm{bot}}^0 + n_{\mathrm{bot}}} - \sqrt{n_{\mathrm{bot}}^0} + \sqrt{n_{\mathrm{top}}^0} \right) - \frac{C_{\mathrm{gate}} V_{\mathrm{gate}}}{e} \right) \right)^2 - n_{\mathrm{top}}^0 \tag{4.8}$$

and

$$n_{\mathrm{bot}} = \left(\left(\frac{C_{\mathrm{TI}} a}{e^2} \right)^{-1} \left(-n_{\mathrm{top}} + \frac{C_{\mathrm{TI}} a}{e^2} \left(\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}} - \sqrt{n_{\mathrm{top}}^0} + \sqrt{n_{\mathrm{bot}}^0} \right) \right) \right)^2 - n_{\mathrm{bot}}^0 \tag{4.9}$$

(For intermediate steps see appendix F.1)

For this set of non-linear equations, we cannot find a simple analytical solution, such that we evaluate equation (4.8) and (4.9) numerically. The resulting values of n_{top} (n_{bot}) as a function of the gate voltage we will use in the three channel transport model as given in eq. 2.

Equation (4.8) and (4.9) are valid as long as the Fermi energy only cuts the TSS on both, top and bottom surface as depicted in fig. 4.7 (b). However, doping or gating of the TI film can result in the case where on one surface the Fermi energy is located within the band gap, only cutting the TSS while on the other surface the Fermi energy lies within the film valence band or conduction band (fig. 4.7 (c)). Due to the presence of many available states in these bands, the quantum capacitance on the corresponding surface, in the present case C_{bq}, becomes very large [39].

In detail, when shifting the bands by applying a gate voltage, as soon as the valence band edge reaches the Fermi level, the gate induced charge carriers are induced exclusively in the corresponding valence bands and the gate induced electric field is completely screened by the bottom channel [59]. Further decreasing the gate voltage will not lead to a further shift of the bands with respect to the Fermi energy, but only to an increase of the gate induced charge carriers in the valence bands - the Fermi level is pinned at the valence band edge. In terms of the replacement diagram in Fig. 4.7 (a) a large value of C_{bq} leads to all the gate induced charge carriers being placed on this capacitor rather than on C_{TI}, which results in the carrier concentration in the top TSS channel to be unchanged.

To include the behavior of the bulk conductivity into our model, we perform in the following a detailed analysis of the band bending on the TI film as a function of the film bulk doping and the applied gate voltage. For this we model a 10 nm thin TI film as a small bandgap semiconductor ($E_{\mathrm{gap}} = 260$ meV), in agreement with our ARPES results. For the band bending calculations we solve the Schrödinger-Poisson equation in the Boltzmann approximation [60] for which we use an effective mass $m^* = 0.15 m_{\mathrm{e}}$, which we extract from the ARPES measurements by fitting a parabolic dispersion to the valence band edge and which is comparable to literature values [55, 61]. A further parameter in the calculations is the TI doping level as it would be observed in a bulk crystal, far away from the surface space charge layer.

Because we do not have access to this quantity experimentally, due to the thin film character of the present sample, we varied this parameter in the range of the band gap and analyzed the resulting band bending.

4.4.4 Band bending calculations

An exemplary band schematic resulting from the calculations, without gating, is shown in Fig. 4.8 (a). Here, the position of the bands at the TI surface is fixed according to the ARPES measurement. As a reference we show as dashed line in Fig. 4.8 (a) the calculated band bending for an extended bulk crystal, with a doping level corresponding to a position of the Fermi level deep in the bulk 30 mV above the bulk valence band edge. The bands are bend upwards from the TI surface into the bulk, until the bulk band positions are reached, resulting in a space charge layer (scl) as indicated in Fig. 4.8 (a). In the corresponding thin film limit however (Fig. 4.8 (a) solid lines), where we set the band positions on both surfaces of the thin film according to ARPES exemplarily, the bands are rather flat due to the long screening length in comparison to the film thickness [39, 40], in combination with the boundary condition of the band positions at the two surfaces.

Since the doping concentration in the film is unknown, we analyze in the following the dependence of the film carrier concentration n_{film} as a function of the bulk doping levels, with respect to the valence band edge as shown in Fig. 4.8 (b). Hereby, the thin film carrier concentration results from integrating over the 10 nm thick film. We find that the amount of charge carriers in the thin film is approximately constant with $n_{\mathrm{film}} = 9 \cdot 10^{11}\ \mathrm{cm}^{-2}$ when the bulk doping is such that the Fermi level is inside of the band gap of the corresponding bulk crystal.

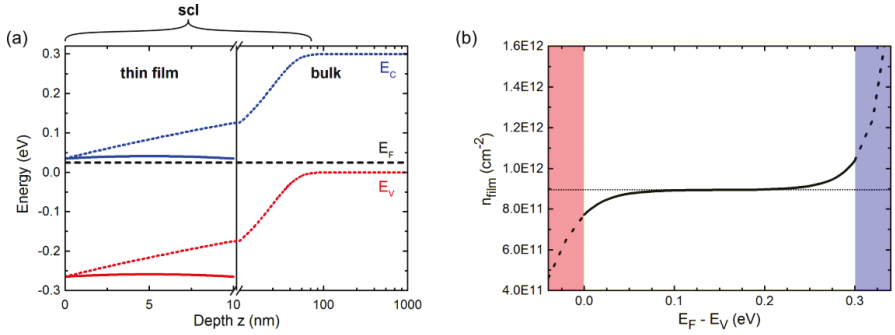

Figure 4.8. Band bending calculations at $\mathbf{V_{gate} = 0\ V}$. (a) Band bending in a semi-infinite bulk crystal (dashed lines) with the crystal surface located at $z = 0$ nm. The plot shows an exemplary bulk doping level with the Fermi energy located 30 mV above the valence band edge. The band positions at the surface of the crystal are fixed by ARPES and the extension of the resulting space-charge layer (scl) is indicated. (solid lines) Band bending throughout the 10 nm thick TI thin film with its two surfaces located at $z = 0$ nm and $z = 10$ nm, respectively. The bands for the thin film are rather flat in comparison to the semi-infinite crystal due to the presence of the second surface. (b) Carrier concentration in the 10 nm TI film as a function of the bulk doping level with respect to the valence band edge $E_{\mathrm{F}} - E_{\mathrm{V}}$. The valence and conduction bands are indicated as red and blue shaded areas, respectively. For all positions

of the Fermi level inside the band gap (i.e. for all reasonable doping levels of the TI film) the integrated charge carrier density of the TI film bulk is approximately constant at $n_{\mathrm{film}} = 9 \cdot 10^{11}\ \mathrm{cm}^{-2}$.

4.5 Application of the gating and transport model to the experimental data

Fitting eq. (4.2) to the experimental data for $\mathrm{V_{gate}} > -32\ \mathrm{V}$ via n^0_{bot}, μ_{top}, μ_{bot} and μ_{film} we find that in the three channel model, the bottom channel reaches the Dirac point and therefore also the valence band edge at $\mathrm{V_{gate}} = -32\ \mathrm{V}$. Below this gate voltage the bottom channel is dominated by bulk *p*-conduction and we therefore apply the gating model which assumes a large density of states at the bulk valence band edge. With the bottom channel dominated by the TSS *n*-conduction at larger gate voltages we can describe the entire range of the experimental data.

The resulting fit of the combined gating and transport model to the experimental data is shown in Fig. 4.9 (a) and results in $\mu_{\mathrm{top}} = 610\,\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, $\mu_{\mathrm{bot}} = 124\,\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, and $n^0_{\mathrm{bot}} = 1.7 \cdot 10^{12}\ \mathrm{cm}^{-2}$, while $n^0_{\mathrm{top}} = 4 \cdot 10^{12}\ \mathrm{cm}^{-2}$ is fixed by the ARPES measurement. Hereby, the gate voltage range corresponds to an amount of gate induced charge carriers $n_{\mathrm{gate}}(V_{\mathrm{gate}} = 40\ \mathrm{V}) = 2.25 \cdot 10^{12}\ \mathrm{cm}^{-2}$ to $n_{\mathrm{gate}}(V_{\mathrm{gate}} = -120\ \mathrm{V}) = 6.75 \cdot 10^{12}\ \mathrm{cm}^{-2}$. We find that in general the model fits very well to the data, only when the filling in the bottom TSS approaches the Dirac point, we observe some deviations between the experimental data and our model. This observation we explain by a smooth transition between the gating regimes in the experiments, due to the room temperature conditions and resulting smeared out Fermi distribution. Given a width of the Fermi function at room temperature $\Delta = 110$ meV, corresponding to $F\left(-\frac{\Delta}{2}\right) = 0.9$ and $F\left(\frac{\Delta}{2}\right) = 0.1$, translates to a smearing out in the TSS according to eq. (4.1) and (4.6) to $\Delta V_{\mathrm{gate}} \approx 10$ V. This value fits well to the experimentally observed transition region in Fig. 4.9 (a). For the bulk holes, we can only determine an upper boundary of $\mu_{\mathrm{film}} < 2\,\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, like before.

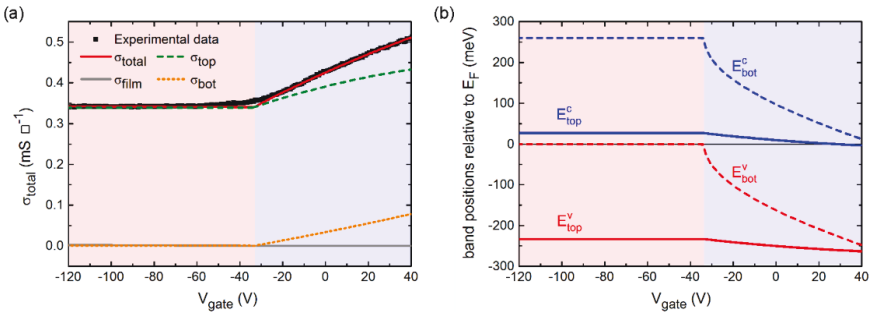

Figure 4.9. Fit of transport model to experimental data. (a) Experimental gate dependent sheet conductivity with a fit of eq. (4.2), resembling the combined gating and three-layer transport model. (b) Band positions with respect to E_{F} in the top and bottom channel as a function of gate voltage, corresponding to (a). $E^{\mathrm{v}}_{\mathrm{top}}$ $\left(E^{\mathrm{c}}_{\mathrm{top}}\right)$ is the position of the valence (conduction) band in the top channel and $E^{\mathrm{v}}_{\mathrm{bot}}$ $\left(E^{\mathrm{c}}_{\mathrm{bot}}\right)$ in the bottom channel, respectively.

In this mode, we find that at $V_{\mathrm{gate}} = 0\,\mathrm{V}$ the portion of the total current through the bulk, top TSS and bottom TSS are 90% and 10%, respectively. For the bottom TSS this is half of the value obtained from the simplified two channel model. Furthermore, at $V_{\mathrm{gate}} = -32\,\mathrm{V}$ the current through the sample is almost exclusively transmitted by the top TSS, as the bottom TSS and the film bulk conductivity are minimized.

Figure 4.9 (b) further shows the band positions relative to the Fermi energy for the top and bottom channel. Here we observed that while the bottom channel band positions are shifted considerably as a function of gate voltage, the band positions in the top channel change only by an amount of $\Delta E \approx 30\,\mathrm{meV}$.

This observation is in agreement with the screening of the gate induced electric field by the bottom TSS. Furthermore, the larger initial filling level of the top channel results in a slower change of the band positions as charges are induced, due to the square-root dependence of the E_{top} with respect to n_{top}.

4.6 Discussion

While the simple two channel transport model allows to estimate the conduction through the TI film, the more general three channel model allows to explain the experimental data better. In detail, only the three channel model, can reproduce the experimentally observed slight negative curvature of the conductivity graph above $\mathrm{V_{gate}} = -32\,\mathrm{V}$, which is the result of the quantum capacitances and the capacitive coupling of the top and bottom TSS channel.
As mentioned before, contrary to the principle of capacitive coupling of the top and bottom TSS, there are literature reports, where gating of TI ultra-thin films with a single gate electrode results in only the TSS closest to the gate electrode to be shifted with respect to the Fermi energy, while the other TSS remains unchanged [22, 44] corresponding to our two channel model. Such a behavior, we explain to be due to the TSS on the corresponding surface further away from the gate being pinned, e.g. by bulk bands. In the corresponding references [22, 44] significant filling of the corresponding TSS channels are reported, which suggests that the Fermi level might indeed be located at the conduction band edge. As a result, the filling of the corresponding TSS and therefore its transport properties do not change significantly by application of a gate voltage, because the additional charges are induced predominantly in the bulk bands, while the transport properties of the corresponding TSS channel are unchanged. Likewise, impurity states within the bulk band gap, as reported in Ref. [62] can also result in a Fermi level pinning.
Furthermore, even when the capacitive coupling is considered certain configurations of initial filling levels in the top and bottom channel, due to e.g. surface doping, can result in the case where the filling level of one of the two channels only changes insignificantly. This effect can also lead to the interpretation that generally only one of the channels is affected by the gate.
We conclude that the TSS at the top and bottom surface are generally coupled and only by certain configurations of Fermi level pinning it can occur that only the TSS filling of one of the two surface states changes by application of a gate voltage, as described in our two-channel model. Even more, when there is a large density of states present at the TI film surface closest to the gate electrode, then the effect of the gate on the TSS can be largely screened such that the top and bottom TSS channel filling both are mostly independent of the gate voltage. This effect also explains often reported problems in first generation TI samples where heavy doping results in the Fermi energy being located well within the valence/conduction bands [38]. As a

result, the overall conductivity of such TI films does not change significantly when applying a gate voltage.
For this reason, we find that for the comprehensive interpretation of transport measurements at TIs it is of utter importance to perform a detailed analysis of the filling levels of the TSS channels in combination with the bulk bands, as provided by the present model. While the gate voltages applied in the present work are rather large, the observed behavior of the TI film can be reproduced in the range of a few volts, as typically used in devices, by use of a suitable gate dielectric [22].

4.6.1 Constant quantum capacitance approximation

For small changes in the Fermi energy corresponding to small amounts of gate induced charge carriers, the quantum capacitance terms can be assumed to be constant, as long as the initial number of charge carriers is much larger than the gate induced carrier concentration. In this case, the quantum capacitance is given by the initial carrier concentrations:

$$C^0_{\mathrm{tq,bq}} = \frac{e^2\sqrt{n^0_{\mathrm{top,bot}}}}{a}$$

and Eq. (4.3) becomes

$$\Delta E_{\mathrm{top}} = e^2\left(\frac{n^0_{\mathrm{top}}+n_{\mathrm{top}}}{C_{\mathrm{tq}}} - \frac{n^0_{\mathrm{top}}}{C^0_{\mathrm{tq}}}\right) \approx e^2\left(\frac{n^0_{\mathrm{top}}+n_{\mathrm{top}}}{C^0_{\mathrm{tq}}} - \frac{n^0_{\mathrm{top}}}{C^0_{\mathrm{tq}}}\right) = \frac{e^2 n_{\mathrm{top}}}{C^0_{\mathrm{tq}}}.$$

This expression is again consistent with eq. (4.2) and results in the equations

$$n_{\mathrm{bot}} = -\frac{1}{\left(1 + C_{\mathrm{gate}}/C^0_{\mathrm{bq}} + C_{\mathrm{TI}}/C^0_{\mathrm{bq}}\right)}\left(\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e} + \frac{C_{\mathrm{TI}}n_{\mathrm{top}}}{C^0_{\mathrm{tq}}}\right). \tag{4.10}$$

and

$$n_{\mathrm{top}} = n_{\mathrm{TI}} = \frac{C_{\mathrm{TI}}\left(\mu_{\mathrm{top}} - \mu_{\mathrm{bot}}\right)}{e^2} \Leftrightarrow n_{\mathrm{top}} = \frac{C_{\mathrm{TI}}/C^0_{\mathrm{bq}}}{\left(1 + C_{\mathrm{TI}}/C^0_{\mathrm{tq}}\right)} n_{\mathrm{bot}}. \tag{4.11}$$

(For intermediate steps see appendix F.2)

The analytical solution of this system of linear equations (4.10) and (4.11) is

$$\begin{aligned} n_{\mathrm{top}} &= \frac{C_{\mathrm{TI}}/C^0_{\mathrm{bq}}}{1 + C_{\mathrm{TI}}/C^0_{\mathrm{bq}} + C_{\mathrm{gate}}/C^0_{\mathrm{bq}} + C_{\mathrm{TI}}/C^0_{\mathrm{tq}} + C_{\mathrm{TI}}C_{\mathrm{gate}}/(C^0_{\mathrm{bq}}C^0_{\mathrm{tq}})} \cdot \frac{C_{\mathrm{gate}}}{e} V_{\mathrm{gate}} \\ n_{\mathrm{bot}} &= \frac{\left(1 + C_{\mathrm{TI}}/C^0_{\mathrm{tq}}\right)}{1 + C_{\mathrm{TI}}/C^0_{\mathrm{bq}} + C_{\mathrm{gate}}/C^0_{\mathrm{bq}} + C_{\mathrm{TI}}/C^0_{\mathrm{tq}} + C_{\mathrm{TI}}C_{\mathrm{gate}}/(C^0_{\mathrm{bq}}C^0_{\mathrm{tq}})} \cdot \frac{C_{\mathrm{gate}}}{e} V_{\mathrm{gate}} \end{aligned} \tag{4.12}$$

These equations directly give the amount of charge carriers induced in the top and bottom TSS by the back gate with the only parameters being C_{TI} and initial carrier concentrations in each channel. Furthermore, from equation (4.11) it directly follows

$$\Rightarrow \frac{n_{\mathrm{top}}}{n_{\mathrm{bot}}} = \frac{\frac{C_{\mathrm{TI}}}{C_{\mathrm{bq}}^{0}}}{\frac{C_{\mathrm{TI}}}{C_{\mathrm{tq}}^{0}} + 1}. \tag{S6}$$

This result is in accordance with previous reports [40] and describes that the ratio of the gate induced charge carriers in top and bottom surface depends on the ratio of quantum capacitances of top and bottom TSS. Note that from this expression it is even possible to have $\frac{n_{\mathrm{top}}}{n_{\mathrm{bot}}} > 1$ which means that the majority of the back gate induced charge carriers are located in the top TSS rather than the bottom TSS.

4.6.2 Maximum applicable gate voltages

For large positive gate voltages $V_{\mathrm{gate}} > 45\ \mathrm{V}$ the measured conductivity in the experiments becomes noisy such that no further data acquisition was possible in this range. From the calculations this is also the value we expect the top TSS to come close to the bulk conduction band edge. In combination with the clear transition of the transport regime at $V_{\mathrm{gate}} = -32\ \mathrm{V}$ we have experimental indications of the actual size of the band gap $E_{\mathrm{gap}} \approx 260\ \mathrm{meV}$. On the other hand, for gate voltages below $V_{\mathrm{gate}} < -175\ \mathrm{V}$ the leakage current through the SOI substrate limits further data acquisition. In the gate voltage range shown in the main text the experiments were reproducible.

4.6.3 Comparison of different samples

In total, for the current studies we have investigated three different samples with respect to their gate-dependent conductivity in the four-tip STM (see Table 4.1). Hereby, sample #1 is the one we focus on in the main text. Figure 4.10 shows the full range of experimental data acquired for this sample. In detail, for large positive gate voltages $V_{\mathrm{gate}} > 45\ \mathrm{V}$ the measured conductivity becomes very noisy such that no further data acquisition was possible in this range. On the other hand, for gate voltages below $V_{\mathrm{gate}} < -175\ \mathrm{V}$ the leakage current through the SOI substrate limits further data acquisition. This behavior was very similar for all samples we investigated, indicating the SOI to be limiting factor. In the viable gate-voltage range shown the experiments were reproducible for all samples.

Sample #	Thickness	Composition	Transferred via	$\sigma_{\mathrm{total}}(V_{\mathrm{gate}} = 0\ \mathrm{V})$
1	10 nm	$(Bi_{0.53}Sb_{0.47})_2Te_3$	UHV	$0.44\ \mathrm{mS}\ \square^{-1}$
2	21 nm	$(Bi_{0.54}Sb_{0.46})_2Te_3$	UHV	$0.98\ \mathrm{mS}\ \square^{-1}$
3	9 nm	$(Bi_{0.66}Sb_{0.34})_2Te_3$	Air	$0.40\ \mathrm{mS}\ \square^{-1}$

Table 4.1. Summary of the different samples analyzed with respect to their gate-dependent sheet conductivity in the four-tip STM.

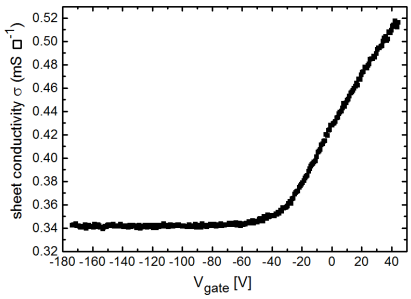

Figure 4.10. Full range of experimental gate-dependent conductivity of sample #1.

Figure 4.11 shows the gate-dependent conductivity of a 21 nm thin film of $(Bi_{0.54}Sb_{0.46})_2Te_3$, where we find that below $V_{\mathrm{gate}} \approx 35$ V the gate-dependent sheet conductivity saturates, while for higher gate voltages we see an increase in the conductivity. Hereby, the absolute conductivity of this TI film is larger in comparison to sample #1, which we address to the composition of sample #2 to be more towards the inherently n-doped Bi2Te3 and which results in even larger carrier concentration than in the already n-type sample #1. The relative change in conductivity of sample #2 in the applicable gate voltage range is however much smaller than that of sample #1. This observation would be explained by the bottom channel valence band edge to be located close to the Fermi energy already without gating, which seems to be counter-intuitive due to the expected larger amount of n-type doping. However, due to the larger film thickness, band bending in this sample may play in increased role in the distribution of charges throughout the film, possibly explaining this result. Furthermore, the increased thickness of the film weakens the capacitive coupling of the top channel with respect to the back gate, which can also explain why we do not see the negative curvature of the graph at $V_{\mathrm{gate}} > -30$ V as evident for sample #1 in Fig. 4.10 and which is a direct evidence of the coupled gating of the transport channels.

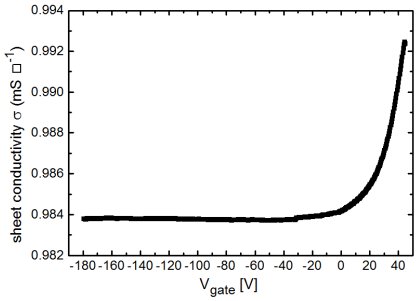

Figure 4.11. Experimental gate dependent conductivity of sample #2 (21 nm thin $(Bi_{0.54}Sb_{0.46})_2Te_3$, UHV transferred).

Sample #3 is an even more n-type sample which was transferred through air to the four-tip STM. As evident in Fig. 4.12, we do not observe a saturation in the conductivity below a certain gate voltage in the applicable gate voltage range which is in contrast to sample #1 and #2. We

explain this finding by a large doping of the sample as result of its composition and the exposure to ambient conditions on the time scale of a few hours, in agreement with literature [24, 25, 46, 47, 48]. In detail, the resulting higher carrier concentration in the film is expected to result in the conduction band to cut E_F such that shifting the bands requires larger gate voltages with respect to the other samples. In this way, the range of applicable gate voltage resulting from the SOI substrate is not sufficient to shift the bands until the Fermi energy coincides with the bottom channel valence band edge like in the other samples. The hump in the graph, located at $V_{gate} \approx -20$ V in this course can be explained as the position of the conduction band edge in the bottom channel being shifted above E_F. In agreement with this explanation is the higher conductivity of this sample in comparison to sample #1 as a result of the larger n-type carrier concentration of sample #3.

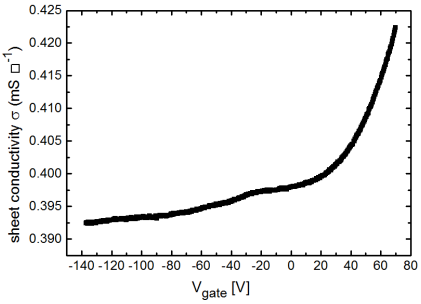

Figure 4.12. Experimental gate dependent conductivity of sample #3 (10 nm thin $(Bi_{0.66}Sb_{0.34})_2Te_3$, transported through air). We do not observe a saturation of the conductivity as function of the gate voltage in contrast to sample #1 and #2.

4.7 Conclusion

From gate-dependent transport measurements, we are able to disentangle the transport through different conduction channels of a $(Bi_{0.53}Sb_{0.47})_2Te_3$ thin film, namely the top and the bottom TSS channel, as well as the interior of the TI film, in form of a bulk conductivity. Hereby, the combination of *in situ* transport measurements in combination with photoemission spectroscopy on the same sample, without exposition to ambient condition, allow us to deduce the carrier concentration, and respective mobility, in each of the three channels. The present gating and transport models are applicable for a wide range of samples including also thicker films. TI samples with a Dirac point located well in the band gap, typically show a local minimum in the film conductivity at the transition from *n*- to *p*-type transport in the TSS [22], which we do not observe in the present sample due to the Dirac point coinciding with the valence band edge. Such a behavior can also be reproduced by the present gating and transport model and would be of interest for further application of the model in order to determine charge carrier properties without the necessity of an external magnetic field. Furthermore, the gating effect can in principle depend on the temperature, e.g. due to a temperature dependent screening of charges by the film bulk and corresponding measurements could clarify this issue.

Chapter 5 Chalcogenide based van der Waals epitaxy: Interface conductivity of Tellurium on Si(111)

5.1 Introduction

For the application of TI films in future electronic devices it is important that their TSS, which governs the promising electronic properties of TIs, can be addressed individually in devices. In the first generation of chalcogenide based van-der Waals TIs (Bi_2Se_3, Bi_2Se_3 and Sb_2Te_3) defect induced doping, due to anti-site defects and Te/Se vacancies led to large charge carrier concentrations in the crystal bulk, such that bulk conductivity was dominant in these samples [38]. This problem has been overcome by refining the crystal preparation methods [63] and use of ternary (e.g. $BiSbTe_3$) and quaternary materials (e.g. $BiSbTe_2Se$), in which the defects compensate [38], resulting in low bulk carrier concentrations and conductivity. Furthermore, the use of ultra-thin films further allows to reduce the influence of the TI bulk on transport.

For the application of TIs in electronic devices large-scale preparation processes have to be established, with the most suitable process being molecular-beam epitaxy (MBE) [64]. A prerequisite for MBE growth hereby is a suitable substrate on which the TI films can be grown in high quality, where amongst others Si(111) has proven to fulfill this requirement [64]. For the growth on Si(111) the substrate surface is however typically passivated to form a template for the subsequent van-der Waals growth. As a result, besides the conductivity of the substrate itself and the transport channels of TI films, which chapter 4 of this thesis dealt with, the substrate interface resulting from the passivation prior to the TI film growth can result in an additional parallel conductance channel which potentially bypasses the TSS and undermines its application in devices.

While the Si(111) substrate bulk can be readily optimized to be low conducting by choosing a low-doped substrate, the passivation of the Si(111) surface prior to the TI film growth can result in a highly conducting interface layer, depending on the used material and exact preparation parameters. To name an example, one possible termination of the Si(111) surface is the Bi/Si(111)$-(\sqrt{3}\times\sqrt{3})$ reconstruction [63] which is reported to have a conductivity of up to $\sigma = 4 \cdot 10^{-3}\,\mathrm{S/\square}$ [54]. This amount of conductivity is in the range of typical TSS conductivities [17] and therefore impracticable for the analysis and further application of the TSS properties. The samples used in this thesis are grown on Si(111) substrates which are saturated with Te to form a template for the TI film growth. The corresponding conductivity of Te on Si(111) is therefore of great interest but we find it not to be reported in literature.

In this chapter, we report the investigation of the structural, electronic and transport properties of the Te saturated Si(111) surface by means of scanning transmission electron microscopy (STEM), low-energy electron diffraction (LEED), scanning tunneling microscopy (STM) and four-probe conductivity measurements in the four-tip STM.

5.2 Chalcogenide based van der Waals epitaxy: Interface conductivity of Tellurium on Si(111)

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F.L., S. J., M.La., M.Ly, V.C., E.N., G.M., D.G. and B.V. conceived the experiments**. F.L.**, S.J., J.D., M.L., E.N., M.L and performed the measurements and analyzed the experimental data. G.B. performed the theoretical calculations. **F.L.**, M.L., G.B., J.D. wrote the manuscript. All authors discussed and commented on the manuscript.

Chalcogenide-based van der Waals epitaxy: Interface conductivity of tellurium on Si(111)

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We present a combined experimental and theoretical analysis of a Te rich interface layer which represents a template for chalcogenide-based van der Waals epitaxy on Si(111). On a clean Si(111)-(1 × 1) surface, we find Te to form a Te/Si(111)-(1 × 1) reconstruction to saturate the substrate bonds. A problem arising is that such an interface layer can potentially be highly conductive, undermining the applicability of the on-top grown films in electric devices. We perform here a detailed structural analysis of the pristine Te termination and present direct measurements of its electrical conductivity by *in situ* distance-dependent four-probe measurements. The experimental results are analyzed with respect to density functional theory calculations and the implications of the interface termination with respect to the electrical conductivity of chalcogenide-based topological insulator thin films are discussed. In detail, we find a Te/Si(111)-(1 × 1) interface conductivity of $\sigma_{2D}^{Te} = 2.6(5) \times 10^{-7}$ S/□, which is small compared to the typical conductivity of topological surface states.

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In recent years, chalcogenide van der Waals (vdW) thin films have emerged as potential disruptive technologies in several fields of applications [1–3]. Among them are topological insulators (TIs) where the spin-momentum locking of topological surface states (TSS) prohibits direct backscattering and makes them an ideal candidate for low-power spintronics and quantum computing [1,4]. The most promising materials for such applications at room temperature are Bi_2Se_3, Bi_2Te_3, and Sb_2Te_3 due to their pronounced band gap [1,5]. For the successful utilization of the auspicious TSS properties in electronic devices it is necessary that an electrical current is transmitted predominantly by these surface states. Hereby, the TI bulk conductivity can play a significant role by the formation of a parasitic parallel conduction channel practically bypassing the TSS, as extensively studied in recent years [6,7]. In consequence, the growth of Bi_2Se_3, Bi_2Te_3, and Sb_2Te_3 TI thin films by molecular-beam epitaxy has become a crucial tool, which allows precise TI bulk and surface engineering and a high surface-to-bulk ratio [8,9]. A common substrate for such growth of TI films is Si(111), where an initial saturation of the substrate bonds is required to form a template for the vdW epitaxy [8,10,11]. The TI film is then grown on top of this template layer and is only weakly bound by vdW interaction to the underlying structure with a sharp interface between the TI film and the substrate [11]. The problem arising is that such terminations of Si can have a high conductivity resulting in an additional parasitic conductivity of the interface layer between the TI film and the substrate [12–16]. Furthermore, such an interface transport channel is difficult to distinguish from contributions of the TSS channel at the bottom of the TI film by conventional transport measurements.

We present here a detailed experimental and theoretical analysis of the structure and charge transport properties at the Te interface of a Bi_2Te_3-based thin film grown on a Si(111) substrate. We first investigate the sample cross section in scanning transmission electron microscopy (STEM) and subsequently prepare the interface termination of the substrate without the TI thin film on top. Here, the combination of low-energy electron diffraction (LEED) and multitip scanning tunneling microscopy (STM) allows us to directly quantify the structural and charge transport properties of the pristine, atomically thin Te layer *in situ*. The results are interpreted with respect to density functional theory (DFT) calculation which we performed in the context of the experimentally observed structures.

To analyze the atomic structure of the Te interface layer, we use a cross-sectional aberration corrected STEM (FEI Titan 80-200) for which sample cross sections are prepared by focused ion-beam (FIB) etching using 5 keV Ga ions and subsequent Ar ion milling (Fishione NanoMill) to reduce the FIB-induced damage. High-resolution STEM images are made in high-angle annular dark field mode where the contrast scales approximately quadratic with the atomic number Z. Figure 1(a) shows a STEM measurement of the TI thin film grown on Si(111) [8]. In detail, the film shown here is Bi_1Te_1 which is grown by an initial saturation of the Si(111) substrate with Te as described below, followed by the codeposition of Bi and Te [17]. The result is in an alternating stacking of Bi_2Te_3 quintuple layers and Bi(111) bilayers as indicated in Fig. 1(b). The substrate interface hereby is identical to that of a pure Bi_2Te_3 film and is reported to be Te rich [8,11]. From the STEM measurements, we find that the Te interface layer atoms, which are deposited prior to the TI film growth to saturate the Si(111) surface, are located directly above the underlying Si(111) substrate atoms, which can be explained by adsorption of Te at the T1 (on top) site corresponding to a (1 × 1) structure. The first layer of the TI film on top of the Te interface is decoupled from the interface layer as evident by its relaxed crystal structure corresponding to the TI bulk lattice parameters [8]. A line scan perpendicular to the interface

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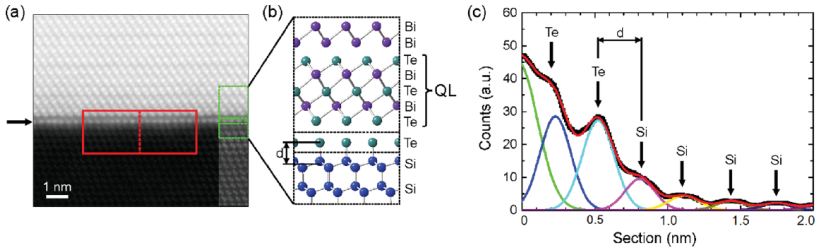

FIG. 1. (a) STEM image of the Bi_1Te_1/Si(111) interface with the atom row of the Te interface indicated by an arrow. The viewing direction with respect to the Si substrate is $(1\bar{1}0)$ and Bi atoms appear brightest due to $\sim Z^2$ contrast. Near the right edge of the image the overall brightness in the region of the substrate was increased to accentuate the Si atom rows. (b) Schematic of the atomic layers near the interface in (a). A quintuple layer (QL) corresponding to Bi_2Te_3 and the Si-Te interlayer distance d are indicated. (c) Line scan perpendicular to the interface averaged over the red frame indicated in (a) (black dots) and corresponding multiple Gaussian peak fit (red curve). The Gaussian peak fits of the Te interface layer and first Si bilayer result in a Si-Te spacing of $d = 2.88(3)$ Å.

layer is shown in Fig. 1(c). The peak positions corresponding to the atomic layers are analyzed by fitting multiple Gaussian peaks. Hereby, Si peaks correspond to the center of mass of the Si(111) bilayers. We measure the distance between the center of mass of the topmost Si(111) bilayer and the Te interface layer to be $d = 2.88(3)$ Å.

Due to the weak vdW coupling of the TI film to the substrate, the properties of the interface layer are expected to be unaffected by the growth of the TI film on top. In the next step, we therefore prepare the sole Te termination of the Si(111) substrate, to further investigate the structural and transport properties of the Te interface. Hereby, we use the same preparation procedure as for the sample mentioned above, on which also the TI film was grown: A low doped p-Si(111) substrate with $\rho_{\text{bulk}} = 22\,\text{k}\Omega\,\text{cm}$ was cleaned using a RCA type procedure [8]. After the final hydrofluoric acid (HF) dip the sample was immediately introduced into the STM/LEED analysis chamber ($p \approx 1 \times 10^{-10}$ mbar). The hydrogen was then desorbed at 700 °C for 10 min. During this step, LEED monitoring shows a clear Si(111)-(1 × 1) surface structure corresponding to the unreconstructed Si(111) substrate. The reactive Si(111)-(1 × 1) surface is then passivated by Te at a sample temperature of 270 °C and a Te rate of 1 ML/min for 10 min [18]. Here, the number of atoms in 1 ML corresponds to the number of atoms on the Si(111)-(1 × 1) surface (7.84×10^{14} atoms/cm^2, i.e., half a bilayer). The Te deposition is stopped by closing the evaporator and quenching the sample to room temperature. After the Te deposition, LEED still shows a (1 × 1) pattern as shown in Fig. 2(a) and in agreement with the STEM measurements. The intensity of the LEED pattern is comparable to that of the pure Si(111)-(1 × 1) surface before Te deposition, indicating a crystalline quality of the Te layer. Note that in the LEED images a diffuse background intensity is observed, both before and after deposition of the Te, which we attribute to a high surface roughness resulting from the HF etching [19,20]. We conclude that we have prepared a single atomic layer of Te on the sample surface resulting in a Te/Si(111)-(1 × 1) reconstruction: Due to the high reactivity of the unreconstructed Si(111) surface, it is certain that at least one layer of Te sticks to the sample surface, in agreement with literature [30]. Furthermore, we confirmed in a separate experiment, where we first deposited ∼20 ML of Te at room temperature and then heated the sample to 270 °C under LEED investigation, that no Te beyond the first layer sticks to the sample surface at this temperature. In detail, in this experiment the initial diffuse LEED image begins to show spots at a sample temperature above ∼200 °C, identical to the LEED image for deposition of 1 ML of Te at elevated temperature.

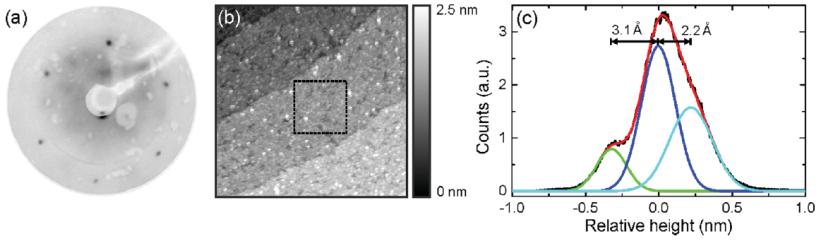

FIG. 2. (a) LEED image of the Te/Si(111) surface recorded at an electron energy of 30 eV. We observe spots corresponding to a (1 × 1) structure with respect to the Si(111) surface. (b) Topography of the Te/Si(111)-(1 × 1) surface showing Si substrate steps with a height of 3.1 Å. The single terraces are found to be rough due to holes in the surface and clusters of additional material on top (sample bias +2 V, 70 pA, scan size 800 nm). (c) Height distribution in the square indicated in (b) with a multiple Gaussian peak fit. The differences between the peak positions are 3.1 and 2.2 Å, corresponding to the average depth of the holes and height of the excess material on top, respectively.

Subsequent STM scans of the sample surface show substrate steps of 3.1 Å height, corresponding to monoatomic steps of the Si(111) surface [Fig. 2(b)]. Hereby, a monoatomic step corresponds to the distance between neighboring bilayers of the Si(111) surface. The terrace width of ~300 nm between steps is in accordance with the miscut of the Si(111) wafer. On the terraces, we observe pits and adsorbates, where we expected the additional material on top of the film to be additional Te adatoms and remainings of the HF cleaning procedure [19]. The average height of the adsorbates we find to be 2.2 Å as shown in Fig. 2(c). From the same graph, we also find that the pits are 3.1 Å in depth corresponding to the monoatomic step height of the Si(111) surface. Such pits and adsorbates, associated with a general surface roughening, are reported to result from the HF cleaning procedure [20,21]. Although we are not able to atomically resolve the Te/Si(111)-(1 × 1) structure in STM, we assume that the Te termination is intact also inside of the pits because the Te deposition should be uniform throughout the surface. The observed surface roughness and adsorbates are also in agreement with the diffuse background intensity in the LEED measurements.

In order to further evaluate the experimental observations, we performed DFT calculations in the local density approximation [22]. We employed the full potential linearized augmented plane-wave method in thin-film geometry [23] as implemented in the FLEUR code [24]. By deposition of a variable amount of Te atoms on the Si(111) surface (modeled by a ten layer film), we calculated two stable surface configurations corresponding to a $p(1 \times 1)$ and $c(2 \times 2)$ reconstruction, respectively. We find the predicted Te/Si(111)-(1 × 1) configuration to be in excellent agreement with our experimental results, while the structure of the $c(2 \times 2)$ reconstruction contradicts our experimental observations. In principle, a $c(2 \times 2)$ Te coverage would be ideal to saturate all dangling bonds and results in an insulating interface. However, the Si-Te interlayer distance of 1.9 Å is in variance with the experimental findings. We have also checked the possibility that this $c(2 \times 2)$ ordered layer is "hidden" in the experiment (e.g., due to the formation of rotational domains) and covered by an extra Te layer. This configuration, however, would place the extra Te layer 4.0 Å above the Si substrate, being also incompatible with the experiment. Finally, we checked different positions of $p(1 \times 1)$ ordered Te layers and found that the hollow (T4) position is almost 1 eV higher in energy than the on-top (T1) position and gives a much too small Si-Te interlayer distance of 1.9 Å. It is therefore also ruled out to be present in our experiments. In consequence, the calculations of the Te/Si(111)-(1 × 1) surface result in the adsorption position of the Te atoms at the on-top (T1) site, corresponding to the STEM and LEED results. In this configuration, the distance between the center of mass of the topmost Si(111) bilayer and the Te interface layer in the DFT calculations amounts to $d = 2.87(1)$ Å, which is in excellent agreement with the interlayer distance we find in STEM measurements $d = 2.88(3)$ Å. For this structure, the calculations show metallic bands and a high density of states in the Te/Si(111)-(1 × 1) layer at the Fermi energy as shown in Fig. 3. The resulting high carrier concentration potentially results in a high conductivity of the Te/Si(111)-(1 × 1) layer. For the Si(111) bulk, the calculations show a band gap of

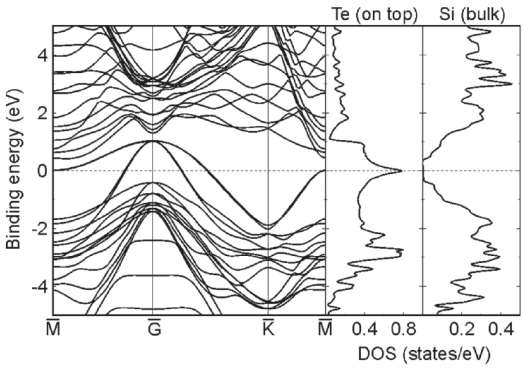

FIG. 3. Calculated band structure and resulting density of states of the Te/Si(111)-(1 × 1) surface in comparison to the Si bulk. The Te layer shows a significant peak in the density of states at the Fermi energy in contrast to the Si bulk, which has a band gap centered at the Fermi energy.

~1 eV corresponding to the expected literature value. As a result, the Te/Si(111)-(1 × 1) system should be dominated by a two-dimensional conduction channel at the sample surface.

To analyze the conductivity of the Te/Si(111)-(1 × 1) surface experimentally, we use here the approach of *in situ* electrical transport measurements by means of a four-tip STM as the atomically thin Te layer would be irretrievably contaminated and altered when exposed to ambient conditions.

The lateral electrical conductivity of the Te/Si(111)-(1 × 1) surface is hereby measured by contacting the sample with the individual tips of the STM in a four-probe geometry, as described elsewhere [14,25]. This approach allows distance-dependent four-probe measurements of the freshly prepared Te/Si(111)-(1 × 1) surface with the result of the measurement shown in Fig. 4. We find that the distance-dependent four-probe resistance can be described by the analytic solution for a two-dimensional conductor. In Fig. 4 we have also indicated the expected behavior for the bulk with the given bulk resistivity of $\rho_{\text{bulk}} = 22\,\text{k}\Omega\,\text{cm}$.

In detail, for equidistant tip spacing a two-dimensional surface conductivity would result in a constant four-probe resistance when varying the tip spacing. However, in the present case we leave three of the four tips at equidistant spacing and move only one tip. The corresponding formulas for the two- and three-dimensional resistivity in this case are [13,14,26]

$$R_{2D}(x) = \frac{1}{2\pi\sigma_{2D}}\left[\ln\left(\frac{2s}{x}\right) - \ln\left(\frac{s}{x+s}\right)\right], \quad (1)$$

$$R_{3D}(x) = \frac{1}{2\pi\sigma_{\text{bulk}}}\left(\frac{1}{x} + \frac{1}{2s} - \frac{1}{x+s}\right), \quad (2)$$

with x and s as defined in the inset of Fig. 4. As evident from the formulas, the x dependence of the resulting graph for a three-dimensional bulk dominated sample is distinctly different from the two-dimensional case. Furthermore, for the present sample the expected conductivity arising from the bulk

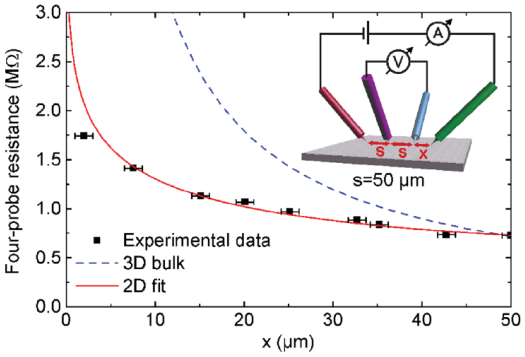

FIG. 4. Distance-dependent four-probe measurement results of Te/Si(111)-(1 × 1) and fit of the corresponding two-dimensional analytical solution (solid red line). The distance-dependent four-probe resistance expected from the pure low doped bulk ($\rho_{\text{bulk}} = 22\,\text{k}\Omega\text{cm}$) is indicated as a dashed blue line. Inset: Schematic of the measurement setup. $s = 50\ \mu$m is kept constant in the measurement while x is varied.

is much lower than the sample conductivity we measure in the experiments. Hereby, the expected bulk conductivity can be reproduced by measurements of the HF treated Si(111) sample surface, before the deposition of Te [14]. We conclude that the bulk conductivity does not play a role in the present measurements. The corresponding Te/Si(111)-(1 × 1) sheet conductivity resulting from fitting Eq. (1) to our experimental data is $\sigma_{2D}^{\text{Te}} = 2.6(5) \times 10^{-7}$ S/□. This value for the Te/Si(111)-(1 × 1) conductivity is relatively small compared to, e.g., $\sigma_{2D}^{\text{Si}} = 5.1(7) \times 10^{-6}$ S/□ of the Si(111)-(7 × 7) reconstruction [14]. This means that, in comparison to a typically even higher TSS conductivity of $\sigma_{2D}^{\text{TSS}} \approx (4-8) \times 10^{-4}$ S/□ [27,28] the Te/Si(111)-(1 × 1) interface contributes only less than 1% of the total conductivity of such a sample. This low observed conductivity at first sight contradicts the large density of states predicted from our DFT calculations. However, we find in the calculated band structure that the largest part of the density of states at the Fermi energy stems from flat bands near the $\overline{\text{M}}$ point which are expected to not contribute much to the electrical conductivity due to their low Fermi velocity [29]. On the other hand, the DFT calculations predict further metallic bands, the unexpected low conductivity of which can be explained by the relatively large surface roughness which we find experimentally. In order to validate the surface structure, we have further tested if the Te/Si(111)-(1 × 1) termination is completely developed by preparation of a sample at a temperature of 350 °C (instead of 270 °C before), where we found no significant variation of the Te/Si(111)-(1 × 1) conductivity compared to the previous measurement. From this finding we conclude that the surface reconstruction is fully developed and stable because otherwise the Te coverage and therefore surface conductivity of the sample would change due to the different equilibrium conditions during the growth.

In conclusion, we report by STEM, STM, LEED, and theoretical calculations that the saturation of an unreconstructed Si(111) substrate surface with Te results in a stable Te/Si(111)-(1 × 1) surface reconstruction. We find experimentally a relatively low electrical conductivity of the sole Te/Si(111)-(1 × 1) surface reconstruction in contrast to a high density of states at the Fermi energy predicted from our DFT calculations. This finding can be partially explained by the low Fermi velocity of the band which contributes the most to the density of states at the Fermi energy. Furthermore, we expect the relatively high surface roughness of the sample surface, due to the initial HF cleaning, to decrease the conductivity with respect to an atomically perfect Te/Si(111)-(1 × 1) layer. However, we would like to stress here that the present preparation procedure is identical to the one used prior to the actual TI film growth and we find the resulting TI films to be of excellent crystalline quality with a sharp interface to the substrate.

Besides the treatment with Te, the saturation of Si(111) substrates prior to vdW epitaxy by, e.g., Se and Bi has also been reported [27,30] and we find the conductivity of the corresponding surface terminations to be not well documented in literature. In general, such interface conduction has to be taken carefully into account not only for topological insulators such as Bi_2Te_3, Sb_2Te_3, and Bi_2Se_3 and corresponding ternary or quaternary materials but also for other vdW materials including GaSe, GaTe, MoS_2, WS_2, $MoSe_2$, WSe_2, and $MoTe_2$.

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Chapter 6 Scanning tunneling potentiometry at ultra-thin Bismuth films

6.1 Introduction

The continuous optimization of electronic devices leads to ever new material designs, e.g. in order to make transistors smaller and less power consuming. Hereby, a fundamental limit of the power consumption of a transistor is given by its on-off ratio which is limited by defects in the corresponding materials and which results in residual resistivity dipoles [65].

Considering a single defect, application of a lateral electric field which leads to a net current through the sample, leads to a scattering of mobile charge carriers at the defects and thereby to the formation of a residual resistivity dipole [65]. While resistivity dipoles can occur at defects of different dimensionalities [19, 66, 67], in general quasi-zero-dimensional defects, such as atomic vacancies, are the most difficult to control considering the application in devices [68].

The underlying mechanism of the formation of resistivity dipoles is the flow of charge carriers past the defect with some of the charge carriers are scattered at the defect. The result is an equilibrium state where and additional electric field with the shape of a dipole is superimposed on the otherwise linear voltage slope across system [19, 65]. The polarity of the superimposed electric field is counteracting the transport field and leads to a macroscopically observed increase in resistance [19, 52]. Depending on the scattering mechanism involved, the amplitude of the resulting resistivity dipoles, and therefore the increase in resistivity, varies. In the following, we differentiate between two sources of scattering at the defect [19]:

- Diffusive transport, corresponding to classical transport
- Ballistic transport, as described by quantum mechanics.

While, the evaluation of the dipole amplitude in the diffusive regime leads to a description in terms of electrostatics according to Ref. [69], the scattering of ballistic charge carriers was described by Rolf Landauer in his commendable paper in 1957 [65]. In detail, the dominant transport regime is determined by the relative size of the defect, with radius a, with respect to the mean free path of the charge carriers λ. For $\lambda \gg a$ the transport dipole is of quantum mechanical nature, and for $a \gg \lambda$ the classical limit applies. This concept is depicted schematically in Fig. 6.1. As a result, in a sample with defects of different sizes and a suitable carrier mean free path, it is possible to investigate the crossover from the classical to the quantum transport limit.

In the present work, we use Bi ultra-thin films in order to investigate the dependence of the amplitude of the resistivity dipoles as function of the defect sizes, as Bi bulk crystals are reported to have a large mean free path of up to several $100\ \mathrm{nm}$ at room temperature. Although, this value is reduced in thin films [19, 70], we find Bi films grown on Si(111) to be an excellent candidate for the rigorous study of transport around defects, not only due to the proposed large mean free path in Bi, but also due to its structural properties when grown on Si(111) resulting in a flat film with well-defined scattering centers [19]. We use scanning tunneling potentiometry

(STP) to map resistivity dipoles around defects and analyze our results with respect to different transport theories and in combination with resistor network calculations. In this way we are able to deduce an analytic function which allows us to describe the amplitude of the resistivity dipoles as a function of the defect size. Furthermore, the model allows us to determine the mean free path and the Fermi wave vector k_F of the sample under investigation.

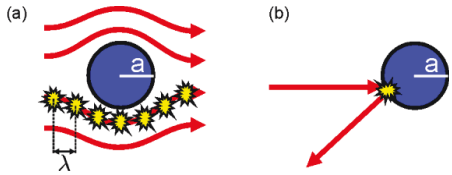

Figure 6.1. Schematic of different transport regimes at a circular defect. (a) The mean free path λ is smaller than the defect size a such that charge carriers are scattered many times as they pass the defect (diffusive transport). (b) The mean free path is much larger than the defect size, such that the charge carriers are scattered exclusively by the defect (ballistic transport).

6.2 Bismuth thin films

Depending on the deposition parameters of Bi on Si(111), a variety of Bi crystal phases can be realized [71, 72]. Below a critical thickness of ~7 ML, the deposition of Bi onto the $\mathrm{Si}(111)-(7\times7)$ surface results in the formation of a Bi{012} film in the black phosphorus phase [71, 72], in the following denoted as Bi-BP.

For the sample preparation, a $8\times4\ \mathrm{mm}^2$ piece of Si(111) ($\rho_{\mathrm{Si}}\approx700\ \Omega\mathrm{cm}$) was degassed at $T_s\approx700°\mathrm{C}$ for several hours, under ultra high vacuum (UHV) conditions, followed by repeated flash annealing cycles at 1230°C for 30 s. After each flash annealing step, the sample was quenched and left at room temperature for several minutes, until the pressure recovered close to the base pressure of $p\approx2\cdot10^{-10}$ mbar. When the pressure during the flash annealing stays below $p\leq1\cdot10^{-9}$ mbar, the sample is considered clean and is quenched to $T_s=1050°\mathrm{C}$ followed by a slow cooling to $T_s=950°\mathrm{C}$ at a rate of $\sim1\ \mathrm{K/s}$. Subsequently, the sample is quenched to $T_s=850°\mathrm{C}$ and the sample is annealed for 30 min at that temperature to form a well ordered $\mathrm{Si}(111)-(7\times7)$ surface structure, followed by a final quench to room temperature. During the sample preparation, the heating current direction was in 'step-up' direction according to the technical current direction such that the resulting $\mathrm{Si}(111)-(7\times7)$ surface shows parallel step-bunches with several-hundred-nanometer-wide, flat terraces in between [73, 74]. Subsequent measurements were performed exclusively on the terraces, where the flow of a lateral current is not influenced by any substrate steps.

One hour after the final quench, 4 ML of Bi were deposited onto the $\mathrm{Si}(111)-(7\times7)$ surface at room temperature from a Knudsen effusion cell at $T_{\mathrm{Bi}}=425°\mathrm{C}$ [75], corresponding to a rate of $1\ \mathrm{ML/min}$ at the position of the sample ($1\ \mathrm{ML}=9.28\cdot10^{14}\ \mathrm{atoms/cm}^2$) [71]. The pressure during the Bi deposition was $p\leq1\cdot10^{-9}$ mbar. The such prepared sample results in a Bi thin film which is almost uniform in thickness but not completely closed – it has holes in

it and additional islands on top. The topography of the film is shown in Fig. 6.2 (a). The holes are found to be 4 ML in depth, which means that they go all the way down to the Si substrate. We do not observe any open intermediate layers within the holes such that the first 4 ML of Bi-BP represent an ideal two-dimensional system. Islands on top of the first 4 ML correspond to an additional $1-5$ ML. A schematic of the sample geometry is shown in Fig. 6.2 (b) and the histogram of the experimental data shown in Fig. 6.2 (c).

As evident from the histogram, the peak at 1.65 nm corresponding to a film thickness of 5 ML is much smaller than the peaks corresponding to a thickness of 4 ML and 6 ML, respectively. We explain this observation by Bi-BP consisting of buckled bilayers as shown in Refs. [71, 72, 76, 77]. As a result, odd numbers of layers have dangling bonds and are therefore energetically unfavorable over even layers. As a result, under certain preparation conditions odd layers are quenched.

The different surface configurations of even and odd layers can be furthermore visualized in thermovoltage measurements, i.e. STP measurements without a lateral current flow, which is sensitive to changes in the material properties. In detail changes in the density of states and derivative of density of states according to chapter 1 of this thesis result in a contrast in thermovoltage maps. The result of such a measurement is shown in Fig. 6.3.

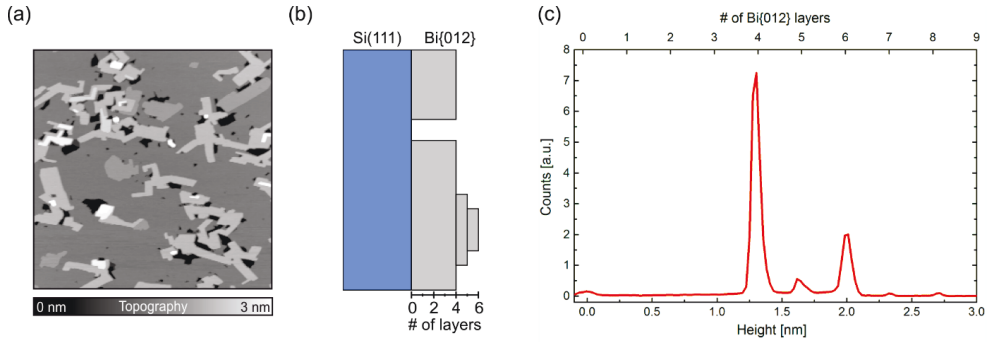

Figure 6.2. Structure of the Bi{012} thin film in the black phosphorus phase. (a) Sample topography of a ~4ML Bi{012} film in the black-phosphorus phase showing additional islands of $1-5$ ML in height and holes of 4 ML in depth going all the way down to the substrate. Scan size: 600 nm. (b) Schematic of the cross section of Bi{012} (gray) grown on a $Si(111)-(7\times7)$ substrate (blue). (c) Histogram of the topography data in (a) with the thickness given in nm and ML. The peak corresponding to a thickness of 5 ML is suppressed in agreement with literature [78].

In the topography (Fig. 6.3 (a)), we find a distribution of islands on the Bi-BP surface, but with smaller number of holes in the film and more islands compared to Fig. 6.2, resulting from the larger amount of deposited Bi (4.5 ML). The corresponding histogram of the topography in Fig. 6.3 (b) shows still a somewhat smaller peak for 5 ML island height in comparison to islands of 6 ML thickness, however not as prominent as in Fig. 6.2. The corresponding thermovoltage measurement is shown in Fig. 6.3 (c), where we observe two distinctly different areas of

thermovoltage signal throughout the sample surface. In detail, the 5 ML high islands show lower thermovoltage signal than the rest of the sample surface. We determine the difference in thermovoltage to be $\Delta V_{\mathrm{th}} = 105(2)$ µV from the histogram in Fig. 6.3 (d) and Gaussian peak fits. Looking closely, one can further find that the thermovoltage signal for 6 ML islands in comparison to the 4 ML film is approximately 20 µV higher. This finding indicates that the electronic configuration of the uppermost bilayer of the 6 ML high islands is also slightly different than in the 4 ML thick film, which is in agreement with theoretical calculations found in literature [79].

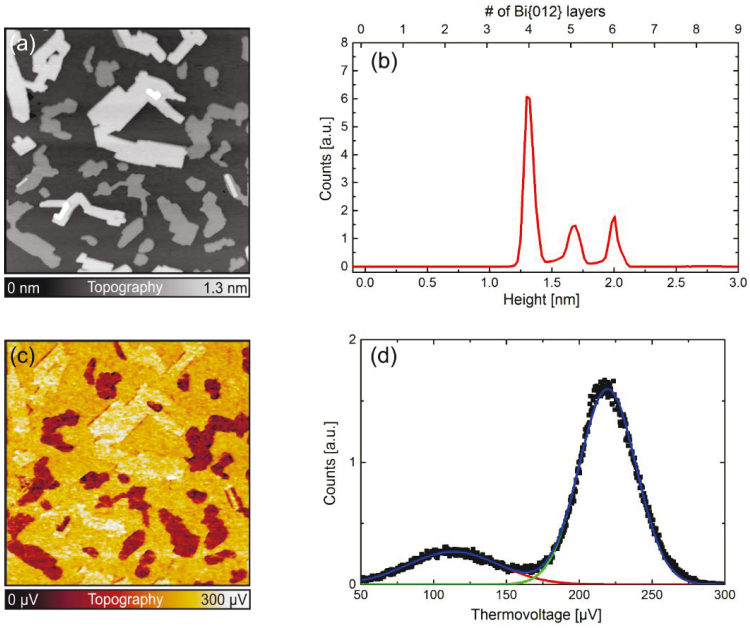

Figure 6.3. Thermovoltage measurement at the Bi{012} surface. (a) Topography of the sample surface after deposition of a 4.5 ML film. (b) Histogram of the topography in (a) showing the peak corresponding to 5 ML high islands being smaller than that corresponding to 6 ML high islands. (c) Corresponding potential map to (a) showing distinctly different potentials of surface areas corresponding to 5 ML film thickness in comparison to 4 ML and 6 ML areas. (d) Histogram of the potential map in (c) (black dots) where we determine the difference in potential between the two levels to be $\Delta V_{\mathrm{th}} = 105(2)$ µV from a multiple-Gauss curve fit (solid lines).

6.3 Resistivity Dipoles

In the classical limit, resembling diffusive charge carrier transport of a free electron gas, it can be shown that the dipole forming around a circular defect in a two-dimensional system is described by [69]

$$V_{\text{diffusive}} = -\frac{\cos(\theta)}{r} \cdot \frac{1}{2} E_0 a^2 \tag{6.1}$$

and is valid as long as $a \gg \lambda$. Here, θ is the angle with respect to the current direction, r is the distance to the defect, E_0 is the overall electric field resulting from the applied lateral voltage across the sample without defects and a is the defect radius. The resulting potential distribution around a defect is shown in Fig. 6.4.

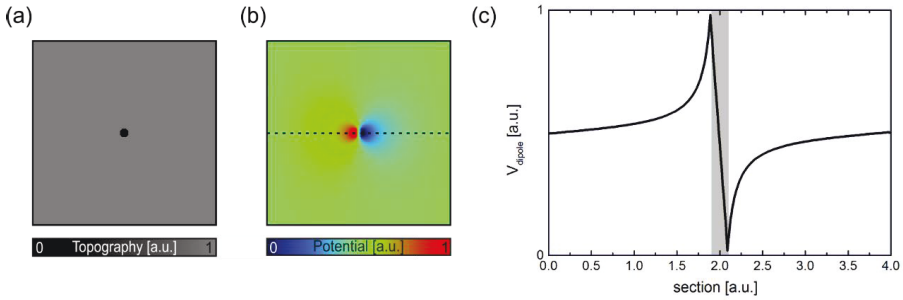

Figure 6.4. Transport dipole around a circular void defect. (a) Topography of the defect. (b) Potential map around the defect upon current flow from left to right. (c) Section of the potential map indicated in (b) by a dashed line. The position of the defect corresponding to its topography is indicated by the shaded area.

On the other hand, the quantum-mechanical Landauer dipole results in a disturbance of the electric potential around the defect according to [80]

$$V_{\text{Landauer}} = -\frac{\cos(\theta)}{r} \cdot \frac{4\hbar j}{k_F e^2} a, \tag{6.2}$$

which is valid as long as $a \ll \lambda$. Here, j is the local current density corresponding to $j = E_0/\rho_{\text{Bi}}$, where ρ_{Bi} is the sheet resistance of the Bi{012} film.

Like eq. (6.1), eq. (6.2) decays with r^{-1} outside of the defect, such that the two above sources of transport dipoles can only be distinguished experimentally by their dipole amplitude. Hereby, the Fermi wave vector k_F, and as a result also the pre-factor of the Landauer dipole $\frac{4\hbar j}{k_F e^2}$, is *a priori* unknown. As a result, the two dipole source can be only distinguished by their dependence on the defect radius a: The quantum mechanical Landauer dipole (eq. (6.2)) depends linearly on a while the diffusive transport dipole (eq. (6.1)) is proportional to a^2.

In order to characterize their size dependence, we have analyzed resistivity dipoles in a Bi thin film by means of scanning tunneling potentiometry implemented into a four-tip STM [52, 81]. Hereby, the sample surface is contacted by two of the four STM tips, injecting a lateral current of $I = 0.4$ mA at a tip distance of $d = 10$ µm. The resulting current density at the position centered between the tips, where we perform the potentiometry scan, is $j = \frac{2I}{\pi d} = 2.5$ A/m [82].

6.4 Evaluation of transport regime

Figure 6.5 shows the results of the STP measurements. The sample topography (Fig. 6.5 (a)) shows a distribution of holes of different sizes with only a small number of additional islands on top. In the corresponding potential map, we find an overall linear voltage slope and after subtraction of the linear slope a fine structure which shows dipole shaped features located corresponding to the position of the holes in the topography (Fig. 6.5 (b)).

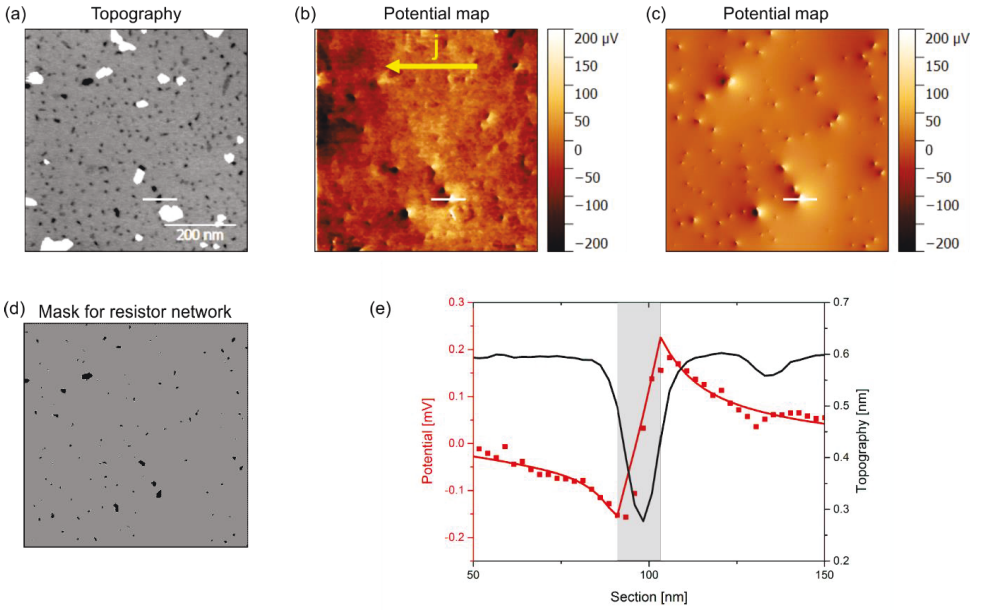

Figure 6.5. Scanning tunneling potentiometry of the Bi{012} surface. (a) Topography of the sample surface. (b) Corresponding potential map to (a) after linear background subtraction. Transport dipoles located at the voids in the sample surface are observed. (c) Result of the resistor network calculations using the mask shown in (d). (e) Sections of topography and potential data indicated in (a)-(c) as white lines. The lateral dimension of the defect is indicated as gray area.

In order to investigate the transport regime present (diffusive or ballistic), the dipole amplitude has to be analyzed as a function of the defect size. However, as evident from the topography the defects in the present sample are not circular and thus the theory given by equations (6.1) and (6.2) cannot be directly applied. In order to lift the limitation of the theoretical equations to circular defects, we present in the following resistor network calculations which allow to determine the classical transport dipole around arbitrarily shaped defects, as already demonstrated in chapter 3 of this thesis. The defect dimensions and shapes are given by a mask which we deduce from the topographic data by applying an automated void detection algorithm implemented in the open source data analysis software Gwyddion. The algorithm is set to detect regions in the topography with a height below a certain threshold. We then use the resulting

mask for the resistor network calculations by setting the resistance inside of the voids to be infinite, whereas on the terrace surrounding the defect the resistors have values according to the film resistivity ρ_{Bi}. No additional parameters are required for the calculation of the resulting potential distribution. The source code of the calculations can be found in the appendix C.1.2 of this thesis. The result of the resistor network calculation is shown in Fig. 6.5 (c) with the used mask shown in Fig. 6.5 (d). Figure 6.5 (e) shows a section of the sample topography and the corresponding measured and calculated potential at the position of a defect, indicated in the corresponding maps as white line. The lateral size of the dipole $2a = 13$ nm and the dipole amplitude $V_{\mathrm{dipole}} = 0.4$ mV are determined as the maximum voltage difference of the potential, parallel to the current direction which occurs at the boundary of the defects. For this defect, the dipole amplitude in the experiments V_{dipole} and resistor network calculation $V_{\mathrm{diffusive}}$ are in very good agreement without any fit parameters included. Thus, we conclude that the transport around this defect is in the classical transport regime.

The next step is the analysis of a several defects of different sizes with respect to their potential deviation from the expected diffusive transport behavior. Such a deviation would be an indication of a quantum mechanical contribution to the observed resistivity dipole, i.e. the Landauer dipole. However, on the one hand the fact that the holes are not circular requires a procedure which allows to map the resistivity dipole which we obtain from the resistor network calculations and experimental results to the theory of circular defects. One way to do this is the calculation of a corresponding defect size a^* which one would expect for a hole with the calculated diffusive resistivity dipole V_{dipole} after

$$a^* = \frac{V_{\mathrm{dipole}}}{E_0}.$$

To validate this analysis method, one requires e.g. to characterize holes for which one is certain that the classical transport regime applies. For such data, the size-dependent resistivity dipoles should represent the expected diffusive behavior given by eq. (6.1).

Another problem in the data analysis is that the mask extracted from the topographic data depends on the chosen threshold in the automated void detection and as a result the void size which enters the calculations varies. The reason for this is that the hole edges are not perfectly sharp in the topographic data but are somewhat rounded as evident in Fig. 6.5 (e). This effect we address mainly to the finite radius of the scanning tip. An analysis of the effect of variations in the threshold on the resulting diffusive transport data which we calculated from the resistor networks, shows that an underestimation of the actual hole size can in principle result in a spurious deviation from the diffusive transport model. To exclude the different possible error sources in the analysis of the experimental data is an ongoing task which we plan to address by additional experiments. In this way, we are confident that it is possible to extract the experimental signature of the Landauer dipole around a single hole in the sample surface, which would be the first direct experimental evidence of this effect since its prediction 70 years ago.

6.5 Conclusion

We have shown that a detailed analysis of transport dipoles at void defects can give access to different transport regimes (classical and quantum mechanical). In detail, the two regimes can be distinguished in local transport measurements by the dependence of the amplitude of the

transport dipoles as a function of the defect size. However, the detailed analysis of the dipole amplitudes with the corresponding analytic models turn out to be difficult because these theories consider only circular defects and small variations in the defect shapes and sizes can have large effects on the resulting expected dipoles. To analyze the experimentally observed resistivity dipoles we facilitate resistor network calculations, which are a versatile tool to describe the diffusive transport around arbitrary defect geometries and allows us to determine the diffusive contribution in the experimentally observed resistivity dipoles. Deviations from the expected diffusive resistivity dipoles we expect to be due to the contributions of the Landauer dipole.

While we have obtained promising results in STP experiments in Bi thin films, still some work has to be done to establish the understanding of the system under investigation and the corresponding theoretical analysis. Especially the detailed analysis of possible error sources in the data analysis is an important task. For this purpose, additional experiments such as low temperature STP measurements, where the mean free path of the charge carriers is larger, are planned. In combination with recent theoretical work [83, 84] these results could further provide a model the transition of the scattering at defects between the diffusive and quantum mechanical transport regime.

The establishment of local transport measurements in the ballistic regime opens the route for intriguing future experiments. For example, the measurement of an orifice promises the investigation of the principles of a quantum point contact in real space [85]. Furthermore, in this experiment it is predicted that the Fermi surface can be studied in real space [86, 87, 88]. In order to perform such an analysis, measurement at low temperatures are administrable, due to the increase in the carrier mean free path [19], better STP measurement resolution [81] and reduced thermal broadening.

Chapter 7 Resistor network calculations

7.1 Introduction

As evident from chapter 3 and 6 of this thesis, resistor network calculations present a powerful tool to analyze scanning tunneling potentiometry data, corresponding to a two-dimensional system. Hereby, resistor network are a simplification of the general relation of electric fields and currents by projection onto a discrete lattice, consisting of nodes which are connected with each other via resistors. The resulting set of equations, connecting potentials and currents in the system via the respective resistors corresponds to Ohm's law in matrix notation, according to

$$\boldsymbol{V} = S^{-1}\boldsymbol{I}, \tag{7.1}$$

where $\boldsymbol{V}$ is the vector of voltages, $\boldsymbol{I}$ is the vector in which the sum of incoming and outgoing currents at each node enters and S is the matrix of conductivities. Hereby, after Kirchhoff's current law $\boldsymbol{I}$ is zero everywhere in the system except where a current is injected. This method allows the calculation of the potential distribution resulting from an arbitrary distribution of resistors and has previously been used to analyze scanning tunneling potentiometry results on e.g. Ag/Si(111)$-(\sqrt{3}\times\sqrt{3})$ [16] and graphene [15, 89]. In these applications it was possible to determine the electrical conductivity of defects like steps and domain boundaries on the sample surfaces. Figure 7.1 shows the schematic of a basic two-dimensional resistor network with $n \times m$ nodes.

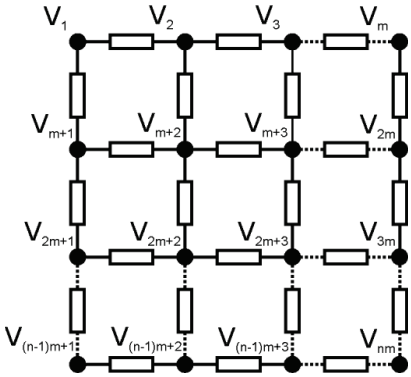

Figure 7.1. Schematic of a resistor network with $n \times m$ nodes.

While in these reports the potential maps are calculated from given arrangements of resistors after eq. (7.1) and then compared to the experimental results, it is also under certain circumstances possible to directly calculate a resistor distribution from a given potential map, the so called 'inverse problem'. The limitation hereby is that the corresponding equation system is in general underdetermined, such that finding a unique solution generally requires certain additional conditions. In detail, the problem in solving eq. (7.1) with respect to S stems from the larger number of unknown resistors in comparison to the number of nodes with given

voltages. In detail, a system with $n \times n$ nodes has $2n^2 - n$ unknown resistors (without considering the boundaries).

In this chapter, first the mathematical concept of the resistor network is introduced in detail. Subsequently, the inverse conductivity problem is discussed and different possibilities which allow to find a unique solution to the problem are presented.

7.2 Forward direction

The resistance between two neighboring nodes V_q and $V_{q'}$ $\{q \in n \times m\}$ is $R_{q\,q'}$ with a corresponding conductance $S_{q,q'} = 1/R_{q,q'} = S_{q',q}$. As a result, at each node the incoming and outgoing currents are

- $I_{q-1,q} = (V_{q-1} - V_q)S_{q-1,q}$
- $I_{q+1,q} = (V_{q+1} - V_q)S_{q+1,q}$
- $I_{q-m,q} = (V_{q-m} - V_q)S_{q-m,q}$
- $I_{q+m,q} = (V_{q+m} - V_q)S_{q+m,q}$

After Kirchhoff's current law it holds

$$I_{q-1,q} + I_{q+1,q} + I_{q-m,q} + I_{q+m,q} = I_q = 0\ \text{A}$$

corresponding to

$$(V_{q-1} - V_q)S_{q-1,q} + (V_{q+1} - V_q)S_{q+1,q} + (V_{q-m} - V_q)S_{q-m,q} + (V_{q+m} - V_q)S_{q+m,q} = 0\ \text{A}$$

which in matrix notation is

$$S\,\boldsymbol{V} = \boldsymbol{I} = \boldsymbol{0} \tag{7.2}$$

corresponds to Ohm's law. Hereby, S is a sparse matrix with less than $4mn$ finite entries and the respective matrix dimensions in eq. (7.2) are as follows:

$$\dim(S) = (\text{mn})^2$$

$$\dim(\boldsymbol{V}) = \text{mn}$$

$$\dim(\boldsymbol{I}) = \text{mn}$$

Note that Kirchhoff's law is only valid in the interior of the resistor network. If we would not allow any current to flow in or out of our resistor network, the result will only be a trivial solution of the system which has a constant potential at all nodes of the network as results. Therefore, at the boundary of the resistor network we allow finite currents to occur, typically on one side of the network incoming and on the opposite side outgoing. Hereby, the number of nodes where the current is injected is arbitrary but is typically one of two cases: A single node, corresponding to a point contact, or an entire side of the resistor network, corresponding to a parallel current flow. In either case, the sum of all incoming and outgoing currents has to vanish, according to Kirchhoff's law.

7.2.1 3 × 3 Resistor Network

As an example, in the following the calculation of an 3 × 3 resistor network (Fig. 7.2) is demonstrated, where we will consider a current of $I = 1$ A to be injected at the node 1 and drained at node 9.

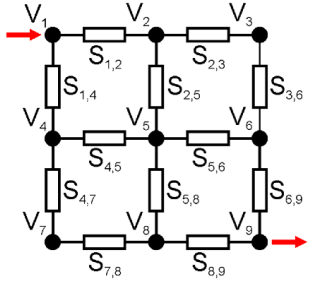

Figure 7.2 A 3 × 3 resistor network. A current $I = 1$ A is injected at node 1 and drained at node 9, as indicated by the red arrows.

Equation (7.2) in this example is

$$\begin{pmatrix} -S_{1,2}-S_{1,4} & S_{1,2} & 0 & S_{1,4} & 0 & 0 & 0 & 0 & 0 \\ S_{1,2} & -S_{1,2}-S_{2,3}-S_{2,5} & S_{2,3} & 0 & S_{2,5} & 0 & 0 & 0 & 0 \\ 0 & S_{2,3} & -S_{2,3}-S_{3,6} & 0 & 0 & S_{3,6} & 0 & 0 & 0 \\ S_{1,4} & 0 & 0 & -S_{1,4}-S_{4,5}-S_{4,7} & S_{4,5} & 0 & S_{4,7} & 0 & 0 \\ 0 & S_{2,5} & 0 & S_{45} & -S_{2,5}-S_{4,5}-S_{5,6}-S_{5,8} & S_{5,6} & 0 & S_{5,8} & 0 \\ 0 & 0 & S_{3,6} & 0 & S_{5,6} & -S_{3,6}-S_{5,6}-S_{6,9} & 0 & 0 & S_{6,9} \\ 0 & 0 & 0 & S_{4,7} & 0 & 0 & -S_{4,7}-S_{7,8} & S_{7,8} & 0 \\ 0 & 0 & 0 & 0 & S_{5,8} & 0 & S_{7,8} & -S_{5,8}-S_{7,8}-S_{8,9} & S_{8,9} \\ 0 & 0 & 0 & 0 & 0 & S_{6,9} & 0 & S_{8,9} & -S_{6,9}-S_{8,9} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \\ V_8 \\ V_9 \end{pmatrix} = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -1 \end{pmatrix}.$$

Note how in the sparse matrix the individual conductivities appear at the position in the matrix according to their numeration, e.g. $S_{2,5}$ is in row 2, column 5 of the matrix. On the diagonal the sum of the adjacent conductivities to that respective node are entered with negative sign. As a result, each line and each row of the matrix adds up to zero, which corresponds again to Kirchhoff's law. The voltage distribution resulting for this system is readily found by entering the corresponding values of $S_{q,q'}$ into the matrix, inverting it numerically and calculating the right side of the equation system according to eq. (7.1). The result for all resistors of conductivity $S_{q,q'} = \frac{3}{2}\ \Omega^{-1}$ is shown in Fig. 7.3

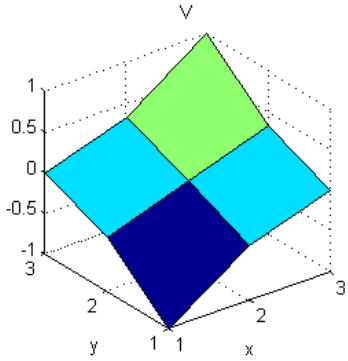

Figure 7.3. Voltage drop across the 3 × 3 resistor network resulting from the system shown in Fig. 7.2 with $S_{q,q'} = \frac{3}{2}\Omega^{-1}$.

7.2.2 Resistor network with quasi-one-dimensional defects

The application of the above scheme for larger resistor networks and with resistor distributions corresponding to a current flow around circular defects was shown in chapter 3 and 6 of this thesis. However, one can also calculate the potential distributions resulting from quasi-one-dimensional defects corresponding to e.g. steps on a sample surface [16]. An example of the voltage drop at a corresponding test structure, in this case a step which results in an increased resistance along a line with a bulge, is given in Fig. 7.4 (a). From this resistor network one can further extract the local current in the two spatial dimensions j_x and j_y, the local absolute current $j_{\mathrm{abs}} = \sqrt{j_x^2 + j_y^2}$ and the local current direction $\omega = \arctan(j_y/j_x)$ which are shown in Fig. 7.4 (b)-(e). This makes resistor network a powerful tool for the analysis of coresponding experimental data, as these quantities are typically not directly accessible otherwise.

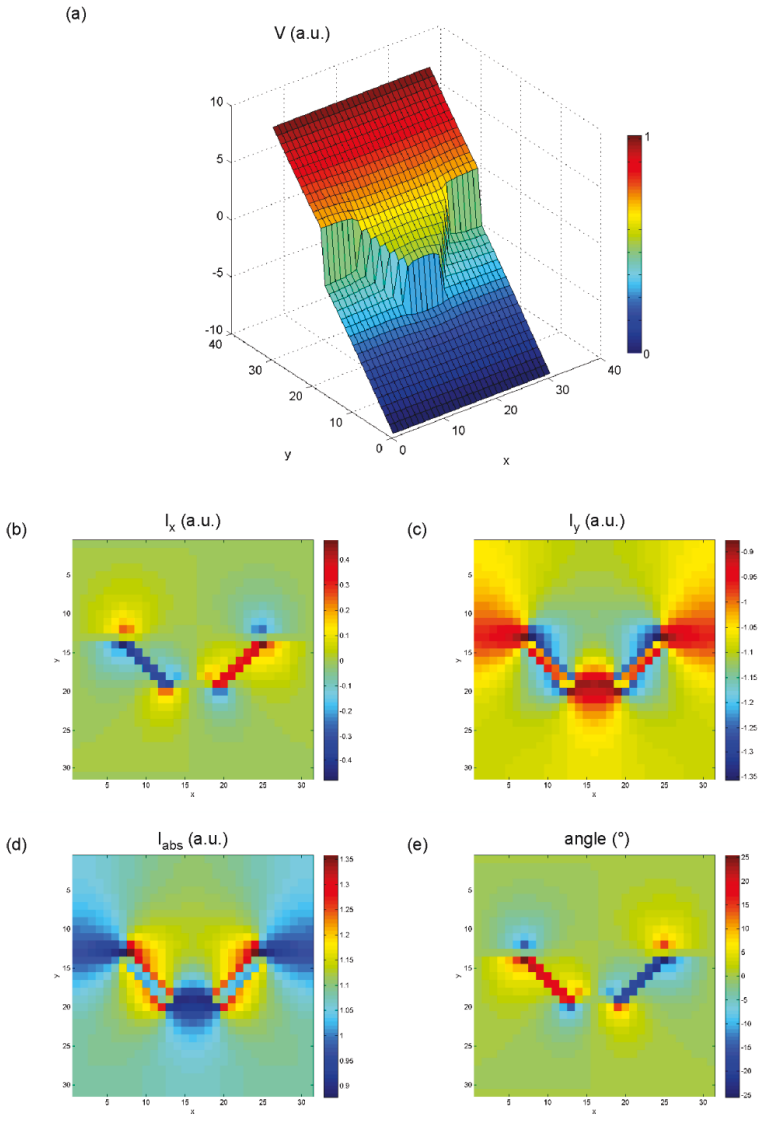

Figure 7.4. Resistor network calculation at a quasi-one-dimensional defect. (a) Surface plot of the resulting potential distribution corresponding to a step edge with a bulge. (b) Local current in x-direction. (c) Local current in y-direction. (d) Absolute current distribution. (e) Local current direction.

7.3 Inverse conductivity problem

After demonstrating the 'forward direction' of calculations with resistor network in chapter 7.2, we turn now to the inverse conductivity problem. Hereby, not the conductivities of the resistor

network are given but the voltages at the nodal points. For addressing this problem, we need to rewrite eq. (7.1):

$$V\,\boldsymbol{S} = \boldsymbol{I} \tag{7.3}$$

Namely, $\boldsymbol{S}$ is now the vector of unknown conductivities and V is the matrix where we enter the known node potentials. The problem can then be solved by inverting V, such that

$$\boldsymbol{S} = V^{-1}\boldsymbol{I}.$$

The problem hereby is, as mentioned before, that due to the underdetermined system, the inverse of V is generally not unique. Graphically speaking, after entering all the equations we receive from applying Kirchhoff's current law to the system, the matrix V has more columns than it has rows. In order to make the system uniquely solvable, there are two possibilities:

- Decrease the number of unknown parameters by putting further restrictions on the system, e.g. by fixing some of the conductivities,
- Increase the number of linearly independent equations which describe the system, e.g. by additional measurements.

In general, the stronger the restrictions on the system are, the easier it is to solve. For example, using the symmetry of a two-dimensional system to reduce it to a one-dimensional problem results in a system which can be readily solved as demonstrated e.g. in Ref. [90]. However, in order to keep the solution as general as possible, the smallest possible amount of restrictions should be put on the system. In this way, instead of introducing further conditions, here it is possible to find a unique solution for the problem without further restrictions, by combining two measurements of the same system [91].

In detail, one needs to record another set of voltages V which fulfil eq. (7.3) with the same set of conductivities $\boldsymbol{S}$. Experimentally speaking, this corresponds to another measurement of the same sample area. However, because to get additional information about the system, this additional set of equations must be linearly independent from the first set of equations. This means that multiple measurements with the same current direction, with different absolute amount of current, will not give additional information about the underlying set of conductivities. Instead, one requires a measurement at a different current direction through the sample under investigation. In principle, the relation of the current directions is arbitrary as long as they are not identical, however, experimentally it makes sense to choose perpendicular current directions in order to minimize the overlap of the two data sets. Furthermore, in two dimensions additional data sets beyond two current directions, again will not add new information about the system because all current directions can be written as a linear combination of the first two. Additional measurements of linearly dependent data sets will therefore only decrease statistical measurement errors, which is however typically better done by fewer but therefore more precise measurements.

Below we present the corresponding MATLAB script, which performs the calculation of a conductivity map from two previously simulated potential maps of perpendicular overall current direction. The script is applied to two different problems:

- A conductivity profile originally proposed by Wang *et al.* [91], corresponding to e.g. an island on a thin film.

- A quasi-one-dimensional defect corresponding to e.g. a step edge on a Si(111) surface.

7.3.1 Island

In this example the conductivity distribution given by the formula [91]

$$\sigma(x,y) = \sigma_0[1 + 5\exp(-(x-y)^2 - 2(x+y)^2) + 3\exp(-3(x-1)^2 - (y+1)^2)]^{-1}.$$

Hereby, for $\sigma_0 = 1$ the conductivity is approximately 1 everywhere on the boundary of the test system, resembling a somewhat circular shaped defect. Perpendicular current directions through the system result in the potential distributions shown in Fig. 7.5 (a) and (b), respectively. The corresponding solution of the inverse conductivity problem is shown in Fig. 7.5 (c) and (d). We find that the initial resistivity profile of the system is very well reproduced from the potential data.

The analysis of the present resistivity profile corresponds to e.g. an island on a 4 ML film of Bi-BP, as shown in chapter 6 of this thesis. In the area of the island the resistivity of the sample is expected to be lower due to the larger film thickness there. Hereby, the decrease in resistivity is expected not to be instantaneous at the edge of the island, but will be smeared out to the inside because the current requires some distance to redistribute into the additional layer on top of the film. Corresponding experimental data would therefore be of great interest to test the present numerical analysis method and allow to determine the influence of additional layers on a thin film on its conductivity. Such an analysis would also enable to determine possible surface state contributions to the conduction through the thin film, if presents.

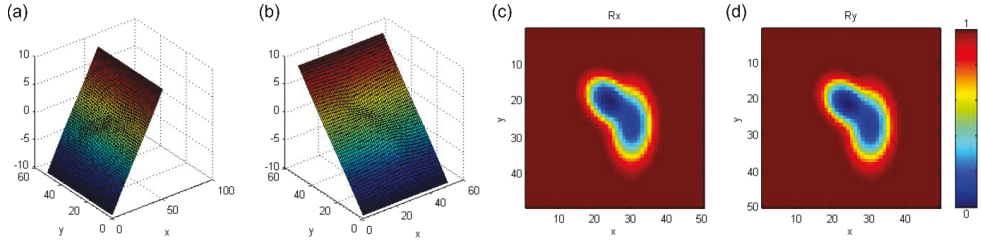

Figure 7.5. Inverse conductivity problem calculated for an island on a thin film. Input potential maps for one current direction (a) and the second current direction (b). Resulting maps of the resistivity in (c) x-direction and (d) y-direction.

7.3.2 Quasi-one-dimensional defect

In the case of the quasi-one-dimensional problem embedded in a two-dimensional matrix, one finds generally two points where the area of increased resistance collides with the boundary of the system. As a result, when considering multiple current directions at some point the node at the boundary where resistors of high resistance are connected will act as a current source. The problem hereby is, that assuming a constant current density at the boundary will result in an unphysical much larger voltage drop at the position of the defect which disturbs the system.

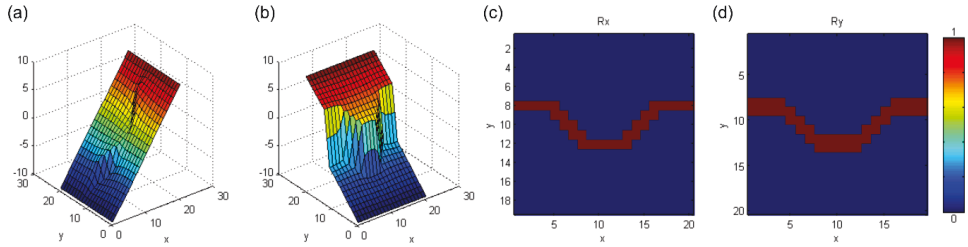

Figure 7.6. Inverse conductivity problem calculated for a quasi-one-dimensional defect. (a) Input potential maps for one current direction and (b) the second current direction (b). Resulting maps of the conductivity in (c) x-direction and (d) y-direction.

A solution for this problem is to scale an incoming current density j at each node according to the resistance connected to it. This process introduces a minimal boundary condition: No change in conductivity perpendicular to boundary where the quasi-one-dimensional defect meets the boundary within first two pixels perpendicular to the boundary. The resulting solution of the inverse conductivity problem is shown in Fig. 7.6. We find that the quasi-one-dimensional defect is very well reproduced from the potential data.

7.3.3 Calculation speed

For convenience, we have also tested the implemented code speed with the resulting computation time as function of the system size plotted in Fig. 7.7. Here, an exponential increase of calculation time is observed with a 100×100 pixel system taking approximately 23 min for calculation on a standard desktop PC.

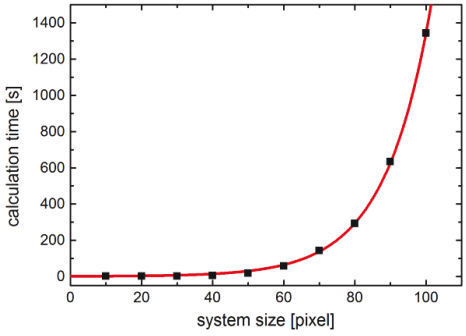

Figure 7.7. Calculation time of the MATLAB code to solve the inverse problem as a function of the system size (black dots) with exponential fit (red line).

7.3.4 Effect of noise on the inverse conductivity calculation

While extracting the distribution of conductivities works nicely in theory as shown above, measurement errors in real experiments turn out to be a critical parameter when trying to solve the inverse problem for experimental STP data. For this reason, the application of the above

calculations to real experiments was not successful up to this point. The reaction of the calculations upon errors in the measurement data can be determined by the so-called condition number of the matrix V [92] which is defined as

$$\kappa(V) = ||V|| \cdot ||V^{-1}||.$$

The condition number gives an estimate of the maximum error in the vector S when the measurements in V are subjected to errors. In mathematical terms: Be $||e||$ the error of the exact solution $||S||$ for eq. (7.3). Then for errors in the matrix V, with $\tilde{\boldsymbol{S}}$ an approximate solution for the disturbed matrix $\tilde{V}$, meaning

$$\tilde{V}\tilde{\boldsymbol{S}} = \boldsymbol{I},$$

the relative error of the solution is

$$\frac{||\boldsymbol{e}||}{||\boldsymbol{S}||} = \kappa(V)\frac{||V - \tilde{V}||}{||V||} + \mathrm{O}\left(||V - \tilde{V}||^2\right),$$

for $||V - \tilde{V}|| \to 0$ [93]. Simply speaking, for an ideal system $\kappa(V) = 1$, which means that the relative error in the solution equals the relative error in the data [93]. Hereby, the condition number can be interpreted as a factor by which the relative error in the measurement is scaled with respect to the final result.

In order to optimize the solution of the inverse conductivity problem one should therefore minimize the condition of the respective matrix, which however varies for different problems and therefore sets of equations. For example, for systems like the Ag/Si(111)$-(\sqrt{3} \times \sqrt{3})$ surface reconstruction, where the resistivity of the sample surface is dominated by step edges the voltage slope across the terraces is very small. In such systems, small amounts of noise in the measured potential maps lead to large variations in the local potential slope and therefore typically result in large relative errors when trying to compute the corresponding conductivity on the terraces.

Furthermore, V is typically non-square as a result of the structure of the resistor network. In this case, the inverse matrix V^{-1} can be determined by a singular value decomposition

$$V = A\Sigma B^*$$

$$\Leftrightarrow\ V^{-1} = B\Sigma^{-1}A^*,$$

where Σ is a diagonal matrix with its diagonal elements being the singular values of V [94]. The singular value matrix Σ has the same condition as V and A and B are unitary matrices, meaning that the inverse of A and B is equal to their conjugate transpose A^* and B^*, which makes the calculation of the inverse of V and therefore also its condition easy.

Below we show the effect of noise in the measurement data on the resulting conductivity distribution by introducing an artificial relative noise of 1% rms on the voltage maps in the test system from chapter 7.3.1. The resulting noise in the calculated conductivity is 15% rms with respect to the conductivity resulting from the voltage data without noise added on top. The results of this calculation are shown in Fig. 7.8. Hereby, the system size is 21×21 nodes and $cond(V) \approx 35$.

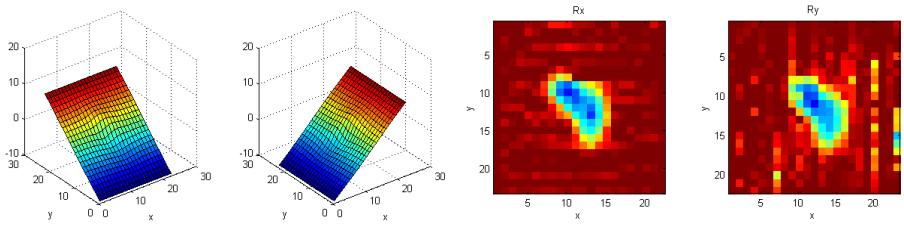

Figure 7.8. Conductivity distribution resulting from 1% rms noise in the voltage data. (a) and (b) input voltage data with added 1% rms on top of the data. System size 21×21 nodes. (c) and (d) resulting conductivity distributions from (a) and (b). The noise level is 15% rms with respect to the result from the voltage data without noise.

In order to enhance the noise performance of the inverse conductivity calculation, without putting further restrictions on the system, the condition of the matrix V should be enhanced. To do so, there are different methods reported in literature, such as the Tikhonov regularization which can in principle be readily applied in terms of the singular value matrix [95]. These optimizations of the present work are planned for the near future with the ultimate goal of a successful application on experimental data. The present calculation method is of great interest for the application to STP data, because it allows to deduce unprecedented information directly from the experimental data.

7.4 Conclusion

Resistor network calculations are a versatile tool when it comes to the analysis of locally resolved transport measurements of nanostructures. In detail, they can provide a toolset to overcome the problem that potential maps along are *a priori* not sufficient to determine the exact current paths in the sample under investigation. However, by fitting a resistor network with the corresponding geometry to the experimental data one can deduce local current direction and amplitudes. By such an analysis different kinds of defect geometries can be analyzed with great detail, providing important information about the sample material properties. The successful application of the technique was demonstrated in chapter 3 of this thesis.

An ultimate goal would be the direct calculation of the resistivity profile throughout the sample from voltage maps, acquired by STP experiments, by inverse conductivity calculations. For the application of the inverse method to experimental data Bi thin films on Si(111) would be a promising system. In this sample, under the correct preparation procedure [42], highly conducting domains can be embedded in an otherwise low conducting film and vice versa. Furthermore, Bi thin films have proven to be excellent candidates to perform STP measurements due to high measurement resolution and good contact stability with the current injecting tips.

As a further outlook, higher-dimensional resistor networks are possible to implement in the same way as presented here. Just to name one example of a possible application: A three-dimensional resistor network allows to calculate the potential distribution at the sample surface for a defect which is buried underneath. While details will not be discussed here, the code

required for calculations in three-dimensional resistor networks can also be found in the appendix.

All MATLAB codes for the calculations shown in this thesis can be found in appendix C.

Chapter 8 Conclusion and Outlook

As shown in this thesis, *in situ* transport measurements by STP are a powerful tool which allows the characterization of samples, e.g. epitaxial thin films, with unprecedented spatial and potential resolution. By only changing the software of the electronic controller, we reported here the successful implementation of STP into a four-tip STM setup. As a result, a corresponding 'upgrade' of similar experimental setups can be performed in a very simple and cost-efficient way.

Based on this technique we have further developed a four-probe measurement method where all the contacts required to perform a multi-probe measurement can be held in tunneling contact. This novel measurement technique enables truly non-invasive *in situ* transport measurements, which are of interest especially for fragile samples, e.g. surface terminations of reconstructed semiconductor surface. This technique is furthermore promising for applications in electronics industry, e.g. to control products between individual processing steps without damaging them. For this reason, we have filed the application for a corresponding patent.

A major advantage of the resulting experimental setup compared to traditional approaches are the possibility of *in situ* combination of different surface analysis tools such as LEED and ARPES. Hereby, the general limitation of comparability between *in situ* spectroscopic measurements and *ex situ* transport measurements, due to the altering of samples under ambient condition and lithography steps can be overcome.

This approach is applied to topological insulator thin films, where we performed STP in combination with ARPES to get a thorough understanding of the conductance through the film under investigation, as shown in chapter 3 of the thesis. In detail, by performing ARPES we are able to determine the filling level of the TSS on the top of the sample which is an important factor in the corresponding transport measurements, because in this way we are able to identify the fraction of the current transmitted by the TSS on the top surface of the thin film, which is important to analyze the STP data. Furthermore, spin-polarized ARPES measurements ensure that the surface state inherits the spin-momentum locking expected for a topological insulator. When performing STP measurements we find three different kinds of defects to result in a local voltage drop: Step edges, domain boundaries and void defects. Hereby, we find the resistance of the domain boundaries to be almost four times larger than that of the step edges and thereby the dominant defect induced contribution to the transport. The resistance of void defects we determined by use of resistor network calculation where we find their contribution to the overall resistance to be small compared to the other defects. In total, the defects make up 44% of the total voltage drop across the sample. The remaining 56% occur on the flat terraces and are attributed to electron-phonon scattering and defects below the resolution of our transport experiments.

In general, it is important to analyze all the conduction channels with respect to their contribution to the overall conduction through the sample. Such a detailed analysis we presented in chapter 4 of the thesis, where we used again a full *in situ* approach and combine ARPES and transport measurements on a TI thin film. For the transport measurements we facilitated a newly developed sample design which enables gating of the sample while performing transport measurements. The results of these measurements we analyze with respect to a model we developed and which in combination with the ARPES results allows us to deduce transport properties of the individual transport channels in the TI film, such as carrier concentrations with

and without gating as well as the carrier mobilities in the two TSS channels. In this context we have performed band bending calculations, from which we find that due to the high dielectric constant in the TI film and the presence of two surfaces, in which the position of the bands relative to the Fermi energy depends on the filling of the Dirac cones, the bands throughout the film are rather flat. To calculate the effect of the application of a gate voltage on the TSS channel at the top and bottom of the film in unprecedented detail, we have further performed calculations based on a gating model which includes the quantum capacitance of the TSS, which results due to the respective low density of states, and the coupling between the top and bottom surface state. Analyzing the gate dependent transport data with this model gives us a conclusive picture of the transport properties in these TI thin films.

We have further analyzed another transport channel of TI thin film samples which is formed at the substrate interface during the epitaxial growth of the films. In detail, we have shown by a combination of STEM, LEED and DFT calculations that the Te passivation of the Si(111) substrate results in a Te/Si(111)$-(1 \times 1)$ termination of the substrate as shown in chapter 5 of the thesis. Due to the Te atoms forming one bond to the directly underlying Si atom, an a priori net positive charge, corresponding to a two-dimensional hole-gas is expected to be present at the substrate surface. This consideration is reflected in a metallic band structure as determined from DFT calculations. Preparation of the sole Te/Si(111)$-(1 \times 1)$ substrate termination and analysis by *in situ* distance dependent transport measurements in the four-tip STM results in a conductivity which is relatively low compared to the typical conductivity of the TSS transport channels, despite the predicted metallic bands. We explain this finding by the relatively high surface roughness which we observe in STM measurements and which is the result of an initial HF etching procedure of the sample substrate. Nevertheless, the TI films grown on the substrate are very smooth and of high crystalline quality.

As shown in chapter 6 of the thesis it is possible to further disentangle classical transport and quantum mechanical transport in a sample by measurement of void defects of different sizes. To do so we performed STP measurements on Bi ultra-thin films, which host naturally such defects with a variety of sizes. A lateral current through the sample then results in the formation of resistivity dipoles at the defects, their amplitude depends on the transport regime at the respective defect – classical transport if the defect size is larger than the carrier mean free path and quantum mechanical when the defect size is smaller than the mean free path. In this way we are able to characterize the transition between the two transport regimes by measurement different sizes of defects. This furthermore allows us to extract parameters like the mean free path and k_{F} from the measurements.

For the detailed analysis of the size dependent resistivity dipoles, resistor network calculations are an important tool because a previous analytic theory only considers circular defects and variations in the defect shape can result in significant changes in the respective dipole amplitudes.

Chapter 7 of the thesis documents the basic principle of the resistor network calculations used throughout the thesis, which is based on Kirchhoff's current law and results in a linear equation system. As a result, it is possible to calculate the potential distribution resulting from an arbitrary distribution of resistances in a system under flow of a current in up to three-dimensions. The resulting potential distributions can be compared to transport measurements and pose an important tool for the understanding and analysis of experimental transport data as evident in chapter 3 and 6 of the thesis. While the calculation of a potential distribution from a given set of resistors and a current is relatively straight forward, it only allows to fit

experimental data by adjusting the resistor distribution and then comparing the resulting potentials to those observed in the experiments. More convenient would be the straight-forward determination of the sample resistivity from a given potential distribution – the so called inverse conductivity problem.

The aim of the inverse conductivity problem is to determine the distribution of resistances in a structure under investigation only from the potentials measured at its surface which, without constraining the system, results in an underdetermined problem. Our approach to solve this problem for a two-dimensional resistor network is the measurement of the same resistor distribution under two different, ideally perpendicular, current directions which gives enough information to solve the corresponding linear equation system. While we have proven that this procedure works in theory, it is susceptible to noise in the potential data sets, which quickly leads to a divergence of the solution and thereby to unphysical results. To address this problem, it is planned to condition the equation system such that noise will have less influence on the solution. After that, the application of the procedure to experimental data, e.g. from STP measurements of Bi thin films on Si(111) in planned.

Plans for future *in situ* transport studies include the utilization of a low-temperature four-tip STM which will be operational soon and allows to perform four-probe measurements and STP at a temperature of down to 4 K. The low temperatures freeze out bulk charge carriers in semiconductor substrates as well as the interior of TI samples, reducing drastically their impact in transport measurements. In this way the transport properties of interest will be better accessible allowing even more detailed studies of their properties. In detail, the phonon scattering at low temperatures is much lower than at room temperature, leading to increase mean free path of the charge carriers, giving better access to quantum mechanical effects. To determine e.g. the Fermi wave vector k_F by studying the size dependent residual resistivity dipoles would therefore be much easier. Furthermore, low temperatures generally result in a more stable system concerning the drift of the STM units but also the stability of the tunneling tips and the achievable energy resolution. As a result, on the one hand spatially more precise measurements can be realized (smaller scan areas, slower scan speed) and much sharper spectroscopic features can be analyzed e.g. in tunneling spectroscopy due to the Fermi distribution in tip and sample being much narrower as at room temperature. Concerning the STP measurements, the low temperature results in a decrease in the noise of the measured voltage, which enhances the potential resolution even further.

The low temperature four-tip STM setup contains also a magnet, which allows application of a magnetic field perpendicular to the sample plane of up to 8 T. In this way it will be possible to cover the full spectrum of magneto-transport measurements under UHV conditions, including measurements of the Hall effect, weak (anti-)localization, Shubnikov-de-Haas oscillations and many more. In STP measurements, the combination of large mean-free paths and magnetic fields should further lead to the opportunity to directly observe spatial variations at the sample surface due to the Aharonov-Bohm effect.

Chapter 9 List of Publications

9.1 Resulting from the present thesis

The numbering is according to the chapters of this thesis from which the publications result, respectively.

1. **F. Lüpke**, S. Korte, V. Cherepanov, and B. Voigtländer, Scanning tunneling potentiometry implemented into a multi-tip setup by software. *Rev. Sci. Instr.* 86, 123701 (2015)

2. **F. Lüpke**, D. Cuma, S. Korte, V. Cherepanov, and B. Voigtländer, Four-probe measurements using current probes with voltage feedback to measure electric potentials. Submitted to *Journal of Physics: Condensed Matter*

   F. Lüpke and B. Voigtländer, Verfahren und Vorrichtung zur Bestimmung des elektrischen Widerstandes eines Objektes, Deutsches Patent, Nummer 102017007578.6

3. **F. Lüpke**, M. Eschbach, T. Heider, M. Lanius, P. Schüffelgen, D. Rosenbach, N. von den Driesch, V. Cherepanov, G. Mussler, L. Plucinski, D. Grützmacher, C. M. Schneider, and B. Voigtländer, Electrical resistance of individual defects at a topological insulator surface. *Nat. Commun.* 8, 15704 (2017)

4. **F. Lüpke**, S. Just, M. Eschbach, T. Heider, E. Młyńczak, M. Lanius, P. Schüffelgen, D. Rosenbach, N. von den Driesch, V. Cherepanov, G. Mussler, L. Plucinski, D. Grützmacher, C. M. Schneider, F.S. Tautz, and B. Voigtländer, Disentangling *in situ* top and bottom surface state transport of a topological insulator ultra-thin film by gating. Submitted to *Nano Letters*

5. **F. Lüpke**, S. Just, G. Bihlmayer, M. Lanius, M. Luysberg, J. J. Doležal, E. Neumann, V. Cherepanov, I. Ošt'ádal, G. Mussler, D. Grützmacher, and B. Voigtländer, Chalcogenide based van der Waals epitaxy: Interface conductivity of Tellurium on Si(111), *Phys. Rev. B* 96, 035301 (2017)

6. **F. Lüpke**, D. Cuma, S. Korte, V. Cherepanov, and B. Voigtländer, Crossover from quantum to classical transport imaged in real space. In preparation.

9.2 Others

- **F. Lüpke**, S. Manni, S. C. Erwin, I. I. Mazin, P. Gegenwart, and M. Wenderoth. Highly unconventional surface reconstruction of Na_2IrO_3 with persistent energy gap. *Phys. Rev. B* 91, 041405(R) (2015)

- T. Druga, M. Wenderoth, **F. Lüpke**, and R. G. Ulbrich, Graphene-metal contact resistivity on semi-insulating 6H-SiC(0001) measured with Kelvin probe force microscopy *Appl. Phys. Lett.* 103, 051601 (2013)

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Appendix A Createc box startup via ethernet connection

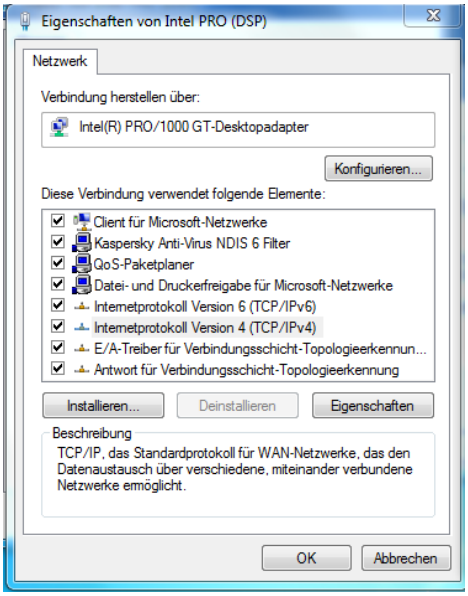
The new electronics is based on the new TMS320C6657 DSP from TI. Communication between the PC and the electronics is based on a Gigabit Ethernet connection. It is expected that the PC is running the 64bit Version of Windows 7. In the standard configuration the software running on the DSP board is loaded from the PC after startup of the electronics. It is therefore necessary to install a TFTP and DHCP Server on the PC.

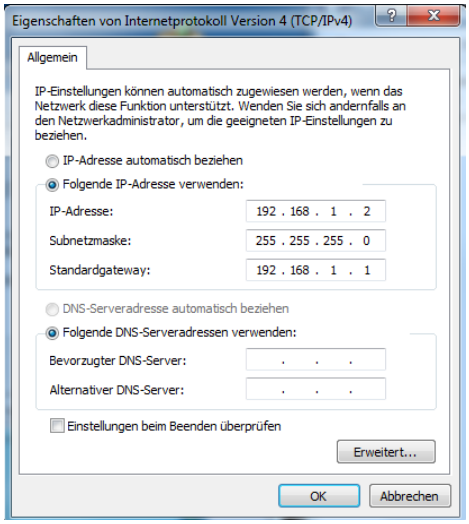
In more detail: Install an Ethernet adapter in the host PC, which is dedicated to communication with the Electronics. A Gigabit Ethernet switch is needed between the electronics and the PC. Disconnect or deactivate all other network connections during the installation process. The address of this adapter has to be 192.168.1.2. Subnet Mask: 255.255.255.0 Gateway 192.168.1.1 (see images below). A suitable TFTP and DHCP Server is TFTPD64. A suitable '.ini' file will be supplied to the DSP as below: The name file downloaded is C6657le.bin (rename it if it has a different name) and has to be located in the current directory of TFTP64 (see image). Start TFTP64 using the settings given in the Graphs below first, then start the electronics. After a few seconds the DSP downloads the '.ini' file resulting in the log viewer to respond as shown in the image below. After a successful boot the new electronics appears with address 192.168.1.102. Test it by using "ping 192.168.1.102" in the windows command window. Then you can finally start the PSTMAFM program on the PC. In the initialization you have to select hardware 5:C6657 save and restart the program.

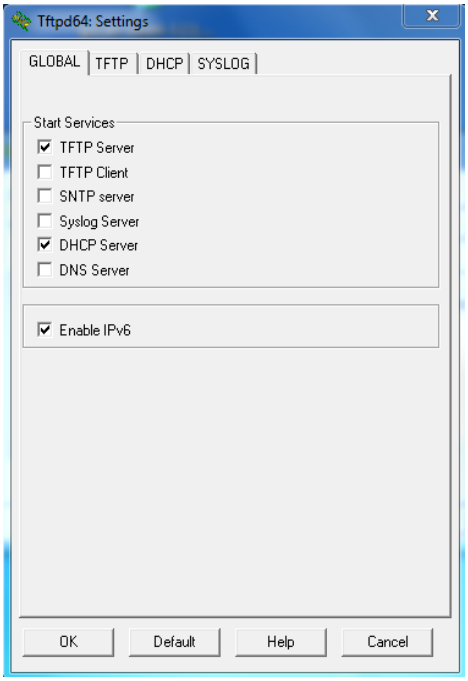
If the boot is successful the STMAFM.log file should read

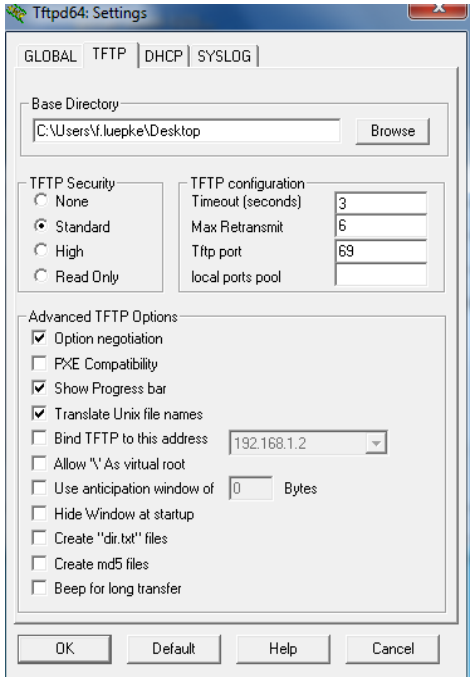
```
09.04.2014 10:35:23: Start STMAFM_Init
09.04.2014 10:35:23: Enter DSPInit
09.04.2014 10:35:23: Flashboot is false
09.04.2014 10:35:23: C6657 Boot Start
09.04.2014 10:35:23: Leave dspinit
09.04.2014 10:35:23: Check pc32addamode
09.04.2014 10:35:23: Create Registry file
09.04.2014 10:35:24: Registry Access finished
09.04.2014 10:35:24: Open STMAFM.cfg
09.04.2014 10:35:24: Close STMAFM.cfg
09.04.2014 10:35:24: Check Ramp Slider
09.04.2014 10:35:24: Set FBControl
09.04.2014 10:35:24: Open Datalogger
09.04.2014 10:35:24: Finish stmafminit
```

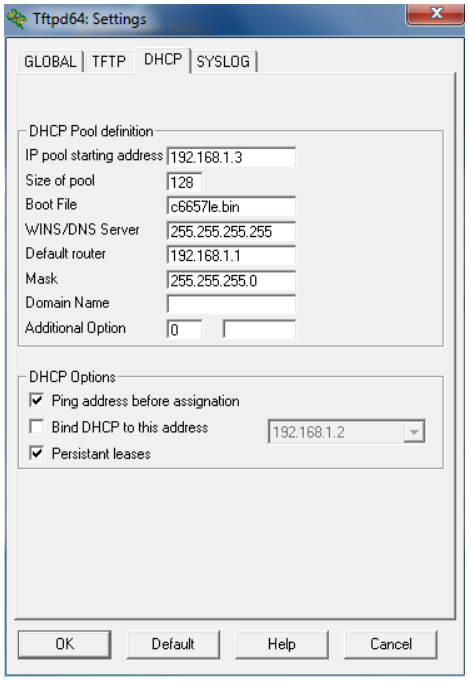
Afterwards, the TFTP server is not needed anymore. In the following, the settings in the corresponding windows are shown.

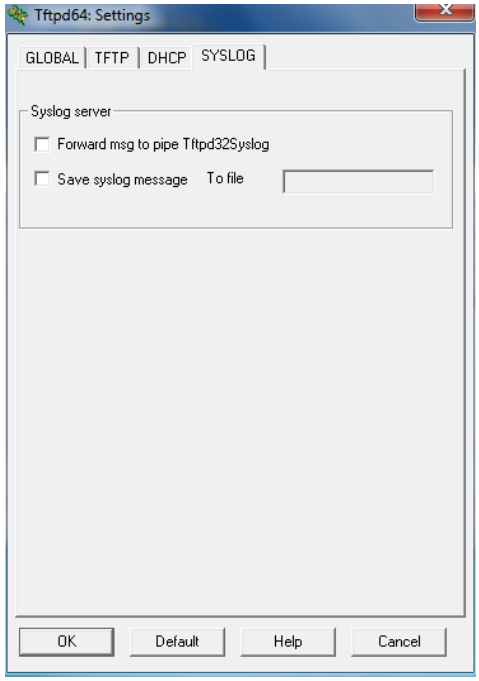

Eigenschaften von Intel PRO (DSP)
Netzwerk
Verbindung herstellen über:
Intel(R) PRO/1000 GT-Desktopadapter
Konfigurieren...
Diese Verbindung verwendet folgende Elemente:
Client für Microsoft-Netzwerke
Kaspersky Anti-Virus NDIS 6 Filter
QoS-Paketplaner
Datei- und Druckerfreigabe für Microsoft-Netzwerke
Internetprotokoll Version 6 (TCP/IPv6)
Internetprotokoll Version 4 (TCP/IPv4)
E/A-Treiber für Verbindungsschicht-Topologieerkennun...
Antwort für Verbindungsschicht-Topologieerkennung
Installieren...
Deinstallieren
Eigenschaften
Beschreibung
TCP/IP, das Standardprotokoll für WAN-Netzwerke, das den Datenaustausch über verschiedene, miteinander verbundene Netzwerke ermöglicht.
OK
Abbrechen

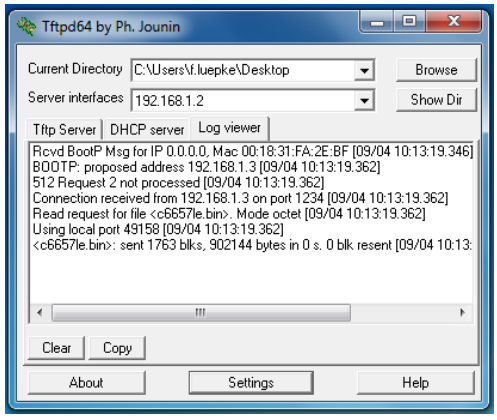

Eigenschaften von Internetprotokoll Version 4 (TCP/IPv4)
Allgemein
IP-Einstellungen können automatisch zugewiesen werden, wenn das Netzwerk diese Funktion unterstützt. Wenden Sie sich andernfalls an den Netzwerkadministrator, um die geeigneten IP-Einstellungen zu beziehen.
IP-Adresse automatisch beziehen
Folgende IP-Adresse verwenden:
IP-Adresse: 192 . 168 . 1 . 2
Subnetzmaske: 255 . 255 . 255 . 0
Standardgateway: 192 . 168 . 1 . 1
DNS-Serveradresse automatisch beziehen
Folgende DNS-Serveradressen verwenden:
Bevorzugter DNS-Server:
Alternativer DNS-Server:
Einstellungen beim Beenden überprüfen
Erweitert...
OK
Abbrechen


Tftpd64: Settings
GLOBAL
TFTP
DHCP
SYSLOG
Start Services
TFTP Server
TFTP Client
SNTP server
Syslog Server
DHCP Server
DNS Server
Enable IPv6
OK
Default
Help
Cancel


Tftpd64: Settings
GLOBAL
TFTP
DHCP
SYSLOG
Base Directory
C:\Users\f.luepke\Desktop
Browse
TFTP Security
None
Standard
High
Read Only
TFTP configuration
Timeout (seconds) 3
Max Retransmit 6
Tftp port 69
local ports pool
Advanced TFTP Options
Option negotiation
PXE Compatibility
Show Progress bar
Translate Unix file names
Bind TFTP to this address 192.168.1.2
Allow '\' As virtual root
Use anticipation window of 0 Bytes
Hide Window at startup
Create "dir.txt" files
Create md5 files
Beep for long transfer
OK
Default
Help
Cancel







Optional:

To change the IP address from the default value of 192.168.1.102: (not for 4pp yet, 2014.04.09). In Initialization change the IP address and press ‘Save to Flash’ button. Afterwards quit the STM Program. Change the IP address of the network card if you changed the subnet and change the corresponding parameters in the TFTP Server. Reboot the DSP. Upon restart of the STM program the DSP will appear under the new address.

Appendix B Potentiometry software manual

- Prerequisite for a potentiometry scan is a stable tunneling contact
- The potential resolution of a STP scan depends strongly on the tunneling resistance
    - Values below 200 MOhm (e.g. 5-500 mV; 0.05-1 nA) are typical scanning parameters. The feedback parameters need to be set according to the tunneling parameters and voltage divider (1:1, 1:10, …). Good starting points are Integrator2=0.0001 (1:1); 0.01 (1:100); 0.1 (1:1000).
    - P-Gain2 should be set to 1 independent of measurement parameters and is typically not required to be adjusted.
- The ADC offset needs to be calibrated to be zero – otherwise the measurement results will be flawed. This is true especially for thermovoltage and surface photovoltage measurements.

The contact resistance of the two current injecting tip can vary during the measurements. To compensate the variation a voltage reference tip can be used. This tip should be contacted to the sample surface close to the scan tip and on the same equipotential line as the scan tip. The potentiometry measurement can then be calculated as the difference of the scanning tip and the reference tip to cancel out offsets in the sample voltage due to the fluctuations in the current injection contact resistances. The method of utilizing a voltage reference tip is however often not required, because small offset fluctuations in the sample voltage can be corrected in the potentiometry scan in post-processing by a line subtraction. For larger fluctuations the potentiometry measurement itself typically becomes so instable that also the voltage reference tip does not help to achieve a good measurement.

B.1 Software settings

Aux1: This channel contains the measured potential data by the scanning tip. It can be renamed in the ‘Initialization’ tab of the software.

Aux2: This channel contains the current of the scanning tip after performing the potential feedback. This value should be zero when the feedback functions properly. It can be renamed in the ‘Initialization’ tab of the software.

ADCs: One should always also acquire the map of one of the ADCs of the current injecting tips, such that the injected current throughout the scan can be related to the potential map afterwards. If present, the ADC channel of the voltage reference tip should be recorded.

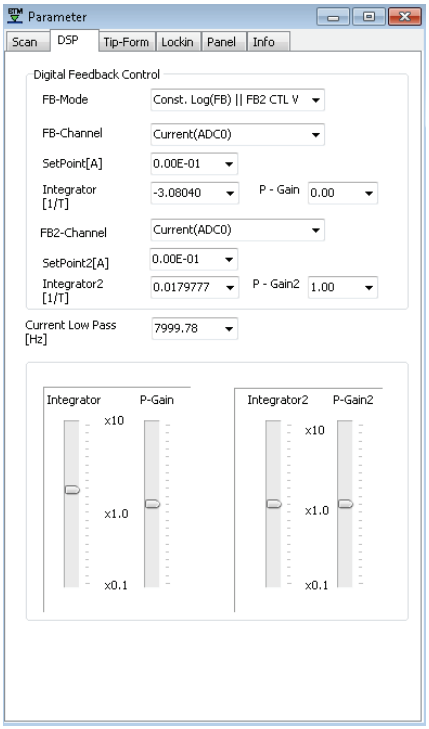


Figure B.1. DSP setting tab in the software with typical settings for a potentiometry scan with 1:100 voltage divider.

B.2 Potentiometry measurement without transport field

In this setup one can measure e.g. the thermovoltage or photovoltage.

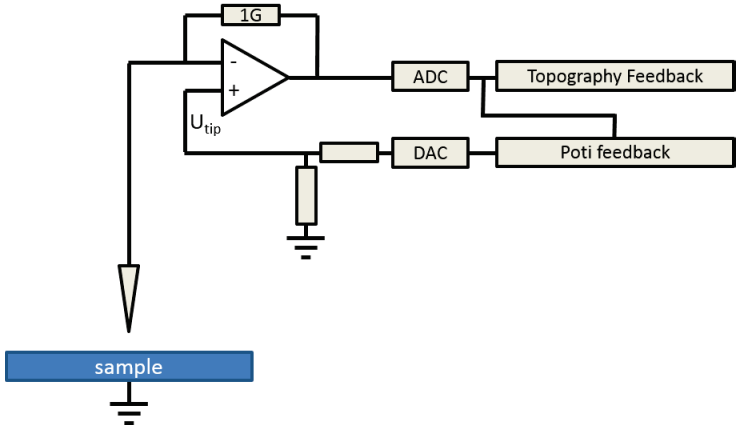


Figure B.2. Schematic of the setup for a potentiometry measurement without a transport field.

- Make sure that the sample is on ground potential
- Auto-approach the scan tip at the desired sample position with approach parameters e.g. 2 V and 0.1 nA
- Perform a topography scan to make sure the sample surface at this position is ok
- Retract the tip by setting the set point to 0 A
- Insert the voltage divider (if required), set the appropriate bias voltage and null the ADC
- Re-approach the tip
- Start the potentiometry scan
- Adjust the scan parameters until the desired scan quality is achieved (typically best visible in the 'LineScanForm' with activated 'Display current ScanProfile')

B.3 Potentiometry measurement with transport field

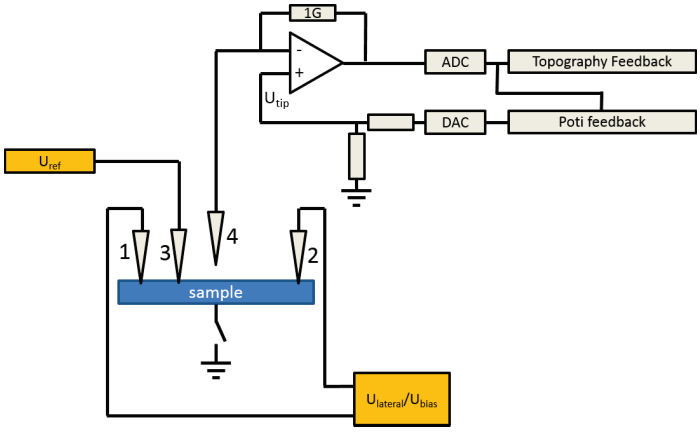


Figure B.3. Schematic of the setup for a potentiometry measurement with applied transport field.

- Make sure that the sample is on ground potential
- Auto-approach the scan tip at the desired sample position with approach parameters e.g. 2 V and 0.1 nA
- Perform a topography scan to make sure the sample surface at this position is ok
- Retract the tip by setting the set point to 0 A and performing slip-stick steps if required
- Position the current injecting tips, typically a few ten or hundred microns away from the scanning tip such that all three tips are on a straight line
- Auto-approach the current injecting tips one at a time
- Auto-approach the scanning tip if retracted by slip-stick steps
- Insert the voltage divider (if required), set the appropriate bias voltage and null the ADC

At this point all tips should be in the vicinity of the sample surface, such that they can be brought into contact to the sample surface by activating their feedback loops.

- Bring current injecting tip 1 into tunneling contact

- Activate the z-limiter of that tip (z-Limit retract 100 nm)
- Set that tips bias voltage to ~ 10 mV
- Set that tips preamp gain to 10^6
- Activate the feedback loop of that tip with maximum current set point ($\sim 8 \cdot 10^{-6}$ A)
- Manually approach the tip to the sample surface by clicking the slider of the z-limiter and moving the tip forward with the arrow keys on the computer keyboard until a stable current of ~ 1 µA flows
- Set the tip voltage to 0 mV and repeat the approaching procedure with the other current injecting tip

- When both current injecting tip are in contact to the sample surface disconnect the sample's connection to ground
- Set the voltage of the two current injecting tips such that the desired lateral current is flowing – the absolute current measured at both current injecting tips should be identical.

(Optional) Contact voltage reference tip

- Auto-approach the voltage reference tip to the surface
- Activate the feedback of the tip
- Activate the z-limiter of that tip (z-Limit retract 100 nm)
- Switch that tip to voltage probe mode
- Manually approach the tip to the sample surface by clicking the slider of the z-limiter and moving the tip forward with the arrow keys on the computer keyboard until the voltage at the tip jumps to 0 V.

Approach scanning tip

- Activate the feedback of the scanning tip with bias voltage larger than the bias voltage of the current injecting tips
- Start a potentiometry scan and determine the approximate potential at the position of the scanning tip
- Adjust the current injecting tips' bias voltage such that the potential at the position of the scanning tip is approximately 0 V

- Retract the tip by setting the set point to 0 A
- Insert the voltage divider (if required), set the appropriate bias voltage and null the ADC
- Re-approach the tip
- Start the potentiometry scan
- Adjust the scan parameters until the desired scan quality is achieved (typically best visible in the 'LineScanForm' with activated 'Display current ScanProfile')

B.4 Opening Potentiometry Files in Gwyddion

When a potentiometry scan is imported in Gwyddion, the z-scale of current and potential images is wrong due to the fact that all z-scales are recomputed using the corresponding piezo constants and Gain values when imported into Gwyddion.

The correct data scale can be retrieve from the original dataset by loading the file into Gwyddion and rescaling the potential/current images under "Data Process->Basic Operations->Dimensions and units" by a factor of

$$s = \frac{10 \cdot 10^9}{\text{GainZ} \cdot \text{ZPiezoconst}},$$

as a result of the piezo constant being in units Å/V. For example, if GainZ=5 and ZPiezoconst= 48.00 scaling by a factor of

$$s = 0.0417 \cdot 10^9 = 41.7 \cdot 10^6$$

yields the correct z-scale. To make sure the z-scale is correct, compare it to the original data in PSTMAFM!

Note: If a voltage divider was used in the measurements, it can be directly factored in when rescaling the data:

Zpiezoconst [Å/V]	Z gain	Voltage divider	Scaling factor s in Gwyddion
48	5	1	**4,167E+07**
48	5	10	**4,167E+06**
48	5	100	**4,167E+05**
48	5	1000	**4,167E+04**
48	20	1	**1,042E+07**
48	20	10	**1,042E+06**
48	20	100	**1,042E+05**
48	20	1000	**1,042E+04**

Appendix C Resistor network MATLAB codes

C.1 Forward direction

The following source code calculates the potential distribution from a given distribution of resistors, corresponding to the 'forward direction' of calculation. The type of defect can be chosen by uncommenting the corresponding function which are explained below.

Source code of 'Resistor_network_forward.m'

```
clear; tic; close all;
x=51; y=51;                          %Pixel dimensions
U1=10; U2=-10;                       %Potential at boundaries
[Sx,Sy,Sz,I]=deal(sparse(x*y,1));    %Predefine for quicker calculation
R=spalloc(x*y,x*y,6*x*y); k=0;

Rho=1;          %bulk resistivity in Ohm*cm
R_defect=10;    %Defect resistivity


noise=0;        %swtich noise on/off
T=[];
r=1; n=20;                                  %radius of circular defects and
number of defects in the random array
% [T] = T_generator_circle(x,y,r);          %circular defect
% [T] = T_generator_step(x,y);              %step defect
% [T] = T_generator_array(x,y);             %array of circular defects
[T] = T_generator_random(x,y,n);            %random distribution of
circular defects
% R_defect=T_generator_kidney(x,y);[T] = zeros(x,y);k=1;  %kidney defect

t=find(T==0);                               %find the resistors to be
replaced

if x>1
    Rx=Rho*ones(y,x);                       %resistors in x-direction
    Rx(t)=Rstufex;                          %set resistor to step resistance
    for i=1:numel(t)
        if t(i)<(x-1)*y && k<1
    Rx(t(i)+y)=Rstufex;                     %set also resistors after node
to step resistance
        end
    end
    Rx(:,1)=[];
    Sx=1./Rx';                              %calculate conductivity
end

if y>1
    Ry=Rho*ones(x,y);                       %resistors in y-direction
    Ry(t)=Rstufey;                          %set resistor to step resistance
    for i=1:numel(t)
        if mod(t(i),x)>0 && k<1
    Ry(t(i)+1)=Rstufey;                     %set also resistors after node
to step resistance
        end
    end
Ry(1,:)=[];
```

```
    Sy=1./Ry';                              %calculate conductivity
end

for a=1:x*y                                 %filling of resistance matrix
        if mod(a,y)>0                       %connection to nodes in +x-
direction, if applicable
            R(a,a+1)=Sx(a-floor((a-1)/y));
            R(a,a)=R(a,a)-Sx(a-floor((a-1)/y));
        end
        if mod(a-1,y)>0                     %connection to nodes in -x-
direction, if applicable
            R(a,a-1)=Sx(a-1-floor((a-1)/y));
            R(a,a)=R(a,a)-Sx(a-1-floor((a-1)/y));
        end
        if  a-1<(x-1)*y                     %connection to nodes in +y-
direction, if applicable
            R(a,a+x)=Sy(a);
            R(a,a)=R(a,a)-Sy(a);
        end
        if a-1>=x                           %connection to nodes in -y-
direction, if applicable
            R(a,a-x)=Sy(a-x);
            R(a,a)=R(a,a)-Sy(a-x);
        end
end

% ____________________data set 1_____________________________________
I(1:y)=1;                                   %current source 1
I(y*(x-1)+1:x*y,1)=1;                       %current source 2

Rb=R;
for i=[(x*(y-1)+1):x*y]
R(i,:)=0;                                   %set potential at boundary 1
independent of reistances
R(i,i)=1/U1;%                               %instead use U1 for voltage at
that boundary
end
for i=[1:y]
R(i,:)=0;                                   %set potential at boundary 2
independent of reistances
R(i,i)=1/U2;                                %instead use U2 for voltage at
that boundary
end
tic;

V1=full(R\I);                               %solve linear equation system

V1=reshape(V1,x,y);                         %matrix representation of
potentials
V1=permute(V1,[2 1]) ;                      %put in corresct order


% ___________________________________data set 2_____________________
I(:,:)=0;
I(1:x:(x-1)*y+1)=1;                         %current source 1
I(x:x:x*y)=1;                               %current source 2

R=Rb;
for i=[1:x:(x-1)*y+1]
R(i,:)=0;                                   %set potential at boundary 1
independent of reistances
```

```
R(i,i)=1/U2;                                %instead use U2 for voltage at
that boundary
end
for i=x:x:x*y
R(i,:)=0;                                   %set potential at boundary 2
independent of reistances
R(i,i)=1/U1;                                %instead use U1 for voltage at
that boundary
end

V2=full(R\I);                               %solve linear equation system
V2=reshape(V2,x,y);                         %matrix representation of
potentials
V2=permute(V2,[2 1]) ;                      %put in corresct order

Vn1=V1;Vn2=V1;Vn3=V2;Vn4=V2;
% _____________________________________end of data set 2_________________
DeltaV=1;
for i=[1:x*y]                               %add noise to potential data
    Vn1(i)=V1(i)+noise*(rand-0.5)/DeltaV/100;
    Vn2(i)=V2(i)+noise*(rand-0.5)/DeltaV/100;
    Vn3(i)=V1(i)+noise*(rand-0.5)/DeltaV/100;
    Vn4(i)=V2(i)+noise*(rand-0.5)/DeltaV/100;
end

PaperSize=[50 10];
h=figure;
set(h,'PaperSize', PaperSize, 'Resize', 'off',
'units','centimeters','outerposition',[0 5 PaperSize(1)+0.2
PaperSize(2)+2.2]);

subplot(1,5,1);
surf(Vn2)
xlabel('x');
ylabel('y');

subplot(1,5,2);
surf(Vn1)
xlabel('x');
ylabel('y');

subplot(1,5,3);
imagesc(flipud(Rx))
xlabel('x');
ylabel('y');
axis square;
title('Rx')

subplot(1,5,4);
imagesc(flipud(Ry))
xlabel('x');
ylabel('y');
axis square;
title('Ry')

dlmwrite('V_1.txt',Vn1,'delimiter',' ','precision',100);
dlmwrite('V_2.txt',Vn2,'delimiter',' ','precision',100);
dlmwrite('V_3.txt',Vn3,'delimiter',' ','precision',100);
dlmwrite('V_4.txt',Vn4,'delimiter',' ','precision',100);
dlmwrite('S_x.txt',Sx,'delimiter',' ','precision',100);
dlmwrite('S_y.txt',Sy,'delimiter',' ','precision',100);
toc
```

C.1.1 Generating different defect geometries

The MATLAB code presented in chapter C.1 can define different defect geometries by loading different 'T_generator' functions at its beginning. In the following are given some example source codes of structures which were investigated in the course of the thesis.

Step with a bulge

Source code of 'T_generator_step.m'

```
function [ T ] = Tgenerator( x,y )
s=0;
T=ones(x,y);
for(i=[ceil(2*x/5.)])
    for j=1:floor(size(T,2)/5.+1)
    T(i,j)=0;
    end
    for j=floor(size(T,2)/5.)+1:floor(2*size(T,2)/5.)
    T(i+j-floor(size(T,2)/5.),j+1)=0;
    end
    for j=floor(2*size(T,2)/5.)+1:floor(3*size(T,2)/5.)
    T(i+floor(size(T,2)/5.),j)=0;
    end
    for j=floor(3*size(T,2)/5.)+1:floor(4*size(T,2)/5.)
    T(i-j+floor(4*size(T,2)/5.)+1,j)=0;
    end
    for j=floor(4*size(T,2)/5.)+1:size(T,2)
    T(i,j)=0;
    end
    T=flipud(T);
end
end
```

Circular Hole

Source code of 'T_generator_circle.m'

```
function [ T ] = Tgenerator( x,y,r )
s=0;
T=ones(x,y);
x0=ceil(x/2);
y0=ceil(y/2);
for i=1:x
    for j=1:y
        if (i-x0)^2+(j-y0)^2<r^2
            T(i,j)=0;
        end
    end
end
end
```

Regular array of holes

Source code of 'T_generator_array.m'

```
function [ T ] = Tgenerator( x,y,r )
s=0;
T=ones(x,y);
for i=1:x
    for j=1:y
        if mod(i,8)==0 && mod(j,8)==0
            T(i-1,j-1)=0;
        else

        end
    end
end
end
```

Random distribution of holes

Source code of 'T_generator_random.m'

```
function [ T ] = Tgenerator( x,y,n )
i=0;
T=ones(x,y);
while i<n
        x0=ceil(rand*(x-1))+1;
        y0=ceil(rand*(y-1))+1;
        if x0<x && y0<y && T(x0,y0)==1 && T(x0+1,y0)==1 && T(x0-1,y0)==1
&& T(x0,y0+1)==1 && T(x0,y0-1)==1
            T(x0,y0)=0;
            i=i+1;
        end
end
end
```

Kidney

Source code of 'T_generator_kidney.m'

```
function [ R ] = Tgenerator( x0,y0 )
a=1.2;                          %size in x-direction
b=1.2;                          %size in y-direction
dx=(x0+2)/a;                    %step-size in x-direction
dy=(x0+2)/b;                    %step-size in y-direction

for i=1:x0
    for j=1:y0
        x=7*(i/(dx))-3.4*a;     %re-scaling of x
        y=7*(j/(dy)-0.6*b);     %re-scaling of y
        sigma(i,j)=(1+5*exp(-(x-y)^2-2*(x+y)^2)+3*exp(-3*(x-1)^2-
(y+1)^2))^-1;
    end
end
R=1./sigma';    %Inversion and rotation of the matrix
end
```

C.1.2 Calculations for Bi thin films

Source code of 'Resistor_network_Bi.m'

```
clear; tic; close all;

M = dlmread('A151119.193814.Poti100.markup_490nm.txt');  %load mask file

M=M(1:end,1:end)';

x=size(M,1); y=x;            %Pixel Dimensions
U1=-0.05e-3; U2=10e-3;       %Potential at left and right boundary
[Sx,Sy,Sz,I]=deal(sparse(x*y,1));
R=spalloc(x*y,x*y,6*x*y);    %Predefine to increase speed

Rs=1;                        %Sheet resistance in Ohm/sq.
Rdefekt=1e10;

t=find(M~=0);

if x>1
    Rx=Rs*ones(y,x);             %Resistors in x-direction
    Rx(t)=Rdefekt;
    Rx(:,1)=[];
    Sx=1./Rx';
end

if y>1
    Ry=Rs*ones(x,y);             %Resistors in y-direction
    Ry(t)=Rdefekt;
    Ry(1,:)=[];
    Sy=1./Ry';
end

for a=1:x*y                                 %fill resistance matrix
        if mod(a,y)>0                       %connection to nodes in +x-
direction, if applicable
            R(a,a+1)=Sx(a-floor((a-1)/y));
            R(a,a)=R(a,a)-Sx(a-floor((a-1)/y));
        end
        if mod(a-1,y)>0                     %connection to nodes in -x-
direction, if applicable
            R(a,a-1)=Sx(a-1-floor((a-1)/y));
            R(a,a)=R(a,a)-Sx(a-1-floor((a-1)/y));
        end
        if  a-1<(x-1)*y                     %connection to nodes in +y-
direction, if applicable
            R(a,a+x)=Sy(a);
            R(a,a)=R(a,a)-Sy(a);
        end
        if a-1>=x                           %connection to nodes in -y-
direction, if applicable
            R(a,a-x)=Sy(a-x);
            R(a,a)=R(a,a)-Sy(a-x);
        end
end

I(1:y)=1;                                           %current source 1
I(y*(x-1)+1:x*y)=1;                                 %current source 2
```

```
Rb=R;
for i=1:y
R(i,:)=0;                                                %set potential at
boundary 1 independent of reistances
R(i,i)=1/U1;                                             %instead use U1 for
voltage at that boundary
end
for i=y*(x-1)+1:x*y
R(i,:)=0;                                                 %set potential at
boundary 2 independent of reistances
R(i,i)=1/U2;                                              %instead use U2 for
voltage at that boundary
end

V=full(R\I);                                              %solve linear
equation system

V=reshape(V,x,y);                                         %matrix
representation of potentials

%______subtract background slope______
S=ones(x,y);                                              E=(U2-U1)/((x-1));
for n=1:x
S(:,n)=U2+E*(n-1);
end
D=V-S;

%_______plot________
PaperSize=[30 10];
h=figure(1);
set(h,'PaperSize', PaperSize, 'Resize', 'off',
'units','centimeters','outerposition',[0 15 PaperSize(1)+0.2
PaperSize(2)+2.2]);

subplot(1,3,1);
imagesc(D)
xlabel('x');
ylabel('y');
axis square;
dlmwrite('CalcPot.txt',D,'delimiter',' ','precision',100);

subplot(1,3,2);
imagesc(Sx)
xlabel('x');
ylabel('y');
axis square;
title('Sx')

subplot(1,3,3);
imagesc(Sy)
xlabel('x');
ylabel('y');
axis square;
title('Sy')
toc
```

C.1.3 Three-dimensional resistor network

Source code of 'Resistor_network_3D.m'

```
clear; tic; close all;
x=50; y=x; z=3;   %pixel dimensions
d=1;              %size of simulation in meter
dx=d/x;           %mesh spacing in meter
U1=1; U2=-1;      %potential at current injection points
[Sx,Sy,Sz,I]=deal(sparse(x*y*z,1)); %Predefine for quicker calculation
R=spalloc(x*y*z,x*y*z,6*x*y*z);     %Predefine for quicker calculation

Rs=1e-5;          %surface sheet resistance in Ohm/sq.
Rho=1;            %Bulk resistance in Ohm*cm
Rkoppel=1;        %coupling resistance between surface and bulk in Ohm
cm^2
Tx=0.5;           %relative x-position of current injection
Ty=0.3;           %relative y-position of current injection

if x>1
    Rx=Rho*x^2/d*ones(y,x,z);           %calculate resistors values in
x-direction
    Rx=permute(Rx,[2 1 3]);             %bring resistor values in
correct order
    Sx=reshape(1./Rx,[],1);             %calculate x-conductivity
end

if y>1
    Ry=Rho*x^2/d*ones(y,x,z);           %calculate resistors values in
y-direction
    Ry=permute(Ry,[2 1 3]);             %bring resistor values in
correct order
    Sy=reshape(1./Ry,[],1);             %calculate y-conductivity
end

if z>1
    Rz(:,:,1)=Rkoppel*x^2/(x*y*d)*ones(y,x,1);  %calculate resistor
values
    Rz(:,:,2:z)=Rho*x^2/d*ones(y,x,z-1);        %resistors in z-
direction
    Rz=permute(Rz,[2 1 3]);                     %bring values in correct
order
    Sz=reshape(1./Rz,[],1);                     %calculate z-
conductivity
end

for a=1:x*y*z                                   %filling of resistance
matrix
        if(mod(a,x)>0)                          %connection to nodes in +x-
direction, if applicable
            R(a,a+1)=Sx(a,1);
            R(a,a)=R(a,a)-Sx(a,1);
        end
        if(mod(a-1,x)>0)                        %connection to nodes in -x-
direction, if applicable
            R(a,a-1)=Sx(a-1);
            R(a,a)=R(a,a)-Sx(a-1);
        end
        if(mod(a-1,x*y)<x*y-x)                  %connection to nodes in +y-
direction, if applicable
            R(a,a+x)=Sy(a+x);
```

```
        R(a,a)=R(a,a)-Sy(a+x);
        end
        end
        if(mod(a-1,x*y)>=x)                    %connection to nodes in -y-
direction, if applicable
            R(a,a-x)=Sy(a-x);
            R(a,a)=R(a,a)-Sy(a-x);
        end
        if(a<=x*y*z-x*y)                       %connection to nodes in +z-
direction, if applicable
            R(a,a+x*y)=Sz(a);
            R(a,a)=R(a,a)-Sz(a);
        end
        if(a>x*y)                              %connection to nodes in -z-
direction, if applicable
            R(a,a-x*y)=Sz(a-x*y);
            R(a,a)=R(a,a)-Sz(a-x*y);
        end
end

Tipx=round(Ty*y*x)+round(Tx*x);                %position of current
injection 1
Tipy=round((y-Ty*y-1)*x)+round(Tx*x);          %position of current
injection 2

I(Tipx,1)=1;                                   %current source 1
I(Tipy,1)=1;                                   %current source 2

Rb=R;

R(Tipx,:)=0;            %set potential at boundary 1 independent of
surrounding reistors
R(Tipx,Tipx)=1/U1;      %instead use U1 for voltage at the position of
current source 1
R(Tipy,:)=0;            %set potential at boundary 2 independent of
surrounding reistors
R(Tipy,Tipy)=1/U2;      %instead use U2 for voltage at the position of
current source 2

V=full(R\I);            %solve linear equation system

I=Rb(Tipx,:)*V(:)

V=reshape(V,x,y,z);     %matrix representation of potentials
V=permute(V,[2 1 3]) ;  %put in corresct order

PaperSize=[40 10];
h=figure;
set(h,'PaperSize', PaperSize, 'Resize', 'off',
'units','centimeters','outerposition',[0 5 PaperSize(1)+0.2
PaperSize(2)+2.2]);

subplot(1,2,1);

for i=1:size(V,3)       %plot matrix as stacked potential planes
[~,h] = contourf(V(:,:,i),x*2,'LineStyle','none');
```

```
hold on;
hh = get(h,'Children');
for j=1:numel(hh)
    zdata = ones(size(get(hh(j),'XData')));  %shift z values to plot
stacked planes
    set(hh(j), 'ZData',1*(1-i*zdata));
end
end
title('Local Potential')
colorbar;
cb = colorbar('vert');
zlab = get(cb,'ylabel');
set(zlab,'String','Potential (V)');
caxis([U2 U1]);
hold off;
view(80,20);
axis('square');

subplot(1,2,2);
plot(permute(V(:,ceil(0.5*x),:),[1 3 2]))   %plot sections of the
potential planes
title('Section')
xlabel('x (a.u.)');
ylabel('Potential (V)');

toc
```

C.2 Inverse conductivity calculation

Source code of 'Resistor_network_inverse.m'

```
clear; close all; tic;
V1= dlmread('V_1.txt'); %load potential distribution 1
V2= dlmread('V_2.txt'); %load potential distribution 2
Sx_ref= dlmread('S_x.txt'); %load original resistivity distribution 1
Sy_ref= dlmread('S_y.txt'); %load original resistivity distribution 1
x=size(V2,1);               %x-size of the loaded data set
y=size(V2,2);               %x-size of the loaded data set
dV=spalloc(2*numel(V2),numel(V2),4*numel(V2)); %predefine for quicker
calculation


for i=1:size(V1,1)-1
for j=1:size(V1,1)-1
    V1(i+1,j)-V1(i,j) + V1(i+1,j+1)-V1(i+1,j) + V1(i,j+1)-V1(i+1,j+1) +
V1(i,j+1)-V1(i,j)
end
end
% _____________________data set 1_____________________________
[dV] = dVmatrix(V1,x,y);      %set up matrix V

double ddV1;
ddV1=dV;
% _____________________data set 2_____________________________
[dV] = dVmatrix(V2,x,y);      %set up matrix V

double ddV2;
ddV2=dV;
%_____________________combine data sets_____________________
ddV=[ddV1; ddV2];       %combine the potentials of the two data set

Sx=ones((x-1)*y,1);     %predefine vector of vertical resistors
Sy=ones(x*(y-1),1);     %predefine vector of horizontal resistors
Rt=[Sx(1:end)' Sy(1:end)']'; %combine x- and y-conductivities

%_____________________Left side of LEQ_____________________

C1=ddV1*Rt;
C1=reshape(C1,x,y);
C1(2:x-1,:)=0;
C1=reshape(C1,numel(C1),1);
C2=ddV2*Rt;
C2(x+1:(x-1)*y)=0;
C=[C1;C2];

A=-1*eye(size(ddV,2),size(ddV,2));
b=zeros(size(ddV,2),1)';

f=zeros(size(ddV,2),1);

S = linprog(f,A,b,ddV,C);
size(S)

%_____solved LEQ -> analyze data__________
```

```
Sx=S(1:x*y);
Sy=S(x*y+1:end);
Rt=[Sx(1:end)' Sy(1:end)']';

l=reshape(Rt(1:(x-1)*y),x,y-1);
m=reshape(Rt(((x-1)*y+1):end),x-1,y);

Sx_ref=flipud(Sx_ref');
DeltaSx=(Sx_ref-l).^2;
DeltaSx=sum(sum(DeltaSx));

Sy_ref=flipud(Sy_ref');
DeltaSy=(Sy_ref-m).^2;
DeltaSy=sum(sum(DeltaSy));

sigmaS=sqrt(1/(2*x*y-1)*(DeltaSy+DeltaSx))

d=(V1(end,1)-V1(1,1))/(x-1);

for i=1:x
    D1(i,:)=V1(i,:)-d*i;
end

%_____Plot_____________________________
PaperSize=[40 10];
h=figure;
set(h,'PaperSize', PaperSize, 'Resize', 'off',
'units','centimeters','outerposition',[0 5 PaperSize(1)+0.2
PaperSize(2)+2.2]);

subplot(1,4,1);
surf(V1);
xlabel('x');
ylabel('y');
axis square;

subplot(1,4,2);
surf(V2);
xlabel('x');
ylabel('y');
axis square;

subplot(1,4,3);
imagesc(flipud(l))
xlabel('x');
ylabel('y');
set(gca, 'Clim', [0 1])
title('Rx')
axis square;

subplot(1,4,4);
imagesc(flipud(m))
xlabel('x');
ylabel('y');
set(gca, 'Clim', [0 1])
title('Ry')
axis square;
toc
```

C.1.2 Function to set up matrix *V*

Source code of 'dVmatrix.m' which is used for the calculation of the inverse problem.

```
function [ dV ] = dVmatrix( V, x, y )
dVx=zeros(x*y,x*(y-1));                  %horizontal voltage differences
dVy=zeros(x*y,x*(y-1));                  %vertical voltage differences
kill=[];

for(j=1:numel(V))

    if j+1<=numel(V)                      %connection to nodes in +y-
direction, if applicable
        dVy(j,j)=V(j+1)-V(j);
    end
    if j-1>0                              %connection to nodes in -y-
direction, if applicable
        dVy(j,j-1)=V(j-1)-V(j);
    end
    if mod(j,x)==0 && j<x*y
        kill=[kill j];
    end

    if j>0 && j<=numel(V)-y               %connection to nodes in +x-
direction, if applicable
        dVx(j,j)=V(j+x)-V(j);
    end

    if j>y && j<=numel(V)                 %connection to nodes in -x-
direction, if applicable
        dVx(j,j-x)=V(j-x)-V(j);
    end
end
dVy(:,kill)=[];
dV=[dVx dVy];
end
```

Appendix D Electrostatics of a current around a sphere or cylinder

D.1 Current around a sphere

This geometry corresponds to a three-dimensional defect embedded in a conductor. For a conductivity inside/outside of the sphere σ_i/σ_o we solve the Laplace equation for finite potentials at the origin

$$\Delta\Phi(\mathrm{r},\theta) = 0$$

Ansatz:

$$\Phi_i = \sum_{n=0}^{\infty} a_n \cdot \left(\frac{r}{R}\right)^n \cdot P_n(\cos(\theta))$$

$$\Phi_o = E_\infty \cdot r \cdot \cos(\theta) + \sum_{n=0}^{\infty} b_n \cdot \left(\frac{r}{R}\right)^{-(n+1)} \cdot P_n(\cos(\theta))$$

boundary conditions

$$\Phi_i(r = R, \theta) = \Phi_o(r = R, \theta)$$

$$\sigma_i \frac{\partial}{\partial r}\, \Phi_i(r = R, \theta) = \sigma_o \frac{\partial}{\partial r} \Phi_o(r = R, \theta)$$

Which equals to

$$\sum_{n=0}^{\infty} a_n \cdot P_n(\cos(\theta)) = E_\infty \cdot R \cdot \cos(\theta) + \sum_{n=0}^{\infty} b_n \cdot P_n(\cos(\theta))$$

$$\sigma_i \sum_{n=0}^{\infty} a_n \cdot \frac{n}{R}\left(\frac{r}{R}\right)^{n-1} \cdot P_n(\cos(\theta))|_{r=R} = \sigma_o E_\infty \cdot \cos(\theta) + \sigma_o \sum_{n=0}^{\infty} b_n \cdot \frac{-(n+1)}{R}\left(\frac{r}{R}\right)^{-n} \cdot P_n(\cos(\theta))|_{r=R}$$

and results in

$$a_0 + a_1 \cdot P_1(\cos(\theta)) + a_2 P_2(\cos(\theta)) \ldots = b_0 + (E_\infty \cdot R + b_1) \cdot P_1(\cos(\theta)) + b_2 P_2(\cos(\theta) \ldots$$

$$\sigma_i \left(\frac{a_1}{R} \cdot P_1(\cos(\theta)) + \frac{2a_2}{R} P_2(\cos(\theta)) + \cdots\right) = -\sigma_o \left(\frac{b_0}{R} + \left(-E_\infty + \frac{2b_1}{R}\right) \cdot P_1(\cos(\theta)) + \frac{3b_2}{R} P_2(\cos(\theta)) \ldots\right).$$

Comparison of coefficients:

$$a_0 = b_0$$

$$a_1 = E_\infty \cdot R + b_1$$

$$a_n = b_n, f\ddot{u}r\ n > 1$$

and

$$\frac{b_0}{R} = 0 \Rightarrow a_0 = 0$$

$$\frac{\sigma_i a_1}{R} = \sigma_o \left(E_\infty - \frac{2b_1}{R}\right)$$

$$\frac{\sigma_i a_n n}{R} = -\frac{\sigma_o b_n (n+1)}{R}, \qquad \text{for n} > 1$$

$$\sigma_i a_n \frac{n}{(n+1)} = -\sigma_o b_n, \qquad \text{for n} > 1$$

From this and $a_n = b_n, f\ddot{u}r\ n > 1$ results

$$a_n = b_n = 0, f\ddot{u}r\ n > 1$$

The only remaining coefficients are

$$a_1 = E_\infty \cdot R + b_1$$

$$\frac{\sigma_i a_1}{R} = \sigma_o \left(E_\infty - \frac{2b_1}{R}\right)$$

Solving for b_1

$$a_1 = R\frac{\sigma_o}{\sigma_i}\left(E_\infty - \frac{2b_1}{R}\right) = E_\infty \cdot R + b_1$$

$$\Rightarrow E_\infty \cdot R\left(\frac{\sigma_o}{\sigma_i} - 1\right) = \left(\frac{2\sigma_o}{\sigma_i} + 1\right) b_1$$

$$\Rightarrow b_1 = E_\infty \cdot R \frac{\left(\frac{\sigma_o}{\sigma_i} - 1\right)}{\left(\frac{2\sigma_o}{\sigma_i} + 1\right)}$$

and therefore

$$\Rightarrow a_1 = E_\infty \cdot R + b_1 = E_\infty \cdot R \left(\frac{\left(\frac{\sigma_o}{\sigma_i} - 1\right)}{\left(\frac{2\sigma_o}{\sigma_i} + 1\right)} + 1 \right).$$

Or in a different representation

$$b_1 = \frac{\sigma_o - \sigma_i}{2\sigma_o + \sigma_i} E_\infty \cdot R \; and \; a_1 = \frac{3\sigma_o}{2\sigma_o + \sigma_i} E_\infty \cdot R$$

$$\Phi_i(\theta = 0) = \frac{3\sigma_o}{2\sigma_o + \sigma_i} E_\infty \cdot r$$

$$\Phi_o(\theta = 0) = E_\infty \cdot r + \frac{\sigma_o - \sigma_i}{2\sigma_o + \sigma_i} E_\infty \cdot \frac{R^3}{r^2}$$

Infinite resistance of the sphere:

$b_1 \xrightarrow{\sigma_i \to 0} \frac{1}{2} E_\infty R$ and $a_1 \xrightarrow{\sigma_i \to 0} \frac{3}{2} E_\infty R$

$$\Phi_i(\theta = 0) = \frac{3}{2} E_\infty \cdot r$$

$$\Phi_o(\theta = 0) = E_\infty \cdot r + \frac{1}{2} E_\infty \cdot \frac{R^3}{r^2}$$

Infinite conductance of the sphere:

$b_1 \xrightarrow{\sigma_i \to \infty} -E_\infty \cdot R$ and $a_1 \xrightarrow{\sigma_i \to \infty} 0$

D.2 Current around an infinite cylinder

This calculation determines the electric field around an infinite cylinder embedded in a conductor. The problem geometry corresponds to a quasi-two-dimensional system.

Ansatz:

$$\Phi_i(r, \theta) = \sum_{n=0}^{\infty} a_n \cdot \left(\frac{r}{R}\right)^n \cdot \cos(n \cdot \theta)$$

$$\Phi_o(r, \theta) = E_\infty \cdot r \cdot \cos(\theta) + \sum_{n=0}^{\infty} b_n \cdot \left(\frac{r}{R}\right)^{-n} \cdot \cos(n \cdot \theta)$$

boundary conditions

$$\Phi_i(r = R, \theta) = \Phi_o(r = R, \theta)$$

$$\sigma_i \frac{\partial}{\partial r} \Phi_i(r = R, \theta) = \sigma_o \frac{\partial}{\partial r} \Phi_o(r = R, \theta)$$

Which equals to

$$\sum_{n=0}^{\infty} a_n \cdot \cos(n \cdot \theta) = E_\infty \cdot R \cdot \cos(\theta) + \sum_{n=0}^{\infty} b_n \cdot \cos(\theta)$$

$$\sigma_i \sum_{n=0}^{\infty} a_n \cdot \frac{n}{R} \left(\frac{r}{R}\right)^{n-1} \cdot \cos(n \cdot \theta) \mid_{r=R}$$

$$= \sigma_o E_\infty \cdot \cos(\theta) + \sigma_o \sum_{n=0}^{\infty} b_n \cdot \frac{-n}{R} \left(\frac{r}{R}\right)^{-(n-1)} \cdot \cos(n \cdot \theta) \mid_{r=R}$$

and results in

$$a_0 + a_1 \cdot \cos(\theta) + a_2 \cos(2\theta) \ldots = b_0 + (E_\infty \cdot R + b_1) \cdot \cos(\theta) + b_2 \cos(2\theta) \ldots$$

$$\sigma_i \left(\frac{a_1}{R} \cdot \cos(\theta) + \frac{2a_2}{R} \cos(2\theta) + \cdots\right) = -\sigma_o \left(\left(-E_\infty + \frac{b_1}{R}\right) \cdot \cos(\theta) + \frac{2b_2}{R} \cos(2\theta) \ldots\right).$$

Comparison of coefficients:

$$a_0 = b_0$$

$$a_1 = E_\infty \cdot R + b_1$$

$$a_n = b_n, \text{für } n > 1$$

and

$$\frac{\sigma_i a_1}{R} = \sigma_o \left(E_\infty - \frac{b_1}{R}\right)$$

$$\frac{\sigma_i a_n n}{R} = -\frac{\sigma_o b_n n}{R}, \qquad for\ n > 1$$

Boundary condition $\Phi_o(r \to \infty, \theta) = E_\infty r$ yields

$$a_0 = b_0 = 0$$

such that the only remaining coefficients are

$$a_1 = E_\infty \cdot R + b_1$$

$$\frac{\sigma_i a_1}{R} = \sigma_o \left(E_\infty - \frac{b_1}{R}\right).$$

Solving for b_1:

$$\frac{\sigma_i a_1}{\sigma_o} = E_\infty \cdot R - b_1$$

$$b_1 = E_\infty \cdot R - \frac{\sigma_i a_1}{\sigma_o}$$

And therefore

$$\Rightarrow a_1 = E_\infty \cdot R + E_\infty \cdot R - \frac{\sigma_i a_1}{\sigma_o}$$

$$\Leftrightarrow a_1 \left(1 + \frac{\sigma_i}{\sigma_o}\right) = 2E_\infty \cdot R$$

$$\Leftrightarrow a_1 = \frac{2}{\left(1 + \frac{\sigma_i}{\sigma_o}\right)} E_\infty \cdot R$$

Resulting in

$$\Rightarrow b_1 = E_\infty \cdot R - \frac{\sigma_i}{\sigma_o} \frac{2}{\left(1 + \frac{\sigma_i}{\sigma_o}\right)} E_\infty \cdot R$$

$$\Leftrightarrow b_1 = E_\infty \cdot R - \frac{2\sigma_i}{(\sigma_o + \sigma_i)} E_\infty \cdot R$$

$$\Leftrightarrow b_1 = \frac{\sigma_o - \sigma_i}{\sigma_o + \sigma_i} E_\infty \cdot R$$

Infinite resistance of the cylinder:

$b_1 \xrightarrow{\sigma_i \to 0} E_\infty R$ and $a_1 \xrightarrow{\sigma_i \to 0} 2E_\infty R$

$$\Phi_i(\theta = 0) = 2E_\infty \cdot r$$

$$\Phi_o(\theta = 0) = E_\infty \cdot r + E_\infty \cdot \frac{R^2}{r}$$

Infinite conductance of the cylinder:

$b_1 \xrightarrow{\sigma_i \to \infty} -E_\infty \cdot R$ and $a_1 \xrightarrow{\sigma_i \to \infty} 0$

Appendix E Deduction of carrier concentration in the Dirac cone

The linear dispersion of the Dirac cone in two dimensions is given by

$$E = \hbar v_F \sqrt{\boldsymbol{k}_x^2 + \boldsymbol{k}_y^2} \equiv \frac{1}{a} k \quad \Leftrightarrow \quad k = a \cdot E \tag{E.1}$$

Furthermore, in a two-dimensional system, the density of states is given by the two-dimensional density of states per unit volume ρ without spin degeneracy, due to the spin-polarized nature of the TSS [96]:

$$\rho(k)dk = \frac{k}{2\pi}\, dk,$$

which with eq. (E.1) becomes

$$\rho(E)dE = \frac{a^2 E}{2\pi} dE.$$

Integration yields

$$n_{2D}(E) = \int \rho(E)dE = \frac{a^2 E^2}{4\pi}.$$

Rewriting again with eq. (E.1), the carrier concentration in the Dirac cone, which is filled up to the Fermi energy E_F, can be determined from the corresponding Fermi wave vector k_F after

$$n_{2D}(E_\mathrm{F}) = \frac{k_\mathrm{F}^2}{4\pi}.$$

Appendix F Deduction of gate formulas

F.1 Full description

This appendix documents the deduction of eq. (4.8) and (4.9) in chapter 4 of the thesis. In detail, combination of eq. (4.3) to (4.5) in this thesis results in

$$n_{\mathrm{bot}} = -n_{\mathrm{TI}} - n_{\mathrm{gate}}$$

$$\Leftrightarrow n_{\mathrm{bot}} = -\frac{C_{\mathrm{gate}}\left(eV_{\mathrm{gate}} - \mu_{\mathrm{bot}}\right)}{e^2} - \frac{C_{\mathrm{TI}}\left(\mu_{\mathrm{top}} - \mu_{\mathrm{bot}}\right)}{e^2}$$

$$\Leftrightarrow n_{\mathrm{bot}} = -\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e} + \frac{C_{\mathrm{gate}}\mu_{\mathrm{bot}}}{e^2} - \frac{C_{TI}\mu_{\mathrm{top}}}{e^2} + \frac{C_{TI}\mu_{\mathrm{bot}}}{e^2}$$

$$\Leftrightarrow n_{\mathrm{bot}} = -\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e} + \frac{C_{\mathrm{gate}}a\left(\sqrt{n_{\mathrm{bot}}^0 + n_{\mathrm{bot}}} - \sqrt{n_{\mathrm{bot}}^0}\right)}{e^2} - \frac{C_{\mathrm{TI}}a\left(\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}} - \sqrt{n_{\mathrm{top}}^0}\right)}{e^2} + \frac{C_{\mathrm{TI}}a\left(\sqrt{n_{\mathrm{bot}}^0 + n_{\mathrm{bot}}} - \sqrt{n_{\mathrm{bot}}^0}\right)}{e^2}$$

$$\Leftrightarrow n_{\mathrm{bot}} + \left(-\frac{C_{\mathrm{gate}}a}{e^2} - \frac{C_{\mathrm{TI}}a}{e^2}\right)\left(\sqrt{n_{\mathrm{bot}}^0 + n_{\mathrm{bot}}} - \sqrt{n_{\mathrm{bot}}^0}\right) + \frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e} + \frac{C_{\mathrm{TI}}a\left(\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}} - \sqrt{n_{\mathrm{top}}^0}\right)}{e^2} = 0$$

$$\Leftrightarrow \frac{C_{\mathrm{TI}}a\left(\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}} - \sqrt{n_{\mathrm{top}}^0}\right)}{e^2} = -n_{\mathrm{bot}} + \left(\frac{C_{\mathrm{gate}}a}{e^2} + \frac{C_{\mathrm{TI}}a}{e^2}\right)\left(\sqrt{n_{\mathrm{bot}}^0 + n_{\mathrm{bot}}} - \sqrt{n_{\mathrm{bot}}^0}\right) - \frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}$$

$$\Leftrightarrow \frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}} - \frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{top}}^0} = \left(-n_{\mathrm{bot}} + \left(\frac{C_{\mathrm{gate}}a}{e^2} + \frac{C_{\mathrm{TI}}a}{e^2}\right)\left(\sqrt{n_{\mathrm{bot}}^0 + n_{\mathrm{bot}}} - \sqrt{n_{\mathrm{bot}}^0}\right) - \frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}\right)$$

$$\Leftrightarrow \frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{top}}^0 + n_{\mathrm{top}}} = \left(-n_{\mathrm{bot}} + \left(\frac{C_{\mathrm{gate}}a}{e^2} + \frac{C_{\mathrm{TI}}a}{e^2}\right)\left(\sqrt{n_{\mathrm{bot}}^0 + n_{\mathrm{bot}}} - \sqrt{n_{\mathrm{bot}}^0}\right) - \frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}\right) + \frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{top}}^0}$$

$$\Leftrightarrow \sqrt{n_{\text{top}}^0 + n_{\text{top}}}$$
$$= \left(\frac{C_{\text{TI}}a}{e^2}\right)^{-1}\left(\left(-n_{\text{bot}} + \left(\frac{C_{\text{gate}}a}{e^2} + \frac{C_{\text{TI}}a}{e^2}\right)\left(\sqrt{n_{\text{bot}}^0 + n_{\text{bot}}} - \sqrt{n_{\text{bot}}^0}\right)\right.\right.$$
$$\left.\left. - \frac{C_{\text{gate}}V_{\text{gate}}}{e}\right) + \frac{C_{TI}a}{e^2}\sqrt{n_{\text{top}}^0}\right)$$

$$\Leftrightarrow n_{\text{top}}^0 + n_{\text{top}}$$
$$= \left(\left(\frac{C_{\text{TI}}a}{e^2}\right)^{-1}\left(\left(-n_{\text{bot}} + \left(\frac{C_{\text{gate}}a}{e^2} + \frac{C_{\text{TI}}a}{e^2}\right)\left(\sqrt{n_{\text{bot}}^0 + n_{\text{bot}}} - \sqrt{n_{\text{bot}}^0}\right)\right.\right.\right.$$
$$\left.\left.\left. - \frac{C_{\text{gate}}V_{\text{gate}}}{e}\right) + \frac{C_{TI}a}{e^2}\sqrt{n_{\text{top}}^0}\right)\right)^2$$

$$\Leftrightarrow n_{\text{top}} = \left(\left(\frac{C_{\text{TI}}a}{e^2}\right)^{-1}\left(\left(-n_{\text{bot}} + \left(\frac{C_{\text{gate}}a}{e^2} + \frac{C_{\text{gate}}a}{e^2}\right)\left(\sqrt{n_{\text{bot}}^0 + n_{\text{bot}}} - \sqrt{n_{\text{bot}}^0}\right) - \frac{C_{\text{gate}}V_{\text{gate}}}{e}\right)\right.\right.$$
$$\left.\left. + \frac{C_{TI}a}{e^2}\sqrt{n_{\text{top}}^0}\right)\right)^2 - n_{\text{top}}^0,$$

where $C_{\text{gate}} = 11\ \text{nF/cm}^2 \ll C_{\text{TI}} = 8\ \mu\text{F/cm}^2$ and therefore

$$n_{\text{top}} \approx \left(\left(\frac{C_{\text{TI}}a}{e^2}\right)^{-1}\left(\left(-n_{\text{bot}} + \frac{C_{\text{TI}}a}{e^2}\left(\sqrt{n_{\text{bot}}^0 + n_{\text{bot}}} - \sqrt{n_{\text{bot}}^0}\right) - \frac{C_{\text{gate}}V_{\text{gate}}}{e}\right)\right.\right.$$
$$\left.\left. + \frac{C_{\text{TI}}a}{e^2}\sqrt{n_{\text{top}}^0}\right)\right)^2 - n_{\text{top}}^0$$

$$\Leftrightarrow n_{\text{top}} \approx \left(\left(\frac{C_{\text{TI}}a}{e^2}\right)^{-1}\left(-n_{\text{bot}} + \frac{C_{\text{TI}}a}{e^2}\left(\sqrt{n_{\text{bot}}^0 + n_{\text{bot}}} - \sqrt{n_{\text{bot}}^0} + \sqrt{n_{\text{top}}^0}\right) - \frac{C_{\text{gate}}V_{\text{gate}}}{e}\right)\right)^2$$
$$- n_{\text{top}}^0$$

Furthermore

$$n_{\text{top}} = n_{\text{TI}} = \frac{C_{\text{TI}}(\mu_{\text{top}} - \mu_{\text{bot}})}{e^2}$$
$$\Leftrightarrow n_{\text{top}} = \frac{C_{\text{TI}}\mu_{\text{top}}}{e^2} - \frac{C_{\text{TI}}\mu_{\text{bot}}}{e^2}$$
$$\Leftrightarrow n_{\text{top}} = \frac{C_{\text{TI}}a\left(\sqrt{n_{\text{top}}^0 + n_{\text{top}}} - \sqrt{n_{\text{top}}^0}\right)}{e^2} - \frac{C_{\text{TI}}a\left(\sqrt{n_{\text{bot}}^0 + n_{\text{bot}}} - \sqrt{n_{\text{bot}}^0}\right)}{e^2}$$

$$\Leftrightarrow \frac{C_{\mathrm{TI}}a\left(\sqrt{n_{\mathrm{bot}}^0+n_{\mathrm{bot}}}-\sqrt{n_{\mathrm{bot}}^0}\right)}{e^2}=-n_{\mathrm{top}}+\frac{C_{\mathrm{TI}}a\left(\sqrt{n_{\mathrm{top}}^0+n_{\mathrm{top}}}-\sqrt{n_{\mathrm{top}}^0}\right)}{e^2}$$

$$\Leftrightarrow \frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{bot}}^0+n_{\mathrm{bot}}}-\frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{bot}}^0}=-n_{\mathrm{top}}+\frac{C_{\mathrm{TI}}a}{e^2}\left(\sqrt{n_{\mathrm{top}}^0+n_{\mathrm{top}}}-\sqrt{n_{\mathrm{top}}^0}\right)$$

$$\Leftrightarrow \frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{bot}}^0+n_{\mathrm{bot}}}=-n_{\mathrm{top}}+\frac{C_{\mathrm{TI}}a}{e^2}\left(\sqrt{n_{\mathrm{top}}^0+n_{\mathrm{top}}}-\sqrt{n_{\mathrm{top}}^0}\right)+\frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{bot}}^0}$$

$$\Leftrightarrow \frac{C_{\mathrm{TI}}a}{e^2}\sqrt{n_{\mathrm{bot}}^0+n_{\mathrm{bot}}}=-n_{\mathrm{top}}+\frac{C_{\mathrm{TI}}a}{e^2}\left(\sqrt{n_{\mathrm{top}}^0+n_{\mathrm{top}}}-\sqrt{n_{\mathrm{top}}^0}+\sqrt{n_{\mathrm{bot}}^0}\right)$$

$$\Leftrightarrow \sqrt{n_{\mathrm{bot}}^0+n_{\mathrm{bot}}}=\left(\frac{C_{\mathrm{TI}}a}{e^2}\right)^{-1}\left(-n_{\mathrm{top}}+\frac{C_{\mathrm{TI}}a}{e^2}\left(\sqrt{n_{\mathrm{top}}^0+n_{\mathrm{top}}}-\sqrt{n_{\mathrm{top}}^0}+\sqrt{n_{\mathrm{bot}}^0}\right)\right)$$

$$\Leftrightarrow n_{\mathrm{bot}}^0+n_{\mathrm{bot}}=\left(\left(\frac{C_{\mathrm{TI}}a}{e^2}\right)^{-1}\left(-n_{\mathrm{top}}+\frac{C_{\mathrm{TI}}a}{e^2}\left(\sqrt{n_{\mathrm{top}}^0+n_{\mathrm{top}}}-\sqrt{n_{\mathrm{top}}^0}+\sqrt{n_{\mathrm{bot}}^0}\right)\right)\right)^2$$

$$\Leftrightarrow n_{\mathrm{bot}}=\left(\left(\frac{C_{\mathrm{TI}}a}{e^2}\right)^{-1}\left(-n_{\mathrm{top}}+\frac{C_{\mathrm{TI}}a}{e^2}\left(\sqrt{n_{\mathrm{top}}^0+n_{\mathrm{top}}}-\sqrt{n_{\mathrm{top}}^0}+\sqrt{n_{\mathrm{bot}}^0}\right)\right)\right)^2-n_{\mathrm{bot}}^0$$

F.2 Limit of constant quantum capacitances

$$n_{\mathrm{bot}}=-n_{\mathrm{TI}}-n_{\mathrm{gate}}$$

$$\Leftrightarrow n_{\mathrm{bot}}=-\frac{C_{\mathrm{gate}}\left(eV_{\mathrm{gate}}-\mu_{\mathrm{bot}}\right)}{e^2}-\frac{C_{\mathrm{TI}}\left(\mu_{\mathrm{top}}-\mu_{\mathrm{bot}}\right)}{e^2}$$

$$\Leftrightarrow n_{\mathrm{bot}}=-\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}+\frac{C_{\mathrm{gate}}\mu_{\mathrm{bot}}}{e^2}-\frac{C_{\mathrm{TI}}\mu_{\mathrm{top}}}{e^2}+\frac{C_{\mathrm{TI}}\mu_{\mathrm{bot}}}{e^2}$$

$$\Leftrightarrow n_{\mathrm{bot}}=-\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}-\frac{a}{\sqrt{n_{\mathrm{bot}}^0}}\frac{C_{\mathrm{gate}}n_{\mathrm{bot}}}{e^2}+\frac{a}{\sqrt{n_{\mathrm{top}}^0}}\frac{C_{\mathrm{TI}}n_{\mathrm{top}}}{e^2}-\frac{a}{\sqrt{n_{\mathrm{bot}}^0}}\frac{C_{\mathrm{TI}}n_{\mathrm{bot}}}{e^2}$$

With $\frac{a}{e^2\sqrt{n_{\mathrm{top}}^0}}=\left(C_{\mathrm{tq}}^0\right)^{-1}$ and $\frac{a}{e^2\sqrt{n_{\mathrm{bot}}^0}}=\left(C_{\mathrm{bq}}^0\right)^{-1}$

$$\Leftrightarrow n_{\mathrm{bot}}=-\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}-\frac{C_{\mathrm{gate}}n_{\mathrm{bot}}}{C_{\mathrm{bq}}^0}+\frac{C_{\mathrm{TI}}n_{\mathrm{top}}}{C_{\mathrm{tq}}^0}-\frac{C_{\mathrm{TI}}n_{\mathrm{bot}}}{C_{\mathrm{bq}}^0}$$

$$\Leftrightarrow n_{\mathrm{bot}}+\frac{C_{\mathrm{gate}}n_{\mathrm{bot}}}{C_{\mathrm{bq}}^0}+\frac{C_{\mathrm{TI}}n_{\mathrm{bot}}}{C_{\mathrm{bq}}^0}=-\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}+\frac{C_{\mathrm{TI}}n_{\mathrm{top}}}{C_{\mathrm{tq}}^0}$$

$$\Leftrightarrow n_{\mathrm{bot}}\left(1+\frac{C_{\mathrm{gate}}}{C_{\mathrm{bq}}^0}+\frac{C_{\mathrm{TI}}}{C_{\mathrm{bq}}^0}\right)=-\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}+\frac{C_{\mathrm{TI}}n_{\mathrm{top}}}{C_{\mathrm{tq}}^0}$$

$$\Leftrightarrow n_{\mathrm{bot}} = -\frac{1}{\left(1+\frac{C_{\mathrm{gate}}}{C_{\mathrm{bq}}^{0}}+\frac{C_{\mathrm{TI}}}{C_{\mathrm{bq}}^{0}}\right)}\left(\frac{C_{\mathrm{gate}}V_{\mathrm{gate}}}{e}+\frac{C_{\mathrm{TI}}n_{\mathrm{top}}}{C_{\mathrm{tq}}^{0}}\right)$$

Furthermore, it follows

$$n_{\mathrm{top}} = n_{\mathrm{TI}} = \frac{C_{\mathrm{TI}}\left(\mu_{\mathrm{top}}-\mu_{\mathrm{bot}}\right)}{e^{2}}$$

$$\Leftrightarrow n_{\mathrm{top}} = \frac{C_{\mathrm{TI}}\mu_{\mathrm{top}}}{e^{2}} - \frac{C_{\mathrm{TI}}\mu_{\mathrm{bot}}}{e^{2}}$$

$$\Leftrightarrow n_{\mathrm{top}} = -\frac{C_{\mathrm{TI}}n_{\mathrm{top}}}{C_{\mathrm{tq}}^{0}} + \frac{C_{\mathrm{TI}}n_{\mathrm{bot}}}{C_{\mathrm{bq}}^{0}}$$

$$\Leftrightarrow n_{\mathrm{top}} + \frac{C_{\mathrm{TI}}n_{\mathrm{top}}}{C_{\mathrm{tq}}^{0}} = \frac{C_{\mathrm{TI}}n_{\mathrm{bot}}}{C_{\mathrm{bq}}^{0}}$$

$$\Leftrightarrow n_{\mathrm{top}}\left(1+\frac{C_{\mathrm{TI}}}{C_{\mathrm{tq}}^{0}}\right) = \frac{C_{\mathrm{TI}}n_{\mathrm{bot}}}{C_{\mathrm{bq}}^{0}}$$

$$\Leftrightarrow n_{\mathrm{top}} = \frac{\frac{C_{\mathrm{TI}}}{C_{\mathrm{bq}}^{0}}}{\left(1+\frac{C_{\mathrm{TI}}}{C_{\mathrm{tq}}^{0}}\right)}n_{\mathrm{bot}}$$

$$\Leftrightarrow \frac{n_{\mathrm{top}}}{n_{\mathrm{bot}}} = \frac{\frac{C_{\mathrm{TI}}}{C_{\mathrm{bq}}^{0}}}{\left(1+\frac{C_{\mathrm{TI}}}{C_{\mathrm{tq}}^{0}}\right)}.$$

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