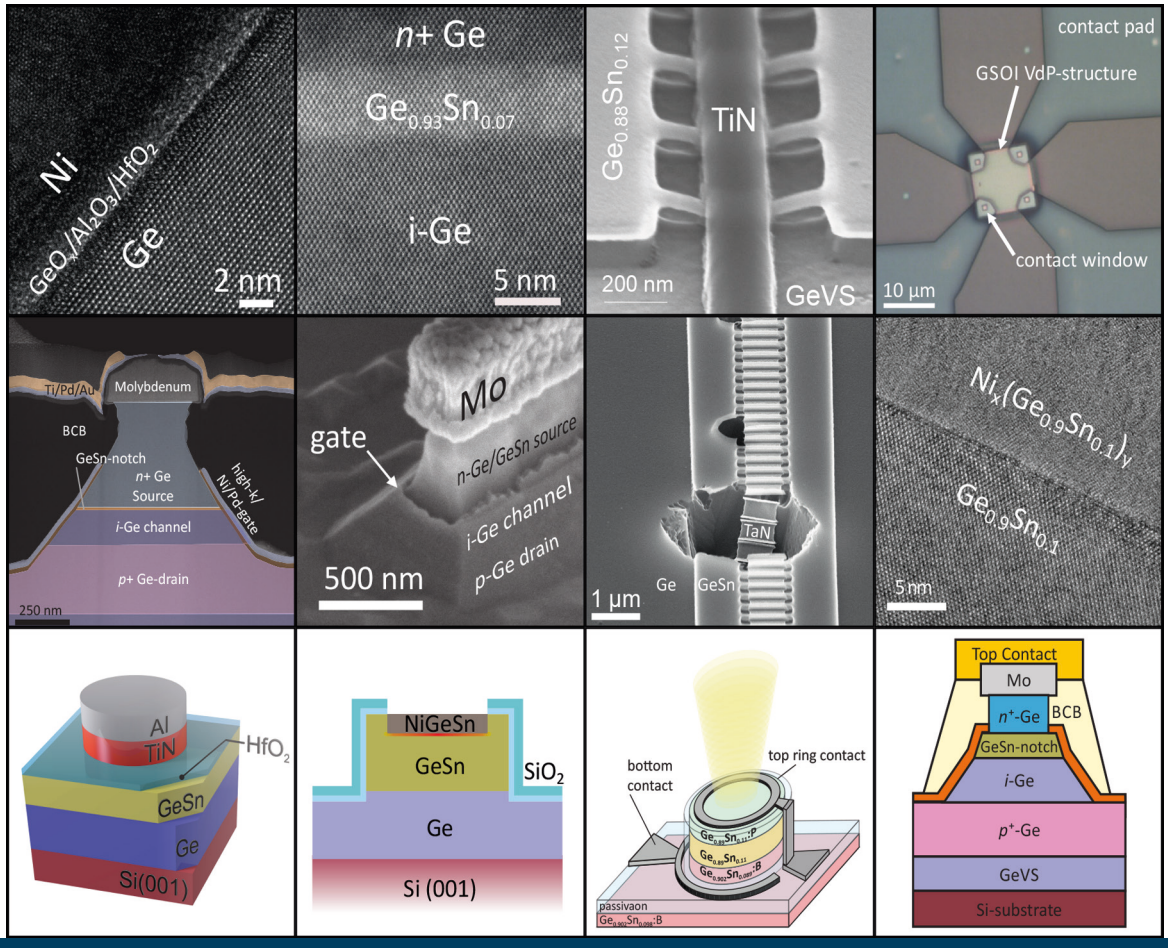

Investigation of GeSn as Novel Group IV Semiconductor for Electronic Applications

Christian Schulte-Braucks

Schlüsseltechnologien / Key Technologies
Band / Volume 168
ISBN 978-3-95806-312-9

Mitglied der Helmholtz-Gemeinschaft

JÜLICH
Forschungszentrum

Schriften des Forschungszentrums Jülich
Reihe Schlüsseltechnologien / Key Technologies Band / Volume 168

Forschungszentrum Jülich GmbH
Peter Grünberg Institut
Halbleiter-Nanoelektronik (PGI-9)

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ISSN 1866-1807 ISBN 978-3-95806-312-9

Bibliografische Information der Deutschen Nationalbibliothek.
Die Deutsche Nationalbibliothek verzeichnet diese Publikation in der
Deutschen Nationalbibliografie; detaillierte Bibliografische Daten
sind im Internet über http://dnb.d-nb.de abrufbar.

Herausgeber und Vertrieb:	Forschungszentrum Jülich GmbH Zentralbibliothek, Verlag 52425 Jülich Tel.: +49 2461 61-5368 Fax: +49 2461 61-6103 zb-publikation@fz-juelich.de www.fz-juelich.de/zb
Umschlaggestaltung:	Grafische Medien, Forschungszentrum Jülich GmbH
Druck:	Grafische Medien, Forschungszentrum Jülich GmbH
Copyright:	Forschungszentrum Jülich 2018

Schriften des Forschungszentrums Jülich
Reihe Schlüsseltechnologien / Key Technologies, Band / Volume 168

D 82 (Diss., RWTH Aachen University, 2017)

ISSN 1866-1807
ISBN 978-3-95806-312-9

Vollständig frei verfügbar über das Publikationsportal des Forschungszentrums Jülich (JuSER)
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Für Lena, Hannes und Theo

Kurzfassung

In den letzten Jahren haben einkristalline GeSn Halbleiterverbindungen deutliches wissenschaftliches Interesse erregt, besonders nachdem 2015 GeSn mit ausreichend hohem Sn-Gehalt und hoher Kristallqualität als direkter Halbleiter experimentell nachgewiesen wurde. Während verbesserte optische Eigenschaften bei einem direkten Material naheliegen, werden für GeSn auch verbesserte elektrische Eigenschaften erwartet, wie z.B. erhöhte Ladungsträgerbeweglichkeiten und Band-zu-Band-Tunnelraten, welche für Metal-Oxid-Halbleiter-Transistoren bzw. für Tunnelfeldeffekttransistoren von Vorteil sind. Die neuartigen GeSn Halbleiter stellen damit ein interessantes Materialsystem dar, welches ein neues Forschungsfeld zur Untersuchung dessen physikalischer, elektrischer, optischer und chemischer Eigenschaften eröffnet. Allerdings verlangt die Neuheit des Materialsystems auch die Entwicklung, Anpassung und Verifizierung aller Prozessschritte zur Herstellung GeSn-basierter Halbleiterbauelemente. Diese Arbeit konzentriert sich in erster Linie auf die elektrischen Eigenschaften von GeSn, deren Abhängigkeiten vom Sn-Gehalt sowie mögliche Anwendungen in elektronischen Bauelementen. Die Bausteine von Feldeffekttransistoren werden einzeln erforscht. Mittels Röntgenphotoelektronenspektroskopie erfolgt zunächst die Untersuchung der Reinigung der GeSn Oberfläche vor der Abscheidung des Dielektrikums sowie die Untersuchung der Oberflächenmanipulation beim selektiven Ätzen von Ge zu GeSn. Zur Verwendung als elektrischer Kontakt in GeSn-basierten Bauelementen werden NiGeSn-Verbindungen strukturell, mittels Röntgenbeugung und elektrisch, mittels Strom-Spannungsmessungen, charakterisiert. Schottky-Barriere, Schichtwiderstand und spezifischer Kontaktwiderstand werden extrahiert. Sehr kleine Schottky-Barrieren von Minimum 0.06 eV werden beobachtet. Erstmals ist es gelungen, die NiGeSn/GeSn Schottky-Barriere mittels Dotierstoffsegregation einzustellen. Als nächster Baustein werden Metal-Oxid-Halbleiter-Kondensatoren umfangreich untersucht. Dielektrikum/GeSn-Grenzflächendefektdichten werden für einen breiten Sn-Gehaltbereich extrahiert. Der Schwerpunkt liegt hierbei auf dem Einfluss der Bandstruktur des GeSn auf die Kapazitäts-Spannungscharakteristika. Es wird ein grundlegender Zusammenhang zwischen der Sn-induzierten Verringerung der Bandlücke und der Minoritätsladungsträgerantwort beobachtet. Die maximal erzielte, flächennormierte Kapazität beträgt ca. $3\,\mu F/cm^2$. Als Schritt in Richtung GeSn-basierter Tunnelfeldeffekttransistoren werden Esaki-Dioden (Tunneldioden) hergestellt und elektrisch charakterisiert. Die Esaki-Dioden verfügen über einen negativen differentiellen Widerstand mit einem Verhältnis aus lokalem Strommaximum und -minimum von 2.3, was als experimenteller Beweis von Band-zu-Band-Tunneln zählt. In $Ge_{0.89}Sn_{0.11}$ *p-i-n*-Dioden werden erhöhte Band-zu-Band-Tunnelraten im Vergleich zu Ge beobachtet, was auf die verringerte und direkte Bandlücke zurückgeführt wird. Auf Grundlage dieser Arbeiten werden schließlich vertikale $Ge_{0.93}Sn_{0.07}$/Ge Tunnelfeldeffekttransistoren realisiert und

umfangreich charakterisiert, wobei Band-zu-Band-Tunneln und defektunterstütztes Tunneln als Hauptbeiträge zum Transistorstrom nachgewiesen werden. Abschließend dienen Hall-Messungen dem experimentellen Nachweis erhöhter Elektronenbeweglichkeiten in GeSn mit direkter Bandlücke. Mit bis zu $4600\,\mathrm{cm}^2/\mathrm{Vs}$ stellen diese die bis jetzt höchsten Volumenladungsträgerbeweglichkeiten in der IV-Hauptgruppe bei einem Dotierniveau von ca. $2.9 \cdot 10^{17}\,\mathrm{cm}^{-3}$ dar.

Abstract

Within the last few years single crystalline GeSn semiconductor alloys aroused significant scientific interest, especially since 2015, when GeSn with sufficiently high Sn content and crystalline quality was demonstrated as fundamentally direct bandgap group IV semiconductor. While enhanced optical properties are evident for direct bandgap materials compared to the fundamentally indirect Ge and Si group IV semiconductors, also enhanced electrical properties like increased carrier mobilities and enhanced band-to-band tunneling are expected for direct bandgap GeSn which are beneficial for metal-oxide-semiconductor transistors and tunnel field-effect transistors, respectively. The novel GeSn semiconductor alloys thereby manifests a fascinating emerging material system allowing a wide scope to study its fundamental physical, electrical, optical and chemical properties. On the other hand the novelty of the material system demands the re-development or modification and verification of all steps necessary to build GeSn based semiconductor devices. A comprehensive study is presented, focusing on the electrical properties of GeSn, their dependence on Sn content and possible applications in novel electronic devices. The building blocks of field-effect transistors are studied individually. GeSn surface composition and manipulation are investigated *via* X-ray photoemission spectroscopy to study pre-high-κ deposition cleaning and highly selective Ge/GeSn etching processes. NiGeSn alloys for the use as electrical contacts of GeSn devices are structurally and electrically characterized using X-ray diffraction, transmission electron microscopy and temperature dependent current voltage measurements, respectively. Schottky barrier height, sheet resistance and specific contact resistivity are extracted. The modification of the NiGeSn/GeSn Schottky barrier height *via* dopant segregation is demonstrated for the first time. Schottky-barrier heights as low as 0.06 eV are observed. As a next module metal-oxide-semiconductor capacitors are comprehensively studied. High-κ/GeSn interface trap densities are extracted for a wide range Sn contents. The focus is placed on the effect of the electronic band structure of GeSn on the capacitance voltage characteristics. Fundamental trends demonstrating the correlation of Sn-induced bandgap shrinkage and minority carrier response are observed. Furthermore a maximum capacitance of approx. 3 μF/cm^2 is achieved. As a step towards GeSn based tunnel field-effect transistors, Esaki diodes (tunnel diodes) are fabricated and electrically characterized. Negative differential resistance with a peak-to-valley current ratio of 2.3 is observed as an experimental proof of band-to-band tunneling. Enhanced band-to-band tunneling rates are observed in $Ge_{0.89}Sn_{0.11}$ *p-i-n* diodes compared to Ge taking advantage of the low and direct bandgap. These studies lead to the realization of vertical heterojunction $Ge_{0.93}Sn_{0.07}$/Ge tunnel field-effect transistors. An extensive analysis is provided identifying the various contributions to the overall transistor current, particularly band-to-band tunneling and trap-assisted tunneling. Finally, Hall

measurements are presented, showing enhanced electron mobilities in direct bandgap GeSn as compared to Ge. With up to $4600\,\mathrm{cm}^2/\mathrm{Vs}$ this marks the highest bulk electron mobilities at the respective doping level of $2.9 \cdot 10^{17}\,\mathrm{cm}^{-3}$ in a group IV semiconductor so far.

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List of Abbreviations

AC Alternating Current

Al Aluminum

ALD Atomic Layer Deposition

APL Applied Physics Letters

Ar Argon

As Arsenic

AVD Atomic Vapor Deposition

Au Gold

B Boron

BCB Benzocyclobuten

BTBT Band-to-Band Tunneling

CET Capacitance Equivalent Thickness

CV Capacitance Voltage (measurement)

CVD Chemical Vapor Deposition

CMOS	Complimentary MOS
Cr	Chromium
DC	Direct Current
DFT	Denstiy Functional Theory
DLTS	Deep Level Transient Spectroscopy
DMSO	Dimethyl Sulfoxide
DOS	Density of States
DS	Dopant Segregation
EBL	Electron Beam Lithography
ECV	Electrochemical CV
EOT	Equivalent Oxide Thickness
EL	Electroluminescence
F	Fluorine
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
FGA	Forming Gas Anneal
FIB	Focused Ion Beam
GaAs	Gallium Arsenide
GaAsSb	Gallium Arsenide Antimonide
GaSb	Gallium Antimonide
Ge	Germanium
GeSn	Germanium Tin

GSOI	GeSn on Insulator
GV	Conductance Voltage (measurement)
GeVS	Ge Virtual Substrate
HCl	Hydrochloric acid
HF	Hydrofluoric acid
HH	Heavy Hole
HNF	Helmholtz Nano Facility
IC	Integrated Circuit
ICSD	Inorganic Crystal Structure Database
ICP	Inductively Coupled Plasma
ICT	Information & Communication Technology
IEDM	International Electron Devices Meeting
IISG	Implantation Into Stanogermanide
IL	Interfacial Layer
InAs	Indium Arsenide
InGaAs	Indium Gallium Arsenide
InSb	Indium Antimonide
IoT	Internet of Things
IV	Current Voltage (measurement)
JAP	Journal of Applied Physics
LED	Light Emitting Diode
LH	Light Hole

MIT	Massachusetts Institute of Technology
Mo	Molybdenum
MOS	Metal-Oxide-Semiconductor
MOSCap	Metal-Oxide-Semiconductor Capacitor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MQW	Multi Quantum Well
MS	Metal-Semiconductor
MSM	Metal-Semiconductor-Metal
Ni	Nickel
NiGe	Nickelgermanide
NiGeSn	Nickelstanogermanide
NDR	Negative Differential Resistance
NIST	National Institute of Standards and Technology
P	Phosphorous
PC	Personal Computer
Pd	Palladium
PECVD	Plasma Enhanced Chemical Vapor Deposition
PGI	Peter Grünberg Institute
PL	Photoluminescence
Pt	Platinum
PVCR	Peak-to-Valley Current Ratio
QMSA	Quantitative Mobility Spectrum Analysis

RBS	Rutherford Backscattering Spectrometry
RCA	Radio Corporation of America
RF	Radio Frequency
RIE	Reactive Ion Etching
RPCVD	Reduced Pressure Chemical Vapor Deposition
RTA	Rapid Thermal Annealing
SBH	Schottky Barrier Height
eSBH	electron Schottky Barrier Height
hSBH	hole Schottky Barrier Height
SC-1	Standard Clean 1
SC-2	Standard Clean 2
sccm	standard cubic centimeters per minute
SEM	Scanning Electron Microscopy
Si	Silicon
SiGeSn	Silicon Germanium Tin
ToF-SIMS	Time of Flight Secondary Ion Mass Spectroscopy
Sn	Tin
SGIDS	Stanogermanidation-Induced Dopant Segregation
SRH	Shockley-Read-Hall
SS	Subthreshold Swing
SSE	Solid State Electronics
STEM	Scanning TEM

SWIR	Short Wavelength Infrared
TaN	Tantalum Nitride
TAT	Trap-Assisted Tunneling
TBTDET	Tris(diethylamido)(*tert*-butlyimino)tantalum $[((C_2H_5)_2N)_3(C_4H_9N)Ta]$
TCAD	Technology Computer Aided Design
TDMAH	Tetrakis(Dimethylamino)Hafnium
TED	Transactions on Electron Devices
TEM	Transmission Electron Microscopy
TEMAH	Tetrakis Ethyl Methyl Amino Hafnium
TFET	Tunnel Field-Effect Transistor
Ti	Titanium
TiN	Titanium Nitride
TLM	Transfer Length Method
TMA	Trimethylaluminium
WKB	Wentzel-Kramers-Brilloin
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction
XTEM	Cross sectional TEM

List of symbols

Symbol	Unit	Description
A	m^2	Area
$\mathcal{A}$	$\mathrm{cm}^{-3}\mathrm{s}^{-1}$	Parameter for BTBT
A^*	$\mathrm{A}/(\mathrm{cm}^2\mathrm{K}^2)$	Effective Richardson constant
A^{**}	$\mathrm{A}/(\mathrm{cm}^2\mathrm{K}^2)$	Reduced effective Richardson constant
$\mathcal{B}$	MV/cm	Parameter for BTBT
C	$\mu\mathrm{F}/\mathrm{cm}^2$	Capacitance per unit area
C_c	$\mu\mathrm{F}/\mathrm{cm}^2$	Series resistance corrected capacitance
C_D	$\mu\mathrm{F}/\mathrm{cm}^2$	Semiconductor depletion capacitance
C_FB	$\mu\mathrm{F}/\mathrm{cm}^2$	Flatband capacitance
C_m	$\mu\mathrm{F}/\mathrm{cm}^2$	Measured gate area normalized capacitance
C_ma	$\mu\mathrm{F}/\mathrm{cm}^2$	Gate area normalized capacitance measured in strong accumulation
C_Ox	$\mu\mathrm{F}/\mathrm{cm}^2$	Oxide capacitance
C_T	$\mu\mathrm{F}/\mathrm{cm}^2$	Trap capacitance
d_BTBT	nm	BTBT generation depth
d_gen	nm	Generation length for TAT
D_it	$\mathrm{cm}^{-2}\mathrm{eV}^{-1}$	Density of Interface Traps
D_t	$\mathrm{cm}^{-2}\mathrm{eV}^{-1}$	Trap density
E_a	eV	Activation energy
E_C	eV	Conduction band edge energy
E_CL	eV	Energy of the L-valley
$E_\mathrm{C\Gamma}$	eV	Energy of the Γ-valley
E_F	eV	Fermi level
$E_\mathrm{F,m}$	eV	Metal Fermi energy
$E_\mathrm{F,s}$	eV	Semiconductor Fermi level
E_G	eV	Bandgap
E_i	eV	Intrinsic level
E_sp	eV	Energy of a spontaneously emitted photon
E_t	eV	Trap energy

E_{TW}	eV	BTBT window
E_{V}	eV	Valence band edge energy
$\mathcal{E}$	V/m	Electrical field
$\mathcal{E}_{\mathrm{Bi}}$	V/m	Built in electrical field
f	Hz	Frequency
f_{peak}	Hz	Frequency of $(G_{\mathrm{P}}/\omega)_{\mathrm{max.}}$
f_{t}	Hz	Transition frequency
f_{c}		Conduction band Fermi distribution
f_{v}		Valence band Fermi distribution
G	$\mu\mathrm{S/cm}^2$	Conductance per unit area
G_{c}	$\mu\mathrm{S/cm}^2$	Series resistance corrected parallel conductance
G_{m}	$\mu\mathrm{S/cm}^2$	Measured gate area normalized parallel conductance
G_{ma}	$\mu\mathrm{S/cm}^2$	Gate area normalized parallel conductance measured in strong accumulation
G_{t}	$\mu\mathrm{S/cm}^2$	Trap conductance
h	Js	Planck constant
$\hbar = \frac{h}{2\pi}$	Js	Reduced Planck constant
$\mathcal{H}$		Hamilton Operator
I	A	Electrical current
I_{DS}	$\mu\mathrm{A}/\mu\mathrm{m}$	Width normalized Drain-Source current
I_{TAT}	$\mu\mathrm{A}/\mu\mathrm{m}$	Width normalized excess current
I_{G}	$\mu\mathrm{A}/\mu\mathrm{m}$	Width normalized gate leakage current
J	$\mathrm{A/cm}^2$	Current density
J_{F}	$\mathrm{A/cm}^2$	Forward bias current density
J_{G}	$\mathrm{A/cm}^2$	Gate leakage current density
J_{R}	$\mathrm{A/cm}^2$	Reverse bias current density
J_{BTBT}	$\mathrm{A/cm}^2$	BTBT current density
J_{TAT}	$\mathrm{A/cm}^2$	Excess current density
J_{thermal}	$\mathrm{A/cm}^2$	Thermal current density
k	1/m	Lattice vector
k_{B}	J/K	Boltzmann constant
L	m	Length

$\mathcal{M}_\mathrm{c}$	$\mathrm{cm^{-3}eV^{-1}}$	Conduction band density of states
$\mathcal{M}_\mathrm{v}$	$\mathrm{cm^{-3}eV^{-1}}$	Valence band density of states
m_e	kg	Free electron mass
m^*	$\mathrm{m_e}$	Effective carrier mass in a semiconductor
m^*_e	$\mathrm{m_e}$	Effective electron mass
m^*_h	$\mathrm{m_e}$	Effective hole mass
m^*_HH	$\mathrm{m_e}$	Heavy hole effective mass
m^*_LH	$\mathrm{m_e}$	Light hole effective mass
m^*_L	$\mathrm{m_e}$	L-valley electron effective mass
m^*_T	$\mathrm{m_e}$	Tunneling effective mass
m^*_Γ	$\mathrm{m_e}$	Γ-valley electron effective mass
n	$\mathrm{cm^{-3}}$	Electron carrier density
n_i	$\mathrm{cm^{-3}}$	Intrinsic carrier concentration of an undoped semiconductor
n_ps	$\mathrm{cm^{-3}}$	Electron carrier density in space charge region (for p-type)
n_po	$\mathrm{cm^{-3}}$	Equilibrium electron carrier density (for n-type)
n_2D	$\mathrm{cm^{-2}}$	Sheet carrier density
N	$\mathrm{cm^{-3}}$	Doping concentration (p or n)
N_A	$\mathrm{cm^{-3}}$	Acceptor concentration
N_D	$\mathrm{cm^{-3}}$	Donator concentration
N_t	$\mathrm{cm^{-3}eV^{-1}}$	Trap density (for a certain energy)
p	$\mathrm{cm^{-3}}$	Hole carrier density
p_ps	$\mathrm{cm^{-3}}$	Hole carrier density in space charge region (for p-type)
p_po	$\mathrm{cm^{-3}}$	Equilibrium hole carrier density (for p-type)
q	As	Elementary charge
$\mathfrak{q}$	1/m	Phonon
r_H		Hall factor
R	Ω	Electrical resistance
R_H	Ω	Hall resistance
R_S	Ω	Series resistance
R_Sht	Ω	Shunt resistance

$\mathcal{R}_{\mathrm{sp}}$	$\mathrm{eV^{-1}s^{-1}m^{-3}}$	Spectral spontaneous emission rate
$\mathcal{R}_{\mathrm{t}}$	$\mathrm{s^{-1}m^{-3}}$	TAT net generation rate
$R_{\square}$	Ω	Sheet resistance
SS	mV/dec	Subthreshold Swing
t_{GeSn}	nm	GeSn epilayer thickness
t_{Ox}	nm	Oxide thickness
T	K	Temperature
T_{BTBT}		Tunneling probability
v_{D}	m/s	Drift velocity
v_{G}	m/s	Group velocity
V_{BD}	V	Breakdown voltage
V_{F}	V	Forward bias
V_{FB}	V	Flatband voltage
V_{G}	V	Gate voltage
V_{D}	V	Drain voltage
V_{DS}	V	Drain-Source voltage
V_{H}	V	Hall voltage
V_{R}	V	Reverse bias
V_{S}	V	Source voltage
W	m	Width
W_{D}	nm	Depletion width
α		Diode ideality factor
β		Image force and static barrier lowering factor
γ		Minority carrier injection ratio
ΔE	eV	Energy range for TAT
ϵ	%	Strain
ε_0	As/Vm	Vacuum permittivity
ε_{s}		Relative permittivity of the semiconductor
$\varepsilon_{\mathrm{Ox}}$		Relative permittivity of the gate oxide
λ	nm	Characteristic scaling length
κ		Same as $\varepsilon_{\mathrm{Ox}}$
μ	$\mathrm{cm^2/Vs}$	Charge carrier mobility

ν	$1/s$	Photon frequency
ρ_c	$\Omega\,\mathrm{cm}^2$	Specific contact resistivity
σ	$1/(\Omega\mathrm{m})$	Conductivity
σ_t	m^2	Trap capture cross-section
τ_m	s	Scattering time
τ_n	s	Minority carrier life-time (electrons)
τ_p	s	Minority carrier life-time (holes)
$q\phi_{Bn0}$	eV	Ideal electron Schottky barrier height
$q\phi_{Bp0}$	eV	Ideal hole Schottky barrier height
$q\phi_B$	eV	Effective Schottky barrier height (p or n)
$q\phi_{B0}$	eV	Zero bias effective Schottky barrier height (p or n)
$q\phi_m$	eV	Workfunction of a metal
$q\phi_\mathrm{n}$	eV	Distance of semiconductor Fermi level to conduction band edge (for n-type)
$q\phi_\mathrm{p}$	eV	Distance of semiconductor Fermi level to valence band edge (for p-type)
Φ	V	Potential
$q\chi_\mathrm{S}$	eV	Semiconductor electron affinity
$q\psi_\mathrm{Bi}$	eV	Build in potential
$q\psi_\mathrm{Bp}$	eV	Distance of semiconductor Fermi level to intrinsic level (for p-type)
$q\psi_\mathrm{S}$	eV	Semiconductor band bending (surface potential)
$q\psi_\mathrm{S0}$	eV	Surface potential in a TFET for zero gate bias as a function of V_D

1 | Introduction

THE undamped trend of functionalization, diversification, omnipresence and performance enhancement in *Information & Communication Technology* (ICT) also known as the *Internet of Things* (IoT) lead and continuously leads to an enormous increase of data traffic. For example in 2015 the global internet traffic of 638 exabyte ($6.38 \cdot 10^{20}$ bytes/year) was equivalent to 26× the volume of the entire global internet in 2005. Until the end of 2020 this traffic is projected to reach $2.3 \cdot 10^{21}$ bytes/year [1]. At that same time only 29 % of the total internet traffic will be due to *Personal Computers* (PC)s while 44 % of all network devices are projected to be mobile connected [1]. Even though the continuous shrinking of conventional *Complimentary Metal-Oxide-Semiconductor* (CMOS) transistors - known as *Moore's law* - strongly reduced the power per computing operation, it is evident that the overall power consumption of ICT drastically increased within the last years [2]. More than that, with the release of the 7 nm node with 15 nm transistor gate length end of 2016 [3, 4] classic Si CMOS technology approaches its physical limits. This triggers materials innovation and a paradigm shift towards diversification and application driven computer architectures summarized under the term *More than Moore* technologies. Especially *quantum computing* [5] and *brain inspired/neuromorphic computing* [6] are promising approaches for certain objectives as efficient factorization, search algorithms or pattern recognition.

However the predominant portion of integrated systems in the IoT will still rely on classical logic operations that demand significant reduction in power consumption both at transistor level and for interconnects. Material innovation towards higher transistor channel mobilities is an evident but not trivial approach to maintain transistors on-current and switching speed while reducing the supply voltage. Strain engineering was the first approach to improve mobility in Si CMOS transistors. As this potential is exploited sustained effort is placed on the co-integration of Ge and III-V materials on the

well established Si platform enabling higher channel mobility to further reduce power consumption on the transistor level [7]. Also novel device concepts are intensively studied that enable a steeper transition between *off* and *on*-state than physically achievable with a classical *Metal-Oxide-Semiconductor Field-Effect Transistor* (MOSFET) and thereby allow significant supply voltage reduction well below 0.5 V. Among several approaches [8–11] the *Tunnel Field-Effect Transistor* (TFET) is one of the most prominent candidates for future energy efficient computing [10, 12]. At the same time ICT dissipates significant amount of energy in electrical interconnects [13]. Here a smart solution is the on-chip (*monolithic*) integration of a light source for optical-based on-chip and chip-to-chip communication [14]. Since Si is known to be an inefficient light emitter this again suggests the integration of III-V materials on Si which faces challenges though due to dissimilar mechanical properties, material quality and cost.

An alternate material approach is the novel all-group IV (Si)GeSn semiconductor family based on *Tin* (Sn). It was experimentally demonstrated that *Germanium Tin* (GeSn) is a direct bandgap semiconductor and for the first time allowed lasing in a group IV material [15], thereby unambiguously proofing its suitability for photonics with possible and starting from 2011 also partially demonstrated applications in *Light Emitting Diodes* (LED)s [16–19], detectors [20], gas sensors [21] or solar cells [22].

While the boon of a direct and engineered bandgap GeSn is evident for Si based photonics such alloys may also serve as a performance booster for electronic devices. The low and direct bandgap properties with a small conduction band effective mass suggest GeSn to be a promising material for TFETs allowing high *Band-to-Band Tunneling* (BTBT) rates [23, 24]. Also enhanced electron mobilities are projected [25, 26] and even proofed within the scope of this work. Last but not least the Si/Sn content depending lattice constant of SiGeSn can be utilized for strain engineering as source/drain stressors [27,28] or directly as strained channel [29]. First GeSn MOSFETs [30,31] and even TFETs were experimentally demonstrated within the last few years, starting in 2011 [32–37].

In short GeSn merges superior properties resulting from III-Vs direct bandgap with the intrinsic Si-compatibility of group IV materials allowing straight forward integration on the established Si platform. Epitaxially grown GeSn with high quality and especially direct bandgap is available since recent years only, enabling the unique possibility to study fundamental physical properties of a novel material. On the other hand all necessary steps to fabricate GeSn-based devices need to be developed or adapted and validated.

In this work the potential of GeSn for electronic applications is studied from fundamental material properties to complete devices including tunnel diodes, LEDs, MOSFETs and TFETs[1]. The thesis contains nine chapters. Relevant background and a brief literature overview is provided at the beginning of each of the seven main chapters. Following this preface, a general introduction into the (Si)GeSn material system is provided in CHAPTER 2. Subsequently individual modules that are essential for each transistor, such as surface manipulation, contact formation and high-κ/metal gate stack are studied in the CHAPTERS 3, 4 and 5, respectively. Special emphasis is placed on the characterization of high-κ/metal gate stacks on (Si)GeSn, particularly on the correlation of bandgap and minority carrier response. In CHAPTER 6 *p-i-n* diodes are evaluated both as LED and as tunnel diodes, the fundamental building block of any TFET. In this context the focus is placed on the capability of GeSn to enable direct BTBT. These studies lead to the experimental demonstration of vertical GeSn/Ge heterojunction TFETs in CHAPTER 7 in conjunction with a comprehensive analysis of the dominant transport mechanisms. In the last main chapter, CHAPTER 8 Hall measurements are presented to evaluate carrier mobility enhancement, carrier density and dominant scattering mechanism in GeSn. MOSFETs, also fabricated within the scope of this work will be not treated here. To that end it shall be referred to Ref. [26].
Finally CHAPTER 9 provides a brief summary of the present work and concludes its key results while giving an outlook of this fascinating emerging material system.

[1]Semiconductor processing and characterization were primarily conducted at PGI9 and HNF [38] of the FZ-Jülich, Germany. Experiments presented in CHAPTER 7 and partially in CHAPTER 5 & 6 were conducted during a research stay at the Suman Datta group at the University of Notre Dame, IN, USA.

2 | The (Si)GeSn material system

In this chapter fundamental properties of the novel (Si)GeSn semiconductor material system are introduced, while reviewing the key step stones of (Si)GeSn's rapid development within the recent past. First, changes in electronic band structure, effective mass and mobility are discussed, arising from strain and Sn/Si incorporation in the Ge-lattice. In the second part thermal stability and doping, both relevant for (Si)GeSn device fabrication are outlined.

The idea of incorporating Sn into Ge is to achieve a direct bandgap semiconductor in group IV and thereby complementing the indirect but well established Si-based technology. The band structure of the diamond lattice group IV materials *Silicon* (Si), *Germanium* (Ge) and α-*Tin* (α-Sn) are depicted in Fig. 2.1(a-c). Whereas Si and Ge are *indirect* semiconductors with their lowest conduction band minima at the X- and L-point respectively, α-Sn is a semi-metal and has a *direct* but negative bandgap. If one alloys Ge with Sn, the bandgap E_G shrinks. As a function of Sn content[1] the Γ-valley decreases faster than the L-valley and for a certain Sn content becomes the lowest conduction band minimum, thereby transforming the alloy into a fundamentally direct semiconductor. The Sn-dependent band structure can be calculated by using the alloy

[1] Sn content in this work is always denoted in atomic percent though is written in (% Sn) for simplicity. It is measured with *Rutherford Backscattering Spectrometry* (RBS) with an accuracy of $\pm 0.5\,\%$ Sn. RBS measurements performed by N. von den Driesch.

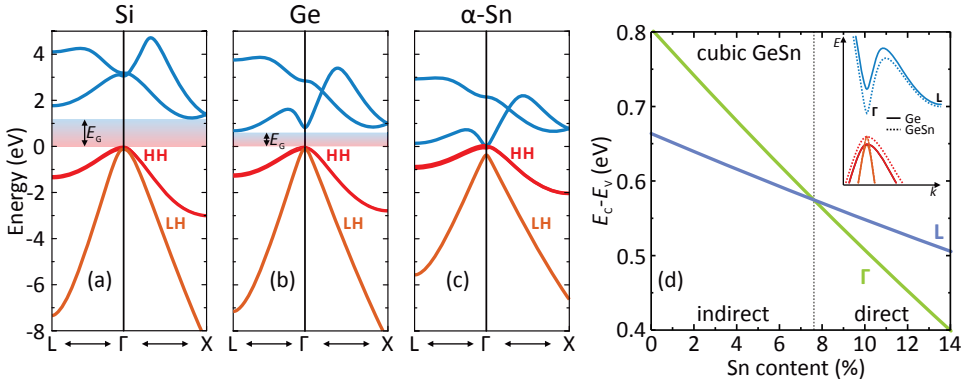


Figure 2.1.: *(a-c) Band structure of Si, Ge and α-Sn. Reprinted from Moontragoon et al. [41], with the permission of AIP Publishing. (d) k.p calculated direct and indirect bandgap of unstrained (cubic) GeSn as a function of Sn content. The inset depicts the DFT-calculated dispersion of Ge and* $Ge_{0.89}Sn_{0.11}$.

bowing factors, deformation potentials, and (at Γ) eight-band $\boldsymbol{k} \cdot \boldsymbol{p}$ theory[2] [39]. The accordingly calculated bandgaps at Γ and L-point are depicted in Fig. 2.1(d). Comprehensive theoretical investigations of the (Si)GeSn band structure are provided in Refs. [40–42].

The possibility of a direct bandgap and enhanced mobility in Sn alloyed Ge, *i.e.* GeSn was first proposed by Goodman in 1982 [43] though it was not clear at that time whether this material could be synthesized and if it features the proposed properties. While the first experimental report of single crystalline GeSn was published only five years later in 1987 [44], it took another 28 years until 2015 Wirths *et al.* [15] experimentally proofed the transition from a fundamentally *indirect* to a fundamentally *direct* semiconductor for $Ge_{1-x}Sn_x$ with Sn contents above $x \approx 0.08$ as later confirmed also by further studies [45, 46].

Prior to this breakthrough significant challenges in epitaxial growth hampered the realization of GeSn epilayers with sufficiently high Sn content, thickness and material quality. One main challenge in GeSn growth and processing is the low solid solubility of Sn in Ge $< 1\,\%$. As a consequence $Ge_{1-x}Sn_x$ with $x > 0.01$ is thermodynamically metastable and Sn tends to diffuse, segregate or precipitate as tetragonal β-Sn during

[2] I gratefully acknowledge the support with band structure and mobility calculations performed by Z. Ikonic, University of Leeds, UK.

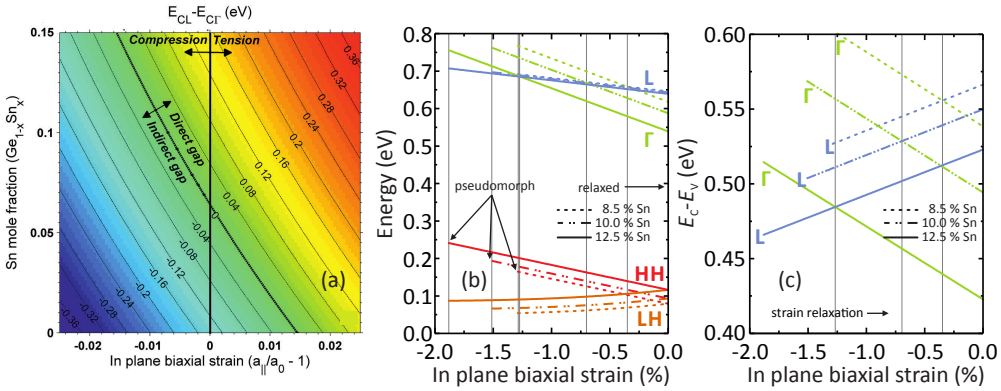


Figure 2.2.: *(a) Contour plot of the directness ($E_{CL} - E_{C\Gamma}$) as a function of Sn content and in plane biaxial strain. Reprinted from Gupta et al. [42], with the permission of AIP Publishing. (b) Band energies and (c) bandgaps at Γ and L vs. strain from pseudomorphically grown on Ge to fully relaxed. Vertical lines in (b) and (c) are guides to the eye.*

growth or subsequent thermal treatment. Only the implementation of *Chemical Vapor Deposition* (CVD) permitted non-equilibrium growth with sufficiently high growth rates that finally enabled epitaxial growth of direct bandgap GeSn. Details regarding (Si)GeSn CVD epitaxy can be found in the following comprehensive works [47–53]. A review is provided in [54].

Despite the Sn content, strain[3] is the second parameter defining the GeSn band structure. α-Sn, Ge and Si have significantly different lattice constants of 6.493 Å, 5.658 Å and 5.431 Å, respectively. While the lattice constant of GeSn lies in between the values of Ge and Sn, GeSn grown on Si or Ge is initially highly compressively strained and plastically relaxes when exceeding a certain critical layer thickness. In fact GeSn with high material quality could be only achieved if grown on Ge not on Si as the lattice missmatch to Si is even larger. If not other specified the GeSn layers studied in this work were grown[4] [52] with an AIXTRON Tricent *Reduced Pressure CVD* (RPCVD) tool on *Ge Virtual Substrate* (GeVS), which are thick, strain relaxed Ge buffer layers grown on 200 mm Si (001) wafers in a different reactor [55][5].

In the band structure compressive strain opposes the goal of a direct bandgap. It lifts

[3]Experimentally strain is always evaluated by *X-ray Diffraction* (XRD) reciprocal space mapping in this work. Reciprocal space maps recorded by G. Mussler.

[4]I gratefully acknowledge the (Si)GeSn growth performed by N. von den Driesch and S. Wirths.

[5]The supply with GeVS by J.M. Hartmann from CEA-Leti, France is greatly appreciated.

up the Γ-valley while diminishing the L-valley. The calculated difference between L and Γ-valley as a function of Sn content and in plane biaxial strain is plotted in Fig. 2.2(a). Negative strain values correspond to compressive, positive strain values correspond to tensile strain. The stronger the compressive strain, the higher Sn content is necessary to achieve a direct bandgap (*i.e.* positive difference of L and Γ-valley energy $E_{\mathrm{CL}} - E_{\mathrm{C}\Gamma}$). Since the lattice constant of unstrained (cubic) GeSn increases with Sn content also the compressive strain in pseudomorphically (coherently) grown GeSn on Ge gets stronger with Sn content, additionally hampering the goal of a direct bandgap as demonstrated in Fig. 2.2(b,c). Thus thick, strain relaxed GeSn is needed to achieve a direct bandgap. The growth of such layers was reported [50, 53].
The incorporation of Si towards ternary SiGeSn has the opposite effect to the incorporation of Sn and leads to an increase of the bandgap with a strong up-shift of the Γ-valley. It thereby provides an additional degree of freedom in the design of bandgap engineered heterostructures and allows to decouple the effect of Sn content and layer strain to some extend. Details regarding SiGeSn growth can be found in the following references [52, 56–58].

2.1. GeSn effective mass and mobility

A comprehensive study of GeSn band structure including effective mass calculations was provided by Lu Low *et al.* [59]. The effective masses m^* of the relevant conduction and valence bands in the center of the Brilloin zone, Γ, *light hole* (LH) and *heavy hole* (HH) are plotted in Fig. 2.3(a,b) as a function of Sn content for electrical transport along the main axes x = [100], y = [010], z = [001] which are equivalent in cubic (unstrained) GeSn. For the L-valley the ellipsoid of constant energy is [111] oriented. Here the longitudinal mass is plotted against Sn content. The L-valley mass along x,y or z direction is calculated as $m^*_{\mathrm{L},xyz} = 3m^*_{\mathrm{Ll}}m^*_{\mathrm{Lt}}/(2m^*_{\mathrm{Ll}} + m^*_{\mathrm{Lt}})$. A clear decrease of the considered effective masses with increasing Sn content is observed and thereby suggests GeSn as high-mobility semiconductor, as first theoretically studied by Sau and Cohen in detail [25]. The reduction of the transverse L-electron effective mass is negligible. It is rather constant at $m^*_{\mathrm{Lt}} = 0.08\,\mathrm{m_e}$, where $\mathrm{m_e}$ is the free electron mass. As a consequence also $m^*_{\mathrm{L},xyz}$ only marginally changes with a value around $0.12\,\mathrm{m_e}$. However the most significant change occurs when going from indirect to direct GeSn considering the large difference between Γ- and L-valley effective masses. Thus especially

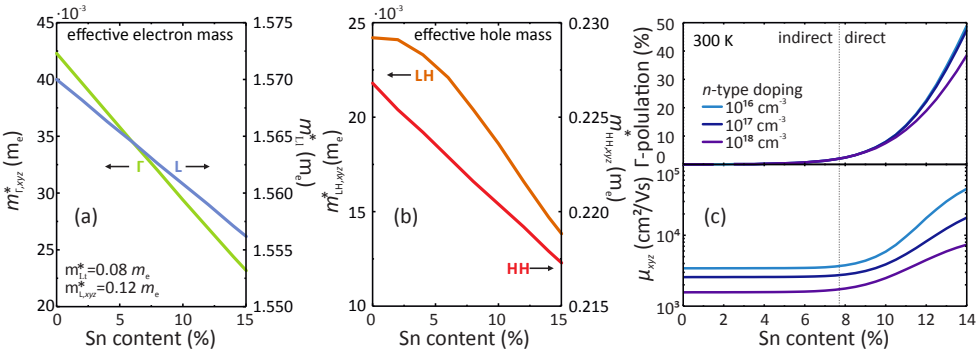


Figure 2.3.: *(a,b) Effective carrier masses of* Γ*-, L-, LH- and HH-band as a function of Sn content; As zero strain is assumed the masses are identical for* x, y, z *i.e. [100],[010],[001] direction. For L-valley l=longitunial, t=transversal to [111] direction. (c) Mobility (lower panel) and* Γ*-valley population (upper panel) vs. Sn content for cubic (unstrained) GeSn.*

as soon as the Γ-valley is significantly populated, high electron mobilities comparable to those of III-V materials are expected. This is demonstrated in Fig. 2.3(c) showing the mobilities calculated for unstrained GeSn *vs.* Sn content, together with the relative population of the Γ-valley for different n-type doping concentrations. The calculations use the computed band structure parameters and follow the approach by Fu *et al.* [60] considering phonon, deformation potential, alloy disorder, ionized impurity, and intervalley scattering. Here the low effective mass of the Γ-valley has a second positive effect on the mobility. It is connected with a low Γ-valley *Density of States* (DOS). Since scattering processes as ionized impurity scattering, acoustic phonon scattering, alloy disorder scattering and defect scattering depend on the DOS, the Γ-valley is less sensitive towards such scattering processes. It should be noted though, that a low DOS might also implicit quantization issues. Other scattering processes are not present at all in the Γ-valley, such as optical phonon scattering which is forbidden and Γ-Γ intervalley scattering since there is just one Γ-valley compared to eight as for the L-valley.

However there is one scattering process that strongly limits the overall mobility of even slightly direct GeSn. This is Γ-L-valley intervalley scattering which is particularly present if the Γ-L-valley energy separation is less than a few $k_\mathrm{B}T$ with k_B being the Boltzmann-constant and T being the temperature in K. Furthermore the high L-valley DOS leads a significant L-valley population for just slightly direct GeSn which additionally limits the mobility. Thus the Γ-L-valley separation should be as high as

possible to populate the Γ-valley and benefit from its high Γ-electron mobilities.
It should be noted that the calculations presented here denote the ideal mobility without considering scattering at defects present in the epilayer. Thus these values should be seen as the theoretical upper limit achievable with GeSn. In CHAPTER 8.3 enhanced mobility in GeSn compared to Ge is experimentally demonstrated (though smaller than the theoretical limit).

2.2. Thermal stability and doping

The metastability of GeSn with Sn contents > 1 at.% results in a reduced thermal stability that does not allow process temperatures as commonly used in SiGe or Ge technology. Too high thermal treatment results in Sn diffusion, metallic β-Sn precipitations and Sn-segregation at interfaces [61]. As a rule of thumb the growth temperature gives a good indication of the thermal stability range. The epilayers used in this work were grown at temperatures between 350 °C (12.5 at.% Sn) and 400 °C (3 at.% Sn). For SiGeSn the thermal stability seems to be higher compared to binary GeSn even for the same Sn content (*cf.* CHAPTER 5.2) and Ref. [62].
Another consequence of the metastability of GeSn is the fact that classic ion-implantation of high doses cannot be used for *p*- and *n*-type doping since annealing experiments conducted within the scope of this work showed that implantation-induced amorphization cannot be recrystalized by thermal annealing. Worse than that, even for implantation doses below the amorphization limit, the implantation damage further reduces the thermal stability. A suitable way to achieve *p*- and *n*-type doping with high activation and crystalline quality was demonstrated to be *in-situ* doping during the epitaxial growth of GeSn [63, 64]. To that end *di-borane* (B_2H_6) and *phosphine* (PH_3) were utilized, respectively.
Un-doped GeSn is *p*-type presumably due to defects as vacancies or dislocations. This un-intentional background doping is in the mid $10^{16}\,cm^{-3}$ to mid $10^{17}\,cm^{-3}$ range. It decreases with the layer thickness and increases with Sn content as also studied in CHAPTER 8.
Peculiarties in the chemical stability of GeSn will be treated in the next chapter.

3 | GeSn Surface Composition and Manipulation

As reviewed in Chapter 1 GeSn is a relatively new material. First experimental studies on devices like planar transistors or LEDs were reported in 2011 [16, 17, 32, 33]. The recently proofed direct bandgap properties of GeSn [15] urged for more advanced structures such as waveguides or suspended microdiscs to study optical properties and lasing of GeSn. Also to investigate the electronic properties of GeSn and to integrate the material in advanced FET devices, structures as free standing nanowires, vertical fins or suspended lamellas were desired. However, as a novel material the surface properties and manipulation such as chemical stability, (selective) wet and dry etching, cleaning and native oxide removal were marginally studied.

In this chapter the GeSn surface composition after different wet and dry chemical treatments is analyzed *via X-ray Photoelectron Spectroscopy* (XPS). First cleaning and native oxide removal are studied, which are crucial for achieving a good interface to the gate dielectric when integrating GeSn into a transistor. Furthermore it is important to reduce surface currents for electrical and surface recombination for optical purposes.

In the second part (un)selective (un)isotropic wet and dry etching processes are studied. A highly selective dry etch process with etch rate ratios of Ge to GeSn of >250:1

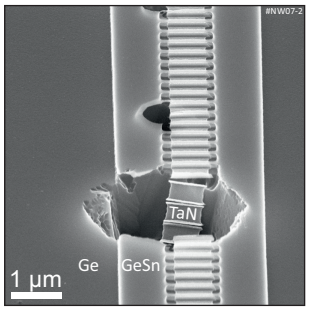


Figure 3.1.: *Tilt-view SEM image of a* HfO_2 *passivated GeSn nanowire array after exposure to* NH_4OH:H_2O_2 *demonstrating excessive material loss if the passivation is slightly discontinuous.*

was developed which resulted in the first optically pumped GeSn microdisc laser [65]. The etching mechanism giving rise to such high selectivities was identified *via* surface composition analysis with XPS.

3.1. Surface Cleaning and Native Oxide Removal

A standard Si cleaning procedure also known as RCA clean, consists of the following steps: (i) H_2SO_4:H_2O_2:H_2O known as *Piranha* to oxidize the surface and remove organic contamination and particles. (ii) Removal of organic contamination and particles in NH_4OH:H_2O_2:H_2O called *Standard Clean 1* (SC-1). (iii) Removal of metallic contamination with HCl:H_2O_2:H_2O *Standard Clean 2* (SC-2). If applicable the oxide that builds up during these steps is removed with *hydrofluoric acid* (HF).
However, GeSn is a Ge-like material and thus underlies similar constrains regarding its chemical stability. Since GeO_2 is water soluble [66], highly oxidizing solutions relying on H_2O_2 such as Piranha, SC-1 or SC-2 that are commonly used in Si-technology cannot be employed for Ge(Sn) as they would result in excessive material loss with etch rates $>$ 100 nm/min [67]. This is impressively but unintentionally demonstrated in the *Scanning Electron Microscopy* (SEM) image in Fig. 3.1. Here a TaN gate metal was meant to be etched on a HfO_2 passivated GeSn nanowire array, with a NH_4OH:H_2O_2-based solution. Only a tiny pinhole in the HfO_2 passivation resulted in excessive material loss of the unterlying GeSn and GeVS.
As an alternate approach Brunco *et al.* proposed the use of solvents for removal of

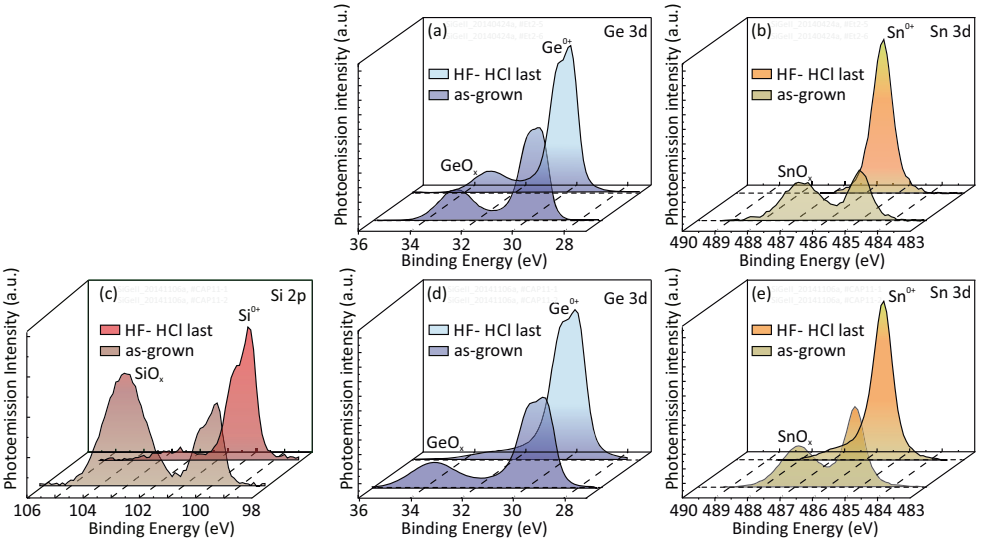


Figure 3.2.: *XPS surface analysis of* $Ge_{0.915}Sn_{0.085}$ *(a,b) and* $Si_{0.1}Ge_{0.81}Sn_{0.09}$ *(c-e) prior to and after "HF:HCl last" cleaning. Thanks to the cleaning the* SiO_x, GeO_x *and* SnO_x *peak intensities are reduced significantly. The transfer to the XPS tool occurred ex-situ.*

organic contamination on Ge [67]. Based on this proposal and following a pre-high-κ deposition cleaning study presented by Gupta *et al.* [68] the following cleaning procedure was employed in this work:

(i) In order to replace *Piranha*, organic contamination and particles are removed in an ultrasonic bath at 60 °C with *Dimethyl Sulfoxide* (DMSO):cyclopentanone (10:3). Thanks to the comparably high density of DMSO the risk of partical redeposition is reduced compared to standardly used acetone. (ii) Possible remnant organic contaminations are removed and an oxide is created in an oxygen-based *Inductively Coupled Plasma* (ICP). (iii) Possible metallic contaminations and the native $GeSnO_x$ are removed with a mixture of HF:HCl (1 % aq.,1 % aq.) without water rinse ("HF-HCl last"). This step is important since Sn oxides can be conductive [69] and thereby could degrade the electrical characteristics of a MOS stack fabricated on GeSn.

The effectiveness of $GeSnO_x$ oxide removal was studied with XPS[1]. This technique relies on the external photo effect. The sample is irradiated with X-rays (in this case

[1]XPS-spectra recording by A. Besmehn and H. Hartmann, ZEA-3, FZ-Jülich is acknowledged.

from the Al K_α line at 1486.7 eV) liberating electrons from the core *s*- and *p*-shells. Since the energy levels of these shells are element specific, a spectroscopic analysis of the photo electron energy spectrum allows to study the elemental composition of the irradiated sample. The core levels slightly shift depending on the chemical bonding of the elements. Thus this technique also yields information on the oxidation state of the detected elements. The detection depth is limited to the escape depth of the photo electrons which is in the range of a few nm. As a consequence XPS is primarily sensitive towards surface composition and surface chemistry.
$Ge_{0.915}Sn_{0.085}$ and a $Si_{0.1}Ge_{0.81}Sn_{0.09}$ were cleaned with the above described procedure. After the HF-HCl-last clean the samples were sealed in nitrogen atmosphere and transferred to the XPS analysis tool as fast as possible, albeit a certain exposure to ambient was unavoidable. The core level spectra of the $Ge_{0.915}Sn_{0.085}$ and a $Si_{0.1}Ge_{0.81}Sn_{0.09}$ samples prior to and after HF-HCl-last clean are depicted in Fig. 3.2. For Si the 2*p* and for Ge and Sn the 3*d* levels are shown. As the sample transfer occurred *ex-situ* the C1s peak at 285.0 eV could be used as a reference. A Shirley background [70] is subtracted from the measurement data in the depicted spectra. The peak positions were assigned to their corresponding chemical elements and compositions by comparison with literature data provided in the NIST data base [71]. Where the as-grown samples show all three elements both in oxidized and in an un-oxidized state, after the wet clean the SiO_x and SnO_x peaks are nearly completely removed and GeO_x is significantly reduced demonstrating the effectiveness as native oxide removal *e.g.* for pre-high-κ deposition cleaning implemented in CHAPTER 5.2.
Comparing the area of the different peaks allows to extract the stoichiometry of the elements in their different oxidation states. The stoichiometry of the 0+ oxidation states of the cleaned samples roughly matches with the "bulk composition" of the alloys obtained by RBS. However, the ratio of Si:Ge:Sn in the $SiGeSnO_x$ is significantly different. In the oxide an increased Si content and a reduced Ge content is observed $(Si_{0.2}Ge_{0.72}Sn_{0.07})O_x$. This is inline with the higher stability of SiO_2 compared to GeO_2 due to a 70 % higher binding energy of SiO_2 [72].

3.2. (Selective) Etching of GeSn

In this section different wet and dry etching processes are analyzed in terms of selectivity between Ge and GeSn. In order to realize suspended GeSn structures such as

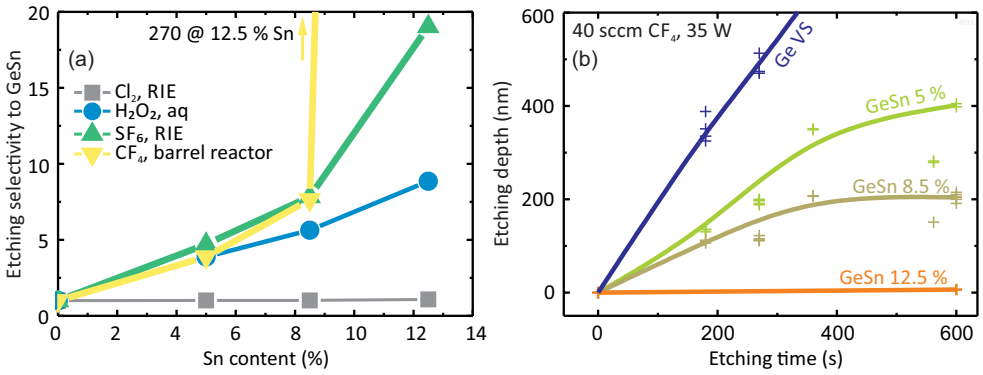


Figure 3.3.: *(a) Etching selectivity to Ge vs. Sn content for several etchants. (b) Etching depth vs. etching time for (Ge)Sn with different Sn contents in CF_4-Plasma.*

free standing nanowires or micro disc resonators a process is needed to remove GeVS selectively below a GeSn layer. The etching selectivity is studied as a function of Sn content while the selectivity mechanism is analyzed *via* XPS surface analysis. Cheng *et al.* [73] previously used a strongly diluted SC-1 solution to etch Ge selectively over GeSn. Gupta *et al.* [74] developed a CF_4 *Radio Frequency* (RF) *Reactive Ion Etching* (RIE) process with significantly higher etching selectivity. In the meantime several studies using similar approaches are reported [75–77]. Fig. 3.3(a) shows the ratio of Ge and GeSn etch depth defined as the etching selectivity to GeSn for several etchants as a function of Sn content. Where a Cl_2-based plasma etch processes shows no selectivity a selectivity of 9:1 is observed for H_2O_2:H_2O (1:10) after 15 min etching. In fluorine-based dry etch processes significantly higher etching sensitivities can be achieved. For 12.5 % Sn a selectivity of ≈ 270 was achieved after 10 min, 40 sccm CF_4 dry etching at 35 W. Here an *Inductively Coupled Plasma* (ICP) with a Faraday cage was utilized in a so called barrel reactor, in order to reduce ion-bombardment and to increase the chemical component of the plasma which essentially defines the etching selectivity. Fig. 3.3(b) shows the etching depth *vs.* etching time in this CF_4 plasma for several GeSn epilayers with different Sn content. Whereas for the GeVS a linear increase of the etching depth is observed, for GeSn the etching rate is not constant it decreases with time while the etching depth saturates. This effect becomes stronger for increased Sn content. The observation suggests the formation of a passivation layer during the etch process that inhibits further surface reactions.

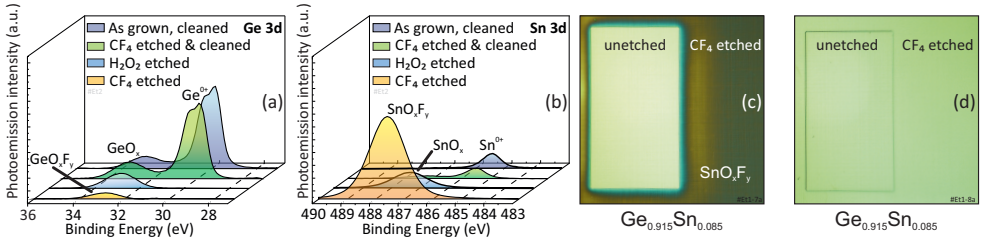


Figure 3.4.: *(a,b) XPS analysis of selective Ge/GeSn etching. (a) Ge3d core level spectra showing the removal of Ge from the sample surface after H_2O_2 or CF_4 etching. (b) On the contrary the Sn3d signal is significantly stronger after H_2O_2 or CF_4 etching. During etching SnO_x or rather SnO_xF_y agglomerate at the surface. After HF-HCl cleaning the passivation layer is removed and the original surface is restored. (c,d) Optical microscopy image of the $Ge_{0.915}Sn_{0.085}$ surface after* 10 min *CF_4 at* 35 W *and after subsequent HF:HCl wet-cleaning.*

XPS is utilized to gain deeper insight into the surface reactions during the etch process and to understand the origin of the etch selectivity. Fig. 3.4(a,b) show the Ge3*d* and the Sn3*d* core level spectra of $Ge_{0.915}Sn_{0.085}$ after different chemical treatments. After CF_4 or H_2O_2 treatment both Ge and Sn at the surface only exist in the oxidized/fluoridized state. The peak energies agree with GeO_xF_y, SnO_xF_y and GeO_x, SnO_x respectively. The surface and subsurface layer do not contain any Ge^{0+} and Sn^{0+}. What is striking, is that after etching the Ge peak is significantly reduced whereas the Sn peak strongly increased, compared to the HF-HCl wet cleaned surface. From core level peak fitting one can deduce the surface stoichiometry. After H_2O_2 treatment the Ge:Sn ratio is 1:1 whereas after CF_4 dry etching a ratio of 1:8 was observed compared to approx. 11:1 in the $Ge_{0.915}Sn_{0.085}$ bulk. That is, Sn strongly agglomerates at the surface during the etching process. Based on these observations and in line with Gupta *et al.* [74] the following mechanism is suspected as origin for the high etching selectivity in the CF_4 plasma:

During the plasma process CF_4 dissociates and forms highly reactive CF_x and F radicals that attack the Ge(Sn) surface. While GeF_4 is gaseous, SnF_y is a solid. As a consequence Ge-containing reaction products desorb from the surface whereas solid SnF_y agglomerates at the surface and thus hampers further surface reactions. It is evident that this effect becomes stronger for higher Sn content and thereby gives rise to the high etching selectivity. In order to achieve even higher selectivities ion energy and mean free path in the plasma should be low to avoid sputtering of the SnF_y passivation layer. In this

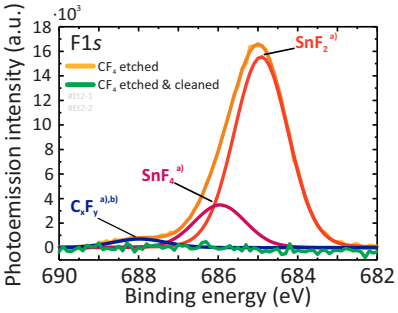


Figure 3.5.: *F1s peak of a* CF_4 *etched* $Ge_{0.915}Sn_{0.084}$ *sample prior to and after HF:HCl cleaning. Thanks to the wet clean* SnF_y *is completely removed and no F is detected after cleaning. Peak positions are taken from literature a) [71], b) [74].*

work this was realized by using an ICP with a Faraday cage. The mean free path can be reduced by increasing the pressure. Here a maximum pressure of 0.132 mBar could be used corresponding to a CF_4 flow of 40 sccm. The mechanism for the etching selectivity in the H_2O_2-based wet chemical solution is similar. The peroxide oxidizes the surface and forms GeO_x and SnO_x. Since GeO_2 is water soluble it is selectively removed from the surface while the SnO_x agglomerates at the surface and protects the sample against further etching.

After etching it is important to be able to remove the SnO_xF_y or SnO_x passivation layer and to restore the original surface. It is demonstrated that this can be achieved by using the HF:HCl (1 % aq., 1 % aq.) wet clean. Fig. 3.4(a,b) show nearly identical Ge3*d* and Sn3*d* spectra, for the "as grown and cleaned" sample and for the "CF_4 etched and cleaned" sample, respectively. Observing the surface with an optical microscope visually demonstrates formation and removal of the SnO_xF_y passivation layer as shown in Fig. 3.4(c,d). The F1*s* spectrum in Fig. 3.5 proofs the complete removal of F containing compounds from the surface thanks to the HF:HCl clean.

Fig. 3.6 depicts several SEM images of structures fabricated with the above discussed processes. In Fig. 3.6(a) a $Ge_{0.875}Sn_{0.125}$ micro disc is first etched using an unselective anisotropic Cl_2/Ar dry etch process and subsequently underetched using CF_4 as shown in Fig. 3.6(b). This structure was utilized for the first demonstration of an optically pumped group IV micro disc laser [65, 78]. Furthermore, suspended GeSn waveguides and nanowires are shown in Fig. 3.6(c,d). Finally the high etching selectivity of the CF_4 process is demonstrated in Fig. 3.7 depicting a *Cross sectional TEM* (XTEM) of a GeSn

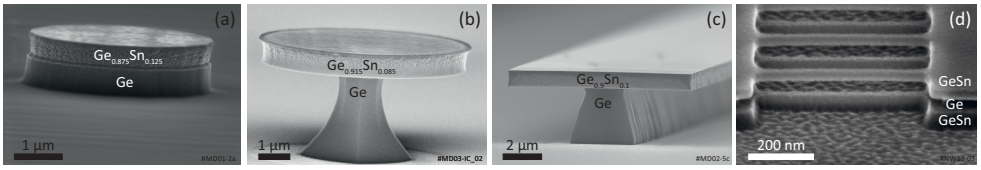


Figure 3.6.: *SEM images of GeSn structures fabricated for photonic and electronic applications. (a) GeSn micro disc after vertical Cl_2/Ar mesa etch, (b) GeSn micro disc after additional selective CF_4 etching of the GeVS, (c) suspended GeSn waveguide, (d) free standing GeSn nano wires. The Ge interlayer between the strain relaxed GeSn buffer and the top GeSn layer was removed selectively with CF_4 dry and H_2O_2 wet etching.*

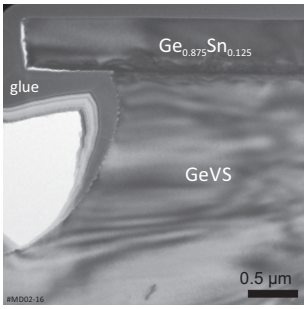


Figure 3.7.: *TEM cross section of a $Ge_{0.875}Sn_{0.125}$ micro disc demonstrating the high etching selectivity of the CF_4 dry etch process. TEM analysis by Steffi Lenk is greatly acknowledged.*

microdisc. While an undercut of several hundred nanometer in the Ge is created, the GeSn is attacked negligibly. Measured etch rates of GeSn exposed to various etchants are tabulated in Appendix B.

3.3. Summary

GeSn surface composition was studied with XPS prior to and after HF:HCl wet cleaning. Effective native oxide removal, necessary for pre-high-κ deposition cleaning was demonstrated. In the second part of the chapter dry and wet chemical processes for GeSn nanostructure fabrication were studied. Both unselective anisotropic and highly selective isotropic processes were presented etching Ge selectively towards GeSn with selectivities > 250. A SnOF/ SnO surface passivation mechanism was identified *via* XPS surface analysis as origin of the etching selectivity in F-based plasmas and H_2O_2-based wet chemical solutions.

4 | NiGeSn alloys as contacts for GeSn

In order to connect any electrical or opto-electronical device to external circuitry a *Metal-Semiconductor* (MS) contact is needed. Ideally, it should posses negligible resistance compared to the resistance of the device and feature linear (Ohmic) *Current Voltage* (IV) characteristics. A key parameter that controls the electric properties of a MS contact is the potential barrier that forms at the MS interface and is denoted as *Schottky barrier* after Walter Schottky who provided fundamental understanding of such systems [79]. To achieve a low resistance contact the *Schottky Barrier Height* (SBH) indeed should be as low as possible while the doping of the semiconductor should be as high as possible.

In this chapter *Nickelstanogermanide* (NiGeSn) alloys as contacts for GeSn-based devices are studied. First the NiGeSn itself is structurally and stoichiometrically analyzed by *X-ray Diffraction* (XRD) and TEM while its sheet resistance is measured with the

Van der Pauw technique [80]. Then the SBH forming at the NiGeSn/GeSn interface is measured with the activation energy method. Finally *Dopant Segregation* (DS) is employed as a technique to tune the SBH and to achieve Ohmic contacts.
The results presented in this chapter are an excerpt of a comprehensive study, recently published in *Journal of Applied Physics* (JAP) [81].

4.1. Metal-Semiconductor Contacts

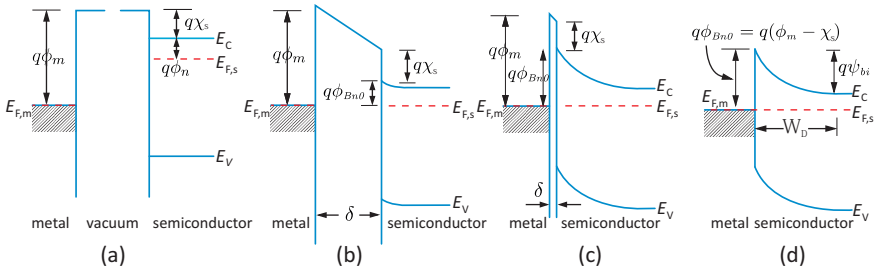


Figure 4.1.: *Formation of a Schottky barrier at a MS interface: (a) metal and semiconductor are not in electric contact. The bands align with respect to the vacuum level. (b) Electric contact aligns the Fermi levels in metal and semiconductor. (c) The gap δ is reduced and finally vanishes (d). From [82].*

First an ideal MS contact is considered *i.e.* assuming the absence of any interface/surface states or other anomalies following the comprehensive description in [82]. A band diagram representing the situation if a metal comes into contact with a semiconductor is depicted in Fig. 4.1. In a gedankenexperiment metal and (n-type) semiconductor are first separated. The position of the Fermi levels with respect to the vacuum level are then given by the work function $q\phi_\mathrm{m}$ and $q(\chi_\mathrm{S} + \phi_n)$ of metal and semiconductor, respectively. $q\chi_\mathrm{S}$ is the semiconductor electron affinity and $q\phi_n$ is the distance of the Fermi level from the conduction band [Fig. 4.1(a)]. q is the elementary charge. As soon as metal and semiconductor are in electrical contact the Fermi levels align. Thanks to the significantly higher DOS in the metal, the Fermi level on this side of the junction barely changes while the Fermi level in the semiconductor is reduced by the difference in the two work functions. Due to the higher electron affinity in the metal, electrons diffuse from the semiconductor into the metal while leaving behind ionized impurity centers within a certain depletion width W_D. This creates a built-in electric field which

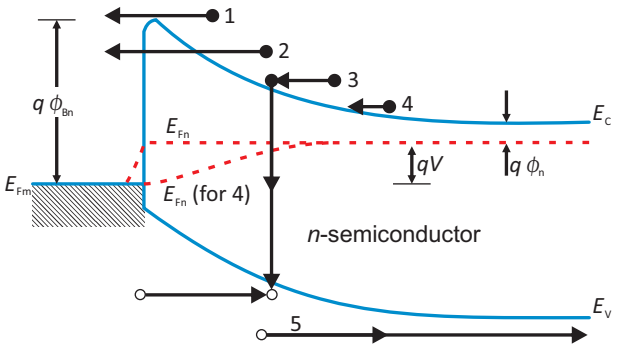


Figure 4.2.: *Transport mechanisms in a forward bias Schottky contact: (1) Thermionic emission, (2) Tunneling, (3) Recombination, (4) Diffusion of electrons, (5) Diffusion of holes. From [82].*

in turn bends up the electronic bands in the semiconductor and counteracts the electron diffusion until thermal equilibrium is restored [Fig. 4.1(d)]. Finally electrons in the metal see the *electron Schottky Barrier Height* (eSBH) $q\phi_{Bn0} = q(\phi_\mathrm{m} - \chi_\mathrm{s})$ while the electrons in the semiconductor see the built-in potential $q\psi_\mathrm{Bi} = q(\phi_{Bn0} - \phi_n)$. The description for a p-type semiconductor is analogous. In this case the *hole Schottky Barrier Height* (hSBH) is given by $q\phi_{Bp0} = E_\mathrm{G} - q(\phi_m - \chi_\mathrm{s})$. Thus for a given semiconductor-metal combination electron and hole SBH add up to the bandgap of the semiconductor (in the idealized case):

$$E_\mathrm{G} = q(\phi_{Bp0} + \phi_{Bn0}) \; . \tag{4.1}$$

The ideal SBH is defined by the material choice but can also be influenced by other effects such as interface states. When applying an external voltage V the potential barrier is modified accordingly $\psi_\mathrm{Bi} - V$. Depending on the polarity it either increases or decreases and thereby hampers or promotes electronic transport giving rise to diode/rectifying behavior. In this case the MS contact is called Schottky diode. On the contrary, if the SBH is very small or the doping in the semiconductor is very high, which causes a very small depletion width W_D and in turn promotes tunneling of carriers through the barrier, the *Current Voltage* (IV) characteristics of a MS contact can become linear. An Ohmic contact is achieved.

4.1.1. Electronic Transport in Metal-Semiconductor Contacts

Following the description by Sze and Ng [82], five transport mechanisms across a MS contact can be identified as sketched in Fig. 4.2 which are relevant under different conditions:

(1) *Thermionic emission* above the SBH is the dominant process for most moderately doped ($\leq 1 \cdot 10^{17}\,\mathrm{cm}^{-3}$) Si or GaAs Schottky diodes at room temperature. That is, in contrast to a *p*-*n* junction transport across an ideal Schottky contact is primarily dominated by majority carriers, which (thanks to the fast response of majority carriers) led to the common application in high-frequency technology.

(2) For highly doped semiconductors the depletion width W_D is short enough to allow the carriers to quantum mechanically tunnel through the barrier without the need of being thermally excited above. Especially if thermionic emission is suppressed at low temperatures, *tunneling* through the barrier dominates. In Si-Au contacts, the tunneling current exceeds the thermionic current for $N \geq 1 \cdot 10^{18}\,\mathrm{cm}^{-3}$ at room temperature. Since tunneling increases for reduced effective carrier masses, in case of GeSn with its significantly smaller electron and hole effective masses compared to Si (*cf.* CHAPTER 2), tunneling is expected to dominate the MS current for significantly smaller doping levels. Tunneling dominated transport is important to achieve Ohmic contacts as it does not show rectifying behavior.

(3) *Recombination* of carriers within the space charge region, which is the same process as in a classical *p*-*n* diode.

(4) *Diffusion* of electrons is applicable for low mobility semiconductors.

(5) Holes injected from the metal diffuse into the semiconductor, which is equivalent to recombination within the neutral region. This *diffusion* of minority carriers (here holes) is also denoted as *minority carrier injection*. For Si Schottky diodes this effect is not relevant under low bias conditions since the ratio γ of minority and majority current is in the 10^{-5} range [82]. However, γ depends quadratically on the intrinsic carrier concentration n_i which in turn exponentially increases when reducing the bandgap [82]. n_i is in the $10^{10}\,\mathrm{cm}^{-3}$ for Si compared to 10^{13} to mid $10^{14}\,\mathrm{cm}^{-3}$ range for GeSn. Thus minority carrier injection might become relevant for Ge(Sn) as expected by Green and Shewchun [83].

The classical *thermionic emission* current was derived by Hans Bethe [84] under the assumption that the SBH $q\phi_B$ is significantly higher than $k_\mathrm{B}T$ and that the MS contact is in thermal equilibrium which in turn is not affected by the current flow. The derived expression for the current density J_n in case of a n-type semiconductor with applied bias V is

$$J_n = A^* T^2 \exp\left(-\frac{q\phi_{Bn}}{k_\mathrm{B}T}\right)\left[\exp\left(\frac{qV}{k_\mathrm{B}T}\right) - 1\right] , \tag{4.2}$$

with the effective Richardson constant

$$A^* = \frac{4\pi m^* k_\mathrm{B}}{h^3} . \tag{4.3}$$

h is the Planck-constant. For a p-type semiconductor equation 4.2 is multiplied with (-1), ϕ_{Bn} is replaced by ϕ_{Bp} and qV is replaced by $-qV$. While equation 4.2 only captures transport *via* thermionic emission, a unified expression, the *thermionic-emission-diffusion theory* also considers contribution from diffusion and quantum mechanical reflection at and tunneling through the barrier. In the consequential modified expression of equation 4.2 the effective Richardson constant A^* is replaced by the reduced effective Richardson constant A^{**} which captures these deviations.

Further generalization of equation 4.2 can be phenomenologically achieved by introducing an ideality factor α to also capture recombination and contribution from quantum mechanical tunneling if this becomes dominant for high doping. Thus the term $\exp(qV/k_\mathrm{B}T)$ is replaced by $\exp(qV/\alpha k_\mathrm{B}T)$.

Finally the SBH itself can also be influenced by both built-in and applied electric field within the MS contact, especially when it is in high reverse bias. This effect is denoted as *image force lowering*. Also dipole interaction of metal and semiconductor can induce a *static lowering* of the SBH even at zero bias. As a consequence the SBH roughly linearly depends on the voltage in reverse bias.

Considering the above extensions to the ideal thermionic emission one can define two separate expressions of the current for absolute values of reverse V_R and forward bias V_F which is valid for $|V| > 3k_\mathrm{B}T/q$ for both p- and n-type semiconductors.

$$J_\mathrm{R} = A^{**} T^2 \exp\left(-\frac{q(\phi_{B0} + \beta V_\mathrm{R})}{k_\mathrm{B}T}\right) , \tag{4.4}$$

$$J_\mathrm{F} = A^{**} T^2 \exp\left(-\frac{q\phi_{B0}}{k_\mathrm{B}T}\right)\exp\left(\frac{qV_\mathrm{F}}{\alpha k_\mathrm{B}T}\right) . \tag{4.5}$$

Here $q\phi_{B0}$ is the *effective* SBH which can be smaller compared to the ideal SBH by zero bias lowering, tunneling or minority carrier injection. In this case equation 4.1 is not valid any more and hSBH and eSBH do not add up to E_G. In the following SBH always denotes the *effective* SBH. β captures the voltage dependence of the effective barrier due to static and image force lowering in reverse bias.

4.2. Properties of NiGeSn

The formation of metal-semiconductor alloys is a common method for achieving low resistance contacts with a well defined interface. Especially metal-silicon (silicide) and metal-germanium (germanide) alloys have been widely studied. Well-established silicides and germanides are for example NiSi, CoSi, TiSi, NiGe or PtGe [85,86]. On the contrary, for GeSn there is only a hand full of studies on *Nickelstanogermanide* (NiGeSn) [87–91] and NiPtGeSn [92]. The lowest contact resistivities on Ge were achieved with NiGe [93], while NiGe and NiPd show the lowest sheet resistances among transition metal germanides [94]. Thus NiGeSn is investigated here in detail.
NiGeSn was formed on several GeSn epilayers covering a wide range of Sn content from 0 % (GeVS) to 12.5 % Sn. To that end the samples were first cleaned following the procedure discussed in SECTION 3.1. After the HF:HCl native oxide removal the samples were directly loaded into a Oerlikon LLSEVO-II sputter tool. To remove contamination possibly adsorbed during *ex-situ* transfer a short Ar-sputter step is utilized followed by 10 nm DC sputter deposition of Ni. The Ni is converted into an approx. 23 nm thick NiGeSn layer while consuming 15 to 19 nm GeSn [95] in a subsequent *Rapid Thermal Annealing* (RTA) step at 325 °C for 10 s in H_2:N_2 forming gas atmosphere. The annealing parameters are based on a process previously utilized by Wirths *et al.* who found 325 °C to be the ideal temperature to achieve a low sheet resistance of NiGeSn. As for germanides [86] the dominant diffusion species is Ni that diffuses into the underlying GeSn to form NiGeSn while the Ge:Sn ratio remains unchanged at moderate temperatures [96]. Only if the annealing temperature is too high, Sn tends to diffuse towards both interfaces of NiGeSn.

4.2.1. Structural Analysis of NiGeSn

X-ray Diffraction (XRD) is a well-established method for the structural characterization of (poly)-crystalline materials and relies on the Bragg reflection of X-rays at the net planes of the crystal. Here, so called θ-2θ scans are employed where the relation between the varied angle of the incident X-ray and detected signal is θ:2θ. Such specular θ-2θ scans were recorded with X-rays generated from a Cu-tube without monochromator in order to yield a higher intensity. Nevertheless, the CuKα1 spectral line is the most intense and is responsible for most of the recorded diffraction peaks. That way NiGeSn layers were analyzed that were formed on several partially relaxed GeSn (thick) layers covering the above mentioned Sn content range up to 12.5 % Sn. The initial GeSn layer thicknesses were approx. 800 nm for 5.5, 8.5 and 10 % Sn, respectively, whereas the 12.5 % Sn layer was 410 nm thick. As depicted in Fig. 4.3(a) the θ-2θ analysis reveals the co-existence of several poly-crystalline NiGeSn phases. Peaks not belonging to the underlying GeSn, GeVS and Si-subsbtrate were assigned to the corresponding $Ni_y(Ge_{1-x}Sn_x)_z$ phases by comparison to reported data on the well studied and closely

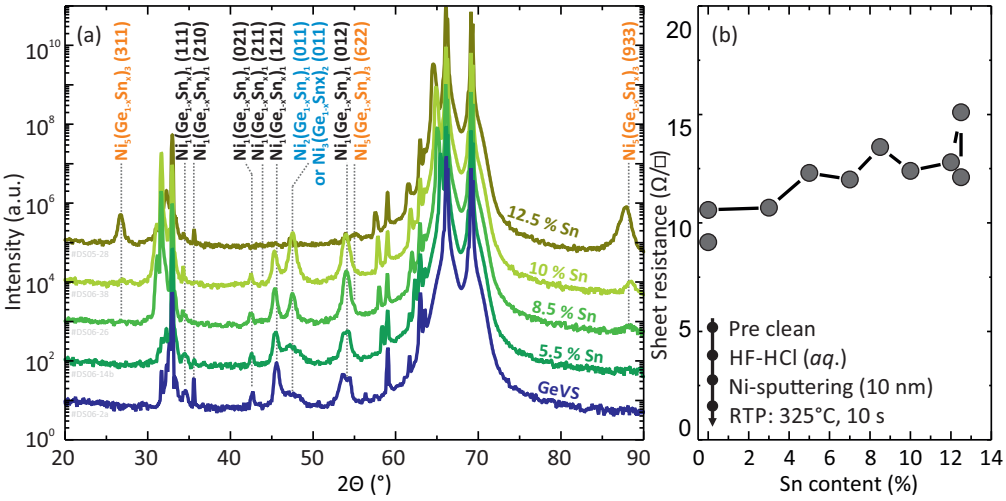


Figure 4.3.: *(a) XRD θ-2θ scans of NiGeSn formed on various GeSn alloys with different Sn contents. The unlabeled peaks belong to reflexes from GeSn, GeVS and Si substrate. (b) Sheet resistance of the studied NiGeSn alloys as obtained by the Van der Pauw technigue. The key steps for NiGeSn formation are shown as an inset. XRD scans recorded by Peter Zaumseil, IHP Frankfurt Oder.*

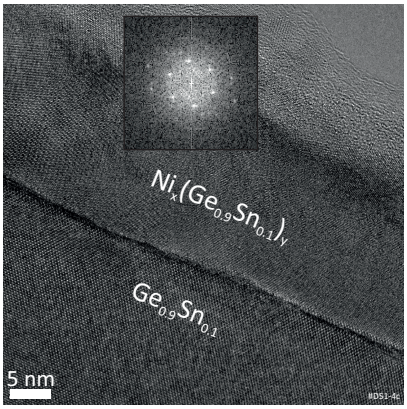


Figure 4.4.: *XTEM of a* $\mathrm{Ni}_x(\mathrm{Ge}_{0.9}\mathrm{Sn}_{0.1})_y/\mathrm{Ge}_{0.9}\mathrm{Sn}_{0.1}$ *MS contact demonstrating a smooth interface. The hexagonal symmetry of the observed* $\mathrm{Ni}_x(\mathrm{Ge}_{0.9}\mathrm{Sn}_{0.1})_y/\mathrm{Ge}_{0.9}\mathrm{Sn}_{0.1}$*-grain is evidenced by a FFT in the inset. TEM sample preparation and image recording by Fabian Wendt are greatly acknowledged.*

related NiGe-system listed in the *Inorganic Crystal Structure Database* (ICSD) [97]. In line with previous studies on NiGeSn formed on pseudomorphic (*i.e.* thin) GeSn a predominance of two phases, the $\mathrm{Ni}_1(\mathrm{Ge}_{1-x}\mathrm{Sn}_x)_1$ [90, 92] and $\mathrm{Ni}_5(\mathrm{Ge}_{1-x}\mathrm{Sn}_x)_3$ [88, 91] phase was observed. Even though all samples were annealed at the same temperature of 325 °C, the NiGeSn phase composition changed with Sn content. Whereas for NiGeSn formed on GeVS and $\mathrm{Ge}_{0.945}\mathrm{Sn}_{0.055}$ primarily the $\mathrm{Ni}_1\mathrm{X}_1$ phase was observed, with increasing Sn content the $\mathrm{Ni}_5\mathrm{X}_3$ phase appeared and for NiGeSn formed on $\mathrm{Ge}_{0.875}\mathrm{Sn}_{0.125}$ was the only phase observed. As deduced from the fact that only multiples of the (311) reflex are observed this hexagonal $\mathrm{Ni}_5(\mathrm{Ge}_{1-x}\mathrm{Sn}_x)_3$ phase is well oriented in out of plane direction. The result is supported by the *Fast Fourier Transform* (FFT) of a XTEM in Fig. 4.4 showing a hexagonal pattern similar to the results reported on $\mathrm{Ni}_5(\mathrm{SiGe})_3$ [98].

This result is surprising since for pseudomorphically grown GeSn, Sn incorporation was reported to stabilize the $\mathrm{Ni}_1\mathrm{X}_1$ phase. However, because pseudomorphic and partially relaxed layers differ significantly in compressive stain, this may play an important role. All in all the phase formation sequence is very similar to those of nickelgermanides [95]. Despite the phase change, only a slight increase of the sheet resistance of NiGeSn is observed for NiGeSn formed on higher Sn content GeSn. The NiGeSn sheet resistance remains in the range 10 to 15 $\Omega/\square$ which is comparable to literature reports on NiGeSn

[88, 92] and NiGe [99, 100]. For the intermediate Sn contents 8.5 % Sn and 10 % Sn also a third phase is observed with a peak at 47.5°. This reflex agrees with the Ni-rich phases $Ni_2(Ge_{1-x}Sn_x)_1$ and $Ni_3(Ge_{1-x}Sn_x)_2$ though the abundance of different phases and orientations makes a clear assignment of the diffraction peaks very challenging. Inded a full crystallographic analysis of NiGeSn would be beyond the scope of this work.

4.2.2. Schottky Barrier Height Extraction of NiGeSn/GeSn contacts

The (effective) SBH is the important parameter affecting the electronic transport across a MS contact. While there are a few studies on the contact resistivity of metal-GeSn contacts, to date indeed there is only one literature report on the eSBH in NiGeSn/*n*-GeSn contacts [90] and one report on the hSBH of NiSiGeSn/*p*-SiGeSn contacts [101], appart from the contribution that was made within the course of this work [26, 81].
There are several methods for the extraction of the SBH such as from the forward bias IV characteristics, from IV's temperature dependence (activation energy method), from *Capacitance-Voltage* (CV) measurements in reverse bias or from photoelectric measurements [82]. With regard to electrical measurements the CV and IV methods are best suited for large SBH. However, for the NiGeSn/GeSn system very small SBH are expected which would impede a reliable SBH extraction using these methods. Thus here the activation energy method is employed which is based on the temperature dependence of the reverse bias IV characteristics of a MS contact and is a well suited method for the determination of very small SBH as reported by Dubois *et al.* [102]. Further advantages of this method are that it neither needs knowledge of material parameters (that might be an additional source of error) nor it needs knowledge of the effective MS contact area which might deviate from the geometric contact area.
To that end NiGeSn/GeSn/NiGeSn *Metal-Semiconductor-Metal* (MSM) diodes were fabricated on various GeSn epilayers. These are two *back-to-back* connected MS diodes. That is, independent of the polarity of the applied bias always one contact is in forward and one is in reverse bias condition. Since the reverse bias current is the limiting factor the IV characteristics of MSM diodes are always defined by the reverse bias MS characteristics. For MSM diode fabrication first the samples were cleaned using the procedure described in chapter 3.1. To avoid possible contribution from surface currents a passivation layer of 10 nm Al_2O_3 from *Atomic Layer Deposition* (ALD) and

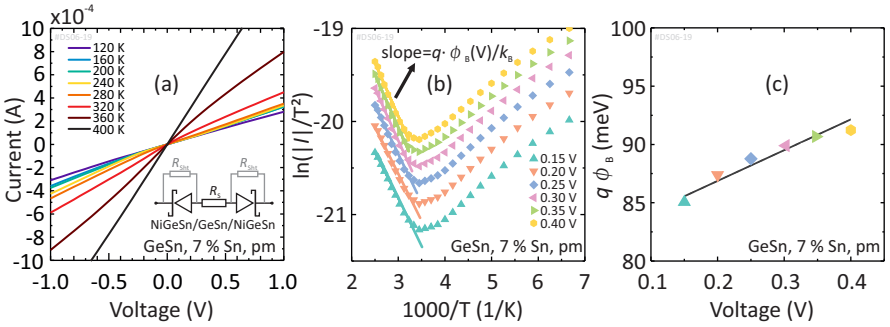


Figure 4.5.: *Exemplaric SBH extraction for* $Ge_{0.93}Sn_{0.07}$*: (a) IV characteristics of MSM diodes for a set of temperatures, (b) Activation energy plot created from the data set in (a). The slope in the linear region yields* $q\phi_B(V)$ *for different voltages and is plotted in (c) against the applied voltage to extrapolate* $q\phi_B(V)$ *to* 0 V*.*

100 nm SiO_2 from *Plasma Enhanced Chemical Vapor Deposition* (PECVD) was used. The active contact area was then defined with photo lithography and dry etching of the passivation layer. Subsequently NiGeSn was formed in the opened contact windows following the NiGeSn process outlined above. The fabrication flow is conform with steps (a,e & f) from Fig. 4.7. A lumped circuit model of a MSM diode is sketched as an inset of Fig. 4.5(a).

Temperature dependent IV measurements were performed in the range 120 to 400 K on MSM diodes fabricated from undoped (p-type) GeSn layers with Sn contents ranging from 3 to 10 % Sn. An exemplary data set for a 7 % Sn MSM diode is shown in Fig. 4.5(a). Only slight non-linear IV characteristics point towards a very small SBH. According to equation 4.4 multiplied with the contact area A one yields the MSM current I which after slight modification shows a linear relationship between $\ln(|I|/T^2)$ and $1/T$

$$\ln\left(\frac{|I|}{T^2}\right) = \ln(AA^{**}) - \frac{q\phi_B(V)}{k_B}\frac{1}{T}\,. \tag{4.6}$$

The slope of such a Richardson plot of $\ln(|I|/T^2)$ *vs.* $1/T$ yields directly the majority carrier SBH $q\phi_B(V)$ that due to static and image force lowering linearly depends on the applied voltage $q\phi_B(V) = q(\phi_{B0} + \beta V)$. The Richardson plot corresponding to the data set in Fig. 4.5(a) is depicted in Fig. 4.5(b). In a real MSM diode the IV characteristics are a combination of the ideal back-to-back diode characteristics and contributions from

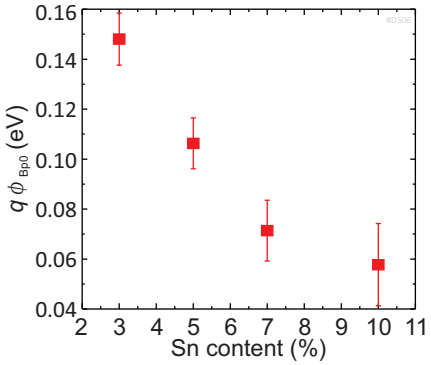


Figure 4.6.: *hSBH, $q\phi_{Bp0}$ vs. Sn content featuring a significant decrease of $q\phi_{Bp0}$ with Sn content.*

series R_S and shunt resistances R_{Sht} as indicated in the inset of Fig. 4.5(a). However, in the temperature regime of a linear declining curve the IV characteristics are dominated by the Schottky characteristics and allow a reliable extraction of $q\phi_B(V)$. Finally the $q\phi_B(V)$ extraction from Fig. 4.5(b) is repeated for several voltages and plotted against the applied bias in Fig. 4.5(c) to extrapolate $q\phi_B(V)$ to 0 V and thereby extract $q\phi_{B0}$. For this 7 % Sn sample a hSBH of $q\phi_{Bp0} = 0.07\,\text{eV}$ was extracted. Similar low hSBHs were obtained for the other Sn contents probed with a clear trend of decreasing hSBH with increasing Sn content. This result suggests that the SBH reduction goes along with the Sn-induced change of the band alignments. However, since in parallel to increasing Sn content also the unintentional p-type background doping increases from mid $10^{16}\,\text{cm}^{-3}$ to mid $10^{17}\,\text{cm}^{-3}$ (*cf.* CHAPTER 8.3) this might also contribute to the change of the apparent hSBH.
Similar low hSBH were reported for the related NiSiGeSn/SiGeSn system with $q\phi_{Bp0} = 0.09\,\text{eV}$ for $Si_{0.07}Ge_{0.86}Sn_{0.07}$ [101]. The results are in line with the typically low hSBH observed at NiGe/p-Ge contacts due to Fermi level pinning close to the valence band caused by *metal-induced gap states* (MIGS) [103, 104].

4.2.3. Dopant Segretation at the NiGeSn/GeSn Interface

As outlined in SECTION 4.1.1 the effective SBH is not solely defined by the material choice but can also be influenced by doping of the semiconductor or by interface states. An approximation of the specific contact resistivity ρ_c in the tunneling dominated regime

[105]

$$\rho_c \approx \rho_0 \exp\left(\frac{2\phi_B}{\hbar}\sqrt{\frac{m_T \epsilon_0 \epsilon_s}{N}}\right) , \tag{4.7}$$

motivates the need of high doping concentration N and low Schottky barrier height $q\phi_B$ to achieve low access resistances. m_T is the tunneling effective mass, $\hbar$ the reduced Planck-constant, ϵ_0 and ϵ_s are the vacuum permittivity and semiconductor relative permittivity, respectively. ρ_0 is a constant. The insertion of a thin, highly doped layer at the MS interface reduces the contact resistance two-fold: The highly doped interlayer results in a steeper decay of the electronic bands and a smaller depletion width, which increases the tunneling component. At the same time the smaller depletion width results in a higher build in electric field, which in turn enhances the static barrier lowering [82]. A well established method to realize this thin interlayer is *Dopant Segregation* (DS) [106]. Dopant segregation relies on the temperature-induced redistribution of dopants at the MS interface. There are two common methods for DS: (i) In the first approach, initially the MS alloy (*e.g.* NiGeSn) is formed. Then dopants are ion implanted into the center of the alloyed region. As final step dopants are driven out to the alloy-semiconductor interface in a second anneal, provided that diffusion, solid solubility and temperature allow the desired dopant redistribution. This approach is denoted as *Implantation Into Stanogermanide* (IISG) (ii) In the alternate approach the dopants are directly implanted into the semiconductor prior to the MS alloy formation. Dopant segregation occurs then in one step during the MS alloy formation anneal. The implantation depth is chosen such that region damaged by ion implantation is fully consumed by the MS alloy. In the following this approach is called *Stanogermanidation-Induced Dopant Segregation* (SGIDS). Using this method very steep doping profiles can be achieved. Furthermore since the dopants diffuse into the undamaged region one circumvents the challenges related to direct ion implantation into GeSn mentioned in CHAPTER 2.2.

As presented below DS is analyzed for the NiGeSn/GeSn system for the common n- and p-dopants P, As and B. The key fabrication steps for both SGIDS and IISG are depicted in Fig. 4.7(a-d) and Fig. 4.7(a,e-h), respectively.

First DS based on the IISG approach is studied. After formation of 23 nm NiGeSn by depositing and annealing of 10 nm Ni as described above [Fig. 4.7(a,e,f)], p-type (BF_2^+, 15.8 keV) and n-type (P^+, 10 keV or As^+, 13 keV) dopants are implanted into the metallic NiGeSn to a dose of $1 \cdot 10^{15}\,\mathrm{cm}^{-2}$ [Fig. 4.7(g)]. To avoid crystal damage of the underlying GeSn the implantation energy was chosen such that the dopants are

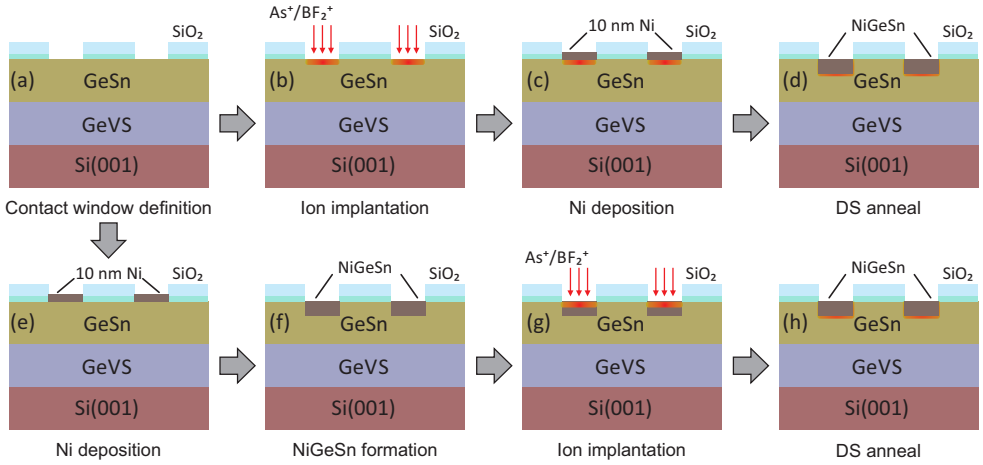


Figure 4.7.: *Key fabrication steps for MSM diodes with dopant segregation: (a-d) Stanogermanidation-Induced Dopant Segregation (SGIDS), (a,e-f) Implantation Into Stanogermanide (IISG).*

located solely within the NiGeSn. The subsequent drive out anneal was conducted at the same temperature of 325 °C, as the NiGeSn formation anneal for 10 s in forming gas atmosphere [Fig. 4.7(h)], which also is close to the highest temperature possible to avoid Sn diffusion for high Sn content GeSn samples.

Time of Flight Secondary Ion Mass Spectroscopy (ToF-SIMS) was employed to study the dopant redistribution[1]. In this technique the surface of the sample is gradually sputtered away with accelerated ions as Cs^+ or O_2^+ while liberated secondary ions from the sample material are analyzed with a mass spectrometer. That way an elementary resolved vertical profile of the sample composition can be recorded.

The ToF-SIMS spectra for IISG with B, P and As are depicted in Fig. 4.8(a-c). The obtained dopant distributions show no dopant pile up at the NiGeSn/GeSn interface leading to the conclusion that DS is not effective in this approach given the limited allowed annealing temperature for GeSn and this choice of dopants. Apparently the dopant diffusion is not strong enough to allow a DS effect.

However, a clear dopant peak at the NiGeSn/GeSn interface was observed for B and As using the alternate SGIDS approach [Fig. 4.8(e,g)]. Here the dopants were implanted

[1]I gratefully acknowledge recording of ToF-SIMS-spectra by Uwe Breuer, ZEA3, FZ-Jülich, Germany.

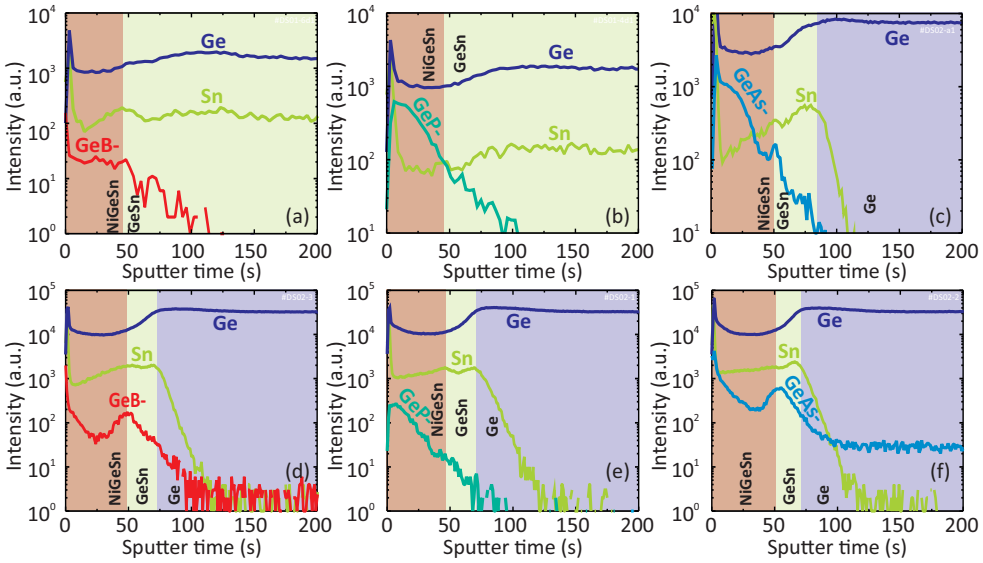


Figure 4.8.: *ToF-SIMS profiles for IISG (a-c) and for SGIDS (d-f). A DS effect with a clear peak at the NiGeSn/GeSn interface is observed for B (d) and As (f) in the SGIDS approach. P in the SGIDS approach and the IISG technique did not show the desired dopant redistribution. ToF-SIMS recorded by Uwe Breuer, ZEA3, FZ-Jülich, Germany.*

directly into GeSn using 10 keV for BF_2^+, 7 keV for P^+ and 13 keV for As^+, respectively to a dose of $1 \cdot 10^{15}\,cm^{-2}$. NiGeSn formation and DS occurred in one step thanks to an anneal at 325 °C for 10 s. In contrast to As and B, for P no DS effect was observed. DS for P was though reported in literature for NiGe at higher temperatures [100] albeit less effective than As DS in NiGe. Since the stanogermanidation process is associated with significant volume changes in the material and the formation of point defects which can enhance dopant diffusion at the evolving NiGeSn interface, this might explain why dopant segregation is effective for SGIDS but not for IISG [107]. The strength of the DS effect in NiGeSn/GeSn contacts changes with Sn content and layer strain. Such effects were also studied within the scope of this work and recently reported in JAP [81].

In literature dopant/impurity segregation in NiGeSn/GeSn contacts was reported for boron [89], sulfur and selenium [90] all using the SGIDS approach. With the findings gained within the course of this work now dopant segregation is available for both *p* and *n*-type dopants.

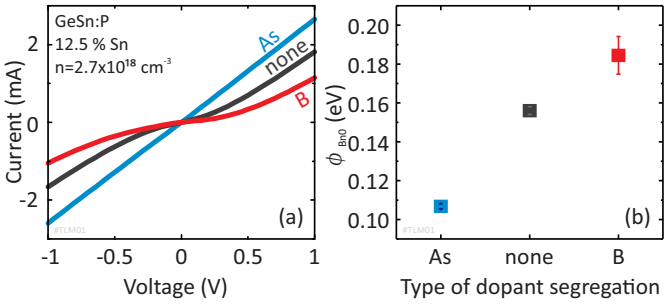


Figure 4.9.: *(a) MSM diode IV characteristics with As and B SGIDS and without additional implantation as a reference on n-doped* $Ge_{0.875}Sn_{0.125}$*:P, (b) corresponding eSBH.*

The effectiveness of SBH modulation using DS was demonstrated for *in-situ* n-type doped $Ge_{0.875}Sn_{0.125}$ with an active carrier concentration[2] of $3 \cdot 10^{18}\,cm^{-3}$. MSM diodes were fabricated using the described SGIDS schemes for As and B and without implantation as a reference. Whereas the MSM diode on n-GeSn without additional implantation shows slight diode like IV characteristics, the behavior with complementary As SGIDS is perfectly linear (Ohmic) [*cf.* Fig. 4.9(a)]. On the contrary counter doping with B SGIDS leads to stronger diode like behavior. This reflects also in the extracted SBH for electrons $q\phi_{Bn0}$ that compared to the reference is decreased for As SGIDS and increased for B SGIDS [*cf.* Fig. 4.9(b)].

The achieved eSBH is comparable to those reported by Tong *et al.* who achieved $q\phi_{Bn0} = 0.11\,eV$ for sulfur segregation on $Ni_y(Ge_{0.958}Sn_{0.042})_z/n\text{-}Ge_{0.958}Sn_{0.042}$ MS contacts. As discussed in SECTION 4.1 ideally one would expect this eSBH and the hSBH from SECTION 4.2.2 to add up to E_G which is apparently not the case even for the sample without DS. However, since the *in-situ* n-type doping is $> 10^{18}\,cm^{-3}$ one expects significant contribution from tunneling leading to the situation of small effective SBH for both electrons and holes.

Finally also the corresponding specific contact resistivities were extracted for NiGeSn-based contacts to *in-situ* n-doped GeSn using the *Transfer Length Method* (TLM) described in [108]. The lowest obtained value is $\rho_c = 1.5 \cdot 10^{-5}\,\Omega cm^2$ for NiGeSn on $Ge_{0.915}Sn_{0.085}$ which is significantly lower than $\rho_c = 6.4 \cdot 10^{-4}\,\Omega cm^2$ reported by Li *et al.* [109] for NiGeSn on $Ge_{0.951}Sn_{0.049}$. The lowest reported values for n-type GeSn are

[2]Carrier density measured with *Electrochemical CV* (ECV) by Nils von den Driesch.

in the low $10^{-6}\,\Omega\mathrm{cm}^2$ range as reported by Srinivasan *et al.* [105].
For *p*-type contacts Han *et al.* achieved $\rho_c = 1.6 \cdot 10^{-5}\,\Omega\mathrm{cm}^2$ for NiGeSn on *p*-type $Ge_{0.947}Sn_{0.053}$. Zheng *et al.* reported $\rho_c = 1.96 \cdot 10^{-6}\,\Omega\mathrm{cm}^2$ for *p*-type $Ge_{0.86}Si_{0.07}Sn_{0.07}$. $\rho_c < 10^{-6}\,\Omega\mathrm{cm}^2$ is needed for production [108] which seams feasible considering the early stage of GeSn technology and the huge progess in Ge-technology with demonstrated $\rho_c = 1.5 \cdot 10^{-8}\,\Omega\mathrm{cm}^2$ [93].

4.3. Summary

To summarize NiGeSn/GeSn metal-semiconductor contacts were comprehensively studied for a wide range of Sn contents (0 to 12.5 % Sn). Structural analysis *via* XRD and TEM revealed the coexistence of several poly-crystalline NiGeSn phases, mainly $Ni_1(Ge_{1-x}Sn_x)_1$ and $Ni_5(Ge_{1-x}Sn_x)_5$. As electrical characterization, low NiGeSn sheet resistance in the range 10 to $15\,\Omega/\square$ was probed with the Van der Pauw technique. Small Schottky barrier heights $< 0.15\,\mathrm{eV}$ and Ohmic IV characteristics were achieved for both electron and hole transport, qualifying NiGeSn as suitable contact alloy. The hole Schottky barrier height decreases with Sn content. As a method to tune the SBH dopant segregation was demonstrated for both *p*- and *n*-type dopants using boron and arsenic, respectively.

5 | MOS-Structures on (Si)GeSn

THE *Metal-Oxide-Semiconductor Capacitor* (MOSCap) is the crucial building block for *Field-Effect Transistor* (FET) devices enabling the control of the electronic bands within the channel and thus providing the basic functionality of any FET. The technological revolution of Si-based highly *Integrated Circuits* (ICs) was mainly driven by the chemically stable SiO_2/Si-interface that can be fabricated with very low defect density by controlled oxidation of the pristine Si-surface [110]. Thanks to this high quality intrinsic oxide Si became the unchallenged material system for today's *Information & Communication Technology* (ICT) even though Si offers relatively low bulk carrier mobilities compared to Ge-based (Ge, GeSn, SiGeSn, *cf.* CHAPTER 8.3) or group III-V

materials [110]. However, with continuous down scaling and performance competition these alternate channel materials more and more urge into focus of research.
Despite the relatively unstable [66] GeO_x/Ge-interface ($1 \leq x \leq 2$) numerous improvements in Ge-surface passivation techniques were achived within the recent past and provide promising results for the realization of high performance Ge-based FETs [111–114]. On the contrary for the new (Si)GeSn material system only a handful of studies exist dealing with fabrication and characterization of GeSn-based MOS-structures [33,68,115–121], in which significant contribution was made within the course of this work [37,122–127].
This chapter provides a comprehensive study of (Si)GeSn-based MOSCaps. First a general introduction to the electrical properties of MOSCaps is presented for Si-based MOS structures as the standard theory and measurement procedures were developed for this material system [82,108,128]. On this basis peculiarities of non-Si, low bandgap semiconductors as GeSn are pointed out to ensure sound data interpretation. In the experimental section first the process for the fabrication of (Si)GeSn-based MOSCaps is optimized and verified according to the reduced thermal stability of GeSn to avoid Sn diffusion and precipitation. Electrically, the MOSCaps were characterized by means of *Current Voltage* (IV) as well as temperature (T) and frequency (f) -dependent *Capacitance Voltage* (CV) and *Conductance Voltage* (GV) measurements to extract key parameters like *gate leakage current density* (J_{Ox}), *oxide capacitance* (C_{Ox}) and *Density of Interface Traps* (D_{it}). As a step forward the gate oxide thickness is scaled down utilizing an optimized process, to achieve high oxide capacitances of $C_{\mathrm{Ox}} = 3\,\mu\mathrm{F/cm^2}$ while maintaining low gate leakage, ideal for novel FET-devices like the TFET. Furthermore a systematic study is presented on the correlation of bandgap (*i.e.* Sn content) and minority carrier response in (Si)GeSn-based MOSCaps. These findings are supported by physics-based numerical simulations. Finally, an analysis of the temperature-dependent minority carrier response allows the extraction of defect levels pertinent to (Si)GeSn epitaxial layers.

5.1. MOS-basics

As depicted in Fig. 5.1(a) a MOSCap consists of an insulating (dielectric) oxide layer that is sandwiched with a top metal electrode and a bottom semiconducting material which is commonly contacted with an Ohmic back contact. The equivalent circuit of a MOSCap can be approximated with a series connection of two capacitances, the oxide capacitance C_{Ox} and the semiconductor capacitance C_{S}. Both are shunted with two according conductances G_{Ox} and G_{S}. Because the oxide layer can generally be assumed to be well insulating G_{Ox} can be neglected in most cases. The semiconductor capacitance depends on the applied bias and is thus labeled with an arrow indicating a variable capacitor. Since the output current of a MOSFET is proportional to C_{Ox} [82], it is desired to be as high as possible. C_{Ox} refers to the area-normalized capacitance and is given by the capacitance of a parallel plate capacitor

$$C_{\mathrm{Ox}} = \varepsilon_{\mathrm{Ox}}\varepsilon_0/t_{\mathrm{Ox}} \ , \tag{5.1}$$

with the vacuum permitivity ε_0, the relative permitivity $\varepsilon_{\mathrm{Ox}}$ of the oxide and the physical oxide thickness t_{Ox}. C_{Ox} thus can be increased either by reducing t_{Ox} or by increasing $\varepsilon_{\mathrm{Ox}}$. While it is obvious that t_{Ox} cannot be decreased to arbitrary small values as it would lead to strong leakage currents or even electric breakdown of the dielectric [129], $\varepsilon_{\mathrm{Ox}}$ is defined by the material choice. Historically the intrinsic oxide SiO_2 ($\varepsilon_{SiO_2} = 3.9$) was the material of choice and was used for several decades in Si-MOS technology. Its natural advantage was that it could be created directly from a clean Si-surface by controlled thermal oxidation. t_{Ox} was continuously reduced with each new technology generation however, as the physical limits of t_{Ox}-scaling were approaching, alternate gate dielectrics with higher $\varepsilon_{\mathrm{Ox}}$ - also known as high-κ materials - were taken into account. A whole zoo of different materials was intensively studied mostly transition metal- and rare earth metal oxides as for instance Al_2O_3, Y_2O_3, ZrO_2, HfO_2, $LaLuO_3$ or Tm_2O_3 to find the best compromise of $\varepsilon_{\mathrm{Ox}}$, bandgap and band offset while maintaining low defect densities comparable to those of the Si/SiO_2-system [130–132]. 2007 Intel Corporation announced the implementation of high-κ/metal gate technology with the launch of their 45 nm-node process [133]. Today these materials, mostly Al_2O_3 ($\varepsilon_{Al_2O_3} \approx 9$) and HfO_2 ($\varepsilon_{HfO_2} \approx 18 - 25$) are prevalent and usually grown by *Atomic Layer Deposition* (ALD) allowing high quality, self-limited and sub-nanometer precise deposition of the dielectric

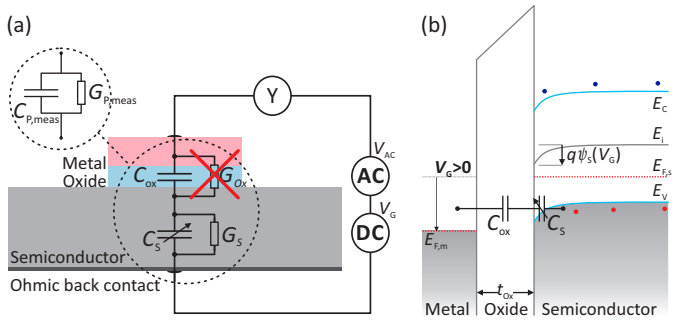


Figure 5.1.: *(a) MOSCap layer cross section sketch, internal equivalent circuit and external measurement circuitry; (b) Real-space electronic band diagram of a positively biased MOSCap on a p-type semiconductor with indicated C_{Ox} and C_{S}. C_{S} and band bending ψ_{s} depend on the applied DC gate bias.*

layer [134].

The electrical properties of a MOSCap are defined by its admittance $Y = G + i\omega C$, the complex combination of parallel conductance and capacitance. Both real- and imaginary part of the admittance can be measured by applying a small AC-voltage of typically $20-50\,\mathrm{mV_{rms}}$ and measuring amplitude and phase shift of the resulting AC-current. This is typically done with a Lock-in-Amplifier or a so called LCR-meter. In case of a LCR-meter, as used in this work, the measured admittance is automatically converted to the components of an appropriate equivalent circuit, in this case a capacitance $C_{\mathrm{P,meas}}$ in parallel to a conductance $G_{\mathrm{P,meas}}$. The frequency range used here is $f = 1\,\mathrm{kHz}$ to $1\,\mathrm{MHz}$. In order to characterize the properties of the semiconductor and the semiconductor/oxide-interface the AC probing signal is superimposed with a DC gate voltage V_{G}(typically in the range $0\,\mathrm{V}$ to $\pm 2\,\mathrm{V}$) that allows bending $\psi_{\mathrm{S}}(V_{\mathrm{G}})$ of the electronic bands and thereby changing the charge carrier density and semiconductor capacitance C_{S} in the vicinity of the semiconductor/oxide interface as outlined in the band diagram in Fig. 5.1(b).

5.1.1. The ideal MOS-Capacitor

As an introduction first an ideal MOS-Capacitor is considered as described by Sze and Kwok [82]. That means, (i) electric charges are only present in metal and semiconductor whereas the oxide is free of charges and (ii) there is no DC-current transport through the oxide such that it serves as an ideal insulator. Also there are no defect states of any

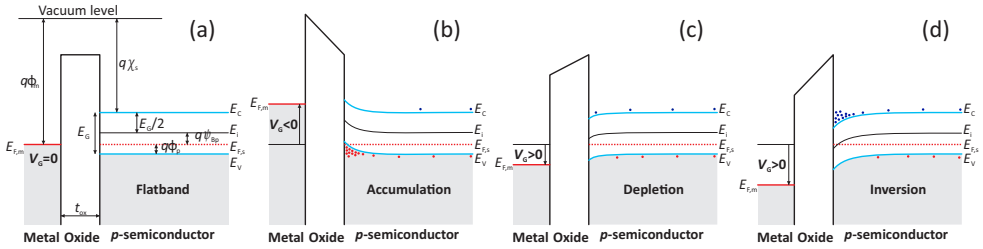


Figure 5.2.: *Band diagram of an ideal p-type MOSCap in different bias regimes: (a) flatband, (b) accumulation, (c) depletion, (d) inversion. From [82].*

kind present in the vicinity of the semiconductor/oxide interface ($D_{\mathrm{it}} = 0\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$). The band diagram of a MOSCap fabricated on a p-type semiconductor is sketched in Fig. 5.2(a-d) for different bias conditions. For zero bias the Fermi levels in $E_{\mathrm{F,m}}$ and $E_{\mathrm{F,s}}$ are aligned [Fig. 5.2(a)]. Φ_{m} and χ_{S} denote work function and electron affinity of metal and semiconductor, respectively. For simplicity the work functions of metal and semiconductor are chosen to be equal such that $\phi_{\mathrm{m}} - (\chi_{\mathrm{S}} + E_{\mathrm{G}}/2q + \psi_{\mathrm{Bp}}) = \phi_{\mathrm{m}} - (\chi_{\mathrm{S}} + E_{\mathrm{G}}/q - \phi_{\mathrm{p}}) = 0$ and the bands in the semiconductor are flat for zero bias (the flatband voltage V_{FB} is zero). ψ_{Bp} and ϕ_{p} describe the position of the Fermi level measured from midgap $E_{\mathrm{i}} = E_{\mathrm{G}}/2$ and from E_{V}, respectively. Since there is no DC-current flow through the oxide the Fermi level and the bands remain flat within the semiconductor far from the interface even when the gate electrode is biased positively or negatively with respect to the semiconductor body. However, in the case of a non-zero bias the bands bend upward or downward close to the semiconductor/oxide interface according to the applied bias as shown in Fig. 5.2(b-d). A close up for positive bias is given in Fig. 5.3.

The electron and hole carrier densities (n, p) exponentially depend on the distance of conduction band and valence bend from the Fermi level ($E_{\mathrm{C}} - E_{\mathrm{F,s}}$ and $E_{\mathrm{F,s}} - E_{\mathrm{V}}$). As a consequence the carrier density is changed in the bent region as function of the applied bias giving this region its name, space-charge region. The potential difference $\psi_{\mathrm{s}}(V_{\mathrm{G}})$ between the bent band at the interface and the bulk is called surface potential. The electron and hole concentration at the interface n_{ps} and p_{ps} of the p-type semiconductor as function of surface potential are given by

$$n_{\mathrm{ps}} = n_{\mathrm{po}} \exp\left(\frac{\psi_{\mathrm{s}}(V_{\mathrm{G}})}{k_{\mathrm{B}}T}\right) \tag{5.2}$$

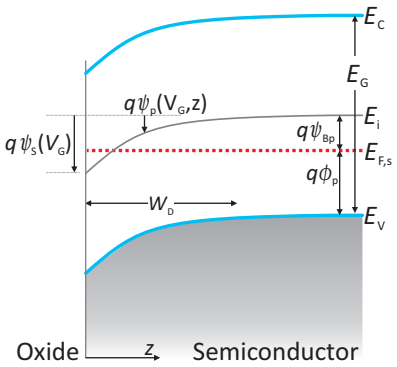


Figure 5.3.: *Detailed band diagram pointing out the surface potential (band bending) of a p-type MOSCap biased in weak inversion ($\psi_s > \psi_{Bp}$). From [82].*

$$p_{ps} = p_{po} \exp\left(\frac{-\psi_s(V_G)}{k_B T}\right) \tag{5.3}$$

n_{po} and p_{po} are the equilibrium (unbiased) electron and hole densities, respectively. Depending on the bias one can distinguish between different regimes of surface potential.

(i) $\psi_s < 0$, **Accumulation**: The metal gate electrode is negatively biased with respect to the semiconductor body [Fig. 5.2(b)]. As a consequence the bands at the interface bend upwards such that E_V moves closer to $E_{F,s}$. Thus thermal generation of holes is easier (*c.f* Eq. 5.3) leading to an accumulation of holes in the vicinity of the semiconductor/oxide interface.

(ii) $\psi_s = 0$, **Flatband**: There is no band bending in the semiconductor. The corresponding gate voltage and capacitance are denoted as flatband voltage V_{FB} and flatband capacitance C_{FB}. For equal work functions of metal and semiconductor this situations occurs at $V_G = V_{FB} = 0$. Experimentally in this work V_{FB} is obtained from the inflection point of the CV curve [135].

(iii) $\psi_{Bp} > \psi_s > 0$, **Depletion**: In case of a slightly positive bias [Fig. 5.2(c)] both E_V and E_C are furthest away from $E_{F,s}$ (*i.e.* the intrinsic level E_i is close to $E_{F,s}$) so that the region close to the interface is depleted from free carriers. The ionized dopants (here acceptors) remain and form the space charge region.

(iv) $\psi_s = \psi_{Bp}$, **Midgap**: Fermi level and intrinsic level coincide at the interface $E_{F,s} =$

E_i. Electron and hole density are equal to the intrinsic carrier concentration $n_\mathrm{ps} = p_\mathrm{ps} = n_\mathrm{i}$.

(v) $\psi_\mathrm{Bp} < \psi_\mathrm{s} < 2\psi_\mathrm{Bp}$, **Weak inversion**: When biasing the MOSCap further positively E_i moves below $E_\mathrm{F,S}$ and the conduction band E_C comes closer to $E_\mathrm{F,S}$. The electron density (minority carriers) exceeds the hole density (majority carriers) $n_\mathrm{ps} > p_\mathrm{ps}$ and the space charge region is inverted.

(vi) $\psi_\mathrm{s} > 2\psi_\mathrm{Bp}$, **Strong Inversion**: The surface minority carrier density n_ps exceeds the equilibrium hole density ($n_\mathrm{ps} > p_\mathrm{po}$ or N_A). The corresponding gate voltage is the threshold voltage V_th marking the turn-on of a MOSFET. Further increase of V_G does not increase ψ_s as the voltage is screened by the inversion charge layer.

The description for an n-type semiconductor is analogous. In that case the inversion charge will be formed by holes instead of electrons.

The capacitance C_S of the space charge region can be calculated by solving the one-dimensional Poisson equation of the potential $\psi_\mathrm{p}(z)$ as function of the position z in the semiconductor [82] (see also Fig. 5.3).

$$\frac{\mathrm{d}^2\psi_\mathrm{p}}{\mathrm{d}z^2} = -\frac{\rho(z)}{\varepsilon_\mathrm{s}} \,, \tag{5.4}$$

with the total space-charge density $\rho(z) = q(N_\mathrm{D}^+ - N_\mathrm{A}^- + p_\mathrm{p} - n_\mathrm{p})$ and the ionized donor and acceptor densities N_D^+ and N_A^- respectively. Integration of equation 5.4 gives the relation of electric field $\mathcal{E}$ and ψ_p ($\mathcal{E} = -d\psi_\mathrm{p}/dz$) and finally the space charge per unit area $Q_\mathrm{s} = -\varepsilon_s\mathcal{E}$. The semiconductor capacitance C_S is defined as

$$C_\mathrm{S} = \frac{\mathrm{d}Q_\mathrm{s}}{\mathrm{d}\psi_\mathrm{s}} \,. \tag{5.5}$$

An approximation for depletion and weak inversion ($\psi_\mathrm{Bp} > \psi_\mathrm{s} > k_\mathrm{B}T/q$) yields the capacitance of the semiconductor depletion layer

$$C_\mathrm{D}(V_\mathrm{G}) = \sqrt{\frac{\varepsilon q p_\mathrm{po}}{2\psi_\mathrm{s}}} = \frac{\varepsilon_\mathrm{s}}{W_\mathrm{D}(V_\mathrm{G})} \,, \tag{5.6}$$

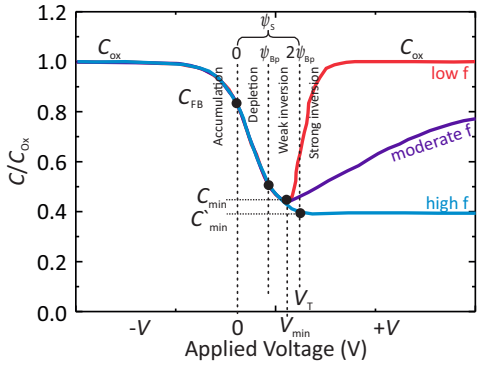


Figure 5.4.: *Typical CV characteristics of a MOSCap on p-type Si for low, medium and high AC-probing frequency. From [82].*

with the gate voltage-dependent depletion width

$$W_{\mathrm{D}}(V_{\mathrm{G}}) = \sqrt{\frac{\varepsilon_{\mathrm{s}}^2}{C_{\mathrm{Ox}}^2} + \frac{2\varepsilon_{\mathrm{s}} V_{\mathrm{G}}}{qN_{\mathrm{D}}}} - \frac{\varepsilon_{\mathrm{s}}}{C_{\mathrm{Ox}}} \,. \tag{5.7}$$

That means the depletion capacitance can be seen as a parallel plate capacitor with the depletion region as dielectric. The total capacitance C of the MOSCap is a series connection of C_{Ox} and C_{D} with

$$C(V_{\mathrm{G}}) = \frac{C_{\mathrm{Ox}} C_{\mathrm{D}}(V_{\mathrm{G}})}{C_{\mathrm{Ox}} + C_{\mathrm{D}}(V_{\mathrm{G}})} \,. \tag{5.8}$$

The C_{Ox}-normalized capacitance C/C_{Ox} of a MOSCap fabricated on p-type Si is depicted in Fig. 5.4 for different bias regimes and frequencies. For negative bias (accumulation) C_{D} is large compared to C_{Ox} so that C is dominated by C_{Ox}. Within the valid region of this approximation ($\psi_{\mathrm{Bp}} > \psi_{\mathrm{s}} > k_{\mathrm{B}}T/q$) C_{D} decreases with increasing V_{G} as W_{D} increases. As a consequence in depletion also the overall capacitance C decreases as a function of V_{G}. Once inversion sets in for further positive biases the inversion charge is generated close to the interface and results in a very large capacitance. As a consequence C increases again and reaches C_{Ox} for strong inversion (low frequency case). For strong inversion the inversion charge density Q_{i} is proportional to the applied bias meaning that the additional AC probing signal slightly undulates Q_{i}. That is, additional minority carriers are generated and annihilate periodically with the probing frequency

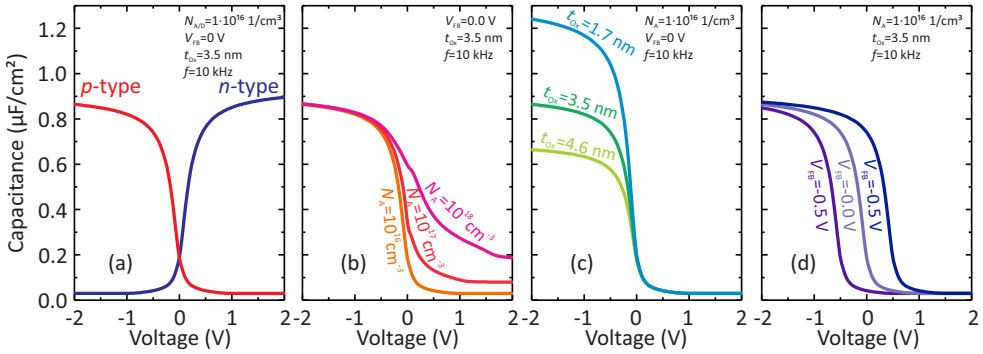


Figure 5.5.: *Simulated MOSCap CV curves on p-type and n-type Si (a) and for different* N_A *(b),* t_{Ox} *(c) and* V_{FB} *(d).*

f. If the probing frequency exceeds the characteristic RC constant for minority carriers (called minority carrier response time τ_R) the generation/recombination cannot follow the AC signal and the semiconductor capacitance remains at the minimum value even when biased in strong inversion (Fig. 5.4, high-f case).

As CV measurements are typically performed in a dark environment, optical carrier generation is negligible so that Shockley-Read-Hall generation/recombination is the dominant carrier generation mechanism [128]. This process relies on thermal generation-/recombination of carriers *via* bulk-traps residing within the bandgap. It is thus more efficient for smaller E_G due to the reduced energy distance from the trap level to the conduction or valence band edges. This results in an exponential dependence of τ_R on $E_G/2$ [$\tau_R \propto \exp(E_G/2k_BT)$] and thereby scales with the intrinsic carrier concentration n_i [128, 136]. Whereas in Si the high frequency case is already reached for a few Hz, up to several hundred kHz are needed for high Sn content GeSn. This correlation of minority carrier response and bandgap will be discussed in SECTION 5.5.

Another effect that can lead to a similar strong inversion response and frequency dispersion as generation/recombination is diffusion of minority carriers from the bulk. This effect becomes relevant for high mobility samples [137]. Both effects can be described by adding a conductance in parallel to the semiconductor capacitance [*cf.* Fig. 5.1(a)] [128]. One way to discriminate between them is investigating the temperature dependence of the parallel conduction and extracting the associated activation energies [128, 136]. For GeSn this is done in SECTION 5.6.

As an example, several ideal CV curves simulated for Si-based MOSCaps are shown in Fig. 5.5 demonstrating the influence of (a) doping type (p- or n-type), (b) doping concentration, (c) oxide thickness and (d) metal electrode work function on the CV characteristics. Changing the doping type from p-type (as used in the previous explanations) to n-type basically mirrors the CV curve with respect to the y-axis [Fig. 5.5(a)]. According to equation 5.7 a substrate with increased doping is more difficult to deplete ($W_\mathrm{D} \sim \sqrt{1/N_\mathrm{D}}$). As a consequence increasing the doping concentration leads to an increased minimum capacitance C_min [Fig. 5.5(b)]. Reducing t_Ox leads to increased C_Ox according to equation 5.1 [Fig. 5.5(c)]. Modifying the metal gate work function shifts the CV curve (flatband voltage V_FB shift) to the left (right) for lower (increased) metal gate work function [Fig. 5.5(d)].
As an extension to the ideal MOSCap the metal gate electrode or the semiconductor bulk material can exhibit a finite resistance. In connection with oxide and semiconductor capacitance this series resistance may lead to an additional RC-constant resulting in a frequency dependency also in accumulation. As a consequence the measured capacitance might be mistaken as too small [138]. Furthermore as this frequency dispersion in accumulation may be confused with a response from interface traps, the series resistance correction described in Appendix A is applied for the measured capacitance C_m and parallel conductance G_m presented in this work.

5.1.2. Impact of Interface Traps on CV Characteristics

The existence of charge traps in the vicinity of the semiconductor/oxide interface is a known issue degrading the electrical properties of a MOSCap. The following list gives a brief overview of common trap types and their related effects on the CV characteristics [82]:

(i) Fixed charges within the oxide layer result in a constant V_FB-shift similar to a modified metal gate work function,

(ii) A V_FB-shift created by mobile ion-charges depends on the gate voltage polarity and thus leads to hysteresis effects. It is primarily due to ionic impurities like Na^+ and possibly also due to H^+ [108].

(iii) Interface trap states screen the gate voltage resulting in a less effective control of the surface potential. This reduced gate efficiency ($V_\mathrm{G} = \eta V_\mathrm{G(external)}$, $\eta \leq 1$)

leads to a stretch out of the CV curve in x-direction [82,139]. In the worst case the movement of the surface potential is completely suppressed and the Fermi level is effectively pinned. This effect is called Fermi level pinning [138].

(iv) Whereas the stretch out is a static effect, traps also dynamically react to the AC signal applied to the MOSCap due to charging and de-charging of the trap levels. This gives rise to an additional frequency-dependent admittance signal [128, 139]. One typical effect is a bump in the depletion region of the CV curve called D_{it}-bump. For III-V materials also a frequency dispersion in accumulation was reported, denoted to so called border traps [140]. In strong inversion the impact of traps on the CV characteristics is usually negligible [128].

In a MOSFET stretch out degrades the switching slope and scattering with interface charges reduces the channel mobility thereby degrading the on-current [110,112,113,141]. Furthermore V_{th}-shifts degrade the overall circuit performance due to mismatching of individual transistors. In TFETs the charging and de-charging of interface states might lead to *Trap-Assisted Tunneling* (TAT) additionally degrading the switching slope [142]. Interface states with the density Q_{it} per unit area are distributed in energy across the bandgap [128]. This leads to the definition of an interface-trap energy distribution described by [82]

$$D_{\mathrm{it}} = \frac{1}{q}\frac{\mathrm{d}Q_{\mathrm{T}}}{\mathrm{d}E} = \frac{C_{\mathrm{T}}}{q^2} \tag{5.9}$$

D_{it} is usually listed in [number of traps/cm^{2}eV]. One can discriminate further between different D_{it}-species correlated with their origin and position such as *Disorder-Induced Gap States* (DIGS) [143] or *border traps* [140, 143]. For simplicity the term D_{it} is used here as a general description of defect states in the vicinity of the semiconductor oxide interface.

Fig. 5.6 shows the simulated CV characteristics of a n-type GaAs MOSCap with different total trap densities. The semiconductor capacitance is smallest in depletion. As a consequence the impact of an additional trap capacitance is strongest in this bias regime [128]. For relatively low trap densities a bump is observed in the CV curve called D_{it}-bump [Fig. 5.6(a)]. When the D_{it} is further increased and exceeds $D_{\mathrm{it}} > C_{\mathrm{Ox}}/q^2$, that is the trap capacitance becomes higher than the oxide capacitance, *weak Fermi level pinning* sets in resulting in a frequency-dependent shift of V_{FB} [Fig. 5.6(b)]. For even higher trap density the CV curve is completely dominated by the traps resulting in an

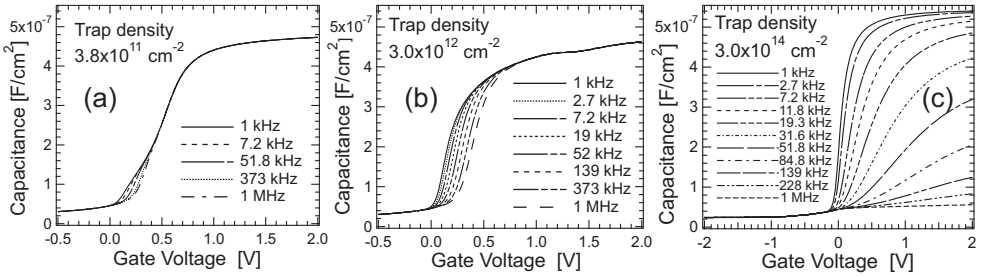


Figure 5.6.: *Simulated CV characteristics of a GaAs MOSCap with different D_{it} levels. Reprinted from [138].*

extreme stretched out and leading to a strong frequency dispersion even in accumulation [Fig. 5.6(c)].

It is obvious that the D_{it} is desired to be as small as possible. Proper sample cleaning and surface passivation techniques are key factors influencing D_{it}. Furthermore dangling bonds at the oxide/semiconductor interface leading to significant D_{it} can be effectively neutralized by thermal treatment in hydrogen rich atmosphere [*Forming Gas Anneal* (FGA)] [108, 144]. In doing so $D_{\mathrm{it}} < 10^{10}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ was achieved for the SiO_2/Si-system [145] and the influence of D_{it} on Si MOSCap properties is usually negligible. However, for less mature material systems as group III-V, Ge or GeSn the D_{it} reduction is a key challenge for achieving high-performance transistors. The analysis of cleaning of GeSn surfaces was presented in CHAPTER 3.1. The effect of FGA on GeSn MOSCap CV behavior is demonstrated in SECTION 5.3 of this chapter along with D_{it} extraction on GeSn-based MOSCaps.

Conductante method

Proposed by Nicollian, Goetzberger and Lopez [145] the conductance method is the most common technique allowing the extraction of D_{it} and trap capture cross section directly from a set of CV and GV measurements without the need of theoretical modeling or fitting of the data. While a detailed derivation and discussion is presented in Ref. [128], here a brief outline of the methodology is presented.

A schematic band diagram of a MOSCap on a n-type semiconductor with interface traps is shown in Fig. 5.7(a). Interface trap levels within the bandgap are filled up to the Fermi level. Due to the applied AC frequency the traps in the vicinity of the

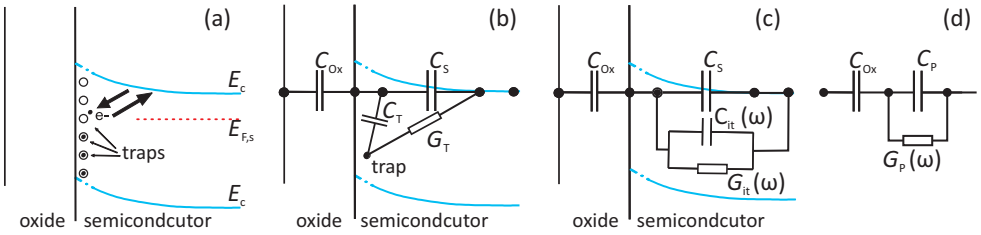


Figure 5.7.: *(a) Band diagram of a MOSCap with traps at the semicondcutor oxide interface showing the capture and emission of electrons with traps close to the Fermi level. (b) The capture and emission process can be modeled electrically by a adding a trap capacitance and a trap conductance (b). Corresponding equivalent circuit (c,d). Adapted from [138].*

Fermi level are charged and discharged periodically. This charge exchange results in an additional parallel trap capacitance. For simplicity we assume a single trap level with C_T denoting its capacitance. The energy dissipation occurring in this process is represented by a conductance G_T connected in series to C_T [Fig. 5.7(b)]. In this model, valid in depletion, only charge exchange with majority carriers (here electrons) is assumed (*i.e.* G_T is only connected to the conduction band, not to the valence band)[1]. The admittance corresponding to this connection of C_S, C_T and G_T on the semiconductor side in Fig. 5.7(b) is

$$Y_\mathrm{S} = i\omega C_\mathrm{S} + \frac{i\omega C_\mathrm{T} G_\mathrm{T}}{G_\mathrm{T} + i\omega C_\mathrm{T}} \,. \tag{5.10}$$

Using the definition of an interface trap lifetime $\tau_\mathrm{T} = C_\mathrm{T}/G_\mathrm{T}$ and sorting equation 5.10 in real- and imaginary part yields

$$Y_\mathrm{S} = \underbrace{\frac{\omega^2 \tau_\mathrm{T} C_\mathrm{T}}{1+\omega^2\tau_\mathrm{T}^2}}_{G_\mathrm{it}=G_\mathrm{P}} + i\omega \underbrace{\left[C_\mathrm{S} + \overbrace{\frac{C_\mathrm{T}}{1+\omega^2\tau_\mathrm{T}^2}}^{C_\mathrm{it}} \right]}_{C_\mathrm{P}} \,. \tag{5.11}$$

That is, the system can be seen as a frequency-dependent conductance $G_\mathrm{it}(\omega) := G_\mathrm{P}(\omega)$ and a parallel capacitance $C_\mathrm{P} = C_\mathrm{S} + C_\mathrm{it}(\omega)$ [Fig. 5.7(c,d)]. This in turn is in series with the oxide capacitance C_Ox. The measured admittance $Y_\mathrm{meas.} = G_\mathrm{meas.} + i\omega C_\mathrm{meas.}$ of the

[1] For a *n*-type semiconductor in depletion the valence band is too far away from the trap level lying at Fermi level to allow efficient charge exchange. However, this situation is different for reduced bandgap materials in weak inversion allowing charge exchange with both bands (see Fig. 5.8).

complete equivalent circuit then is

$$Y_{\text{meas.}} = \left[(i\omega C_{\text{Ox}})^{-1} + (G_{\text{P}} + i\omega C_{\text{P}})^{-1}\right]^{-1} . \tag{5.12}$$

Solving this equation for G_{P} allows to describe G_{P}/ω in terms of the measured quantities $G_{\text{meas.}}$ and $C_{\text{meas.}}$

$$\frac{G_{\text{P}}}{\omega} = \frac{\omega\tau_{\text{T}}C_{\text{T}}}{1+\omega^2\tau_{\text{T}}^2} = \frac{\omega C_{\text{Ox}}^2 G_{\text{meas.}}}{G_{\text{meas.}}^2 + \omega^2(C_{\text{Ox}} - C_{\text{meas.}})^2} , \tag{5.13}$$

where C_{Ox} can be measured in strong accumulation when $C_{\text{meas.}}$ is dominated by C_{Ox}. Equation 5.13 undergoes a maximum for $\omega\tau_{\text{T}} = 1$. That is, measuring G_{P}/ω as a function of ω for a given gate bias yields directly

$$C_{\text{T}} = 2\left(\frac{G_{\text{P}}}{\omega}\right)_{\text{max.}} \tag{5.14}$$

from the peak value and $\tau_{\text{T}} = 1/\omega = 1/(2\pi f)$ from the peak position. With $D_{\text{it}} = C_{\text{T}}/q^2$ (equation 5.9) this method allows to directly extract the D_{it} form the measured conductance as

$$D_{\text{it}} = \frac{2}{q^2}\left(\frac{G_{\text{P}}}{\omega}\right)_{\text{max.}} , \tag{5.15}$$

giving this technique its name *conductance method*. Equation 5.15 describes the D_{it} of a single trap level. However, in a real structure a distribution of traps across the bandgap exists that could be modeled in analogy with Fig. 5.7(b) as cascading of C_{T}, G_{T} networks. As a consequence G_{P}/ω is modified by a convolution of equation 5.13 with a trap distribution and occupation function. A solution for a single level trap type distributed over the bandgap was derived first by Lehovec [146]. An approximate solution yields a modified version of equation 5.15

$$D_{\text{it}} \approx \frac{2.485}{q^2}\left(\frac{G_{\text{P}}}{\omega}\right)_{\text{max.}} . \tag{5.16}$$

Repeating the G_{P}/ω-*vs.*-ω sweeps for a set of gate voltages moves the band and thereby the trap states through the Fermi level. It thus allows the extraction of a D_{it}-*vs.*-V_{G} profile. In order to receive a D_{it}-*vs.*-energy profile and to locate the D_{it} with respect to the majority carrier band edge the gate voltage has to be translated to the corresponding surface potential. The relation between V_{G} and ψ_{s} can be obtained by calculating the

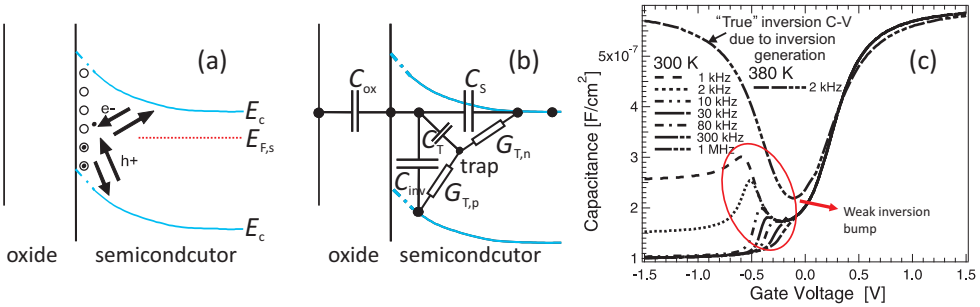


Figure 5.8.: *(a) Band diagram of a MOSCap with traps at the semicondcutor oxide interface biased in weak inversion, showing charge exchange with both bands. (b) Corresponding equivalent circuit. (c) Simulated MOSCap on n-Ge with a* D_{it} *of* $7 \cdot 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ *showing weak inversion response. Adapted from [138].*

so called Berglund integral from a low frequency CV curve as described in Ref. [128]

$$\psi_{\mathrm{s}}(V_{\mathrm{G}}) - \psi_{\mathrm{s}}(V_{\mathrm{FB}}) = \int_{V_{\mathrm{FB}}}^{V_{\mathrm{G}}} \left[1 - \frac{C_{\mathrm{LF}}(V_{\mathrm{G}})}{C_{\mathrm{Ox}}}\right] \mathrm{d}V \;, \tag{5.17}$$

where $\psi_{\mathrm{s}}(V_{\mathrm{FB}}) := 0$. The Berglund integral yields the trap position in the bandgap up to an integration constant that is given by the position of the Fermi level in flatband condition $q\psi_{\mathrm{Bp}} = (k_{\mathrm{B}}T/q)\ln(N_{\mathrm{A}}/n_{\mathrm{i}})$ [*cf.* Fig. 5.3]. The trap energy relation is then (for a *p*-type semiconductor):

$$E_{\mathrm{T}} - E_{\mathrm{V}} = \frac{E_{\mathrm{G}}}{2} + q\psi_{\mathrm{s}}(V_{\mathrm{G}}) - q\psi_{\mathrm{Bp}} \;. \tag{5.18}$$

Since the energy position depends on the flatband voltage this technique might be inaccurate for samples with a frequency-dependent flatband voltage shift. However, the aim here is to get a rough overview of trap density and energy rather than a precise trap energy profile. The conductance method is used in SECTION 5.3 for the extraction of D_{it} in GeSn. For the discussion of other D_{it}-extraction methods see the comprehensive works by Schroder [108] and by Nicollian and Brews [128]. More advanced methods rely on numerical fitting of the experimental data with a distributed trap model [147, 148].

Peculiarties for novel low bandgap semiconductors

As discussed above the conductance method does only take into account charge exchange of traps with the majority carrier band. This assumption is correct in depletion since the minority carrier band is too far away from the Fermi level to allow efficient charge exchange. However, it is not valid in weak-inversion [128]. Here traps can communicate with both majority carrier and minority carrier band as sketched in Fig. 5.8(a,b). The additional admittance resulting from this "dual communication" [138] is stronger than the trap response in depletion. As the semiconductor capacitance is still small in weak inversion, this so called *weak inversion response* can have significant influence on the CV characteristics in this bias regime. For Si this situation is of marginal relevance since D_{it} is usually very low and its impact is limited to the D_{it}-bump in depletion [128]. Most importantly the frequencies to observe this phenomenon are below the common range of 1 kHz-1 MHz at 77-300 K. It was though observed for very low frequencies and for x-ray-irradiated Si MOSCaps [146, 149]. That is Si MOSCaps usually feature well-formed, steep CV characteristics without noticeable frequency dispersion. Even without forming gas resulting in $D_{\mathrm{it}} \approx 1 \cdot 10^{12}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ the D_{it} does not dominate the CV characteristics [138].

However, the situation is completely different for novel lower bandgap materials as Ge, GeSn or InGaAs. Here correct D_{it} extraction is not straight forward [137, 150]. First D_{it} is generally much higher for this less mature materials so that effects like stretch out and *weak Fermi level pinning* become relevant [138, 151]. Second as a consequence of their low bandgap these materials are also more sensitive towards D_{it} [152]. Here both majority carrier and minority carrier band are closer to the traps in the vicinity of Fermi level thereby allowing an easier charge transfer from the trap into either of the bands. The frequency range at which weak inversion is observable exponentially depends on the bandgap [$\propto \exp(-E_{\mathrm{G}}/k_{\mathrm{B}}T)$] and moves into the applicable range of 1 kHz to 1 MHz for lower bandgaps. As a consequence the *weak inversion response* has significant impact on the CV characteristics in these semiconductors. Even for moderate D_{it} it leads to a distinct bump in the CV curve as shown in Fig. 5.8(c) that is denoted as *weak inversion bump* and should not be confused with the D_{it}-bump occurring in depletion for significantly higher D_{it} [137]. That is, low bandgap semiconductors are more sensitive towards D_{it} than higher bandgap semiconductors as Si [153]. Consequently the *weak inversion response* impedes application of the *conductance method* for D_{it} extraction.

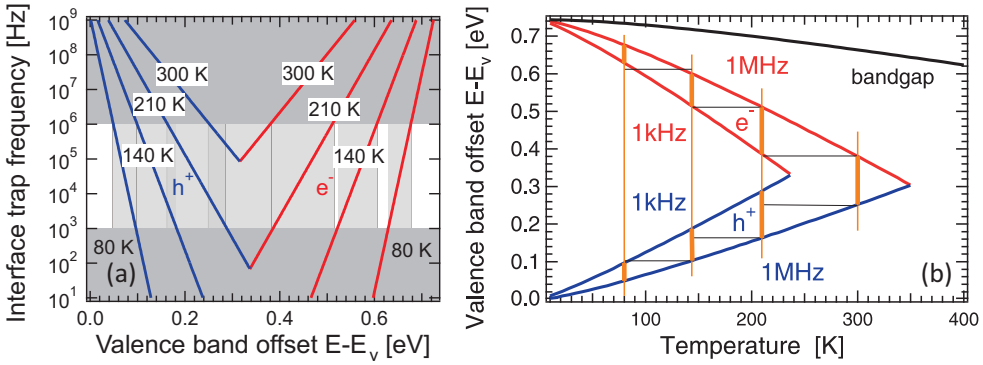


Figure 5.9.: *(a) Calculated interface trap frequency* $1/(2\pi\tau_T)$ *vs. trap energy measured from valence band for different temperatures. The measurable range* 1 kHz *to* 1 MHz *is shaded light gray. (b) Detectable trap energy range vs. temperature. Calculations for Ge. Reprinted from [138].*

The *weak inversion bump* would be confused as major D_{it} contribution resulting in falsely high D_{it}-values. A model for the description of the admittance behavior in weak inversion was developed by Cooper and Schwartz [154]. The peculiarties for low bandgap semiconductors were first described by Martens *et al.* [137] and by Batude *et al.* [153]. For a reliable D_{it} extraction in these materials either modified versions of the conductance method should be used that take into account the enhanced interaction with minority carriers [137,147], or the minority carrier response should be suppressed by reducing the temperature. However, the latter is done at the expense of a smaller energy window that can be sampled and a possible underestimation of D_{it} due to trap response freeze-out [137,150]. The trap time constant exponentially depends on the energetically distance ΔE of a trap to the adjacent band [138]

$$\tau_T \propto \exp(\Delta E/k_B T) \, . \tag{5.19}$$

For lower bandgap semiconductors ΔE is smaller resulting in a significantly shorter τ_T and higher corresponding (G_P/ω) peak frequencies. Fig. 5.9(a) shows τ_T as a function of the trap position in the bandgap for several temperatures, as calculated for Ge. The corresponding detectable trap energy range *vs.* temperature is depicted in Fig. 5.9(b). For Ge only a small range around midgap is detectable and is impaired by the minority carrier response. A reduction of the measurement temperature separates majority and

minority carrier responses and moves the detectable energy range closer to the band edges.

For the high Sn content samples treated in this work the bandgap is small enough that even at room temperature the weak inversion regime can be fully masked by a strong inversion response due to enhanced minority carrier generation which results in a U-shaped CV curve similar to the one depicted in Fig. 5.8(c) for 380 K. Thus temperature-dependent measurements are indispensable for an unambiguous discrimination between weak inversion and D_{it} [138].

5.2. Fabrication and Verification of (Si)GeSn MOS-Structures

The fabrication of GeSn MOS structures is a key step for the realization of GeSn-based FET-devices. Within the experimentally feasible Sn content range of 0-15 % GeSn can be treated as a Ge-like alloy so that findings from Ge MOS-structure optimization might be transferred to GeSn and can be used as a starting point for further optimization. Thus first a brief overview of Ge MOS-technology is given. Detailed descriptions can be found in [113, 155–157]. In contrast to the compliant SiO_2/Si-interface, the Ge/GeO_x-interface is both thermally and chemically less stable. If exposed to air a mixture of GeO and GeO_2 with different morphologies is formed on a pristine Ge-wafer [66, 158]. Due to its high vapor pressure GeO tends to desorb from the Ge/GeO_x-interface during thermal treatment (for example during high-κ deposition) leaving behind a defective film with Ge-suboxides and high D_{it} [157, 159]. On the other hand hexagonal and amorphous GeO_2 (α-GeO_2) are soluble in water and tend to absorb moisture and organic molecules from ambient [66, 113]. As a consequence one might come to the conclusion that the formation of a GeO_x-interlayer between Ge and the high-κ dielectric should be suppressed as much as possible. Indeed, thanks to the fact that the formation of GeO_x is less favorable, it was shown that the fabrication of an interlayer-free high-κ/Ge stack is possible [155, 160], in contrast to Si where the formation of a thin SiO_x *Interfacial Layer* (IL) is unavoidable. This in turn might suggest that high-κ scaling to achieve high C_{Ox} seems to be easier on Ge than on Si [155, 160]. However, counter intuitively it turned out that the electrical properties of Ge MOS structures without IL have worse electrical properties than those with an intentionally formed interlayer [144,155,160,161]. Mainly intermixing of Ge and the high-κ layer was suspected as possible explanation for the degraded electrical properties [144,156,162,163]. Recently Zeng *et al.* identified the

delayed, island type nucleation and growth mechanism of Al_2O_3 on oxide free (hydrogen terminated) Ge as an origin of dangling bonds and increased leakage [161]. On the other hand they found that an intentionally formed GeO_x-interlayer efficiently suppresses oxygen diffusion from the high-κ into Ge. That is, precice control of an interlayer as an interface passivation is the key for realizing high-quality Ge MOS stacks. Numerous approaches have been investigated such as (i) replacing the GeO_x-interlayer with a SiO_x interlayer by deposition of a few monolayers of Si [164,165], (ii) nitridation [160,162,166], (iii) sulfurisation [167] and (iv) different forms of Ge-oxidation in controlled environment [111, 144, 155, 156]. The latter method resulted in the demonstration of very low, Si-comparable D_{it} of $\approx 5 \cdot 10^{10}\,cm^{-2}eV^{-1}$ [168] especially when diffusion/desorption of GeO was suppressed [169], for example by high pressure oxidation [159] or by so called *in-situ plasma post oxidation* through a thin Al_2O_3-layer [168]. In terms of high-κ material selection, a stack of $GeO_x/Al_2O_3/HfO_2$ delivered the best compromise of low D_{it} and high C_{Ox} [113, 114, 161] but also other dielectrics as $HfZrO_2$ or $LaLuO_3$ are promising candidates for Ge MOS technology [130, 170, 171].

When translating from Ge to (Si)GeSn MOSCaps two further constraints should be taken into account: (i) The metastability of (Si)GeSn results in a limited thermal budget such that all fabrication steps should be below 300-350 °C in order to avoid Sn diffusion and the formation of β-Sn precipitates [61,172]. (ii) The pre-high-κ deposition cleaning is a crucial step for MOS stack fabrication. However, tin oxide SnO_2 can show metallic behavior [69] and it is evident that the formation of a metallic interlayer is undesired. Worse than that, due to the water solubility of GeO_2, SnO_x tends to accumulate at the GeSn-surface during wet chemical treatment (*cf.* CHAPTER 3.1) such that special care should be taken to assure a process start on a pristine, native oxide free wafer prior to the controlled formation of a [(Si)GeSn]O_x-interlayer. Cleaning of GeSn was analyzed in CHAPTER 3.1 and verified *via* XPS analysis. This procedure including the "HF-HCl-last" native oxide removal is implemented here as the latter was reported to improve GeSn MOS CV characteristics [68].

For GeSn passivation several strategies were reported, similar to those used for Ge. They include ozone oxidation [116], sulfur passivation [118] and Si passivation [31, 33]. As a starting point for (Si)GeSn MOSCap fabrication here a process was adapted previously developed in our group and reported by S. Wirths *et al.* for initial experiments on tensely strained Ge and GeSn [119]. Subsequent to the "HF-HCl"-last clean (Si)GeSn

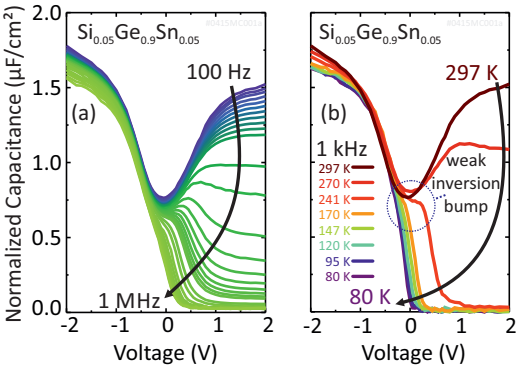


Figure 5.10.: *(a,b) CV measurements of a* $Pt/HfO_2/(SiGeSn)O_x/Si_{0.05}Ge_{0.9}Sn_{0.05}$ *MOSCap. (a) Frequency dependence at* 300 K*; (b) Temperature dependence at* 1 kHz*.*

unintentionally doped (p-type) samples with different Si/Sn content were directly loaded into a 300 mm AIXTRON ALD cluster tool. This process utilizes the reactive ozone precursor for the intentional *in-situ* formation of a $GeSnO_x$-interlayer by use of 5 min continuous ozone injection at 300 °C. As a next step 5 nm HfO_2 were deposited at 300 °C using *Tetrakis Ethyl Methyl Amino Hafnium* (TEMAH), $Hf[(CH_3)(H_2H_5)]_4$ and ozone (O_3) as precursors.

To verify this process, as a start Pt was used as gate metal which was evaporated through a shadow mask using electron beam evaporation. The fabrication ended with a FGA (4 % H_2 in 96 % N_2) where 300 °C turned out to be a the upper limit to ensure minimal Sn and Ge diffusion through the MOS stack and epilayer [119]. CV measurements were performed with an Agilent E4980A LCR-meter. If not otherwise specified the measurement occurred "top-to-top". That is, the low-potential probe was placed on a capacitor that is several orders of magnitude larger than the one to be tested. As both capacitors are connected in series the characteristics are fully governed by the smaller capacitance. That way the fabrication of an Ohmic back contact could be omitted. A representative multifrequency measurement on a $Si_{0.05}Ge_{0.9}Sn_{0.05}$ MOSCap is shown in Fig. 5.10(a). Despite a slight frequency dispersion in accumulation that might be attributed to series resistance, the MOSCap shows decent switching characteristics similar to those of state of the art Ge or low bandgap III-V MOSCaps [138, 173]. As discussed in the previous SECTION 5.1.2, thanks to enhanced minority carrier generation originating from the small bandgap, the MOSCaps show U-shaped low frequency behavior even at moderate

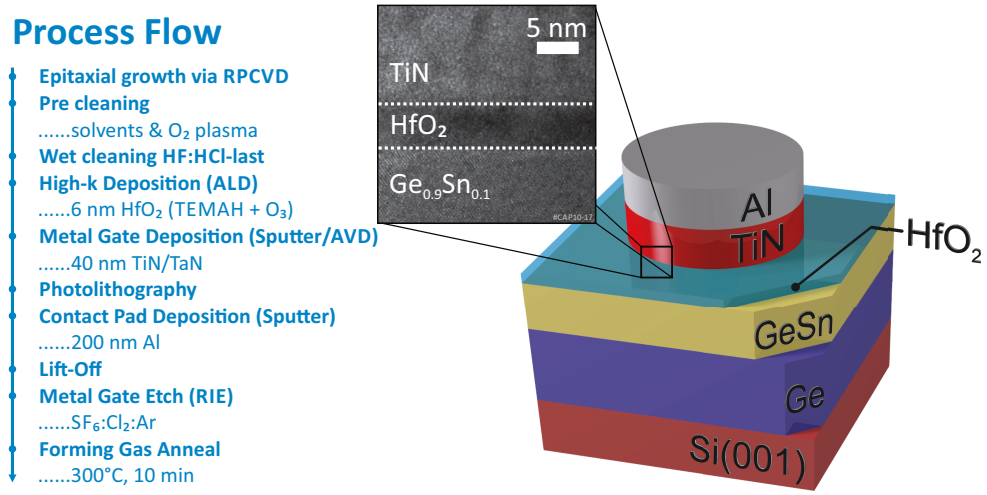


Figure 5.11.: *Left: (Si)GeSn MOSCap fabrication flow for device integration with TiN/TaN metal gates. Right: sketched layer stack and XTEM of a TiN/*$HfO_2Ge_{0.9}Sn_{0.1}$ *MOSCap. XTEM recorded by Steffi Lenk.*

frequencies $> 1\,\text{kHz}$ at room temperature. The CV characteristics feature a *weak inversion bump* typical for low bandgap semiconductors [152, 153] as introduced in SECTION 5.1.2. Temperature-dependent measurements shown in Fig. 5.10(b) reveal a successful suppression of the minority carrier response and thereby also of the weak inversion bump at reduced temperatures. This enables the applications of the conductance method for D_{it}-extraction in SECTION 5.3. At temperatures below 150 K this MOSCap shows a steep CV curve without a noticable D_{it}-bump in depletion. The CV characteristics are in analogy with a *n*-Ge MOSCap reprinted from Ref. [138] in Fig. 5.8(c) reflecting the observed behavior.

With a verified high-κ deposition process at hands the integration of a CMOS compatible *Titanium Nitride* (TiN) or *Tantalum Nitride* (TaN) metal gate process is highly desirable for FET device fabrication and process reliability especially because the available ALD-AVD cluster tool allows automated *in-situ* transfer from the high-κ ALD chamber to the AVD-metal gate reactor. *Atomic Vapor Deposition* (AVD) is a technique similar to ALD relying on the surface reaction of two precursors. However, here the metal precursor TBTDET[2] is injected in pulses whereas the reduction agent ammonia, NH_3

[2] Tris(diethylamido)(*tert*-butlyimino)tantalum $[((C_2H_5)_2N)_3(C_4H_9N)Ta]$

is delivered continuously. That way 40 nm TaN are deposited. Alternatively, a 40 nm TiN metal gate is deposited *via* reactive sputtering in a 200 mm Oerlikon LLSEVO sputter tool. The metal gate is structured by defining 200 nm thick Al contact pads applying a lift-off process. The Al pads act as a hard mask in the subsequent metal gate etch in a Cl_2:SF_6:Ar RIE plasma. Like MOSCaps with Pt gate, the fabrication ends with a FGA at 300 °C for 10 min. The key fabrication steps are summarized in Fig. 5.11 together with an illustrated MOSCap and a cross sectional TEM (XTEM) of a TiN/HfO_2/$Ge_{0.9}Sn_{0.1}$ MOSCap demonstrating high GeSn crystalline quality and smooth interfaces.

Typical metal gate deposition processes for Si technology require process temperatures ≥ 450 °C [174]. Despite the fact that this is well above growth temperature and stability range of high Sn content (≥ 10 % Sn) GeSn, proper CV characteristics are observed for a TaN/HfO_2 MOSCap fabricated on ternary $Si_{0.1}Ge_{0.81}Sn_{0.09}$ with a 450 °C TaN process as shown in Fig. 5.12. In fact the characteristics are comparable to those obtained for Pt metal contacts deposited without intentional heating. This is supported by a ToF-SIMS analysis of this sample indicating only marginal intermixing of HfO_2/$Si_{0.1}Ge_{0.81}Sn_{0.09}$ and HfO_2 layer [Fig. 5.13(a)]. In contrast, when this process was applied to a binary $Ge_{0.9}Sn_{0.1}$ with approximately the same Sn content of 10 % no regular CV characteristics could be measured. The MOSCap showed no insulating behavior indicating strong diffusion of Sn through the dielectric as confirmed by the ToF-SIMS analysis in Fig. 5.13(b) showing a smear out of the Sn-layer and a Sn peak at the HfO_2/GeSn interface. Furthermore, Sn precipitations are observed with optical microscopy as can be seen in Fig. 5.13(c) which are most probably metallic β-Sn forming patterns typically observed on GeSn after thermal treatment above the thermal stability range [61, 172, 175]. That is, the incorporation of Si towards ternary SiGeSn results in an apparent improvement of the thermal stability for a given Sn content. This was predicted by Xie *et al.* by the increased mixing entropy of SiGeSn as compared to the binary [62]. However, for successful

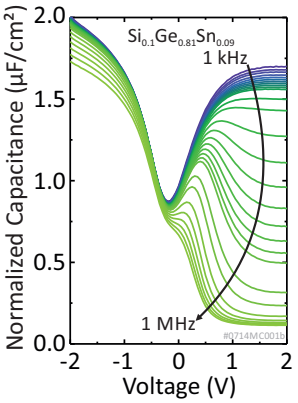


Figure 5.12.: *Multifrequency CV characteristics of a TaN/HfO_2/SiGeSn MOSCap fabricated with a 450 °C TaN metal gate process.*

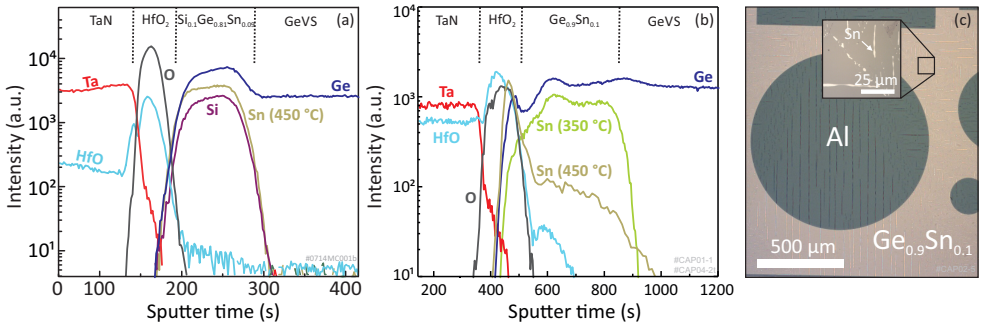


Figure 5.13.: *ToF-SIMS analysis of MOS stacks with in-situ AVD-TaN deposition on* HfO_2*/*$Si_{0.1}Ge_{0.81}Sn_{0.09}$ *(a) and on* HfO_2*/*$Ge_{0.9}Sn_{0.1}$ *(b). For a deposition temperature of* 450 °C *insignificant Sn diffusion is observed for* $Si_{0.1}Ge_{0.81}Sn_{0.09}$ *compared to strong Sn diffusion and interface smear out for* $Ge_{0.9}Sn_{0.1}$*. A reduction of the deposition temperature to* 350 °C *suppresses Sn diffusion in* $Ge_{0.9}Sn_{0.1}$*. The strong HfO signal within the TaN-layer is caused by mass interference of HfO and TaN. (c) Sn precipitates visible in an optical microscopy image after* 450 °C *TaN deposition on* $Ge_{0.9}Sn_{0.1}$*. ToF-SIMS recorded by Uwe Breuer, ZEA-3, FZ-Jülich.*

process integration with GeSn a reduction of the TaN metal gate temperature is mandatory. With a reduction down to 350 °C Sn diffusion is significantly suppressed as can be seen from the Sn signal in Fig. 5.13(b). Indeed, solely reducing the AVD deposition temperature without further process optimization results in a degraded TaN film with increased resistivity. This is mainly due to stoichiometry changes, a reduced density with consequential post-deposition *ex-situ* oxygen uptake and the contamination with carbon rich by-products as a consequence of an incomplete reaction [124]. Thanks to an optimized process developed in our group a low TaN resistivity of 200 µΩ cm could be restored despite the reduced temperature of 350 °C as reported in ACS Applied Materials & Interfaces [124].

This process was successfully applied to several samples with Sn contents ranging from 0 % (GeVS) to 12.5 % Sn using 5 nm HfO_2 as high-κ dielectric. As process verification the samples were characterized in a Karl Süss PA300 automated wafer prober allowing the measurement of dozens of capacitors for variability analysis. A set of CV curves for frequencies from 10 kHz to 1 MHz on GeVS, $Ge_{0.915}Sn_{0.085}$ and $Ge_{0.875}Sn_{0.125}$ is shown in Fig. 5.14. The MOSCaps feature well-behaving CV curves with minimal frequency-dependent flatband voltage shift and only slight variations from device to device indicating no significant diffusion of Sn into the high-κ stack. This is supported

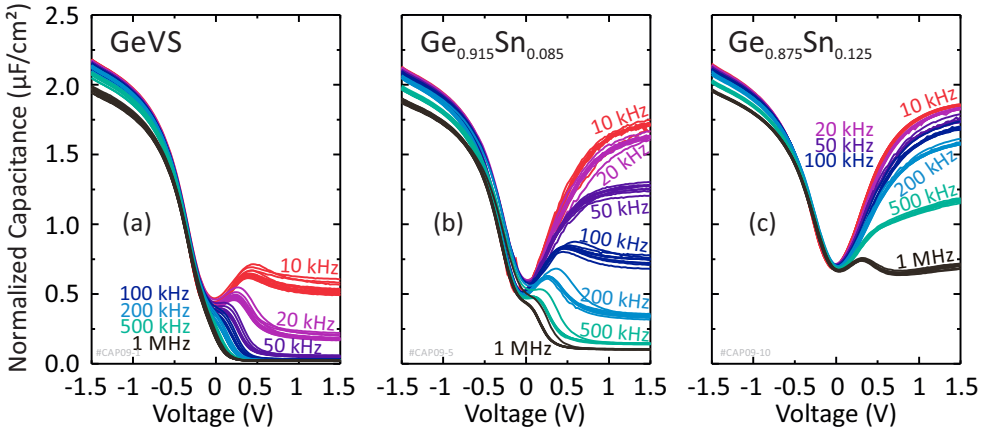
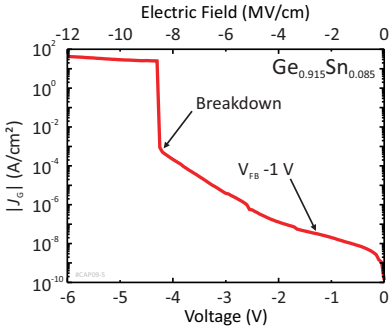


Figure 5.14.: *Variability of AVD-TaN/*HfO_2*-Ge(Sn) MOSCaps CV characteristics: (a) Ge, (b)* $Ge_{0.915}Sn_{0.085}$*, (c)* $Ge_{0.875}Sn_{0.125}$*.*



x_{Sn} (%)	V_{BD} (V)	$\mathcal{E}_{BD}$ (MV/cm)	V_{FB} (V)	J_G @ ($V_{FB}-1$ V) (A/cm²)
0	-4.2	-8.4	-0.35	$2.8 \cdot 10^{-8}$
8.5	-4.3	-8.6	-0.30	$3.2 \cdot 10^{-8}$
12.5	-3.9	-7.7	-0.30	$4.2 \cdot 10^{-8}$

Figure 5.15 & Table 5.1.: *IV measurements of* 350 °C *deposited AVD TaN/* 5 nm HfO_2 *MOSCaps on Ge(Sn) biased in accumulation. (left) gate leakage vs. gate bias for* 8.5 % Sn*, (right) breakdown voltage* V_{BD}*, corresponding electric field* $\mathcal{E}_{BD}$ *and gate leakage current density* J_G *for different Sn contents.* V_{FB} *from Fig. 5.14.*

in a subsequent analysis of gate leakage current J_G and breakdown field $\mathcal{E}_{BD}$. For this purpose a metallic back contact was realized by sputtering Al on the backside of the samples. J_G was measured DC with a Keithley 4200SCS semiconductor parameter analyzer. A representative measurement of the 8.5 % Sn-sample is shown in Fig. 5.15.

Gate leakage is very low with $3.2 \cdot 10^{-8}\,\mathrm{A/cm^2}$ at $V_{FB} - 1\,\mathrm{V}$. Electrical breakdown occurs at approximately $V_G = -4.3\,\mathrm{V}$ corresponding to an electric field of $\mathcal{E}_{BD} = 8.6\,\mathrm{MV/cm}$ which is a typical value for HfO_2 [176]. The leakage characteristics are summarized in table 5.1 for the three stacks from Fig. 5.14. No trend with Sn content is observed supporting the hypothesis of reduced Sn diffusion for this 350 °C process.

If not otherwise specified all CV curves presented in this work are measured on MOSCaps subjected to FGA. The influence of FGA on the CV characteristics was reported to be beneficial for Ge-based MOSCaps [144] and is demonstrated in Fig. 5.16 for a $Ge_{0.937}Sn_{0.063}$ MOSCap with 3 nm HfO_2 and TiN metal gate. Prior to FGA the CV curve suffers from a high C_{min} pointing to an impeded band bending due to *weak Fermi level pinning*. Furthermore there is a strong frequency-dependent flatband voltage shift and strong deviation from a regular CV curve for low frequencies. The latter is probably due to gate leakage. On the contrary after FGA C_{min} is significantly reduced and well behaving CV curves are observed.

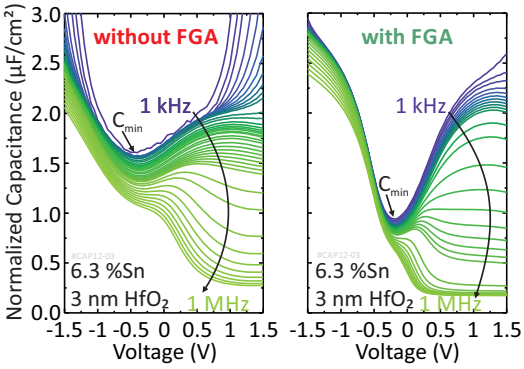


Figure 5.16.: *Demonstration of the positive effect of FGA on CV characteristics of a TiN/HfO_2/$Ge_{0.937}Sn_{0.063}$ MOSCap.*

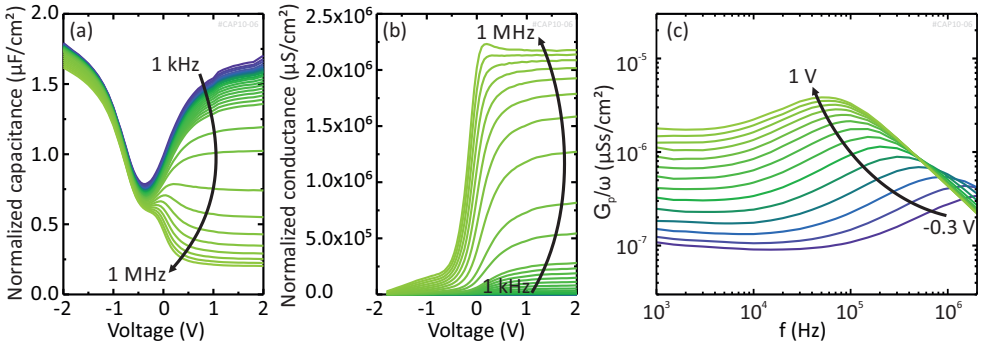


Figure 5.17.: *Characteristics of a TiN/*5 nm $HfO_2/Ge_{0.915}Sn_{0.085}$ *MOSCap:(a) CV,(b) GV, (c)* G_p/ω *vs.* f.

5.3. Extraction of Interface Trap Densities

A comprehensive and quantitative characterization of the high-κ/(Si)GeSn stack also contains the extraction of the interface trap density D_{it}. The methodology was explained in SECTION 5.1.2. That way numerous (Si)GeSn MOSCaps with a wide range of Si and Sn contents were characterized using multifrequency temperature-dependent CV and GV measurements in the range 1 kHz-1 MHz and 80 K-300 K. An exemplary set of CV and GV measurements obtained on a TiN/6 nm $HfO_2/Ge_{0.915}Sn_{0.085}$ MOSCap is presented in Fig. 5.17(a,b). For D_{it} extraction a transposed data set of *C-vs.-f* and *G-vs.-f* measurements is used and G_P/ω is calculated according to equation 5.13 for each gate voltage and plotted against the frequency [Fig. 5.17(c)]. The D_{it} is then extracted from the maximum of G_P/ω with use of equation 5.16. Only traps in the vicinity of the Fermi level respond to the AC-probing signal. By changing the gate voltage the bands move through the Fermi level and thereby the trap distribution within the bandgap is scanned. As can be seen in Fig. 5.17(c) the characteristic frequency f_{peak} at which the G_P/ω-maximum occurs decreases with increasing gate voltage as the sampled trap levels move further away from the valence band [see also Fig. 5.18(c) and equation 5.19].

In order to locate the traps within the bandgap the extracted D_{it}-*vs.*-V_G distribution is translated to an D_{it}-*vs.*-energy distribution by calculating the Berglund integral from the CV data as described in SECTION 5.1.2, equation 5.18. The measured characteristic frequency *vs.* trap energy is presented in Fig. 5.18(c) and reflects the temperature

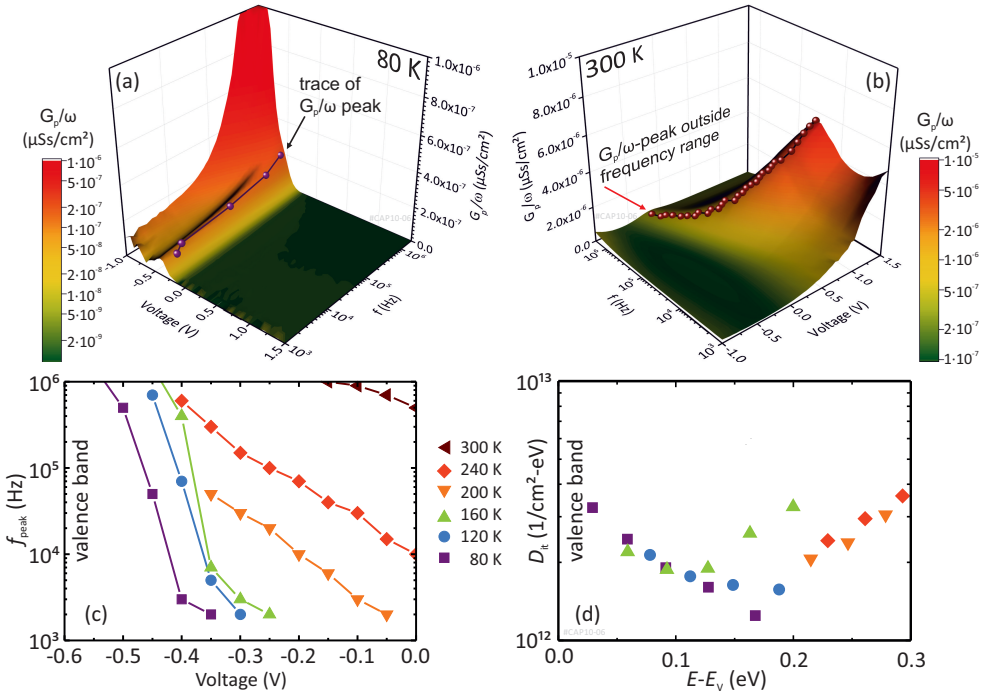


Figure 5.18.: *D_{it}-extraction for a TiN/6 nm HfO_2/$Ge_{0.915}Sn_{0.085}$ MOSCap: (a,b) 3D-plot of G_P/ω vs. V_G and f for 80 K and for 300 K. (c) Characteristic trap frequency vs. gate voltage for different temperatures demonstrating a reduction in the energy window with a shift towards the valence band edge with reduction of the measurement temperature. (d) Corresponding D_{it}-vs.-trap energy profile.*

dependence expected from Fig. 5.9(a). As discussed in SECTION 5.1.2 at room temperature weak inversion bump and minority carrier generation impede the application of the conductance method. However, these effects can be suppressed by reducing the sample temperature. This is shown in 3D-plots of G_P/ω *vs.* V_G and f in Fig. 5.18(a,b) demonstrating a suppressed parallel conductance in inversion (positive bias) for low temperature and thereby allowing the application of the conductance method. On the other hand a reduction of the sample temperature reduces the energy window sampled by the conductance method. At reduced temperatures traps in the middle of the bandgap cannot exchange carriers with either of the bands such that the sampled energy window shifts to the band edges as also expected from equation 5.19. This effect is illustrated

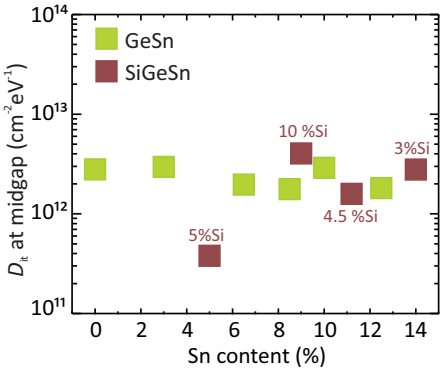


Figure 5.19.: *D_{it} at midgap vs. Sn content for several samples covering a wide range of Sn content. GeSn with TiN and SiGeSn with Pt metal gate, respectively.*

by the trace of the G_P/ω peak in Fig. 5.18(a,b,c) covering a much narrower gate voltage window ($\hat{=}$ energy window) for 80 K as compared to 300 K. The extracted D_{it}-*vs.*-trap energy profile is presented in Fig. 5.18(d) for a set of measurement temperatures. The reduced temperature allows the D_{it} extraction for traps closer to the valence band edge in consistency with literature reports [115]. It should be noted that data for values above 200 K might be erroneous due to enhanced minority carrier response. Also the Berglund integral extraction of specific trap energies might be impeded due to stretch out of the CV curves. The D_{it} at midgap extracted for samples with a wide range of Si and Sn contents is presented in Fig. 5.19. Reasonable D_{it} values in the low to mid $10^{12}\,cm^{-2}eV^{-1}$-range have been achieved. It is noticeable that the incorporation of Sn does not seem to degrade the interface properties. This point is important as it suggests that the enormous progress achieved on Ge MOS technology might be transferred to GeSn. Indeed the intentional incorporation of Sn in $GeSnO_x$ was reported to enhance the interface properties of Ge MOSCap as Sn and other metals can stabilize the GeO_x and thereby reduce intermixing with Ge [161, 163].

5.4. high-κ scaling on GeSn MOS-Structures

For MOSFETs high C_{Ox} is desired, since it yields increased output currents. In turn for a TFET a high C_{Ox} is essential for realizing both steep switching and high on-current [10]. Common figures of merit when comparing different high-κ stacks are the

Capacitance Equivalent Thickness (CET) and the *Equivalent Oxide Thickness* (EOT). The definition of CET stems from the transition from SiO_2 as gate dielectric to high-κ layers and defines the corresponding thickness of a SiO_2-based capacitor that is needed to achieve the same capacitance as the high-κ device under test:

$$\mathrm{CET} = \frac{\varepsilon_0 \varepsilon_{\mathrm{SiO_2}}}{C_{\mathrm{Ox}}} \,. \tag{5.20}$$

For thin oxides charge quantization in the inversion layer results in a slight displacement of the charge centroid away from the high-κ/semiconductor interface. This quantum mechanical correction is taken into account with the definition of the EOT = CET − QM_{corr}. The correction is $QM_{\mathrm{corr}} \approx 0.3\,\mathrm{nm}$ for Ge [177].

Achieving low EOT while maintaining low leakage and small D_{it} is a challenging task. For Si the low-κ SiO_2-interlayer that forms unavoidably between Si and high-κ is a big obstruction. In contrast for Ge an interlayer can be completely suppressed but is needed for maintaining low D_{it}. Indeed it was shown that D_{it} in Ge decreases with increasing GeO_x thickness [112, 113]. Because HfO_2 has a high κ-value (= high $\varepsilon_{\mathrm{Ox}}$) it seemed to be a promising candidate for scaled Ge MOSCaps, however, intermixing of HfO_2 with Ge occurs if the GeO_x-interlayer is too thin, resulting in high D_{it}, increased leakage and thus limits the scalability [162]. On the contrary Al_2O_3 was shown to stabilize the GeO_x interlayer and thereby reduces intermixing and D_{it} albeit at the expense of the lower dielectric constant of Al_2O_3 [113, 178]. Indeed the best compromise for Ge was achieved with a tri-layer stack of thin Al_2O_3 passivated GeO_x covered with a top high-κ layer of HfO_2 [113, 114, 179].

The CV characteristics of such a stack of 1 nm Al_2O_3 and 2 nm HfO_2 fabricated with the available O_3 ALD-cluster tool are shown in Fig. 5.20(a-c) for three different Sn contents. Despite the ultra thin gate dielectric a relatively low accumulation capacitance of $\sim 2.4\,\mu\mathrm{F/cm^2}$ was measured. Even though in this case no intentional O_3 oxidation step was used, a GeO_x interlayer thickness of $\sim 0.8\,\mathrm{nm}$ is estimated from the accumulation capacitance, which is in good agreement with literature reports [144]. For the estimation an interlayer GeO_x relative permittivity of $\varepsilon_{\mathrm{GeO_x}} = 6$ [179], $\varepsilon_{\mathrm{Al2O_3}} = 8.5$ and $\varepsilon_{\mathrm{HfO_2}} = 18$ was assumed. The high reactivity of O_3 results in subcutaneous Ge oxidation and leads to a relatively thick interlayer whose thickness is more or less independent of the fact whether the process started on an intentionally formed GeO_x-layer or on an oxide free Ge-surface [144]. This limits the scalability of O_3-based processes and suggests the use

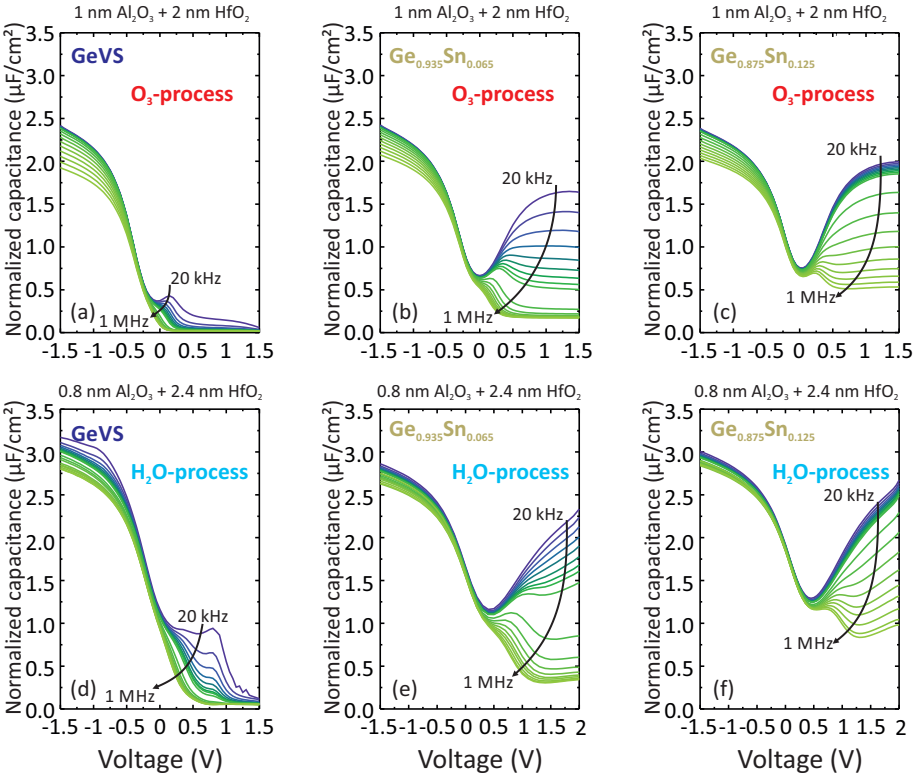


Figure 5.20.: *Comparison of O_3- and H_2O-based ALD process for three different Sn contents.*

of H_2O as oxidant precursor for ultra scaled gate-dielectrics on Ge and GeSn in order to avoid uncontrolled regrowth of the interlayer during high-κ deposition [144].

In cooperation with the Pennsylvania State University a H_2O-based process, originally developed for Ge was successfully transferred to GeSn as recently reported in Transactions on Electron Devices [37]. Detailed analysis of the the Ge process can be found in the following references [114, 161, 179]. Whereas the original process used an *in-situ* hydrogen plasma clean, for GeSn the *ex-situ* "HF:HCl-last" wet-clean described in CHAPTER 3.1 was found to be optimal for native oxide removal. The following deposition steps were performed at 250 °C to avoid any Sn or Ge diffusion. During immediate *ex-situ* transfer into the ALD-cluster tool organic contamination unavoidably absorbs from the ambient. This thin layer was effectively removed by use of an *in-situ*

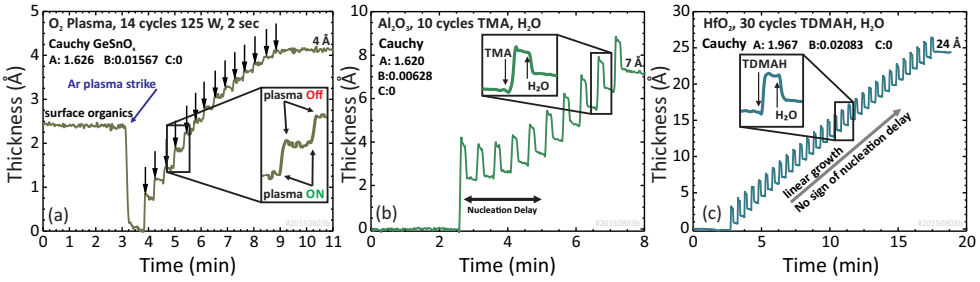


Figure 5.21.: *In-situ ellipsometry monitoring of the growth of (a) $GeSnO_x$, (b) Al_2O_3, (c) HfO_2 on* $Ge_{0.875}Sn_{0.125}$*. The parameters, A,B,C used for fitting with a Cauchy model are also provided. Ellipsometry data recorded by M. Barth and B. Rayner.*

argon plasma-strike of 125 W for 5 s as demonstrated in Fig. 5.21(a). The complete process was monitored by *in-situ* spectroscopic ellipsometry allowing a precise verification of each deposition step [180]. Respective layer thickness were extracted from the ellipsometry data by fitting the observed spectra with a Cauchy model previously calibrated on thick layers. As next step a 4 Å-thick $GeSnO_x$ interlayer was grown in a controlled manner by use of 14-cycles of *in-situ* remote oxygen plasma with 125 W and 2 s each. For the subsequent high-κ layer H_2O was used as oxidant. Prepulsing of 25 cycles H_2O hydroxylates the surface and ensures uniform nucleation of the subsequent Al_2O_3 layer [181] without changing the $GeSnO_x$ thickness. A slight nucleation delay was observed for the first six cycles of the Al-precursor *Trimethylaluminium* (TMA) and H_2O. A detailed reactive force simulation analysis performed by Zheng *et al.* identified a preferred reaction of TMA with oxygen from the GeO_x interlayer denoted as "self-cleaning" effect as origin of this nucleation delay [161]. On the contrary linear growth was observed for the subsequent 2.4 nm-thick HfO_2 high-κ layer deposited in 30-cycles of *Tetrakis(Dimethylamino)Hafnium* (TDMAH) and H_2O. A 20 nm thick Ni metal gate was realized by thermal evaporation through a shadow mask followed by 20 nm Pt as contact pad. The fabrication ended with a FGA at 300 °C for 10 min.

Thanks to the reduced interlayer thickness applying this H_2O process to the same GeSn epilayers as previously used for the O_3-based recipe, yields high accumulation capacitances of $\sim 3\,\mu F/cm^2$ as shown in Fig. 5.20(d-f) corresponding to an EOT of 0.85 nm. At the same time relatively low leakage in the $1 \cdot 10^{-5}$ to $1 \cdot 10^{-4}\,A/cm^2$ range at $V_{FB} - 1\,V$ is maintained. D_{it} remained comparable to the results reported in the previous section. In Fig. 5.22 the two above discussed processes are compared with other literature re-

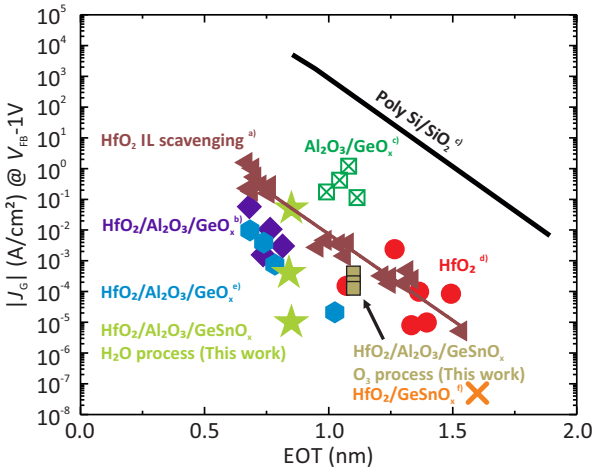


Figure 5.22.: *Gate leakage-vs.-EOT benchmark of GeSn MOSCaps fabricated with the above discussed processes together with literature reports. a) [182], b) [183], c) [112], d) [184], e) [114], f) [124].*

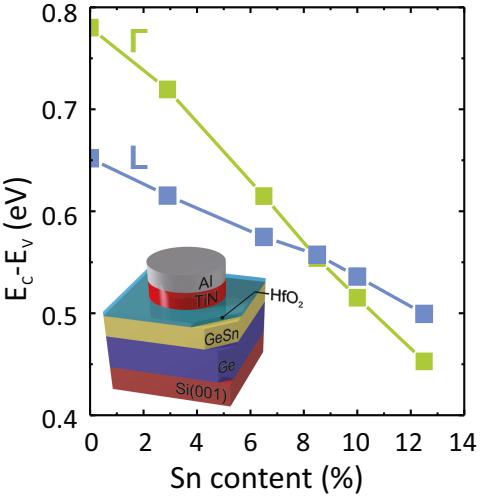
ports on Si, Ge and GeSn demonstrating the advantage of the optimized H_2O process in terms of EOT. This process is well suited for realizing GeSn-based TFETs as will be reported in CHAPTER 7.

5.5. Correlation of Bandgap and CV Characteristics of (Si)GeSn MOS-Structures

As outlined in CHAPTER 2 the (Si)GeSn-system opens unique opportunities in group IV semiconductor band engineering. The Sn/Si-induced changes in the electronic band structure do not exclusively manifest in the optical properties of (Si)GeSn but also in the electrical properties. While the mobility of GeSn is studied in CHAPTER 8, in this section the influence of bandgap and Sn/Si content on CV and GV characteristics in (Si)GeSn MOSCaps is analyzed systematically. A significant part of this work was recently reported in ACS Applied Materials & Interfaces [127].

5.5.1. Minority Carrier Response in (Si)GeSn MOSCaps

In SECTION 5.2 a clear trend of increasing minority carrier response with increasing Sn content was evidenced [*cf.* Fig. 5.14]. For a systematic study of this effect first a series of six binary GeSn samples with increasing Sn content from 0 % to 12.5 % Sn was utilized. The impact of the incorporation of Si towards ternary SiGeSn is studied in the second part of this section.



x_{Sn} (%)	t_{GeSn} (nm)	ϵ_{xx} (%)	E_G (eV)	E_{Cmin} @
0	2500	0.15	0.652	L
2.9	51	−0.3	0.615	L
6.3	265	−0.31	0.575	L
8.5	768	−0.15	0.540	Γ
10	835	−0.27	0.515	Γ
12.5	414	−0.43	0.453	Γ

Figure 5.23 & Table 5.2.: *(left) Bandgap at Γ and L-point vs. Sn content of the analyzed samples, (right) corresponding key material parameters: Sn content x_{Sn}, GeSn epilayer thickness t_{GeSn}, biaxial strain ϵ_{xx}, resulting bandgap E_G and position of the lowest conduction band minimum E_{Cmin}.*

MOSCaps were fabricated following the scheme described in SECTION 5.2. Because the focus of this study was to analyze intrinsic effects of the GeSn-epilayer, rather than realizing an aggressively scaled MOS stack, a relatively thick 6 nm HfO_2 with 5 min O_3 oxidation prior to the high-κ deposition was used to ensure low gate leakage. 60 nm sputtered TiN was used as metal gate. The bandgap of the GeSn epilayers is defined by both Sn content and residual compressive strain which were determined by RBS and XRD reciprocal space mapping, respectively. The corresponding bandgap was then calculated as based on material bowing parameters and $\boldsymbol{k} \cdot \boldsymbol{p}$-theory (at Γ), described in SECTION 2. Starting from GeVS with a bandgap of 0.65 eV[3] the bandgap decreases

[3] As a consequence of the fabrication process the GeVS is slightly tensely strained and thus has a

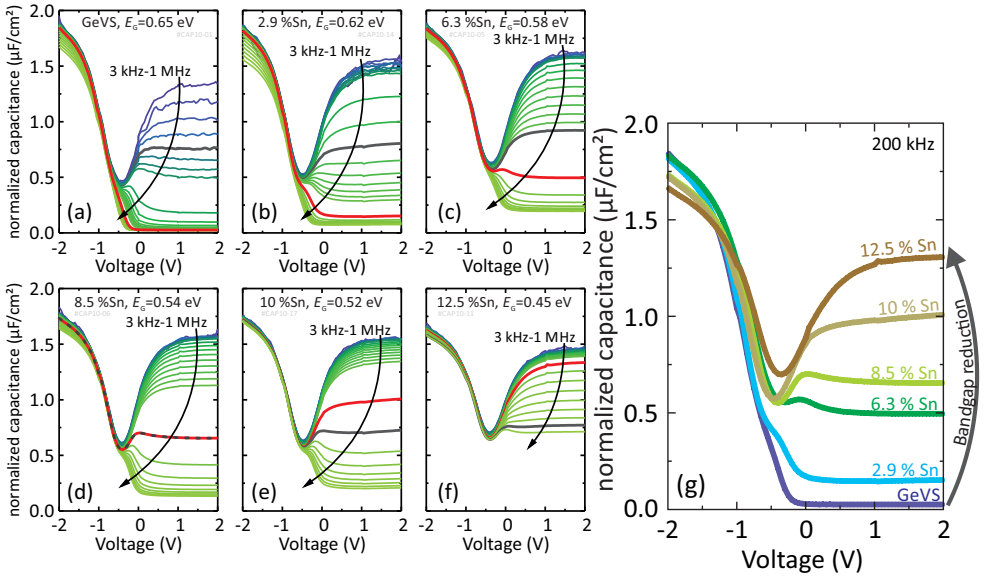


Figure 5.24.: *(a-f) Room temperature CV characteristics of GeSn-based MOSCaps with different Sn contents.* 200 kHz *curve red,* f_t *curve black. (g) Corresponding* 200 kHz *curves merged in one plot.*

down to 0.45 eV for partially relaxed $Ge_{0.875}Sn_{0.125}$. The first three samples are indirect semiconductors whereas the latter three feature their lowest conduction band minimum at the Γ-point and thus are direct bandgap semiconductors. Table 5.2 summarizes the key material parameters of the analyzed samples. The bandgaps at Γ and L-point are depicted in Fig. 5.23 *vs.* Sn content. All samples are undoped with an unintentional acceptor concentration that increases with Sn content. It is in the low 10^{16} 1/cm^3 range for GeVS and in the mid 10^{17} 1/cm^3 for high Sn content GeSn (*cf.* CHAPTER 8.3).
The room temperature CV characteristics of these MOSCaps are shown in Fig. 5.24(a-f). A lucid trend of increasing inversion response with increasing Sn content is visible. That is, with increasing Sn content strong inversion occurs already at lower frequencies. This trend can be visualized clearly when picking a certain frequency (here 200 kHz, red line) and plotting the corresponding CV curves of all six Sn contents together as in Fig. 5.24(g). As a quantitative measure of the inversion response the transition frequency f_t is defined. f_t denotes the frequency at which the capacitance is midway between low

marginally reduced bandgap compared to bulk Ge

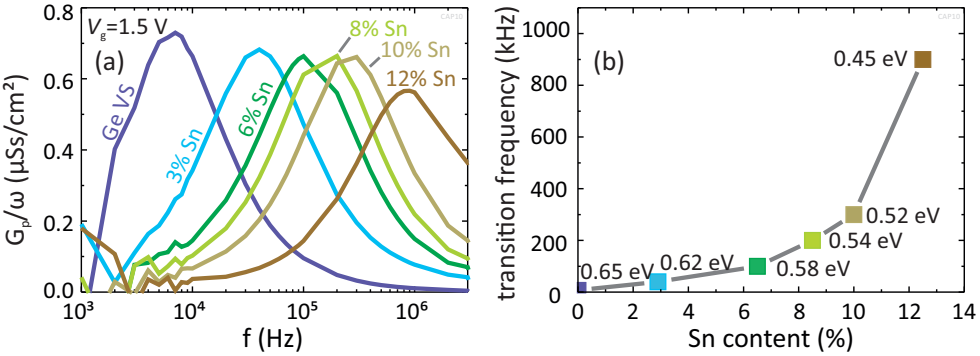


Figure 5.25.: *(a) Parallel conductance divided by angular frequency vs. frequency when biased in strong inversion. The peak yields f_t and is plotted in (b) vs. Sn content showing a superlinear increase with Sn content. The corresponding bandgaps are indicated next to the data points.*

frequency inversion capacitance C_{LF} and high frequency inversion capacitance C_{HF} *i.e.* $C_{f_t} = 0.5(C_{LF} + C_{HF})$. It was shown that when biased in strong inversion (here +1.5 V) the parallel conductance G_P/ω plotted *vs.* modulation frequency f features a local maximum at f_t [128,173]. Such a plot provides an easy and accurate method for determining the transition frequency and is shown in Fig. 5.25(a). For increased Sn content a clear shift of the f_t peak towards higher frequency is visible. In Fig. 5.25(b) the extracted transition frequency is plotted against Sn content and demonstrates an exponential increase with Sn content in accordance with the expected bandgap dependence of the minority carrier response time since $f_t \propto 1/\tau_R \propto \exp(-E_G/k_BT)$ described in SECTION 5.1.1. In Fig. 5.24(a-f) the CV curves measured at f_t are printed in black.

As further analysis the following three points are addressed in more detail: (i) A clear correlation of Sn-induced bandgap shrinkage and enhanced minority carrier response is self-evident. However, it should be ruled out that secondary effects as for example a possible Sn-induced increase of material or interface defects lead to the observed increase of f_t with Sn content. (ii) Are the minority carriers giving rise to the enhanced inversion response generated within the inversion layer by *Shockley-Read-Hall* (SRH) or by diffusion from the bulk? (iii) To what extend does it play a role whether the GeSn epilayer is a direct or an indirect semiconductor?

The first point (i) is addressed by means of ternary SiGeSn MOSCaps in the following section. (i) and (iii) are supported by physics-based simulations treated in SECTION

5.5.2. (ii) is answered by an analysis of the temperature dependence of the parallel conductance in SECTION 5.6.

Impact of Si-incorporation in ternary SiGeSn MOSCaps

In binary GeSn, Sn content and bandgap are inherently coupled. The bandgap decreases with Sn content. On the contrary the incorporation of Si towards ternary SiGeSn has the opposite effect on the band structure and leads to an increase of the bandgap [185]. This allows to decouple Sn content and bandgap. That way for example two epilayers can be realized with the same bandgap but with different Sn content. In case of the higher Sn content sample a certain amount of Si needs to be incorporated to compensate the Sn-induced bandgap shrinkage. The comparative study of such alloys permits to unlink effects arising from the change in bandgap from those arising from changes in material quality for example due to defects induced by growth challenges of high Sn content alloys.

For this purpose a series of five (Si)GeSn MOSCaps with different Si/Sn ratios was analyzed keeping either Si or Sn content constant while changing the other. In this case Pt evaporated through a shadow mask was used as metal gate on 5 nm HfO_2. The multifrequency CV characteristics of these MOSCaps are shown in Fig. 5.26. The three horizontally arranged data sets present the influence of Sn incorporation on SiGeSn MOSCaps, while the Si content is kept constant. As already demonstrated for binary GeSn the minority carrier CV-response (positive biases) increases with Sn content along with the bandgap reduction. On the contrary increasing the Si content suppresses the minority carrier response as seen in the vertically arranged curves. This is in line with the expected bandap increase for the incorporation of Si [185]. Fig. 5.27(a,c) illustrate both effects by plotting the 500 kHz curves of each series in one plot. A quantitative comparison is provided by means of the transition frequency in Fig. 5.27(b,d) underlining the observed qualitative trends.

That is, bandgap changes are suspected to be the factor dominating the observed minority response, rather than possible changes in material quality. In order to substantiate this hypothesis, it is interesting to compare the inversion response of SiGeSn ternaries with those of Ge(Sn)-layers, especially for samples that differ in Sn content but have approximately the same bandgap. Incorporating 6.3 % of Sn into Ge increases the transition frequency from 7 kHz for GeVS to 100 kHz for $Ge_{0.937}Sn_{0.063}$ along with a bandgap

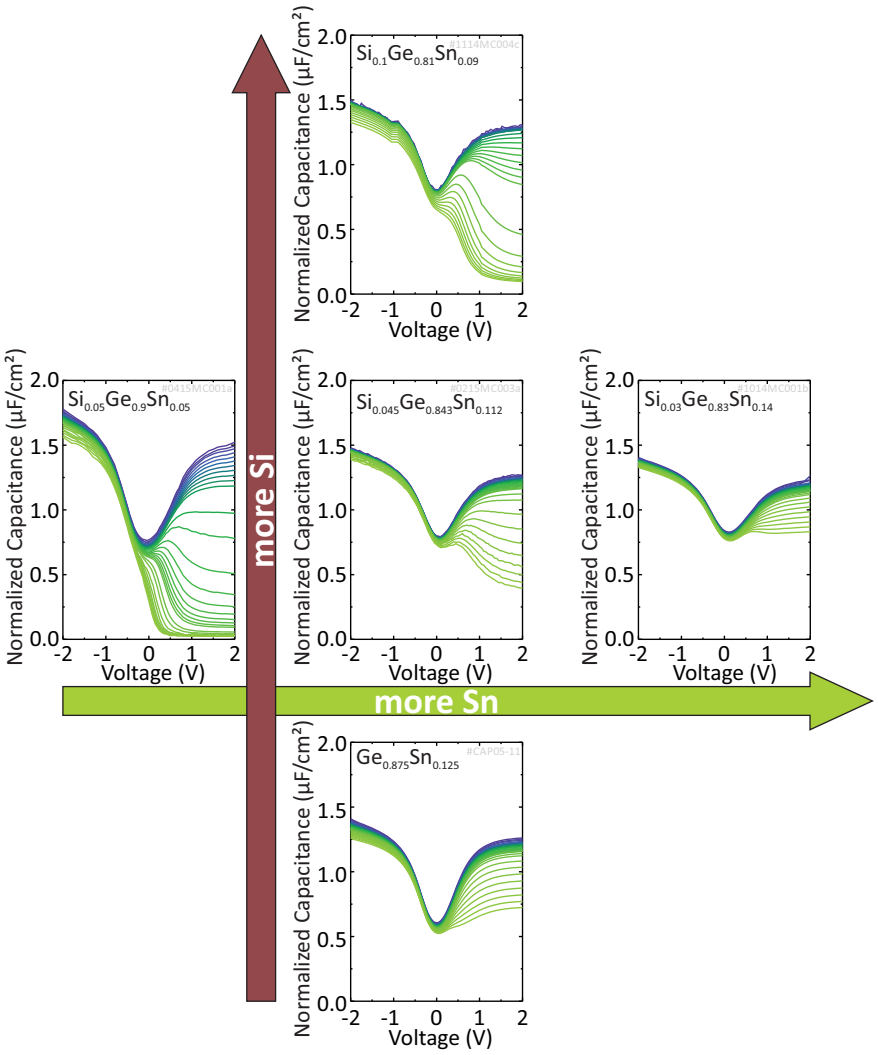


Figure 5.26.: *Room temperature multifrequency CV characteristics of (Si)GeSn MOSCaps demonstrating the the influence of Sn and Si incorporation on the minority carrier response.*

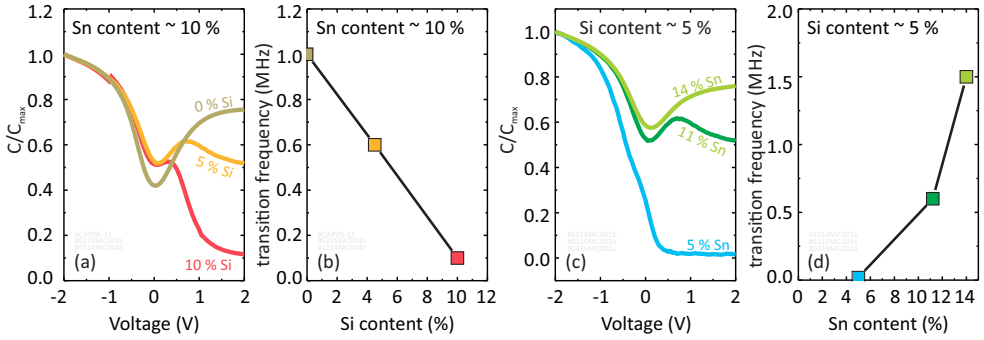


Figure 5.27.: *(a,c)* 500 kHz *characteristics demonstrating the suppressed (a) (increased) (c) minority carrier response for increased Si (Sn) content. (b,d) corresponding transition frequencies vs. Si (Sn) content.*

decrease from 0.65 eV to 0.58 eV (see Fig. 5.24). If now additionally a similar amount of Si is incorporated one restores the bandgap of GeVS, which is approximately the case for $Si_{0.05}Ge_{0.9}Sn_{0.05}$ that has a calculated bandgap of 0.64 eV. Also the measured transition frequencies match quite well (7 kHz for GeVS and 9 kHz for $Si_{0.05}Ge_{0.9}Sn_{0.05}$). If the incorporation of Sn and Si would have induced significant amounts of defects that serve as minority generation centers one would expect similar high transition frequencies for $Si_{0.05}Ge_{0.9}Sn_{0.05}$ and for $Ge_{0.937}Sn_{0.063}$. This observation also holds for other combinations of GeSn binaries and SiGeSn-ternaries that have comparable calculated bandgaps. For example the bandgap of $Si_{0.05}Ge_{0.84}Sn_{0.11}$ matches the one of $Ge_{0.915}Sn_{0.085}$ with 0.54 eV. The measured transition frequencies, 500 kHz and 200 kHz respectively are in reasonable agreement.

Another possible source, the contribution from interface traps due to changes in the high-κ interface quality with Sn content can be ruled out since the interaction with interface traps is generally low in strong inversion [128, 153]. Furthermore no D_{it}-increase was observed when going to higher Sn contents.

This leads to the conclusion that the bandgap has the strongest influence on the minority carrier response whereas changes in interface or material quality play a secondary role.

5.5.2. Numerical simulations for minority carrier generation analysis

Numerical simulations of MOSCap CV characteristics offer the unique possibility to independently study the influence of bandgap width, bandgap type (indirect/direct),

minority carrier generation time constant and doping on the inversion response and thereby allow to substantiate the experimental observations. The device characteristics were obtained with the simulation tool TCAD Sentaurus Device that enables simulations of electronic device properties based on physical models[4]. Material input parameters describing the GeSn band structure of the sample series used in SECTION 5.5.1 were calculated based on the experimentally determined Sn content and strain values listed in table 5.2 using the methods described in CHAPTER 2. Parameters calculated in this way are band energies, bandgaps, effective masses and nonparabolicity coefficients. The permittivity was linearly interpolated between Ge, $\varepsilon_{\mathrm{Ge}} = 16.2$ [186] and Sn, $\varepsilon_{\alpha-\mathrm{Sn}} = 24$ [187]. In GeSn the two relevant conduction band minima Γ- and L-valley are energetically very close. As a consequence a multivalley bandstructure model needs to be used since also the second lowest conduction band minimum can have significant influence on the electrical properties (*cf.* CHAPTER 2.1). In order to focus on the influence of bandstructure on the CV characteristics no interface traps were assumed to be present in the devices. Since we are mainly interested in the CV characteristics in inversion this presumption is justified because interaction with interface traps is low in strong inversion [128, 153]. In the next SECTION 5.6 temperature-dependent conductance measurement will show that diffusion of carriers which are SRH generated in the bulk is the dominant mechanism for minority carrier generation in these low bandgap samples in the analyzed temperature range. SRH generation/recombination is included in the simulation by assuming trap levels residing in the middle of the GeSn bandgap. If not otherwise specified the SRH time constant is set to $\tau_{\mathrm{n}} = 500\,\mathrm{ps}$ in the range reported by Wirths and Geiger *et al.* [15]. In the analyzed MOSCaps the drift/diffusion parameters were set to those of Ge bulk for simplicity. Quantization is included in the simulations. EOT was set to 1.5 nm.

The simulated CV characteristics at 200 kHz are depicted in Fig. 5.28(a) for different Sn contents. The qualitative agreement with the experimental data from Fig. 5.24(g) is evident, while it should be noted that the intent of these simulations is to study the physical parameters influencing the inversion response rather than precisely reproducing the experimental data. Such a quantitative analysis though is possible and allows the extraction of material parameters as the minority carrier lifetime which has significant importance for optical applications and was reported by Monaghan *et al.* [173] for

[4]I gratefully acknowledge Keyvan Narimani for support with the TCAD simulations.

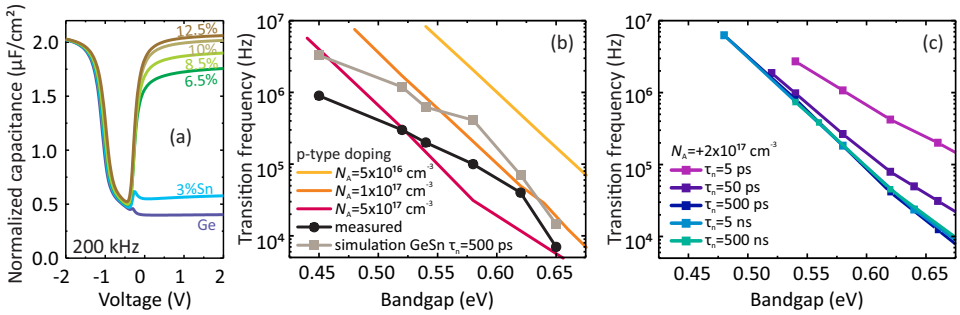


Figure 5.28.: *(a) Simulated CV characteristics. (b,c) Transition frequency vs. bandgap width: (b) as measured (black), calculated for GeSn bandstructure (grey) and calculated for Ge-bandstructure as a function of bandgap for three different doping levels (orange shaded); (c) as (b) but with constant doping and SRH constant τ_n as parameter.*

InGaAs.

In the following, the impact of doping, bandgap, band structure and SRH constant on SRH dominated minority carrier response is studied where the transition frequency serves as a measure of the inversion response. First in order to demonstrate a "pure bandgap trend" the transition frequency is calculated for Ge MOSCaps where the bandgap is artificially varied in the range 0.45 eV to 0.7 eV while the other band structure parameter (effective mass, Γ-L-offset *etc.*) are kept constant. Such curves for a fixed minority carrier lifetime $\tau_n = 500\,\text{ps}$ and three different p-type doping levels N_A are plotted as orange-shaded curves in Fig. 5.28(b) against the bandgap. The dependence expected from an approximation provided by Nicollian and Brews is

$$f_t = \frac{C_D}{2\pi(C_{Ox}+C_D)} \cdot \frac{1}{\tau_R} \propto \frac{\mathcal{M}_c\mathcal{M}_v}{N_A\tau_n} \exp(-E_G/2k_BT)\ , \tag{5.21}$$

with $\tau_R \propto \tau_n N_A/n_i \propto \tau_n N_A/[\mathcal{M}_c\mathcal{M}_v \exp(E_G/2k_BT)]$ and reflects in the simulated curves for different doping N_A. The transition frequency decreases exponentially with the bandgap and linearly with the doping concentration such that changes in N_A lead to a set of parallel lines in the f_t-*vs.*-E_G plot in Fig. 5.28(b). However, it is noticeable that the experimental curve does not strictly obey the $\exp(E_G/k_BT)$ dependence but is flattened out slightly. The background doping concentration of GeSn in the experiment increases with Sn content from the low $10^{16}\,1/\text{cm}^3$ range up to low $10^{17}\,1/\text{cm}^3$ range for

12.5 % Sn (*cf.* CHATPER 8.3). Thus, one could suspect the doping changes as origin of the flattening out of the experimental f_t-*vs.*-E_G plot in compliance with equation 5.21 and Fig. 5.28(b). What is striking though and opposes this hypothesis is the simulated (gray) curve. Here a fixed doping of $2 \cdot 10^{17}\,1/\mathrm{cm}^3$ and $\tau_n = 500\,\mathrm{ps}$ was used together with the calculated band structure parameters corresponding to the experimental sample series with varying Sn content. Despite the fixed doping, also here the f_t-*vs.*-E_G curve is flattened out compared to the "pure bandgap trend". What has to be taken into account is that with increasing Sn content not only the bandgap decreases also the band structure changes. The effective masses decrease with Sn content as described in SECTION 2.1 and the alloy undergoes a transition from an indirect to a direct semiconductor. Thanks to the significantly smaller effective mass of the Γ-valley compared to the L-valley also the conduction band DOS $\mathcal{M}_c$ for the direct bandgap case is reduced. The changes in the slope of the f_t-*vs.*-E_G plot can thus be attributed to changes in the conduction band DOS which is in line with the approximation provided in equation 5.21. This can be seen more clearly in Fig. 5.29. Here the blue curve shows the f_t-*vs.*-E_G plot for a Ge-like band structure where in case of the green curve the Γ- and L-energies are swapped resulting in artificially direct Ge. While the bandgap changes the Γ-L offsets and effective masses are kept constant. Both curves follow roughly the exponential bandgap dependence but in case of the artificially direct Ge, f_t is shifted to lower values as a consequence of the smaller Γ-valley DOS. The experimental curve (black) lies within these extremes while the samples undergo the transition from an indirect to a direct semiconductor within the analyzed Sn content range. It should be noted though, that in this scenario for a fixed τ_n and SRH generation of carriers, momentum conservation does not apply and thus the fact if the sample has a direct bandgap or an indirect bandgap does only play a role in terms of DOS.

The last dependence of f_t that needs to be studied, is the one on the minority carrier life time. τ_n inversely depends on the defect density in the alloy and thus is a clear indicator of material quality and possible contamination. The f_t-*vs.*-E_G plot for a Ge band structure with τ_n as a parameter is depicted in Fig. 5.28(c) and shows that f_t increases with decreasing τ_n as qualitatively expected from equation 5.21. However, the dependence of f_t on τ_n is weaker that on E_G when varying τ_n within the experimentally meaningful range. That means even changes in τ_n of several orders of magnitude, corresponding to an enormous increase of the defect density when going to higher Sn contents could not

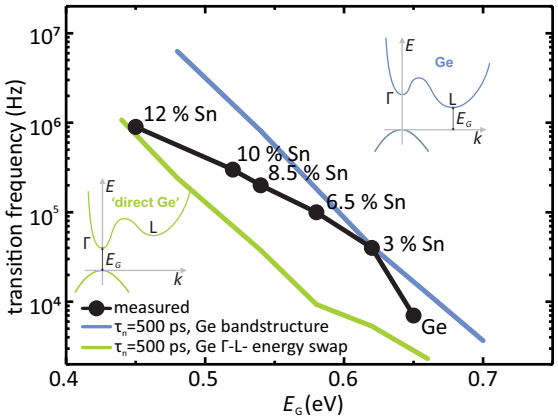


Figure 5.29.: *Transition frequency vs. bandgap as obtained experimentally for GeSn with varying Sn content and as simulated for Ge and artificially direct Ge with swapped* Γ *and L-valley energy.*

explain the experimentally observed increase of f_t.

To summarize the influence of the parameters bandgap E_G, doping N, SRH time constant τ_n and band structure (indirect/direct): In compliance of experiment and simulations one can conclude that the enhanced inversion response in GeSn is essentially dominated by the Sn-induced bandgap shrinkage albeit changes in doping, material quality and band structure still can play a secondary role.

5.6. Temperature Dependence and Deep Defect analysis

As indicated in SECTION 5.2, Fig. 5.10(b) the strong inversion response in (Si)GeSn-based MOSCaps underlies a significant temperature dependence and can be effectively suppressed by reducing the sample temperature whereas the accumulation behavior remains largely unaffected. An analysis of the temperature dependence of the corresponding parallel conductance in inversion allows to identify the physical mechanism behind this enhanced minority carrier response. It will be shown that in this case the prevailing process in inversion is diffusion of carriers that are generated in the bulk, to the semiconductor/high-κ-interface. The temperature analysis allows the extraction of deep defect levels that are the dominant centers for minority generation. Thereby this methodology provides unique opportunities to study intrinsic defect levels within the

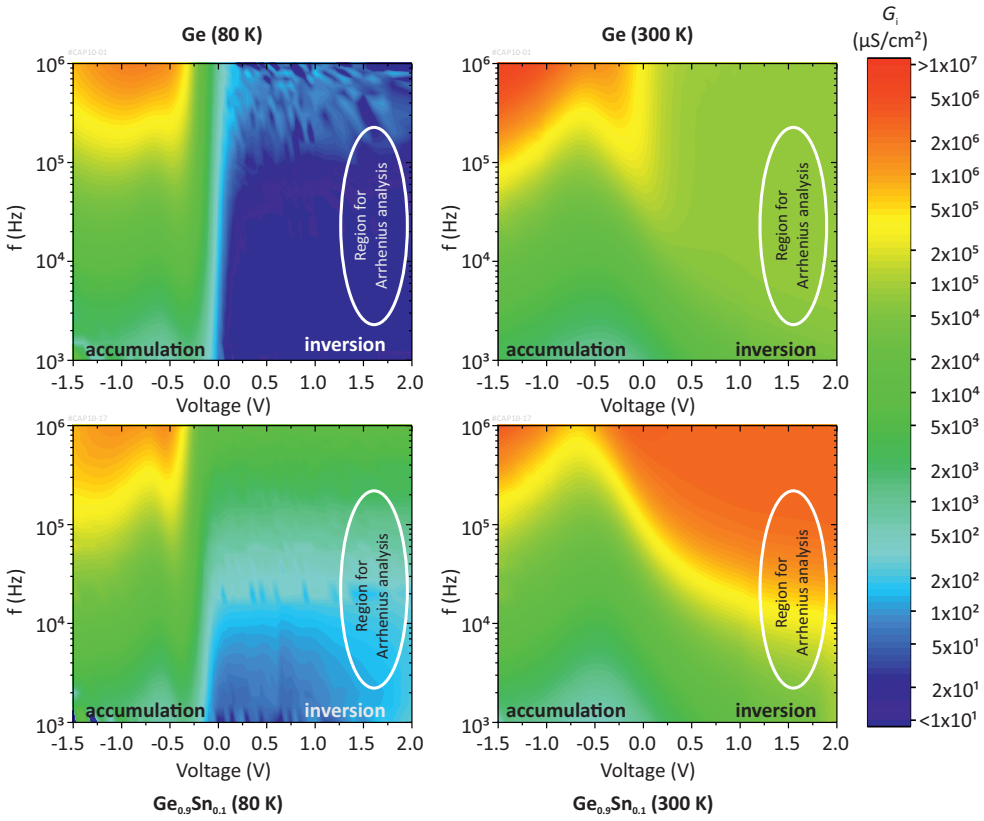


Figure 5.30.: *Minority carrier conductance G_i map as a function of gate bias and AC-frequency for GeVS and* $Ge_{0.9}Sn_{0.1}$ *at* 80 K *and* 300 K. *G_i shows strong temperature dependence in inversion allowing an Arrhenius analysis as demonstrated in Fig. 5.31.*

GeSn epilayer complementing other deep level characterization techniques such as *Deep Level Transient Spectroscopy* (DLTS). Few data on DLTS characterization of GeSn was provided by Gupta *et al.* [120, 188] and by Takeuchi *et al.* [121].

The CV characteristics of a MOSCap in inversion can be approximated with the equivalent circuit depicted in Fig. 5.31(b). In this circuit minority carrier response is modeled by a parallel conductance G_i that is parallel to the depletion capacitance C_D [128]. Minority carrier response can have contributions from generation/recombination G_{gr} within the inversion layer at the high-κ/semiconductor interface and from diffusion G_d

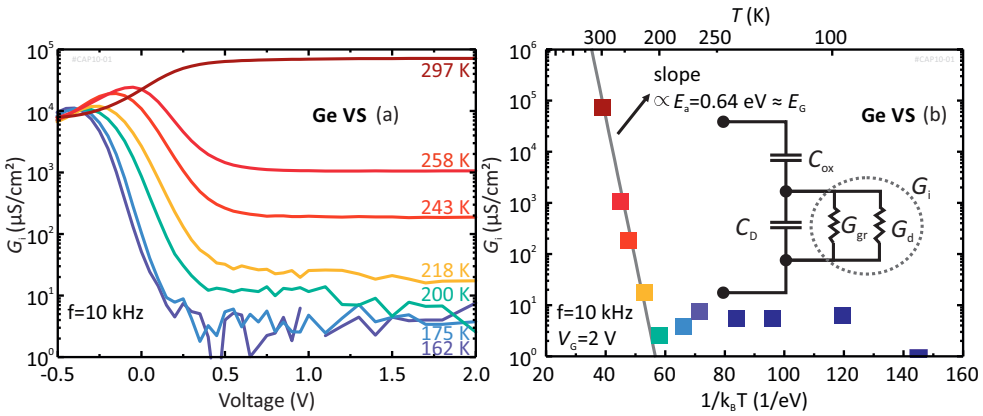


Figure 5.31.: *(a) G_i vs. V_G in inversion for a set of temperatures, (b) G_i is extracted from (a) at 2 V and plotted vs. inverse temperature for activation energy extraction. The inset depicts the equivalent circuit.*

of minority carriers generated within the quasi neutral bulk. That is, $G_\mathrm{i} = G_\mathrm{gr} + G_\mathrm{d}$. G_i can be calculated from the measured capacitance $C_\mathrm{meas.}$ and parallel conductance $G_\mathrm{meas.}$ [128]:

$$G_\mathrm{i} = \frac{\omega^2 C_\mathrm{ox}\tau_0(1+\omega^2\tau_m^2)}{\omega^2\tau_0^2 + [\omega^2\tau_m(\tau_0-\tau_m)-1]^2}\,, \tag{5.22}$$

with $\tau_m = C_\mathrm{meas.}/G_\mathrm{meas.}$ and $\tau_0 = C_\mathrm{Ox}/G_\mathrm{meas.}$. That way 2D conductance maps of G_i *vs.* V_G and f are generated as shown in Fig. 5.30 for Ge and $Ge_{0.9}Sn_{0.1}$ at 80 K and 300 K. It is evident that a reduction of the temperature strongly suppresses G_i in inversion where the conductance in accumulation changes insignificantly. The temperature dependence of G_i in inversion will now be used to identify the dominant minority carrier response mechanism SRH or diffusion. G_i *vs.* V_G is plotted in Fig. 5.31(a) for a set of temperatures. In strong inversion G_i only slightly depends on V_G but decreases continuously with temperature. In an Arrhenius plot G_i extracted from this bias regime ≥ 1.5 V is plotted semilogarithmically against $1/k_\mathrm{B}T$ in Fig. 5.31(b). A fit in the linear region yields characteristic activation energies E_a for minority carrier response and reveals the dominant mechanism. If $E_\mathrm{a} \approx E_\mathrm{G}$ the minority carrier inversion response is governed by diffusion of minority carriers generated in the bulk, whereas for $E_\mathrm{a} \leq E_\mathrm{G}/2$ generation/recombination *via* deep levels within the inversion layer prevails [128]. For GeVS $E_\mathrm{a} = 0.64\,\mathrm{eV} \approx E_\mathrm{G}/2$ was extracted and thereby identifies diffusion of minority carriers

x_{Sn} (%)	ϵ_{xx} (%)	E_a (eV)	E_G (eV)
0	0.15	0.64	0.652
2.9	−0.3	0.39	0.615
6.3	−0.31	0.32	0.575
8.5	−0.15	0.41	0.540
10	−0.27	0.41	0.515
12.5	−0.43	0.25	0.453

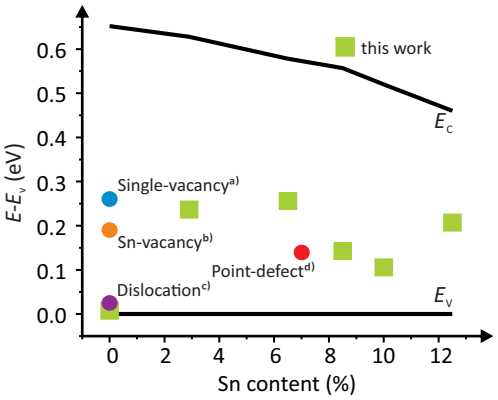


Table 5.3 & Figure 5.32.: *Activation energies extracted from Arrhenius analysis of the minority carrier response. The position of the trap levels within the bandgap is also displayed (right) together with defect levels from literature. a) [189], b) [190], c) [191], d) [188].*

generated in the bulk as origin of the minority carrier response at room temperature and below as also observed by Martens *et al.* for Ge [137]. This analysis was conducted for the GeSn sample series from Table 5.2 and Fig. 5.24, respectively. The extracted activation energies, depicted in Table 5.3 are $> E_G/2$ and also here diffusion of carrier from the bulk into the inversion layer is the source of minority carrier response. In these intrinsically *p*-type epilayers electrons are minority carriers. Hence E_a is measured relative to the conduction band. The trap position in the bandgap $E_t = E_c - E_a$, referenced to the valence band E_v is shown in Fig. 5.32. This depiction reveals that, whereas the incorporation of Sn leads to a conduction band downshift the extracted defect levels E_t reside in the lower half of the bandgap. As a consequence one can explain the enhanced minority carrier inversion response for higher Sn contents by the Sn-induced downshift of the conduction band with respect to the trap levels that allows easier carrier generation. Comparison with defect levels reported in literature provides good agreement with point defects [188] and specifically vacancies [189, 190]. In case of GeVS the inversion response stems from generation *via* dislocations in the bulk.

5.7. Summary

A comprehensive analysis of (Si)GeSn-based MOSCaps was presented. After reviewing the state of the art in Ge MOS technology peculiarities in fabrication and analysis of MOS stacks on Sn-based low bandgap alloys were discussed. Process and methodology were adopted for GeSn accordingly, taking into account the reduced thermal budget and optimized surface cleaning for MOS fabrication. It turned out that SiGeSn showed higher thermal stability compared to binary GeSn. For electrical analysis peculiarities arising from the reduced bandgap, especially the enhanced interaction with minority carriers were discussed and accounted for. D_{it} analysis revealed reasonable interface trap densities in the $10^{12}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ range independent of the Sn content. High accumulation capacitances of $\sim 3\,\mu\mathrm{F/cm}^2$ corresponding to an EOT of 0.85 nm were achieved applying an optimized H_2O-based ALD process.

CV characteristics of GeSn MOSCaps are governed by a strong minority carrier response in inversion. The comparative analysis of binary GeSn and ternary SiGeSn MOSCaps allowed to decouple effects originating from changes in Sn content from those arising from changes in the bandgap width. Detailed analysis of the conductance's temperature dependence identified diffusion of carriers generated in the bulk as dominant mechanism for minority carrier response which is promoted by the small bandgap. A clear correlation between the Sn-induced bandgap shrinkage and enhanced minority carrier response was proofed by a comprehensive analysis of GeSn MOSCaps and underlined by TCAD device simulations.

The dominant deep defect level for minority carrier generation lies in the lower half of the bandgap and could be attributed to point defects.

6 | GeSn p-i-n Diodes

The *p-i-n* diode represents an important building block for both electronic and optoelectronic applications. Depending on its design in optoelectronics it can be utilized as *Light Emitting Diode* (LED) or as detector with its common application in CMOS image sensors. In electronics it is mainly used as high-frequency oscillator and amplifier. A reverse biased, gated *p-i-n* diode is the essential element of a TFET and thereby gains increasing interest for ultra low power applications.
For high doping levels in the *p*- and *n*-regions, the reverse and low forward bias characteristics of a *p-i-n* diode are dominated by quantum mechanical *Band-to-Band Tunneling* (BTBT) rather than by diffusion/thermal emission. In this case they are denoted as tunnel diodes or Esaki diodes and thereby provide a powerful tool for the analysis of BTBT and the calibration of the respective models [192, 193]. GeSn is especially interesting for integration in tunnel diodes since BTBT increases for reduced bandgap, smaller effective mass and is promoted by the direct bandgap since no phonon inter-

action is required. All these requirements can be fulfilled by GeSn and have led to an increasing interest in GeSn for TFETs including first experimental results [34–37, 126]. Ungated GeSn tunnel diodes though were rarely studied before. The main contribution was made within the scope of this work [194].
The direct bandgap properties qualify GeSn also as material for LEDs enabling efficient light emission in a group IV alloy that is commonly known only from III-V materials. Especially since the experimental demonstration of optically pumped lasing in GeSn [15,65] the quest for improving this Si-compatible light source gained significant interest and lead to several studies on GeSn [18,20,195–198] LEDs and even SiGeSn/GeSn Multi Quantum Well (MQW) LEDs [19].
In this chapter the fabrication and characterization of GeSn *p-i-n* diodes is reported first as tunnel diode and second as LED. Emphasis is placed on the analysis of BTBT for the integration in Tunnel FETs by using temperature-dependent IV measurements in conjunction with numerical simulations. The successful integration in a TFET is demonstrated in the next CHAPTER 7. Parts of the results were presented in Applied Physics Letters [194] in Transactions on Electron Devices [37] and on the International Electron Device Meeting (IEDM) 2016 [126].

6.1. The Esaki Diode

The Esaki or tunnel diode is named after Leo Esaki who in 1958 for the first time observed the characteristic *Negative Differential Resistance* (NDR) as a sign of BTBT in Ge *p-n* junctions. It consists of a *p-n* or *p-i-n* structure where the key is that at least one of the doped regions is degenerate. As a consequence, the conduction band of the *n*-region lies below the valence band on the *p*-side as sketched in the lower panel of Fig. 6.1(a) and thereby enables the possibility of BTBT within the overlap window. To be precise, once a bias is applied BTBT occurs provided that (i) the tunnel barrier is thin enough and (ii) occupied states on the side from which the carriers are tunneling match energetically with unoccupied, allowed states on the side where they tunnel to [*cf.* Fig. 6.1].
When a reverse bias is applied $V_\mathrm{d} < 0\,\mathrm{V}$ the band overlap increases further and electrons tunnel from the valence band on the *p*-side across the junction into empty states in the conduction band on the *n*-side resulting in a significant reverse current [Fig. 6.1(b)]. This discriminates a tunnel diode from a regular *p-n* diode that ideally blocks current

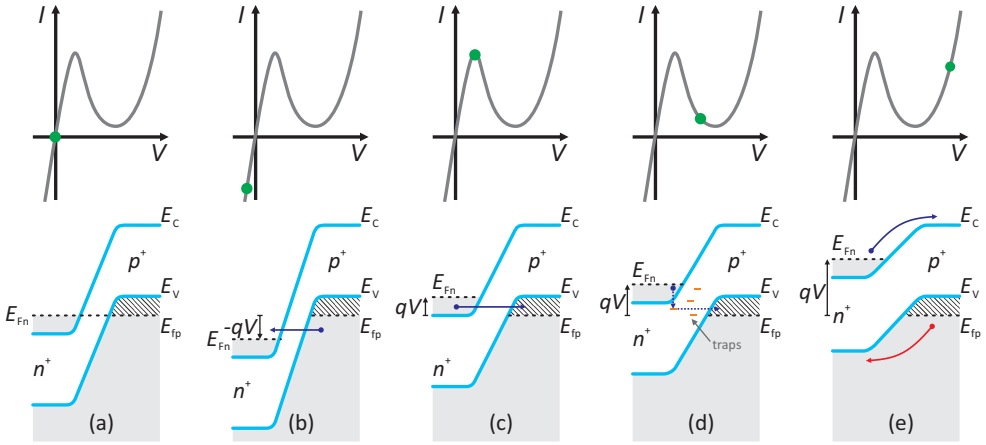


Figure 6.1.: *Band diagrams (lower panel) and corresponding schematic IV characteristics (upper panel) of a tunnel diode in different bias regimes: (a) idle, $V_\mathrm{d} = 0\,\mathrm{V}$; (b) reverse bias $V_\mathrm{d} < 0\,\mathrm{V}$ BTBT dominated; (c) slight forward bias $V_\mathrm{d} = V_\mathrm{peak}$, BTBT dominated, (d) NDR regime $V_\mathrm{d} = V_\mathrm{valley} > V_\mathrm{peak}$, TAT dominated; (e) excess current regime $V_\mathrm{d} > V_\mathrm{valley}$, diffusion/thermal emission dominated. Adapted from [199].*

flow in this bias regime. A forward bias pulls up the bands on the n-side. As long as the band overlap and thereby the tunneling window is maintained, BTBT prevails by electrons that tunnel from the conduction band on the n-side to empty-states (holes) in the valence band on the p-side, and the current increases with increasing bias. The BTBT current peaks once the bands are aligned such that electron distribution on the n-side and hole distribution on the p-side are energetically matched Fig. 6.1(c) $V_\mathrm{d} = V_\mathrm{peak}$. Increasing the bias further from this point mismatches the carrier distributions and finally closes the tunneling window once the conduction band edge on the n-side moves above the valence band edge on the p-side. As a consequence in this bias regime the current decreases with increasing bias leading to a negative slope of the IV curve denoted as NDR [Fig. 6.1(d)]. Even though the diode is biased slightly in forward direction the diffusion/thermal emission current is so small in this regime that in an idealized case the current could drop by several orders of magnitude and reach a local minimum at $V_\mathrm{d} = V_\mathrm{valley}$. However, parasitic effects create an excess current that lifts up the valley current and thereby degrades *Peak-to-Valley Current Ratio* (PVCR). By biasing the diode even further positively the p-n junction becomes sufficiently flat that carriers can be thermally excited above the junction. The diode reaches the on-state and the current

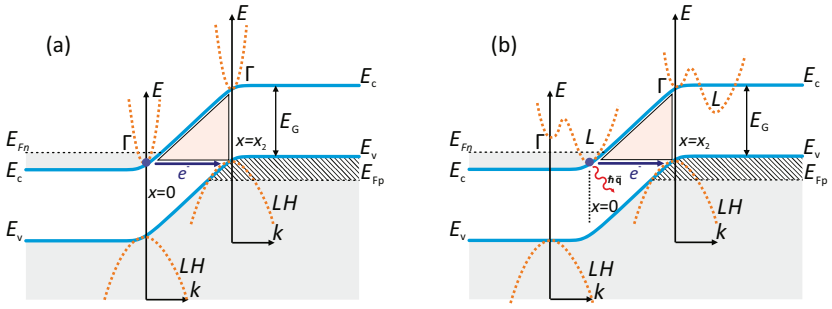


Figure 6.2.: *Band diagram for (a) direct and (b) indirect tunneling with indicated triangular potential barrier approximation. For indirect tunneling the electron has to emit a phonon $\hbar\boldsymbol{q}$ to conserve momentum.*

increases exponentially as also known from a regular p-n diode [Fig. 6.1(e)].
The three contributions to the total current *band-to-band tunneling*, *excess current* and *thermal current* shall now be further elucidated.

6.1.1. Band-to-Band Tunneling

A common approach for the calculation of the band-to-band tunneling current is Kane's *local tunneling model* with the *constant and uniform field approximation* [200]. To describe the electric transport one separates energy E and momentum $\boldsymbol{k}$ in the contributions parallel $\parallel$ (x-direction) and perpendicular $\perp$ to the transport direction.
The *Landauer-Büttiker* formalism yields the current density by solving the following expression [201]

$$J_{\mathrm{BTBT}} = \int\int qT_{\mathrm{BTBT}}[f_{\mathrm{v}} - f_{\mathrm{c}}]v_{\mathrm{G}}(k_{\parallel})\mathcal{M}_{\parallel}(k_{\parallel})\mathcal{M}_{\perp}(k_{\perp})\mathrm{d}k_{\parallel}2\pi k_{\perp}\mathrm{d}k_{\perp}\,, \tag{6.1}$$

where T_{BTBT} is the tunneling probability, f_{v} and f_{c} are the Fermi distribution in valence and conduction band on p- and n-side of the junction, respectively, v_{G} is the group velocity and $\mathcal{M}_{\parallel}$ and $\mathcal{M}_{\perp}$ are the respective density of states for parallel and perpendicular direction. Note that $T_{\mathrm{BTBT}}(E)$ and $f_{\mathrm{v}}(E)$, $f_{\mathrm{c}}(E)$ *via* the dispersion relation $E(\boldsymbol{k})$ implicitly also depend on the momentum.
To calculate T_{BTBT} one approximates the band diagram of the p-n junction to be of triangular shape (Fig. 6.2). As the electric field is the gradient of the potential $\boldsymbol{\mathcal{E}} = \nabla\Phi$ the constant and uniform field approximation implies that the potential Φ only varies

slowly along the tunneling direction allowing the application of the *Wentzel-Kramers-Brilloin* (WKB) approximation $T_{\mathrm{BTBT}} \approx \exp(-2\int_0^{x_2} |k_\parallel(x)|\mathrm{d}x)$. Plugging this in equation 6.1 with the simplification of an arbitrary steep Fermi distribution ($f_\mathrm{v} - f_\mathrm{c} \approx 1$) and neglecting the transverse component $\perp$ yields for direct tunneling in reverse bias condition[1]

$$J_{\mathrm{BTBT}} = \mathcal{A} V_\mathrm{R} \mathcal{E} \exp\left(\frac{-\mathcal{B}}{\mathcal{E}}\right) \quad \text{with} \tag{6.2}$$

$$\mathcal{A} = \frac{q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_\mathrm{T}^*}{E_\mathrm{G}}} \quad \text{and} \quad \mathcal{B} = \frac{4\sqrt{2m_\mathrm{T}^*}E_\mathrm{G}^{3/2}}{3q\hbar} \,. \tag{6.3}$$

V_R is the effective reverse bias and is a function of the externally applied drain bias V_D. $\mathcal{E}$ is the electric field in the junction. m_T^* is the reduced tunneling mass which in this case is the reciprocal sum of electron and hole effective mass $m_\mathrm{T}^* = [1/m_\mathrm{e}^* + 1/m_\mathrm{h}^*]^{-1}$. Note that $\mathcal{E}$ depends essentially on the band profile at the tunneling junction which in turn is defined by both doping and V_D. Thus $\mathcal{E}(V_\mathrm{D} = 0) \neq 0$ due to the built in potential in the *p-n* junction.

A schematic band diagram illustrating the BTBT process is shown in Fig. 6.2 including the indicated triangular potential well. For *direct* tunneling [Fig. 6.2(a)] an electron tunnels from the Γ-valley in the conduction band into an unoccupied state (hole) in the *Light Hole* (LH) valence band valley while keeping its momentum $\boldsymbol{k} = 0$. On the contrary, for *indirect* tunneling [Fig. 6.2(b)] the electron tunnels from a conduction band valley with $\boldsymbol{k} \neq 0$ (*e.g.* the L-valley) and thereby has to change momentum to reach the valence band at $\boldsymbol{k} = 0$. It thus has to disperse its momentum with a phonon $\hbar\boldsymbol{q}$ making this process less probable. A slightly more advanced version of equation 6.2 taking into a account such effects is used in Ref. [202] based on the formulations provided by [203,204].

$$J_{\mathrm{BTBT}} = \mathcal{A} V_\mathrm{R} \left(\frac{\mathcal{E}}{\mathcal{E}_0}\right)^P \exp\left(\frac{-\mathcal{B}}{\mathcal{E}}\right) \tag{6.4}$$

with $\mathcal{E}_0 = 1\,\mathrm{MV/cm}$. The additional power P is 2 for direct BTBT and 2.5 for indirect BTBT respectively. Furthermore, the $\mathcal{A}$ and $\mathcal{B}$ parameter differ significantly for direct and indirect BTBT since for the indirect case additional variables for the interaction with phonons are taken into account such as the phonon occupation number, phonon energy and the phonon deformation potential. The formulations for the calculation of $\mathcal{A}$ and

[1] A more detailed derivation can be found in Ref. [201].

$\mathcal{B}$ in both cases are provided in the comprehensive work by Kao *et al.* [203]. Note that direct tunneling (equation 6.2) does not directly depend on the temperature whereas for indirect BTBT due to the phonon interaction a certain temperature dependence is expected. A yet more sophisticated model is the *non-local BTBT* model which is for example implemented in the numerical simulation tool Sentaurus Device [204]. This allows the calculation of BTBT in arbitrary (non-triangular) band profiles. Here BTBT is treated as distributed generation/recombination of electrons and holes on either side of the tunneling barrier.
While a further discussion of this model is beyond the scope of this work, equation 6.2 with the $\mathcal{A}$ and $\mathcal{B}$ parameters in equation 6.3 allow a qualitative impression of the parameters influencing BTBT. The exponential dependence is given by

$$J_{\mathrm{BTBT}} \propto A\mathcal{E} \exp\left(-c\frac{\sqrt{m_{\mathrm{T}}^{*}}E_{\mathrm{G}}^{3/2}}{\mathcal{E}}\right) \quad c = \mathrm{const.} \tag{6.5}$$

That is, BTBT increases by reducing the bandgap and the effective tunneling mass and by strengthening the electric field. While the former are defined by the material choice, the latter can be influenced by the abruptness of the *p-n* junction. Furthermore thanks to the non-phonon involvement for a given bandgap *direct* BTBT would always be dominant compared to the *indirect* process which is implicated in the $\mathcal{A}$ parameter in Ref. [203]. While the approximations in equation 6.2 and 6.4 are only valid in reverse direction, a generalized solution provided in [82] is modified with an overlap integral that considers the BTBT tunneling dependence on the band overlap and thereby also describes the BTBT turn off when the tunneling window closes for sufficient positive bias.

6.1.2. Excess Current

It turned out that one of the most challenging processes degrading Esaki diode characteristics and especially TFET switching performance for low biases is *Shockley-Read-Hall* (SRH) generation/recombination and particularly *field enhanced SRH* also known as *Trap-Assisted Tunneling* (TAT) [142]. As indicated in Fig. 6.1(d) and in the close up provided in Fig. 6.3(a) the presence of traps within the middle of the bandgap allows non-radiative capture and emission of carriers between either of the bands resulting in an *excess current* even when conduction and valence band do not overlap and the regular

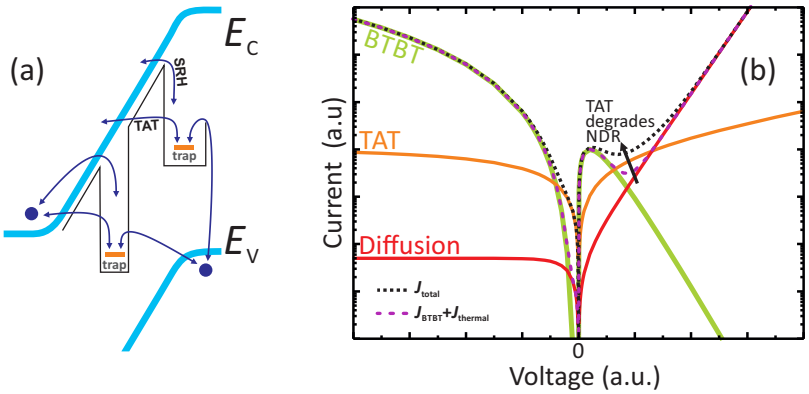


Figure 6.3.: *(a) Illustration of TAT process with two trap states within the bandgap and several indicated thermal emission and tunneling paths; (b) IV characteristics of an arbitrary tunnel diode demonstrating the three contributions BTBT, TAT and diffusion to the total current. TAT degrades the NDR regime.*

BTBT current is switched off. In a bias regime where BTBT is still low TAT, masks the BTBT current and smears out the BTBT onset. In the classical SRH mechanism an electron in the valence band absorbs a phonon and thereby is excited into a trap state within the bandgap. By absorbing a second phonon the electron is then released to the conduction band or vice versa. In the presence of an electric field this trap assisted generation/recombination process is significantly enhanced and also allows tunneling from the trap state directly into the respective band. This combination of phonon absorption and tunneling is called *Trap-Assisted Tunneling*. Fig. 6.3(b) shows the calculated IV characteristics of an arbitrary tunnel diode. The total current is split into its individual contributions from BTBT, TAT and from the regular thermal/diffusion current. While BTBT and diffusion dominate for strong reverse and forward bias, respectively TAT dominates the characteristics in the transition between BTBT turn-off and diffusion onset. Thereby it degrades the NDR as seen for the total curves with (black) and without (purple) the contribution from TAT. This can also shift the position of the current valley [205].

A unified expression for SRH and TAT was derived by Hurkx *et al.* [206]. The net generation rate $\mathcal{R}_t(x)$ per volume at a certain position x in the p-n junction for a given

trap density N_t can be calculated by

$$\mathcal{R}_\mathrm{t} = \int \frac{n_i^2 - np}{\tau_p \frac{n+n_1}{1+\Gamma_p} + \tau_n \frac{p+p_1}{1+\Gamma_n}} N_\mathrm{t} \mathrm{d}E \ , \tag{6.6}$$

where n_i is the intrinsic and n and p are the electron and hole concentrations, respectively. τ_n and τ_p are the respective minority carrier lifetimes per volume and the terms n_1 and p_1 are given by $n_1 = n_i \exp\{(E_\mathrm{t} - E_i)/k_\mathrm{B}T\}$ and $p_1 = n_i \exp\{(E_i - E_\mathrm{t})/k_\mathrm{B}T\}$ with the trap energy E_t and the intrinsic level E_i.

The enhancement factor $\Gamma(\Delta E, \mathcal{E}, m_\mathrm{T}^*)$ accounts for the generation rate increase due to field enhanced tunneling within the energy window ΔE and vanishes for zero field. In this case equation 6.6 simplifies to the classic SRH rate. The excess current can be calculated by integrating equation 6.6 along the *p-n* junction $J_\mathrm{TAT} = q \int \mathcal{R}_\mathrm{t} \mathrm{d}x$ [142]. From equation 6.6 it is evident that J_TAT increases with $n_i \propto \exp(-E_\mathrm{G}/2k_\mathrm{B}T)$ which in turn increases when reducing the bandgap. Due to this n_i dependence and the phonon involvement J_TAT shows a much stronger temperature dependence as direct BTBT. However, the tunneling process included in the enhancement factor $\Gamma(\Delta E, \mathcal{E}, m_\mathrm{T}^*)$ is very similar to BTBT resulting in the same qualitative dependence on bandgap, effective mass and electric field. That means for a given trap density all efforts to increase J_BTBT will also increase J_TAT to a certain extent so that one has to find the right compromise in the material parameters E_G and m_T^* while placing the emphasis on reducing N_t.

6.1.3. Thermal Current

When applying a sufficiently positive bias across the *p-i-n* diode the *thermal emission* or *diffusion current* turns on which is described by the familiar expression of a regular *p-n* diode

$$J_\mathrm{thermal} = J_0 \left[\exp\left(\frac{qV_\mathrm{D}}{\alpha k_\mathrm{B} T} \right) - 1 \right] \ , \tag{6.7}$$

where J_0 describes the off-current and depends among others on n_i and the doping levels on *p*- and *n*-side. J_0 strongly depends on the temperature. The ideality factor α lies between one and two. It accounts for classic generation/recombination and is one for diffusion dominated current and two for recombination dominated current.

The total current through the *p-i-n* junction is the sum of these three combinations $J_\mathrm{tot}(V_\mathrm{D}) = J_\mathrm{BTBT}(V_\mathrm{D}) + J_\mathrm{TAT}(V_\mathrm{D}) + J_\mathrm{thermal}(V_\mathrm{D})$ which are relevant in their respective

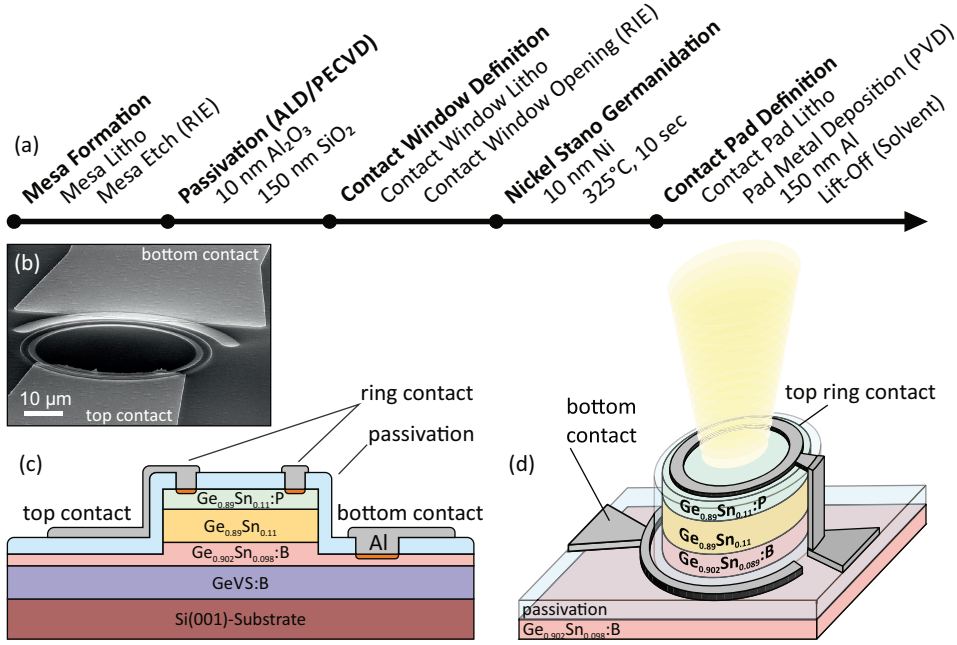


Figure 6.4.: *Fabrication of Ge(Sn) p-i-n diodes: (a) process flow; (b) SEM tilt-view of a fabricated p-i-n diode with top ring-contact for light emitting purpose; (c) cross sectional sketch; (d) 3D sketch of a vertical p-i-n diode with top-ring contact and indicated light emission.*

voltage regimes.

Reviewing current literature, tunnel diodes were realized on various group IV materials including Si [207], SiGe [208] and Ge [209], in which the highest tunneling currents in the 10^5 A/cm^2 range [210] and PVCR of 28:1 [211] were achieved with direct bandgap III-V materials as InAs and GaAs, respectively. Thanks to the small and direct bandgap enhanced BTBT is also expected for GeSn without the need of sustained effort in the integration of III-V materials on Si. The fabrication and characterization of GeSn *p-i-n* diodes is presented in the following sections.

6.2. Diode Fabrication

Diode fabrication of Ge(Sn) *p-i-n* structures as shown in Fig. 6.4(c), relies on standard semiconductor processing technology albeit at reduced temperatures $\leq 325\,^{\circ}$C to avoid

Sn diffusion or precipitation. *In-situ* doping during epitaxial growth is utilized to ensure well defined doping profiles with high dopant activation while avoiding implantation-induced damage (*cf.* CHAPTER 2.2). Boron and phosphorous are used for p and n-type doping respectively. On such vertical structures first a mesa is etched to uncover the p-type bottom layer. To avoid surface currents the structure is passivated using a stack of 10 nm Atomic Layer Deposition (ALD) deposited Al_2O_3 ensuring a good interface [212] covered with 150 nm of SiO_2 for electrical isolation, deposited by PECVD. As a next step contact windows are defined using photo lithography and dry etching of the passivation layer with CHF_3. Both diodes with areal top contacts and with ring contacts are fabricated. The latter can also be biased as LEDs. Good electrical contacts are ensured by the use of approx. 20 nm thick NiGeSn formed at 325 °C (*cf.* CHAPTER 4 and Ref. [81]). Finally, 200 nm Al is used as contact pads. The key fabrication steps are summarized in Fig. 6.4(a). Furthermore, a tilt view SEM, a 3D and a cross sectional sketch are shown in Fig. 6.4(b-d).

6.3. Electrical Characterization and Modeling

First a $Ge_{0.89}Sn_{0.11}/Ge_{0.902}Sn_{0.098}$ p-i-n diode is studied in detail. A cross sectional sketch of this stack is provided in Fig. 6.4(c). Thickness and active carrier concentrations of the top and bottom doped layers are 50 nm, $1 \cdot 10^{20}\,cm^{-3}$ n-type and 80 nm, $2 \cdot 10^{19}\,cm^{-3}$ p-type, respectively while the thickness of the intrinsic region amounts to 116 nm. Even if the intrinsic region is not intentionally doped a p-type carrier concentration of $\sim 1 \cdot 10^{18}\,cm^{-3}$ was measured with Electrochemical CV (ECV) profiling [213] which is most probably due to point defects induced by the low temperature growth at 350 °C as described in CHAPTER 2. The total layer thickness of 246 nm is significantly above the critical thickness for pseudomorphic growth such that the $Ge_{0.89}Sn_{0.11}$ layer is partially relaxed with a residual compressive strain of $\epsilon = -0.55\,\%$ as obtained from XRD reciprocal space mapping. As the band structure is defined by Sn content and strain (*cf.* CHAPTER 2) these parameters were used to calculate the bandgap energies and the respective effective masses, as listed in table 6.1. Thanks to the relaxation-induced down shift of the Γ-valley the $Ge_{0.89}Sn_{0.11}$ layer is expected to be slightly direct with a Γ-L offset of 13 meV. The bandgap in the n and i-layer amounts 0.507 eV. These diodes where wire bonded into a chip carrier and mounted in a liquid helium cold finger cryostat that was also used for electroluminescence measurements in SECTION 6.4.

Table 6.1.: *Calculated material parameters of the GeSn p-i-n structure grown on GeVS based on the measured Sn content and layer strain. The GeVS top valence band defines the zero energy. Sn content x_{Sn} (%), biaxial strain ϵ (%), energies in (eV), masses in (m_e); tunnel direction z=[001]. For L-valley l=[111] and t transverse to that. L mass in z direction can be calculated as described in chapter 2.1.*

x_{Sn}	ϵ	E_{HH}	E_{LH}	E_{Γ}	E_{L}	m_{LHz}	m_{HHz}	$m_{\Gamma z}$	m_{Lt}	m_{Ll}	m_{Lz}
11	-0.55	0.131	0.079	0.638	0.651	0.022	0.220	0.033	0.08	1.559	0.117
9.8	-0.37	0.109	0.073	0.640	0.648	0.022	0.221	0.033	0.08	1.559	0.117

IV curves were recorded for different diode sizes in a temperature range from 4.2 K to 295 K. The area normalized IV characteristics of a diode with a diameter of 50 µm are shown in Fig. 6.5(a) and show clear evidence of the three discussed current contributions (i) BTBT, including NDR, (ii) *excess current* due to TAT and (iii) *thermal/diffusion* current. This first demonstration of NDR in GeSn *p-i-n* diodes was reported in *Applied Physics Letters* (APL) [194].

The *p-i-n* diode features a strong reverse bias current that only very slightly depends on the temperature. At a reverse bias of −0.5 V the currents temperature dependence follows an activation energy of $E_a < 0.01$ eV that clearly points toward direct BTBT [192, 193] that only slightly decreases at reduced temperatures along with the bandgap increase. In contrast, a strong influence of the temperature is present in forward bias. NDR as a proof of BTBT is observed for temperatures below 175 K. For

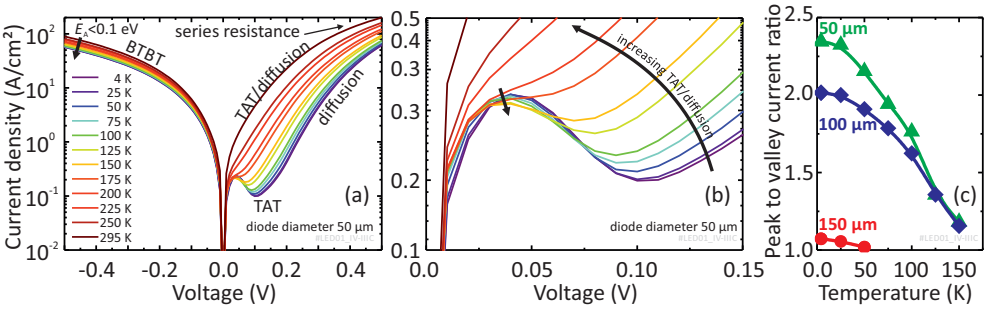


Figure 6.5.: *(a) Temperature-dependent IV characteristics of GeSn p-i-n diodes showing NDR at low temperatures, (b) close up of (a) in the NDR-region, (c) PVCR vs. temperature for different diode diameters.*

higher temperatures it is masked by excess current and diffusion current. A close up of the NDR regime is plotted in Fig. 6.5(b).

Whereas the valley current as expected increases with temperature due to strong enhancement of TAT and diffusion the inquiring eye observes a decrease of the peak current with temperature. This observation is related to two effects: First, even if $Ge_{0.89}Sn_{0.11}$ is a fundamentally direct semiconductor the Γ-L-valley separation is very small (13 meV) so that due to the higher L-valley DOS (larger effective mass) at higher temperatures a significant amount of electrons is not occupying the Γ but the L-valley which results in less favorable indirect tunneling with significantly higher tunneling masses (*cf.* Table 6.1). The L-valley occupation increases with doping such that for a total electron concentration of $1 \cdot 10^{18}\,\mathrm{cm}^{-3}$ at 300 K a majority of 68 % of the electrons reside in the L-valley. By reducing the temperature the electrons more and more condensate into the lower Γ-valley thereby promoting direct BTBT. That is, the increase of the peak current for reduced temperatures can be explained with the Γ-valley occupancy changes and is also observed in simulations presented later. Second, at the peak current, hole and electron distributions perfectly match as discussed in the previous section (*cf.* Fig. 6.1). Reducing the temperature removes the tails of the Fermi distributions and thereby increases the overlap within the tunneling window, which in turn increases the peak current [214].

For biases above 0.1 V the conduction band and valence band do not overlap anymore and NDR vanishes for all temperatures [Fig. 6.6(a)]. The reduced bandgap of the sample results in a strongly enhanced TAT and diffusion current. The PVCR at 4.2 K is 2.3 and roughly linearly decreases with temperature [Fig. 6.5(c)] which is in line with literature reports [208]. PVCR also degrades for larger diode diameters and for the 150 µm diameter device already vanishes at 50 K which might be related to current crowding effects.

To complement the experimental observations and to study the transport further, device simulations were performed using the simulation tool TCAD Sentaurus Device[2]. The band parameters from table 6.1 in conjunction with the charge carrier depth profile obtained by ECV shown in Fig. 6.6(a) upper panel, served as input parameters for the calculation of the band diagram in the lower panel of Fig. 6.6(a). For $V_D = 0\,V$ the conduction band in the top *n*-doped layer and the valence band in the *i*-layer overlap

[2]I thank Sebastian Blaeser for support with TCAD the simulations.

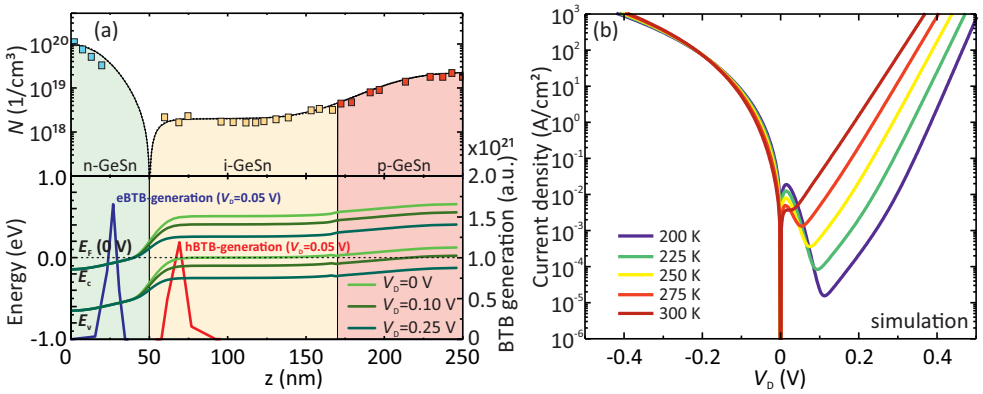


Figure 6.6.: *(a) (upper panel) The carrier density profile as measured by ECV is fitted and used for the band diagram calculation in the lower panel. Band to band (BTB) generation is also shown. (b) simulated IV characteristics for several temperatures.*

by approximately 0.14 eV which is essential for the observation of NDR. The band overlap vanishes if the forward bias is slightly above 0.1 V which is in line with the experimentally observed current valley position. Both direct and indirect BTBT was implemented in the simulations using the non-local BTBT model available for Sentaurus Device [204]. The relevant $\mathcal{A}$ and $\mathcal{B}$ tunneling parameters were calculated following the paper by Kao *et al.* [203] with the band parameters from table 6.1. TAT is not included in the simulations for simplicity and to focus on the effect of BTBT. Classical SRH though is implemented assuming mid gap trap levels. For the calculation of the thermal current parameters for Ge were used. Note that these simulations aim to qualitatively study the electrical characteristics with the focus on *direct vs. indirect* BTBT while precise fitting of *p-i-n* diode curves is done later for BTBT model calibration.

The simulated IV characteristics of this diode are shown in Fig. 6.6(b) for a set of temperatures and qualitatively mimic the experimentally observed behavior, though the simulated currents are higher probably due to underestimated circuit/contact resistances. Even if the simulation does not take into account TAT, at room temperature no NDR is observed in the simulation which agrees with the experiment. Due to the low bandgap and the relatively small band overlap of only 0.14 eV the strong thermal current masks BTBT at room temperature. However, in the simulation only a slight reduction of the temperature of 25 K is sufficient to unmask the NDR region while in the experiment NDR was only observed below 175 K. This difference is attributed to

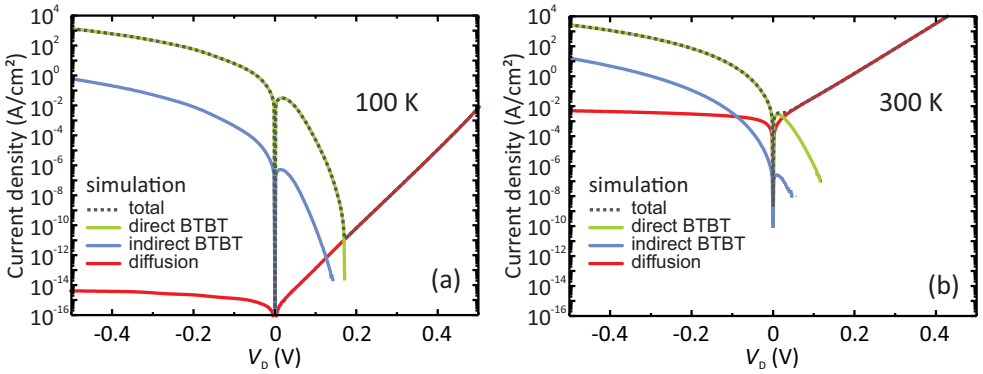


Figure 6.7.: *Current split in contributions from direct BTBT, indirect BTBT and diffusion. (a) for* 100 K *and (b) for* 300 K.

the absence of TAT in the simulations which strongly degrades the current valley in the experiment. Nevertheless, the voltage regime at which NDR is observed ($V_D \lesssim 0.1\,V$) is comparable for experiment and simulation. BTBT occurs at the *p-i*-junction as can be seen from the electron and hole band to band generation rates included in Fig. 6.6(a), lower panel, right *y*-axis.

The simulation allows to break down the total current through the diode into the different contributions from direct BTBT, indirect BTBT and diffusion, which is done in Fig. 6.7 for 100 K and for 300 K. In spite of the only slight directness of the diode and the higher DOS at 300 K the L-valley occupation is stronger than Γ-valley occupation, direct BTBT is several orders of magnitude stronger than indirect BTBT thanks to the non-phonon involvement and the significantly lower Γ-valley mass. This agrees with simulations results from Kao *et al.* [203] who found that even in pure Ge direct BTBT prevails despite the fact that the L-valley is 140 meV lower than the Γ-valley. This preferred direct BTBT is for example utilized in the Zener emitter to inject more carriers in the Γ-valley and thereby enhances electroluminescence from Ge [215].

While the thermal current is strongly suppressed at low temperatures, both direct and indirect BTBT only change slightly. A reduction of the temperature from 300 K to 100 K in reverse bias ($V_D = -0.5\,V$) changes the simulated direct BTBT only by a factor of 2 while the indirect component is reduced by a factor of 60 compared to several orders of magnitude in the thermal saturation current. The measured reverse bias current at $-0.5\,V$ only changes by a factor 1.5 and thereby proofs the direct BTBT dominance in

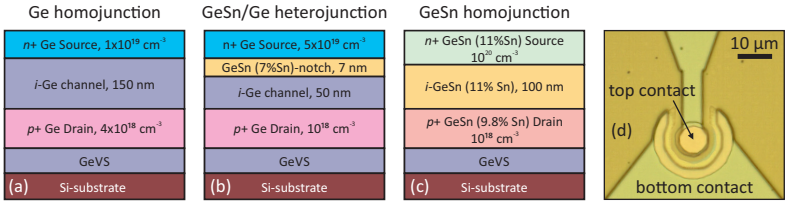


Figure 6.8.: *(a-c) Illustrated layer stacks of the three analyzed p-i-n structures. (d) Optical microscopy image of a fabricated diode.*

these *p-i-n* diodes.

During the period of this work that was conducted and the University of Notre Dame, Indiana, USA, the influence of the Sn-incorporation on the BTBT characteristics was studied. For this purpose two additional *p-i-n* layer stacks were epitaxially grown by RPCVD[3] one with pure Ge and one on a heterostructure of Ge where a 7 nm thin $Ge_{0.93}Sn_{0.07}$ notch layer is introduced between the highly doped n^+-Ge-source and the intrinsic Ge-channel. The layer stacks are depicted in Fig. 6.8(a-c). Diodes were fabricated on these two layers and on the previously studied $Ge_{0.89}Sn_{0.11}$-stack for comparison by transferring the established process from FZ-Jülich to the University of Notre Dame. An optical microscopy image of a fabricated *p-i-n* diode is shown in Fig. 6.8(d).

The temperature-dependent IV measurements on these three diode types were obtained on a LakeShore CPX cryogenic probe station and are shown in Fig. 6.9. While the characteristics of the $Ge_{0.89}Sn_{0.11}$ diode could be reproduced including NDR, the $Ge/Ge_{0.93}Sn_{0.07}$ heterojunction and Ge-homojuction do not feature a NDR-region. Indeed NDR is not expected for these layers since the carrier concentration in the undoped Ge-channel is too low to create a band overlap. For sufficient large reverse bias though such an overlap can be created thereby enabling BTBT. This can be seen for the $Ge/Ge_{0.93}Sn_{0.07}$ heterojunction diode in Fig. 6.9(b) that features a strong temperature dependence in both low forward and reverse bias but only a slight temperature dependence for reverse bias $< -1\,\mathrm{V}$. The strongly temperature activated behavior of this diode in the low bias regime of $V_D = \pm 0.3\,\mathrm{V}$ is most probably due to increased TAT at the heterojunction interface. In the reverse bias BTBT regime a clear trend of increasing current is present when going from the Ge-homojuction to $Ge_{0.93}Sn_{0.07}$

[3] I greatly acknowledge the supply of these Ge and GeSn/Ge heterostructures from TSMC and IMEC respectively.

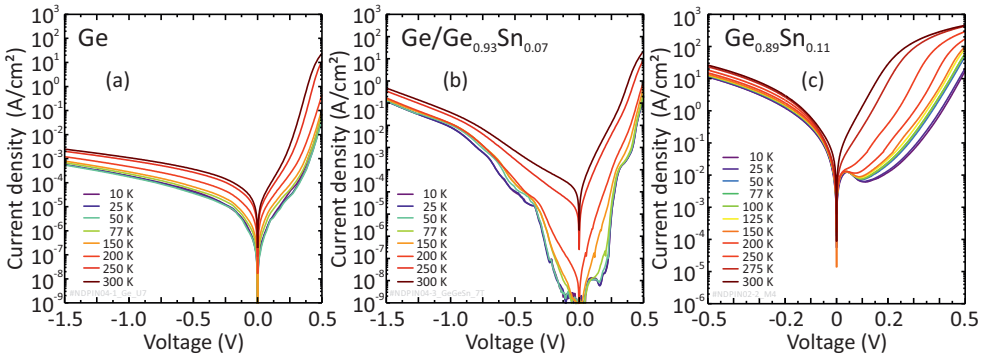


Figure 6.9.: *Temperature-dependent IV characteristics of (a) Ge-homojunction, (b) GeSn/Ge-heterojunction and (c) GeSn-homojunction p-i-n diode.*

heterojuction to $Ge_{0.89}Sn_{0.11}$ homojuction which goes hand in hand with the Sn-induced bandgap shrinkage.

A quantitative analysis of BTBT was performed in cooperation with the group of D. Antoniadis at the *Massachusettts Institute of Technology* (MIT). Fitting of the IV curves of the three diodes was done with a compact model described by Sajjad *et al.* [202] using the BTBT and TAT formalism introduced in equations 6.4 and 6.6, respectively in conjunction with the regular thermal emission/diffusion current from equation 6.7. Here, the needed material parameters were calculated by density functional theory and $\boldsymbol{k} \cdot \boldsymbol{p}$-theory. The good agreement of experiment and model is evident in Fig. 6.10(a). The

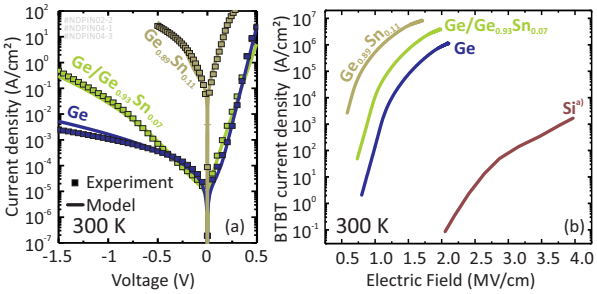


Figure 6.10.: *(a) Best fit obtained for* 300 K *p-i-n diode characteristics. (b) Extracted BTBT current density vs. electric field for the three analyzed structures compared to data on Si from literature* [a)] *[216].*

ideality factors of the diodes are between 1.1 and 1.5. From the modeled IV curves the dependence of the BTBT current on the electric field within the junction was extracted as shown in Fig. 6.10(b) and compared to literature data for Si in the field range that corresponds to the operation regime of TFETs. The experimentally observed increase of the reverse bias (BTBT) current with Sn content also reflects in Fig. 6.10(a). Thanks to the reduced and direct bandgap in conjuction with the low Γ-electron mass the $Ge/Ge_{0.88}Sn_{0.11}$ homojunction yields the highest BTBT current and thereby qualifies GeSn as suitable material for TFETs.

6.4. Electroluminescence from GeSn p-i-n Diodes

The same properties that suggest GeSn for application in tunneling devices promote it as material for optoelectronic application. The direct bandgap properties allow efficient *Photoluminescence* (PL) [45], *Electroluminescence* (EL) [18, 19] or even lasing [15, 46, 65, 78]. The bandgap range that can be achieved with the SiGeSn system of 0.4 eV-0.9 eV corresponds to a *Short Wavelength Infrared* (SWIR) spectrum of 1.4 µm to 3 µm that is very interesting for communication as well as for sensor application *e.g.* for trace gas analysis [21].
The fabrication design of the *p-i-n* diodes presented in Fig. 6.4(d) includes the use of ring electrodes as top contacts and thereby enables to bias them also as LED allowing to complement the electrical analysis with electroluminescense measurements.

A short Background of Electroluminescence

Within the space charge region of a forward biased *p-n* or *p-i-n* diode the electron current being the majority carrier current on the *n*-side converts into a hole current as majority carrier current on the *p*-side of the junction [Fig. 6.11(a)]. This process occurs *via* recombination and can be mediated by several different *radiative* or *non-radiative* mechanisms. Typical non-radiative recombination processes are (i) the previously discussed SRH recombination *via* traps within the bandgap, (ii) *surface recombination*, (iii) *Auger-recombination* due to interaction with other charge carriers. Radiative recombination occurs for electrons residing in the conduction band that spontaneously recombine with a hole while emitting a photon with energy $E_{sp} = h\nu$ [Fig. 6.11(b,c)]. This *spontaneous emission* can occur both in direct and indirect semiconductors. However, the

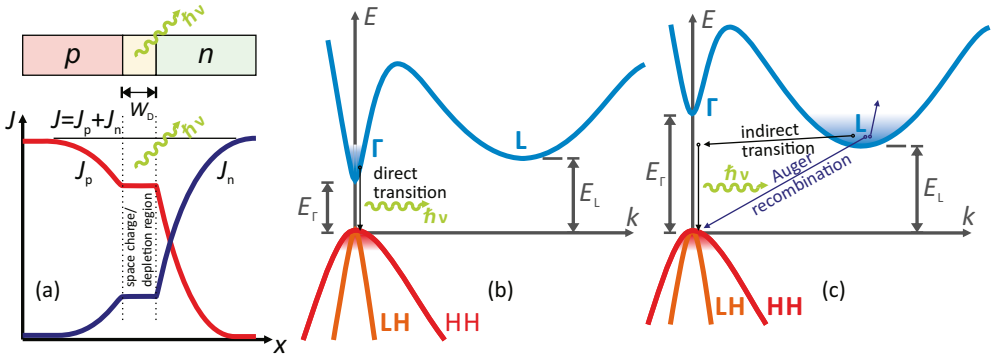


Figure 6.11.: *Recombination in a forward bias $p-n$ diode (a) By recombination in the space charge region the electron current j_n on the n-side converts into a hole current J_p on the p-side of the $p-n$-junction while the total current J is conserved. (b) Recombination in a direct semiconductor (c) recombination processes in an indirect semiconductor. (a) From [82].*

total momentum needs to be conserved such that in case of electrons not residing in the Γ-valley a phonon has to be involved making this process less probable.

The spontaneous emission rate depends on the occupation of electrons in states in the conduction band $f_c(E_c)$ that recombine with unoccupied states $1-f_v(E_v)$ in the valence band described by the Fermi-Dirac distributions. $E_c(\boldsymbol{k})$ and $E_v(\boldsymbol{k})$ are the dispersion relation of conduction band and valence band respectively. The spectral spontaneous emission rate $\mathcal{R}_{sp}(h\nu)$ is calculated by summing up the rates for recombination with each of the three valence bands, light hole, heavy hole and split-off band [217].

$$\mathcal{R}_{sp}(E_{sp}) \propto \sum_{v=LH,HH,SO} |\mathcal{H}|^2 \mathcal{M}(E_{sp}) f_c(E_c)[1-f_v(E_v)]\delta(E_c - E_v - E_{sp}) \,, \tag{6.8}$$

where $\mathcal{H}$ is the dipole matrix element for the recombination process and $\mathcal{M}$ the total optical density of states. For low doped semiconductors the carriers are far above the Fermi level such that the Fermi-Dirac distribution can be approximated by the Boltzmann distribution. Furthermore if $\mathcal{H}$ is assumed to be independent of energy and only one parabolic conduction band is assumed, equation 6.8 can be simplified to

$$\mathcal{R}_{sp}(E_{sp}) \propto \sqrt{E_{sp} - E_G} \exp\left(-\frac{E_{sp} - E_G}{k_B T}\right) \tag{6.9}$$

The square root term is related to the 3D DOS while the spectrum for higher energies

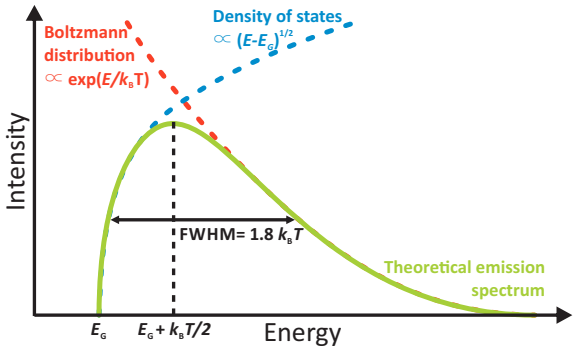


Figure 6.12.: *Theoretical EL spectrum for direct transitions.*

is dominated by the exponential Boltzmann term. A theoretical spectrum based on equation 6.9 is depicted in Fig. 6.12. Equation 6.9 peaks at $E_G + k_B T/2$ with a theoretical peak width of $1.8 \cdot k_B T$. The final EL intensity depends on the ratio of radiative and non-radiative recombination. This results in the following temperature dependence of EL for direct and indirect semiconductors, respectively.

In case of a *direct* semiconductor at room temperature a certain percentage of carriers is thermally excited from the Γ-valley in the next higher valley (L-valley in case of GeSn). While cooling down the sample more and more electrons condensate into the lower Γ-valley thereby enhancing more probable direct recombination. Simultaneously non-radiative processes like SRH decrease due to the strong temperature dependence of the phonon occupation. As a consequence for a strong *direct* semiconductor EL continuously increases while reducing the temperature.

For EL in an *indirect* semiconductor electrons either need to be thermally excited from the indirect into the Γ-valley from which they can recombine directly or they recombine from the indirect valley *via* phonon interaction. Both processes decrease when reducing temperature such that EL of a clear indirect semiconductor decreases as well for low temperatures. Semiconductors that are close to the transition from direct to indirect can also show intermediate behavior where the EL first slightly decreases and then increases while reducing the temperature. This effect is attributed to the temperature dependence of the non-radiative recombination times [15].

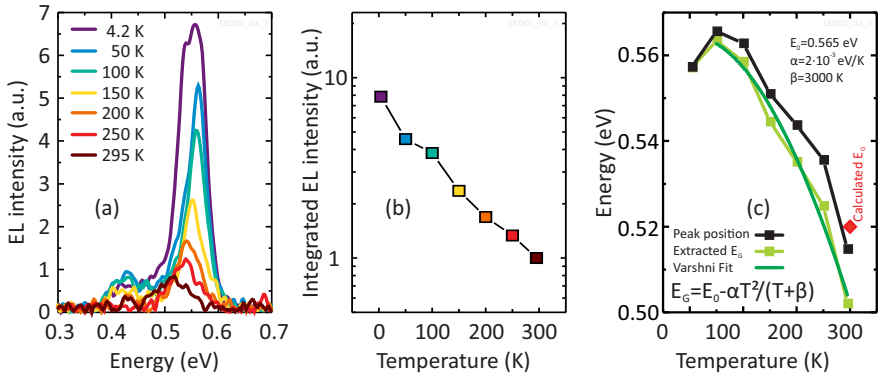


Figure 6.13.: *(a) Measured EL spectra at different temperatures, (b) Integrated EL intensity from (a). (c) Extracted peak position and bandgap from (a). EL recorded by Daniela Stange.*

Electroluminescence Measurements

The ring electrode layout from Fig. 6.4(b-d) was utilized to characterize the EL on the $Ge_{0.89}Sn_{0.11}/Ge_{0.902}Sn_{0.098}$ diodes. To that end the diodes where mounted in a liquid helium cold finger cryostat and scattered EL was detected with a liquid nitrogen cooled InSb detector. Whereas BTBT occurs in the reverse and slight forward bias regime, for EL measurements the diode is biased in strong forward direction of 2.5 V corresponding to 538 A/cm^2 to avoid unwanted tunneling and ensure sufficient light intensity even at room temperature. For a better signal to noise ratio the bias was pulsed with 2 kHz and a 50 % duty cycle to allow the use of a Lock-In-Amplifier. Integration time was 300 ms.

The measured EL-intensity spectra for the temperature range 4.2 K to 295 K are shown in Fig. 6.13(a) and exhibit a continuous increase with decreasing temperature typical for direct bandgap semiconductors. This result is supported when integrating the spectra from Fig. 6.13(a) as shown in Fig. 6.13(b). A continuous increase of the integrated EL with decreasing temperature is observed here as well, clearly pointing towards this material being a fundamentally direct or at least "at the transition" to fundamentally direct semiconductor. It might be worth noticing that as fabricated end of year 2014 this would be the first direct bandgap group IV LED demonstrating a big step towards efficient Si-compatible group IV light emitters.

A clear shift of the peak position towards higher energies is visible when reducing the temperature. This goes along with the bandgap increase for low temperatures. The

EL peak positions are extracted by fitting the experimental spectra with a bi-Gaussian function. According to equation 6.9 the bandgap is extracted by subtracting $0.5k_BT$. The bandgap measured that way is plotted in Fig. 6.9(c) against the temperature. The experimental data follows roughly the commonly used empirical Varshni formula

$$E_G = E_0 - \alpha T^2/(T+\beta)\ , \tag{6.10}$$

using E_0, α and β as fitting parameters shown in the inset of Fig. 6.13(c). However, the error for the extracted α and β parameters is in the range of the numbers itself such that these values are not trustworthy and the fit can only be seen to have qualitative agreement. The extracted bandgap at room temperature of 0.50 eV is slightly lower than the theoretically calculated bandgap of 0.52 eV presented in table 6.1. However, when taking into account the uncertainty resulting from typical strain ±0.1 % and Sn content variation ±0.5 % Sn, the extracted bandgap is in good agreement with the calculated data.
At the lowest temperature of 4.2 K the EL seems to feature a double peak whose left flank might be attributed to the less probable Γ-valley-HH transition. Furthermore the peak position at 4.2 K is shifted to slightly lower values which might be due to localized states as also observed in photoluminescence experiments [45]. The slight peak, visible around 0.4 eV is most probably due to defects.

6.5. Summary

GeSn *p-i-n* diodes where analyzed for the application as tunnel diode and as LED. Temperature-dependent IV measurements in conjunction with device simulations proofed the dominance of direct band to band tunneling. The analysis of different layer stacks revealed increased BTBT compared to Ge and Si demonstrating the advantage of low bandgap and low effective mass in GeSn. Negative Differential Resistance with a Peak-to-Valley Current Ratio of 2.3 at low temperatures was experimentally observed in GeSn for the first time. At room temperature trap assisted tunneling masks the Negative Differential Resistance.
Electroluminescence measurements showed a temperature dependence typical of *direct* semiconductors. The demonstration of the first direct bandgap group IV LED marks an important step towards efficient group IV light emitters.

7 | GeSn-based Tunnel FETs

THE *Tunnel Field-Effect Transistor* (TFET) is a promising candidate as complement or even as a successor to MOSFETs for ultra low power applications. The fundamentally different operation principle of a TFET relies on BTBT rather than on thermionic emission allowing to reduce the supply voltage beyond the physical limit of a MOSFET and thereby to decrease power consumption for both logic and analog/sensor application [10].

As discussed in the previous chapter the direct and low bandgap properties of GeSn qualify this novel group IV semiconductor as a promising material for TFETs [29, 34]. In the first section of this chapter a brief review of history and state of the art of Tunnel FETs is provided along with the operation principle. Based on this introduction basic design considerations are derived to improve TFET characteristics. The following sections describe fabrication, characterization and modeling of GeSn/Ge heterojunction TFETs. These results were partially presented on the *International Electron Devices Meeting* (IEDM) and in *Transactions on Electron Devices* (TED) [37, 126]. Also the suitability of TFETs for analog application was experimentally demonstrated within the scope of this work and reported in *Solid State Electronics* (SSE) [218] but shall not be treated here in more detail.

7.1. The Tunnel FET

A Tunnel FET is a reverse biased gated *p-i-n* diode. Its operation principle relies on tuning the tunnel barrier with an external gate voltage and thereby allowing or suppressing BTBT. This concept was first described in 1978 by Quinn *et al.* [219] whereas the usage as a transistor was first demonstrated in 2000 by Hansch *et al.* [220]. A typical band diagram of a TFET is sketched in Fig. 7.1. If the gate is negatively biased with respect to the *n*-type source contact the bands in the channel are pulled upwards and create a band overlap that enables BTBT. The device turns on. Furthermore the bands bend stronger for higher $|V_G|$ and reduce the tunneling distance yet enhancing BTBT. The device sketched in Fig. 7.1 is called *p*TFET since it relies on hole transport in the channel. It operates at $V_G, V_D < 0$. The complementary device using a highly doped *p*-type source and an electron channel is called *n*TFET and has $V_G, V_D > 0$.
The Fermi-Dirac distribution $f(E)$ is also indicated in Fig. 7.1. As BTBT is only possible within the yellow shaded tunneling window defined by the band overlap, the tails of the Fermi function do not contribute to the electrical transport. This band pass filter function effectively cools the carrier distribution and thereby allows switching characteristics steeper than the limit of 60 mV/dec for thermionic transport in a MOSFET. As a consequence the steep turn on of a TFET allows to further scale down the transistor operation voltage without compromising off-current or on-off-ratio.

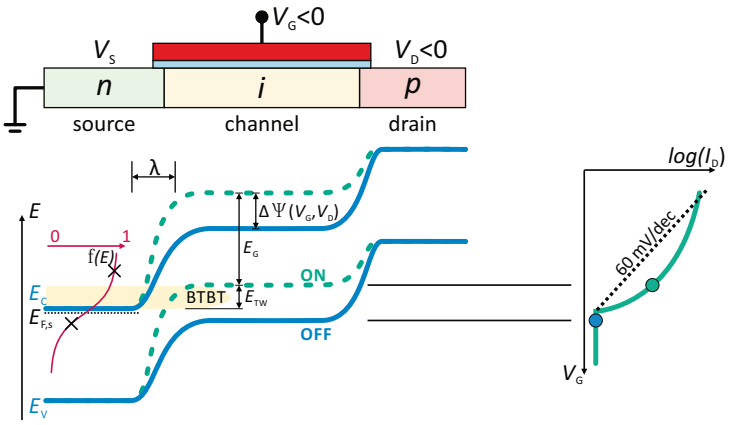


Figure 7.1.: *Operation principle of a pTFET with corresponding band diagrams and idealized IV characteristics.*

Here the TFET current is described by means of a compact model derived by Sajjad *et al.* [142,202], which is used in SECTION 7.3 to model the experimentally observed TFET characteristics. The model is based on the same formalism as a reverse biased *p-i-n* diode (Eq. 6.2 and 6.4) however in this case the electric field depends on both drain voltage V_{D} and gate voltage V_{G}. Recapitulating equation 6.4 multiplied with the depth of the BTBT region below the gate, yields the device width normalized BTBT-current

$$I_{\mathrm{BTBT}} = d_{\mathrm{BTBT}} \mathcal{A} V_{\mathrm{R}} \left(\frac{\mathcal{E}}{\mathcal{E}_0}\right)^P \exp\left(-\frac{\mathcal{B}}{\mathcal{E}}\right) . \tag{7.1}$$

The electric field $\mathcal{E}$ can be approximated by $\mathcal{E} \approx \mathcal{E}_{\mathrm{Bi}} + \psi_{\mathrm{S}}/\lambda$, where the characteristic scaling length λ describes the abruptness of the tunneling junction and consists of contributions from the doping profile λ_{dop} and the electrostatic gate control λ_{ch}, $\lambda = \lambda_{\mathrm{dop}} + \lambda_{\mathrm{ch}}$. $\psi_{\mathrm{S}}(V_{\mathrm{G}}, V_{\mathrm{D}})$ is the surface potential. The built-in electric field is $\mathcal{E}_{\mathrm{Bi}} = 0.5 E_{\mathrm{G}}/\lambda$ while assuming the doping to be such that in the unbiased case the Fermi level coincides with the valence band edge on the source side and with $E_{\mathrm{G}}/2$ for the intrinsic channel.
The reverse bias V_{R} is essentially controlled by the tunneling window E_{TW}: $V_{\mathrm{R}} = F_{\mathrm{sd}} \cdot E_{\mathrm{TW}}/q$. With the saturation function F_{sd} stemming from the Landauer formalism [202]. The DOS of valence and conduction band edges are not infinitively sharp and thus also not the tunneling window E_{TW}. Indeed the DOS is blurred out by the Urbach-tail U_0 describing the intrinsic decay at the band edge. V_{R} and E_{TW} are thus given by

$$V_{\mathrm{R}} = F_{\mathrm{sd}}(V_{\mathrm{D}}) \cdot E_{\mathrm{TW}}/q = F_{\mathrm{sd}}(V_{\mathrm{D}})/q \cdot U_0 \ln\left[1 + \exp\left(\frac{\psi_{\mathrm{S}}(V_{\mathrm{G}}, V_{\mathrm{D}}) - \psi_{\mathrm{S0}}(V_{\mathrm{D}})}{U_0}\right)\right] , \tag{7.2}$$

Where $\psi_{\mathrm{S0}}(V_{\mathrm{D}})$ describes the surface potential for zero gate bias. Equation 7.1 and 7.2 in the first order do not depend on the temperature which is in line with the reverse bias *p-i-n* characteristics discussed in the previous section. From equation 7.1 the *Subthreshold Swing* (SS) can be calculated

$$SS = \left[\frac{\partial \log(I_{\mathrm{D}})}{\partial V_{\mathrm{G}}}\right]^{-1} = \ln(10)\left[\frac{1}{V_{\mathrm{R}}}\frac{\partial V_{\mathrm{R}}}{\partial V_{\mathrm{G}}} + \frac{P\mathcal{E} + \mathcal{B}}{\mathcal{E}^2}\frac{\partial \mathcal{E}}{\partial V_{\mathrm{G}}}\right]^{-1} . \tag{7.3}$$

Further simplification of equation 7.3 yields $SS \propto \ln(10) V_{\mathrm{G}}$ whereas for a MOSFET the SS is physically limited to $SS = \ln(10) k_{\mathrm{B}} T/q \approx 60\,\mathrm{mV/dec}$ at room temperature. That means $SS < 60\,\mathrm{mV/dec}$ can be achieved with TFET. Since SS is lower for small gate voltages TFETs are especially interesting for low voltage applications.

The equations 7.1-7.3 imply the following **TFET design considerations**

- **Material parameters:** BTBT current increases for reduced and direct bandgap E_G and for small effective masses of electrons and holes. In that sense group IV Ge(Sn) alloys or III-V materials are promising candidates for implementation in TFETs.

- **Doping:** In accordance with Fig. 7.1 the *source doping level* should be such that the Fermi level coincides with the conduction band edge. For too low doping the high energy tail of the Fermi distribution would lie within the tunneling window diluting the filter function. On the contrary for too high doping especially when the source is degenerately doped the DOS of the conduction band edge smears out [221, 222] leading to a long *Urbach-tail* U_0. A high U_0 decreases the derivative $\partial V_R/\partial V_G$ and thereby corrupts the SS according to equation 7.3. The *doping profile* should be as abrupt as possible to ensure a small λ which in turn leads to a strong electric field $\mathcal{E}$ at the tunneling junction and an increased $\partial\mathcal{E}/\partial V_G$ resulting in increased I_{BTBT} and reduced SS.

- **Electrostatics:** Good electrostatic control of the bands in the channel increases the derivative $\partial V_R/\partial V_G$ and thereby reduces the SS (Eq. 7.3). Ideally dV_R/dV_G approaches unity. Good electrostatics can be ensured by a high oxide capacitance and a thin body of the channel both reducing λ. A small λ increases the electric field which in turn boosts the tunneling current (Eq. 7.1). Ideally the gate controls the channel not only from the top but from several sides. Typical multigate geometries are the FinFET (Trigate) or ultimately the gate-all-around nanowire geometry.

TFET nonidealities

A TFET might suffer from the same parasitic currents as a tunnel diode, SRH and TAT. Furthermore non-idealities related to the gate-dielectric reduce on-current and SS. Typical TFET non-idealities are

- **Interface traps:** As discussed in CHAPTER 5.1.2 the presence of an interface trap capacitance C_{it} dilutes the efficiency to move the bands with the gate voltage and thereby degrades the SS: $V_G = \eta V_{G(external)}$, $\eta = C_{Ox}/(C_{Ox} + C_{it})$.

- **Parasitic currents:** SRH and TAT currents essentially degrade off-state and low-bias regime of a TFET and thereby mask the steepest region of TFETs switching characteristics. It features the same dependences as the excess current described in CHAPTER 6.1.2. A compact expression for the TAT current was derived by Sajjad *et al.* [202] based on equation 6.6

$$I_{\mathrm{TAT}} = \frac{q}{2}\, n_i \sigma_{\mathrm{t}} v_{\mathrm{th}} D_{\mathrm{t}}\, \Gamma d_{\mathrm{gen}} \left[1 - \exp(-qV_{\mathrm{D}}/k_{\mathrm{B}}T)\right], \tag{7.4}$$

  with the trap capture cross section σ_{t}, the thermal velocity v_{th} and the generation length d_{gen}.

  TAT current is proportional to the total trap density $D_{\mathrm{t}} = D_{\mathrm{it}} + D_{\mathrm{bt}}$ that contains both contributions from traps at the source-channel interface and the gate-channel interface pointing out the importance to optimize the two of them. That is, D_{it} degrades TFET characteristics twofold by a reduced gate efficiency and by increased TAT. SRH and TAT increase with decreased bandgap and decreased effective masses. As a consequence one has to find the right compromise in material choice between high BTBT and acceptable off-current. Heterojunction designs utilizing different bandgap materials at source and drain are one approach to tackle this issue. However, TAT turned out to be a crucial challenge in TFETs. Reducing both interface and bulk trap density is thus the key enabler for achieving sub 60 mV/dec switching characteristics. *Gate leakage* can also degrade the off-current and thereby mask the steepest part of the TFET characteristics. While the gate oxide thickness should be as thin as possible to achieve good electrostatics, significant gate leakage has to be avoided.

- **Ambipolarity:** In the on-state off a pTFET carrier tunnel from the n-doped source into the channel. If the device is turned Off, the bands in the channel are pushed down (*cf.* Fig. 7.1) closing the tunneling window on the source side. However, when the bands are further pushed down a band overlap at the channel-drain side can be created, leading to parasitic drain-channel BTBT. That way a pTFET turns into a nTFET or *vice versa*. This effect is denoted as *ambipolarity*. It can be decreased by implementing a heterojunction design that uses a larger bandgap material on the drain side.

Numerous experimental demonstrations of TFETs on group IV, group III-V materials and even on novel materials as graphene, carbon nanotubes or 2D materials have been reported and also subthreshold swings below 60 mV/dec were achieved [223]. Despite the relatively large and indirect bandgap to date the majority of leading edge devices with $SS < 60\,\mathrm{mV/dec}$ is based on Si, thanks to its superior material quality and mature interface technology. However, the sub 60 mV/dec operation regime is limited to relatively small currents $< 1\,\mathrm{nA/\mu m}$. In terms of bandgap engineering, III-V materials are very promising due to their direct bandgap and compositional flexibility. In fact III-V material-based TFET generally allow higher on-currents albeit up to now the less mature high-κ interface with high D_{it} hampered the potential of III-V TFET and compromised the SS to values significantly larger than 60 mV/dec. Only recently nTFETs with MOSFET competitive performance based on GaAsSb/GaSb were reported [224] justifying sustained efforts for possible integration of III-V materials on Si. However, the challenge remains for pTFETs that generally feature worse switching characteristics than nTFETs.

The novel group IV (Si)GeSn material system offers an alternate route to III-Vs. It combines III-V properties like low direct bandgap and low effective masses with the easy integration of group IV materials on Si. Several theoretical studies promote GeSn as a superior material for TFETs [23, 24, 225] and also the growth of SiGeSn/GeSn heterostructures for TFETs was experimentally demonstrated [29]. However, as novel material it faces challenges similar to III-Vs in terms of material and interface quality that urge for individual optimization. Indeed, only a few experimental studies on GeSn TFETs have been reported [34–36] including substantial contribution that was made within the course of this work [37, 126].

7.2. Fabrication of Vertical GeSn/Ge Heterojunction TFETs

Vertical heterojunction $Ge_{0.93}Sn_{0.07}$/Ge pTFETs were fabricated from the p-i-n stack analyzed in CHAPTER 6.3. The layer stack including a XTEM of the tunneling junction is depicted in Fig. 7.2(a,b). Such a heterojunction design was theoretically predicted to be superior to a homojunction design with the same Sn content thanks to reduced ambipolarity and off-current [24]. A corresponding band diagram is sketched in Fig. 7.2(c) and illustrates the reduced tunneling barrier at the source/channel junction thanks to the GeSn-notch layer, whereas a larger barrier is present at the channel/drain junction

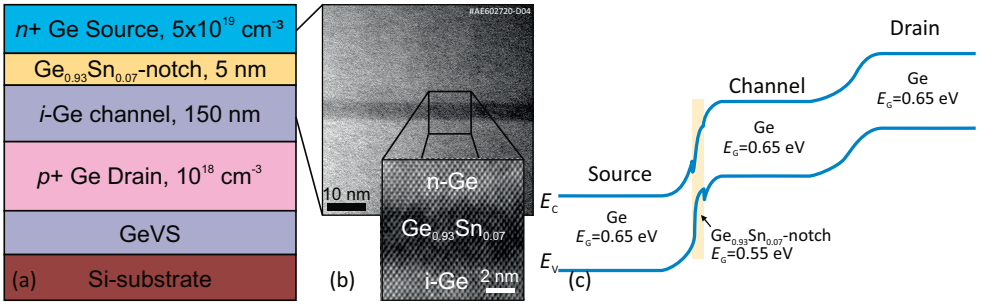


Figure 7.2.: *Layer stack used for GeSn pTFET fabrication: (a) sketch, (b) XTEM, (c) band diagram sketch. I greatly acknowledge TEM analysis by Lidia Kibkalo.*

to reduce ambipolarity. The used vertical device geometry enables a self aligned gate deposition and is adopted from a process previously developed for III-V InGaAs/GaAsSb-TFETs [226]. Such devices [126] are also considered for performance benchmarking in SECTION 7.3. However, due to the different chemical properties of InGaAs/GaAsSb and Ge/GeSn new etching recipes were developed for Ge/GeSn to achieve the mesa profiles needed for self aligned gate deposition.

An overview of the key fabrication steps is provided in Fig. 7.3. Device cross-sections and corresponding SEM images are marked with according colors. The fabrication started with pre cleaning and native oxide removal followed by the "HF-HCl-last" procedure described in CHAPTER 3.1. As source metal contact 200 nm of the refractory metal *Molybdenum* (Mo) was deposited to ensure survival of the top metal contact in subsequent chemical treatments. The contact area was defined using a lift-off Ti/Cr hardmask fabricated with *Electron Beam Lithography* (EBL) and electron beam evaporation. The fin-structure was transferred to the underlying Mo and n^+-Ge source layer by vertically etching Mo with SF_6:O_2 RIE and Ge with Cl_2:Ar RF:ICP (100 W:1000 W) dry etch chemistry. For self aligned gate deposition a tapered etch profile of the channel is crucial. Thus $Ge_{0.93}Sn_{0.07}$-notch layer and Ge-channel were etched down to the p^+-drain using a modified Cl_2:Ar RF:ICP (5 W:1000 W) recipe with reduced RF-power to decrease the directionality of the plasma (bright blue marked step in Fig. 7.3). As a next step an undercut is created at the Mo-Ge-junction by wet etching Ge with H_2O_2:H_2O (1:10)[1].

[1]Base concentration of H_2O_2 is 30 wt%

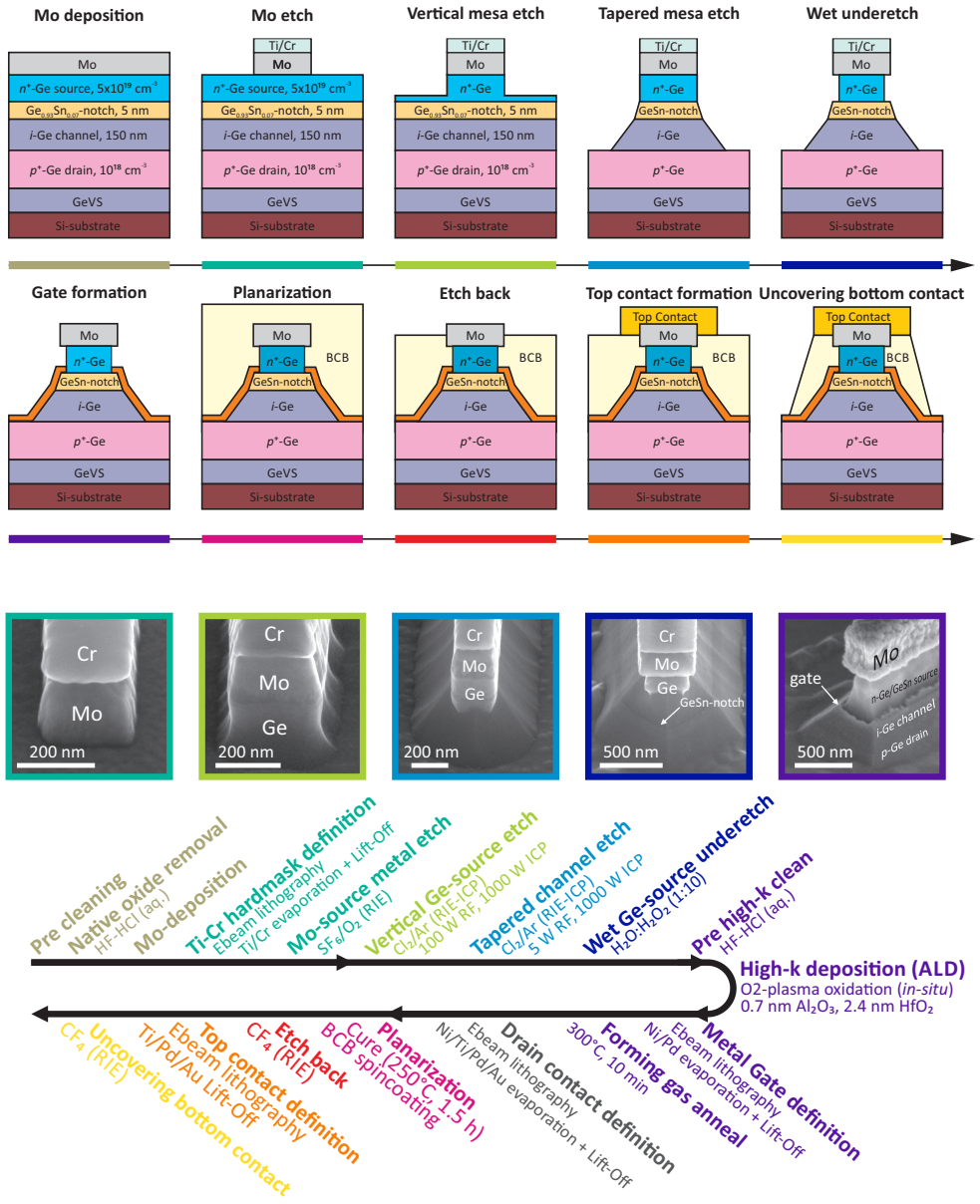


Figure 7.3.: *Key steps for vertical Ge/GeSn TFET fabrication. The cross sectional sketches in the first two rows are color coded with the corresponding SEM images and the flow-diagram below.*

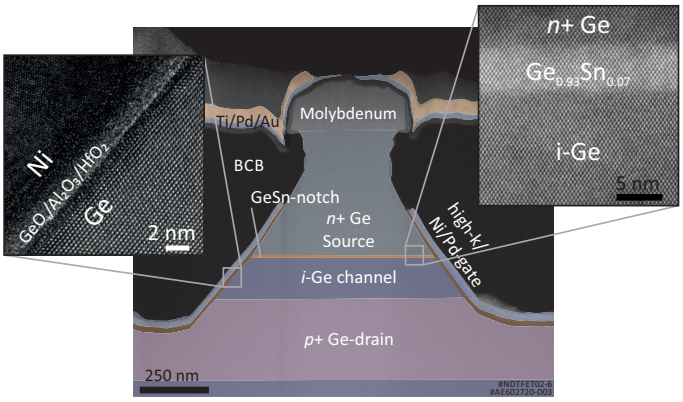


Figure 7.4.: *False colored high-resolution STEM cross section of a GeSn/Ge TFET with close ups of the high-κ channel interface and the tunnel-junction. I greatly acknowledge FIB-lamella preparation and TEM analysis by Tatjana Orlova and Sergej Rouvimov, respectively, NDIIF, Notre Dame, IN, USA.*

Subsequently the scaled $HfO_2/Al_2O_3/GeSnO_x$ tri-layer gate stack described in CHAPTER 5.4 was deposited. As a metal gate 20 nm Ni and 20 nm Pd were deposited on the fins using a lift-off process with EBL in conjunction with thermal and ebeam evaporation, respectively. The undercut at the Mo-Ge junction together with the tapered etching profile ensured a well separation of metal gate and source metal contact (purple marked step in Fig. 7.3). A forming gas anneal is performed at 300 °C for 10 min.

The following steps served as source and drain contact formation. The bottom drain contact is created by EBL and ebeam evaporation of Ni/Ti/Pd/Au. Then the polymer *Benzocyclobuten* (BCB) is used to planarize and passivate the whole structure. Afterwards BCB was etched back with CF_4-based RIE to uncover the top Mo contact and to define a top contact pad with EBL and Ti/Pd/Au lift-off. Finally remnant BCB was removed to lay bare the bottom drain contact.

A high resolution *Scanning TEM* (STEM) cross-section of a TFET fabricated in this manner is depicted in Fig. 7.4 showing high material quality at the $Ge_{0.93}Sn_{0.07}/Ge$ tunneling junction and a smooth high-κ/Ge-channel interface.

7.3. Electrical Characterization and Modeling

Well behaving I_{DS}-V_G characteristics are obtained featuring switching over four orders of magnitude with an on-current of 2.4 µA/µm at $V_{Gov} = -2\,V$ and $V_{DS} = -0.5\,V$ as shown in Fig. 7.5(a). At $V_{Gov} = V_{DS} = -0.5\,V$ a drain current of $I_{DS} = 0.012\,\mu A/\mu m$ was achieved. V_{Gov} denotes the gate overdrive with respect to the minimum in drain current defined as I_{off}. The output (I_{DS}-V_{DS}) characteristic plotted in Fig. 7.5(b) feature a slight super-linear increase with V_{DS}. Towards positive V_{DS} the I_{DS}-V_{DS} characteristics are diode like with minor gate control, while the *p-i-n* structure is forward biased. This asymmetry is a characteristic of TFETs as unidirectional device and thereby suggests TFET operation. A minimum substhreshold swing of $SS_{min} = 215\,mV/dec$ at $V_{DS} = -0.5\,V$ was obtained at room temperature. Even though a $SS < 60\,mV/dec$ was not achieved this is the lowest reported SS for the novel GeSn material system. Table 7.1 demonstrates the superior performance of this device in terms of I_{On}/I_{Off} ratio and SS_{min} compared to other GeSn *p*TFETs. Significant improvements are expected for

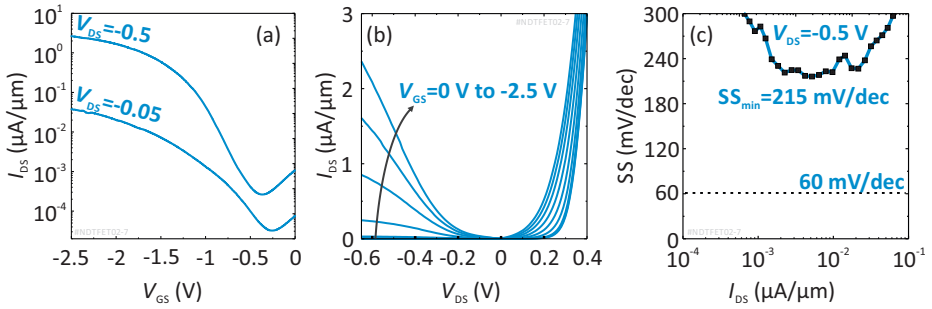


Figure 7.5.: *Room temperature characteristics of a* $Ge_{0.93}Sn_{0.07}$*/Ge-pTFET: (a)* I_{DS}-V_{GS}*, (b)* I_{DS}-V_{DS}*, (c)* SS-I_{DS}*.*

Table 7.1.: *Benchmarking of* SS_{min} *and* I_{On}/I_{Off} *ratio of GeSn pTFETs.*

Reference	SS_{min} (mV/dec)	I_{On}/I_{Off}	V_{DS} (V)
[36] $Ge_{0.96}Sn_{0.04}$	1100	$1.1 \cdot 10^1$	−0.5
[36] $Ge_{0.92}Sn_{0.08}$	1400	$1.1 \cdot 10^1$	−0.5
[35] $Ge_{0.92}Sn_{0.08}$	310	$5.7 \cdot 10^1$	−0.5
[23] $Ge_{0.958}Sn_{0.042}$	390	$1.8 \cdot 10^2$	−0.3
This work $Ge_{0.93}Sn_{0.07}$	215	$9.2 \cdot 10^3$	−0.5

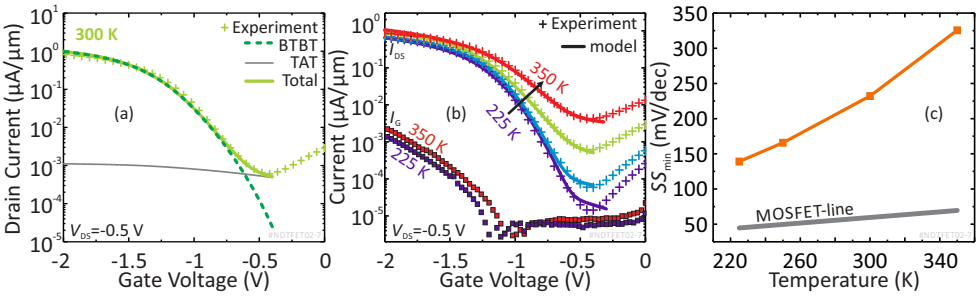


Figure 7.6.: *Electrical characterization at different temperatures and theoretical modeling: (a) Current breakdown in components from BTBT and TAT at room temperature. (b) temperature dependence, (c) $SS_{\min}$ vs. temperature.*

better material and interface quality suggested by the enormous progress in Ge gate stack technology [113].

In order to gain further insights in the different processes contributing to electrical transport and to identify the mechanism hampering sub-60 mV/dec operation, temperature-dependent IV measurements were performed in conjunction with modeling. To that end the compact model developed by R.N. Sajjad from MIT as described in SECTION 7.1, was utilized [202][2].

The temperature-dependent transfer (I_{DS}-V_{GS}) characteristics are depicted in Fig. 7.6(b). For negative bias the pTFET is in the on-state. Here BTBT prevails and shows only minimal temperature dependence. On the contrary, the off-state and low bias regime is strongly affected by changes in the temperature pointing towards significant contribution from thermally activated processes such as SRH and TAT. This is also visible in the temperature dependence of the minimal substhreshold swing $SS_{\min}$ in Fig. 7.6(c) exhibiting a stronger and nonlinear temperature dependence as the theoretical thermionic MOSFET limit. This is a typical sign for a TAT-limited SS [*cf.* Eq. 7.4] and is also reported in literature [227]. Gate leakage I_G, also displayed in Fig. 7.6(b) only becomes relevant for the lowest temperature of 225 K but does not deteriorate the transfer characteristics at higher temperatures.

Fitting of temperature-dependent I_{DS}-V_G characteristics occurred according the following procedure:

Material input parameters such as effective masses and bandgap were calculated with

[2] I gratefully acknowledge Redwan N. Sajjad for support with modeling of the TFET curves.

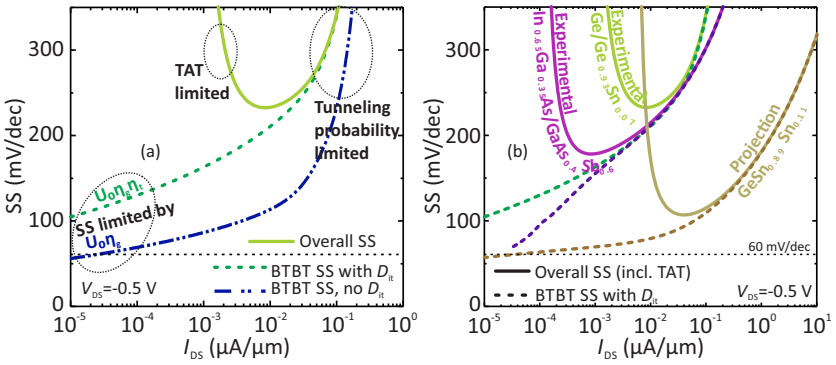


Figure 7.7.: *SS vs.* I_{DS}*: (a) Breakdown of the overall (experimental) SS into contributions from TAT and gate control reduction due to interface traps. (b) Experimental Ge/GeSn heterojunction pTFET data compared to experimental III-V pTFET data and projected GeSn pTFET data with higher Sn content assuming* $D_{\mathrm{t}} = 1 \cdot 10^{13}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$.

DFT and $\boldsymbol{k} \cdot \boldsymbol{p}$ theory to compute the $\mathcal{A}$ and $\mathcal{B}$ tunneling parameters. In the fitting procedure first the TAT contribution, defining the off-current was modeled at different temperatures [Fig. 7.6(a,b)]. It is described by equation 7.4 where $d_{\mathrm{gen}} = 1\,\mathrm{nm}$ and $\sigma_{\mathrm{t}} = 5 \cdot 10^{-17}\,\mathrm{m}^2$ are assumed, stemming from numerical simulations [142]. The width of the energy range that the electrons can tunnel to ΔE was varied between $E_{\mathrm{G}}/4$ and $E_{\mathrm{G}}/2$ to fit the slope of the V_{G}-I_{TAT} curve. The remaining key fit-parameter was the trap density D_{t} to define the absolute TAT level, while assuming midgap trap levels. A trap density of $D_{\mathrm{t}} = 5 \cdot 10^{13}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ yielded best agreement with the experimental data at all temperatures. The SS is essentially defined by the Urbach tail parameter U_0 and the gate efficiency η. A choice of $U_0 = 25\,\mathrm{meV}$ and $\eta_t = 0.65$, $\eta_g = 0.42$ was found to fit the SS best at different temperatures. Finally the on-current is defined by the electrostatics implicated in $\psi_{\mathrm{S}}(V_{\mathrm{G}}, V_{\mathrm{D}})$ and $\psi_{\mathrm{S0}}(V_{\mathrm{D}})$. A breakdown of the I_{DS}-V_{G} curve in the contributions from TAT and BTBT is shown in Fig. 7.6(a) and demonstrates that TAT masks the steepest part of the curve in the low bias regime.

In Fig. 7.7(a) The SS-I_{DS} plot is separated into contributions from various physical mechanisms which allows to identify the limiting factors of the overall SS in different current regimes. Without TAT one yields the BTBT characteristics compromised by the intrinsic band edge steepness (U_0) and the limited gate efficiency due to traps ($\eta_t = 0.65$) and the relatively thick body ($\eta_g = 0.5$) (green dash line). Finally assuming the absence

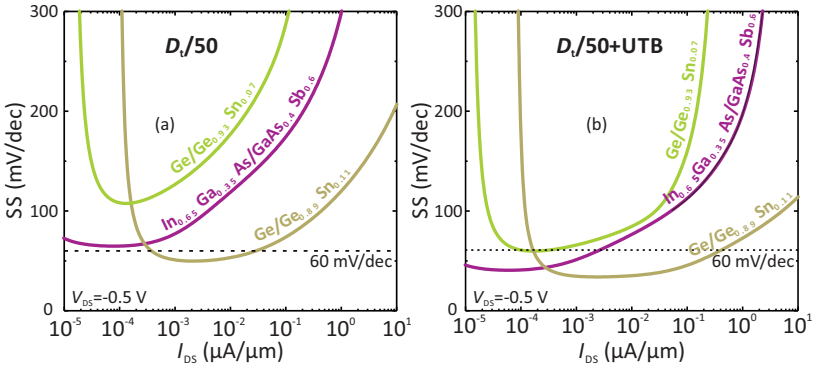


Figure 7.8.: *Projected SS-I_{DS} characteristics for (a) reduced D_t and (b) reduced D_t plus ultra thin body geometry.*

of any traps degrading the gate control ($\eta_t = 1$) yields sub 60 mV/dec operation, though at very low I_{DS} with $I_{60} = 28\,pA/\mu m$. The I_{60} current is defined as the drain-source current at the transition from sub- to super $SS = 60\,mV/dec$ operation [228].

Next, in Fig. 7.7(b) the experimental SS-I_{DS} data of the $Ge/Ge_{0.93}Sn_{0.07}$ pTFET is compared to experimental results from III-V $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ pTFETs fabricated in the same device geometry and with projected data for the $Ge_{0.89}Sn_{0.11}$ homo structure from CHAPTER 6.3, both with $D_{it} = 1 \cdot 10^{13}\,cm^{-2}eV^{-1}$. Thanks to the higher Sn content the projected $Ge_{0.89}Sn_{0.11}$ pTFET would achieve higher BTBT currents and lower SS than both the $Ge/Ge_{0.93}Sn_{0.07}$ and the $In_{0.65}Ga_{0.35}As/GaAs_{0.4}$ $Sb_{0.6}$ heterojunction devices. It should be noted that this comparison is made on the base of experimentally available GeSn p-i-n structures. Following the TFET design considerations from SECTION 7.1 one would expect even better switching characteristics for a heterojunction design with increased Sn content.

Finally the following changes are made in the model: First the total trap density is assumed to be $\times 50$ lower compared to the current status, motivated by the enormous improvements achieved with Ge gate stack technology with $D_{it} < 1 \cdot 10^{11}\,cm^{-2}eV^{-1}$ [113] and supposed improvements in GeSn material quality. As a consequence the gate efficiency η_t due to traps approaches unity and the projected SS-I_{DS} curve in Fig. 7.8(a) shows improved characteristics with sub 60 mV/dec operation for the 11 % Sn homojunction. As a second step an ultra thin body (5 nm) geometry is assumed [Fig. 7.8(b)]. In this case the geometric gate efficiency η_g becomes unity as well and the projected 11 %

Sn homojunction would achieve more than three orders of magnitude sub-60 mV/dec switching with an I_{60} of 0.4 µA/µm.

7.4. Summary

Vertical Ge/$Ge_{0.93}Sn_{0.07}$ heterojunction *p*TFETs were fabricated and comprehensively studied. On-currents of 2.4 µA/µm and 12 nA/µm were achieved with $V_{DS} = -0.5$ V at $V_{Gov} = -2$ V and $V_{Gov} = -0.5$ V, respectively. Even if sub-60 mV/dec operation was not achieved, with SS_{min} of 215 mV/dec and an on-off-ratio of $9.2 \cdot 10^3$ at $V_{DS} = -0.5$ V the presented *p*TFET feature superior characteristics in terms of on-off-current ratio and minimum substhreshold swing compared to other experimental reports on the novel GeSn material system. A detailed temperature-dependent electrical characterization supported by modeling identified the dominant contributions to the carrier transport as BTBT and TAT. In the present devices TAT and reduced gate efficiency hampered sub-60 mV/dec operation. However, based on the experimental data, projections for improved channel-source and channel-gate interfaces (*i.e.* reduced TAT), increased Sn content and improved electrostatics revealed competitive performance with sub-60 mV/dec switching over more than three orders of magnitude.

8 | Hall Measurements on GeSn

In CHAPTER 1 the integration of GeSn in electronics was motivated by its potentially increased carrier mobility supported by mobility calculations in CHAPTER 2.1. Indeed channel mobility enhancement in GeSn MOSFETs was experimentally demonstrated by several groups [33, 117, 229]. However, the bulk mobility as fundamental material property is always higher than the channel mobility and there were no published data on bulk mobility measurements of direct bandgap GeSn. This is of particular interest since especially the Γ-valley electron mobility is expected to be significantly higher than the L-valley electron mobility leading to projected mobilities comparable to those of III-V materials.

In this chapter bulk electron and hole mobilities of GeSn are determined by Hall measurements for various temperatures and compared to theoretical calculations. Higher electron mobilities than the classical Si and Ge group IV semiconductors are demonstrated at a given doping concentration.

8.1. (Magneto)transport in Semiconductors

Classical electronic transport in macroscopic semiconductors (bulk) without any quantum effects or corrections can be described by the Drude-model, named after Paul Drude who in 1900 published his "electron theory of metals" [230]. Even without applied electric field at finite temperatures electrons within a metal or the conduction band of a semiconductor are moving randomly, though without creating a net current flow. Once an electric field $\boldsymbol{\mathcal{E}}$ is applied, electrons get accelerated in direction of the force $q\boldsymbol{\mathcal{E}}$ until they scatter from an impurity or a (quasi) particle such as a phonon and lose their momentum or change their direction of travel. Considering an average momentum relaxation time τ_m and an average drift velocity $\boldsymbol{v_D}$ one yields the momentum change (force)

$$\frac{m^*\boldsymbol{v_D}}{\tau_m} = q\boldsymbol{\mathcal{E}} \;\Rightarrow\; \boldsymbol{v_D} = \underbrace{\frac{q\tau_\mathrm{m}}{m^*}}_{:=\mu}\boldsymbol{\mathcal{E}}\,, \tag{8.1}$$

leading to the definition of the electron mobility μ [cm^2/Vs]. Assuming an electron density[1] n one yields the net current density following Ohms law[2]

$$\boldsymbol{J} = qn\boldsymbol{v_D} = qn\mu\boldsymbol{\mathcal{E}} = \sigma_0\boldsymbol{\mathcal{E}}\,. \tag{8.2}$$

$\sigma_0 = qn\mu$ is defined as the (Drude) conductivity.
In a real semiconductor the overall mobility is limited by several scattering mechanisms. If these mechanisms can be seen as independent the overall scattering time can be calculated by inversely adding the scattering times for the individual processes according to Matthiessen's rule [231]:

$$\frac{1}{\tau_\mathrm{eff}} = \sum_i \frac{1}{\tau_i} \;\Rightarrow \frac{1}{\mu_\mathrm{eff}} = \sum_i \frac{1}{\mu_i}\,. \tag{8.3}$$

Typical scattering mechanisms are: i) *Phonon scattering*, ii) *surface roughness*, iii) *random alloy scattering* due to potential fluctuations induced by the randomly distributed Sn-atoms in the GeSn alloy, iv) *impurity scattering*, v) *inter- and intra-band scattering*. In bulk materials at room temperature primarily phonon scattering is the limiting factor.

[1] The approach for p-type semiconductors is analogous.
[2] If both p and n-type conduction are relevant σ_0 is $q(\mu_n n + \mu_p p)$ with electron and hole mobilities μ_n and μ_p, respectively.

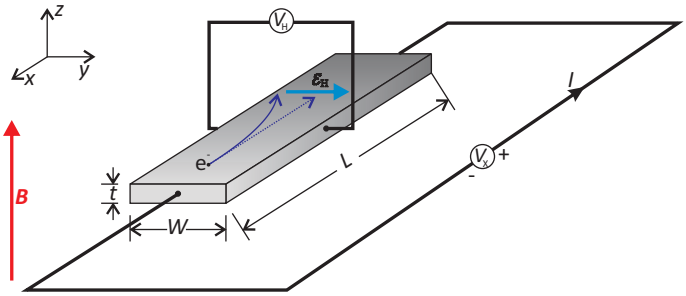


Figure 8.1.: *Illustration of the classical Hall effect. In the presence of an out of plane magnetic field, electrons contained in a net current flow are deflected as a consequence of the Lorentz force and give rise to the Hall voltage V_H perpendicular to the current flow.*

At low temperature, the mobility is limited by scattering from impurities/defects.

A well known method for measuring carrier concentration and mobility are Hall measurements based on the effect of a magnetic field on electric transport first described by Edwin H. Hall in 1879 [232]. The Hall effect is schematically illustrated in Fig. 8.1. Assuming a current flowing in x-direction and an out of plane applied magnetic field $\boldsymbol{B} = B\boldsymbol{e_z}$, the Lorentz force deflects the electrons to the side and thereby builds up an electric field $\boldsymbol{\mathcal{E}_H} = \mathcal{E}_H\boldsymbol{e_y}$ in y direction and a corresponding voltage V_H called Hall voltage. $\boldsymbol{e_x}$,$\boldsymbol{e_y}$,$\boldsymbol{e_z}$ are the unity vectors in x,y,z direction, respectively. Assuming an n-type carrier density n and a thickness t the Hall voltage is

$$V_H = -\frac{r_H}{qn}\frac{BI}{t} = A_H\frac{BI}{t}\,, \tag{8.4}$$

where r_H with $1 \leq r_H \leq 2$ is a correction factor depending on the scattering mechanism called Hall factor. A_H is denoted as Hall coefficient. For a p-type semiconductor it is analogous and V_H changes sign:

$$V_H = \frac{r_H}{qp}\frac{BI}{t} = A_H\frac{BI}{t}\,. \tag{8.5}$$

Following equation 8.4 or 8.5 measuring the Hall voltage for a given magnetic field and applied current one can calculate the carrier concentration. By additionally measuring the conductivity σ_0 (for example with the Van der Pauw technique) one can calculate

the mobility from $\sigma_0 = qn\mu$.

$$r_{\mathrm{H}}\mu = \sigma_0 \frac{V_{\mathrm{H}}}{BI} \tag{8.6}$$

Since the Hall factor is not easy to access, for simplicity the Hall mobility $\mu_{\mathrm{H}} := r_{\mathrm{H}}\mu$ is defined. In the following the term "mobility" always denotes the "Hall mobility", if not otherwise specified.

If both types of carriers, or generally, two conducting channels contribute significantly to electric transport, the situation is more complex and the effective (measured) Hall carrier concentration and mobility are

$$n_{\mathrm{eff}} = \frac{(n_1\mu_1 + n_2\mu_2)^2}{n_1\mu_1^2 + n_2\mu_2^2} \text{ and } \mu_{\mathrm{eff}} = \frac{n_1\mu_1^2 + n_2\mu_2^2}{n_1\mu_1 + n_2\mu_2}\,, \tag{8.7}$$

for fields with $\mu B \ll 1$ [233]. This would impede a direct mobility extraction from the Hall voltage. For such multichannel systems, magnetic field-dependent measurements in conjunction with modeling can yield the mobility of each conducting channel and is known under the term *Quantitative Mobility Spectrum Analysis* (QMSA) [234], but would be beyond the scope of this work.

8.2. Fabrication of GeSn on Insulator - GSOI

In order to completely exclude any contribution from the substrate to the Hall measurements the natural choice would be to physically remove the (GeVS) substrate below the GeSn. Thanks to the extremely high etching selectivity achieved with CF_4 dry etching presented in CHAPTER 3.2, indeed a process was developed to selectively remove the GeVS and thereby realize Van der Pauw structures as *GeSn on Insulator* (GSOI). To that end, GeSn epilayers with relatively large thickness $> 400\,\mathrm{nm}$ and high Sn content $> 8\,\%$ Sn are utilized. First squares of the size of several µm are defined by *Electron Beam Lithography* (EBL) and vertically etched into the underlying GeVS by use of an anisotropic unselective Cl_2/Ar dry etch [Fig. 8.2(b)]. The GeVS is then selectively etched by use of the isotropic CF_4 process introduced in CHAPTER 3.2. In a first step the undercut is chosen such that a thin Ge post in the center of the structure remains [Fig. 8.2(c)]. As a bottom isolation layer to the Si-substrate, subsequently SiO_2 is deposited with electron beam evaporation. The directionality of the molecular SiO_2 beam is utilized as follows. The sample is mounted in the evaporation tool by use of a

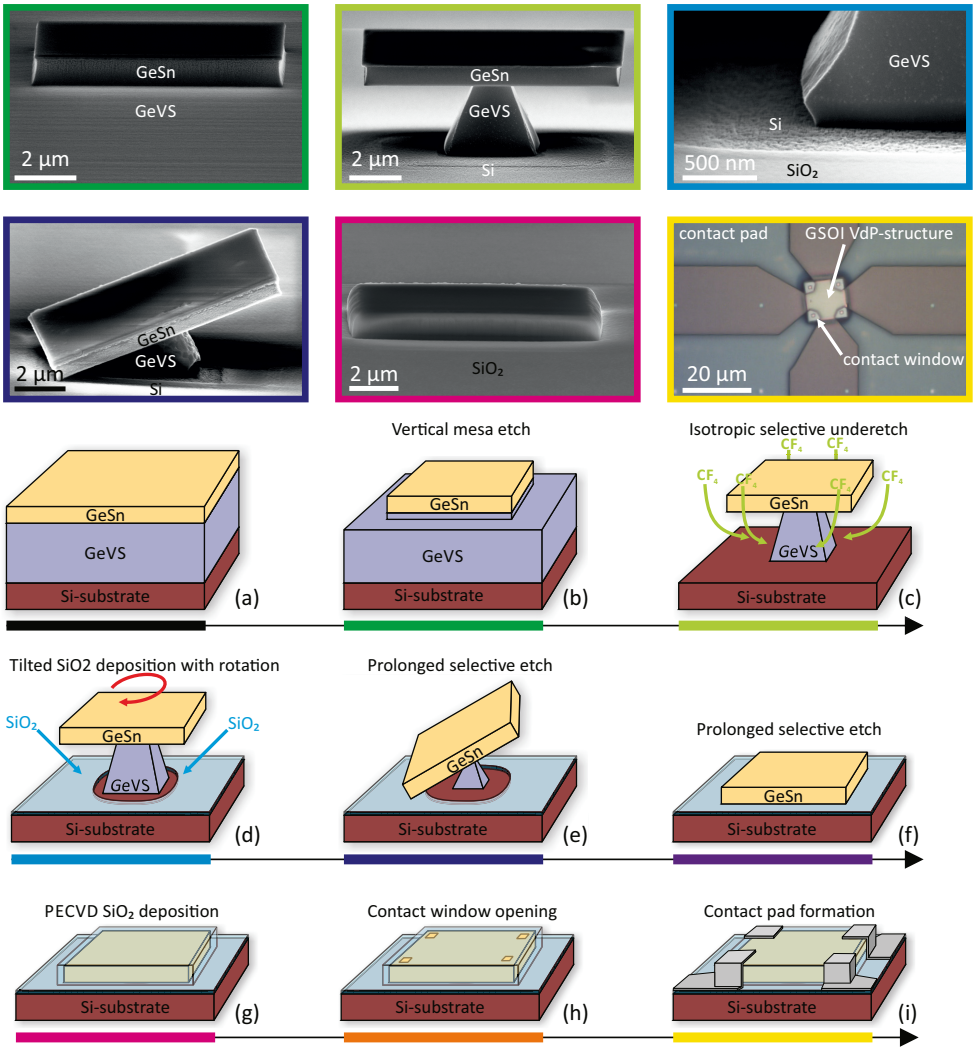


Figure 8.2.: *Key steps for GSOI fabrication. SEM images above the illustrated process steps are framed with according colors.*

special apparatus that allows to tilt it by 45° with respect to the molecular beam and to rotate it during evaporation [Fig. 8.2(d)]. As a consequence, the SiO_2 is also deposited in a region below the GeSn structure. However, the geometric dimensions are chosen such that the SiO_2 does not cover the remaining Ge-pillar. This Ge-pillar is then etched in the next step by prolonged exposure to the CF_4 plasma and the GeSn structure is placed down on the SiO_2/Si substrate [Fig. 8.2(e,f)]. Encapsulation and fixing of the GeSn structure on the substrate is realized by PECVD of SiO_2. In the following steps, the GeSn squares are located under SEM and contact EBL layouts are created according to the individual position of the structures [Fig. 8.2(h,i)]. Contact windows are etched with CHF_3 dry etching and contact pads are created by a Ni/Al lift-off process.

8.3. Hall Measurements

Hall measurements were performed on both bulk GeSn and GSOI for *p* and *n*-type epilayers. As *p*-type layers, as-grown wafers were used since undoped GeSn is intrinsically *p*-type. To achieve *n*-type GeSn, *in-situ* doping with phosphorous was utilized during growth. The measurements were performed in a LakeShore 8400 HMS Hall measurement system covering a temperature range of 10 to 350 K and a magnetic field up to 1.6 T, while 100 mT were used for a standard Hall measurement.
Carrier concentration and mobility of several *p*-type Ge(Sn) samples with 0, 8.5, 10 and 12.5 % Sn are depicted in Fig. 8.3(a-c). The respective layer thicknesses are 2500, 768, 835 and 414 nm. Even if these layers are undoped a systematic increase of the *p*-type carrier density with Sn content is evidenced. The *p*-type carriers in un-doped Ge(Sn) are most probably due to defects, such as vacancies and/or dislocations [121], while the vacancy density increases with Sn content as indicated by positron annhilation measurements for low Sn contents [235]. During growth the Sn content is primary controlled by the growth temperature. To achieve high Sn contents, low growth temperatures are needed which promotes the formation of point defects as consequence of a reduced adatom surface mobility. As both GeSn epilayer and the underlying GeVS are *p*-type one might suspect significant contribution of the GeVS to the GeSn measurements. However, owing to the significantly lower carrier density in GeVS especially at lower temperatures, a relevant contribution can be excluded. This was confirmed by subtracting the GeVS contribution from the GeSn measurements by use of equation 8.7. From the saturation range in Fig. 8.3(a) at moderate temperatures the background

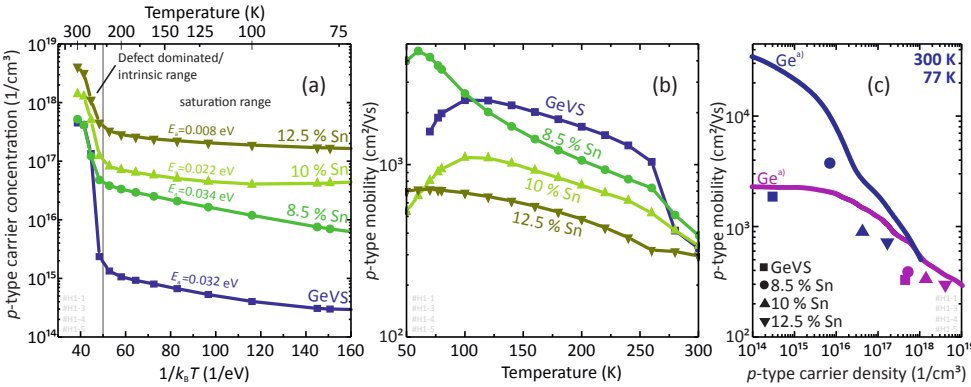


Figure 8.3.: *Hall measurements on Ge(Sn). Undoped GeSn is p-type. (a) carrier concentration vs. temperature, (b) hole mobility vs. temperature, (c) hole mobility vs. carrier density.* [a] *Comparative Ge-data from Golikova et al. [236].*

doping density can be estimated. It increases from $1 \cdot 10^{15}\,\mathrm{cm}^{-3}$ for GeVS to approx. $3 \cdot 10^{17}\,\mathrm{cm}^{-3}$ for $Ge_{0.875}Sn_{0.125}$ and is in line with ECV measurements by von den Driesch [52]. Activation energies obtained in the saturation range confirm the presence of shallow acceptor levels in compliance with Takeuchi *et al.*, who identified single- & multivacancies as well as dislocations in that energy range [121]. A reduction of the *p*-type background doping will be an important challenge for the successful implementation of GeSn in electronic devices. A background carrier density in the mid $10^{17}\,\mathrm{cm}^{-3}$ range as for high Sn content GeSn would create high junction leakage and especially hamper the realization of low *n*-type doping since the *p*-type background level needs to be overcompensated.

In the following the carrier mobility is derived from the Hall measurements. The hole mobility in *p*-type GeSn is lower compared to GeVS. Only the 8.5 % Sn sample shows higher hole mobilities at low temperatures. This opposes mobility calculations that yield increased hole mobilities in both compressive and tensile strained GeSn. The strain-induced splitting of the HH- and LH-bands reduces intervalley scattering leading to enhanced projected mobilities. Furthermore, the compressive strain present in the partially relaxed layers reduces the effective masses compared to the relaxed case. However, one should consider the larger background doping for high Sn contents induces stronger impurity scattering and thereby degrades the *p*-GeSn mobility. To allow a comparison with literature data the mobility is considered at a certain carrier concentration.

This is done in Fig. 8.3(c) showing the measured hole mobility *vs.* hole carrier density in comparison to literature data for bulk Ge wafers. While at room temperature the measured mobilities are comparable to those in bulk Ge wafers, at liquid nitrogen temperature the hole mobility in bulk Ge is significantly higher. At room temperature the mobility is primary limited by phonon scattering which is comparable for GeSn, GeVS and bulk Ge. On the contrary at lower temperatures impurity and defect scattering is the limiting mechanism which is stronger in epitaxially grown GeSn compared to bulk Ge wafers.

The highest mobilities are projected for *n*-type GeSn with Sn contents beyond the indirect-to-direct bandgap transition utilizing small Γ-electron masses. However, GeSn, grown on GeVS is compressively strained and, as discussed in CHAPTER 1, compressive strain counteracts the effect of Sn incorporation and thereby reduces the Γ-L-valley difference. The growth of thick GeSn layers helps to induce partial strain relaxation and thereby to increase the directness of the GeSn. Here *in-situ* phosphorous doped GeSn with 12.5 % Sn with a thickness of 550 nm is used, which has a remaining compressive strain of −0.43 % corresponding to a relaxation degree of 78 % and results in a directness of approx. 55 meV. However, in virtue of its higher effective mass the L-valley DOS is significantly higher than the Γ-valley DOS. As a consequence at room temperature, despite the directness of the material, band structure calculations reveal only approx. 11 % of the total conduction band electrons residing in the Γ-valley while the rest remains in the lower mobility featuring L-valley. Furthermore for low Γ-L offsets strong intervalley scattering additionally limits the overall electron mobility. Further strain relaxation is needed to increase the Γ-L-valley offset and thereby to increase the Γ-valley population. Thus fully relaxed GSOI is fabricated from *n*-doped GeSn with approx. 12.5 % Sn. The strain relaxation increases the directness from 55 meV to 89 meV and thereby increases the Γ-population at 300 K from 11 % to 24 %.

Hall measurements on *n*-GeSn epilayers are depicted in Fig. 8.4(a-c) for two different doping levels of which the higher one was also used for GSOI fabrication. The carrier concentration shows only minimal temperature dependence pointing towards GeSn being degenerate already for doping in the mid $10^{17}\,\mathrm{cm}^{-3}$ range. The advantage of the GSOI is evident when measuring the electron mobility for epilayer GeSn and GSOI as shown in Fig. 8.4(b). Thanks to the higher Γ-valley occupation the GSOI shows a significantly higher electron mobility at room temperature. At 300 K for GSOI a mobility as high as

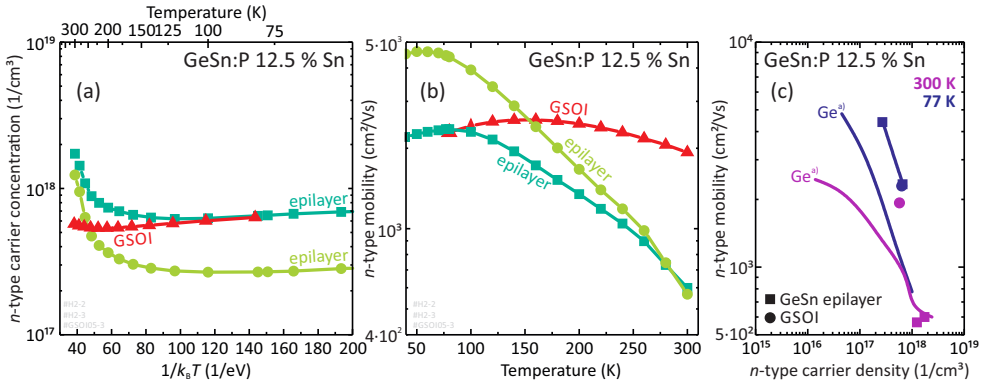


Figure 8.4.: *Hall measurements on in-situ n-doped* $Ge_{0.875}Sn_{0.125}$ *for bulk and GSOI: (a) n-type carrier concentration vs. temperature, (b) electron mobility vs. temperature, (c) electron mobility vs. carrier density.* [a)] *Ge-data for comparison from Fistul et al. [237].*

1930 cm^2/Vs is observed compared to 600 cm^2/Vs for the corresponding GeSn epilayer and Ge at the respective carrier density.

At lower temperatures the mobility difference between GSOI and GeSn epilayer vanishes. In parallel for both cases the electrons condensate in the Γ-valley as lowest conduction band minimum, leading to a nearly 100 % Γ-valley occupancy for both GeSn epilayer and GSOI at 77 K. At low temperatures the mobility for both cases is limited by impurity scattering which does not differ for GSOI and bulk GeSn. The highest electron mobility was obtained with a slightly lower doped GeSn epilayer which in turn features less impurity scattering. At 50 K this sample has a peak mobility of 4600 cm^2/Vs which is significantly higher than for bulk Ge at the respective carrier concentration of approx. $3 \cdot 10^{17}$ cm^{-3}. This is demonstrated in Fig. 8.4(c) showing the electron mobility *vs.* carrier density at room temperature and 77 K for GeSn in comparison to literature data for bulk Ge wafers. At room temperature the electron mobility of the GeSn epilayer closely matches with those of bulk Ge. This makes sense considering the dominant L-valley population for both GeSn and bulk Ge at 300 K. On the contrary the GSOI enjoys an increased Γ-valley population and shows a twofold mobility enhancement at 300 K compared to bulk Ge. At 77 K the lower doped GeSn epilayer even shows a 2.3× electron mobility enhancement compared to bulk Ge.

It should be noted that even if the observed GeSn electron mobilities are significantly higher than those of bulk Ge at low temperatures, they are still much lower than the

theoretically predicted mobilities based on effective mass and band structure calculations discussed in CHAPTER 2.1. At room temperature where phonon scattering is the limiting factor, calculated mobility for unstrained GeSn and the measured GSOI mobility agree within an order of magnitude ($\mu_{\text{calc.}} = 6000\,\text{cm}^2/\text{Vs}$ *cf.* $\mu_{\text{GSOI}} = 1930\,\text{cm}^2/\text{Vs}$). However, at 77 K theoretically one would expect III-V comparable mobilities $> 2 \cdot 10^5\,\text{cm}^2/\text{Vs}$ in this doping range compared to experimentally observed $4458\,\text{cm}^2/\text{Vs}$ for GeSn. This discrepancy can be explained by the fact that the mobility calculations did not take into account scattering with defects, which at low temperatures is the limiting factor. Especially at the growth interface between *n*-GeSn and GeVS one expects a significant concentration of both, point defects and dislocations, as described by von den Driesch *et al.* [50]. Considering scattering with point defects in the simulations can be realized by modeling scattering on a spherical potential [238]. Reported electron binding energies for that process are 2 meV for Si and 0.5 meV for Ge [238]. As no values for GeSn are known, 1 meV was assumed. This estimate would yield a point defect density of approx. $1 \cdot 10^{17}\,\text{cm}^{-3}$ to match the mobilities of experiment and simulation at 77 K. This value seems realistic considering the observed defect related background doping in the $10^{17}\,\text{cm}^{-3}$-range. Another effect that might limit the observed mobilities is the contribution of minority carriers (holes). However, field-dependent Hall measurements did not indicate the presence of a relevant second conducting channel. In this regard, QMSA measurements might provide further insight in future studies.
In order to achieve III-V competitive electron mobilities, increasing material quality and reducing the defect density is a key challenge. Furthermore the possibility to achieve low active *n*-type doping $< 10^{17}\,\text{cm}^{-3}$ is needed which is connected to the reduction of the *p*-type background doping.

8.4. Summary

Hall measurements were performed on both *p*- and *n*-type GeSn. At room temperature Ge-comparable hole mobilities were achieved at respective carrier densities. Measurements on undoped (*p*-type) GeSn revealed a relatively high background doping concentration in the mid $10^{16}\,\text{cm}^{-3}$ to mid $10^{17}\,\text{cm}^{-3}$ range that increases with Sn content. Shallow acceptor levels that correlate with crystal defects could be identified from the temperature dependence of the carrier density.
Regarding *n*-type GeSn, higher electron mobilities were achieved compared to bulk Ge

both at 300 K and at low temperatures, which thereby mark the highest bulk electron mobilities observed in a group IV semiconductor at the respective doping levels so far. The advantage of increased directness of the GeSn alloy due to strain relaxation was demonstrated by the realization of fully relaxed GeSn on insulator and lead to increased room temperature mobility close to $2000\,\mathrm{cm}^2/\mathrm{Vs}$ at a carrier density of approx. $5.6 \cdot 10^{17}\,\mathrm{cm}^{-3}$. However, the derived peak mobility of $4600\,\mathrm{cm}^2/\mathrm{Vs}$ observed at a sample with a slightly lower carrier density of approx. $3 \cdot 10^{17}\,\mathrm{cm}^{-3}$ was limited by scattering with defects at low temperatures. Thus improvement of material quality and reduction of the *p*-type background doping will be the key challenges to achieve lower doped *n*-type GeSn with III-V competitive electron mobilities as well as high mobility *p*-type GeSn, both at room- and at cryogenic temperatures. Furthermore, reduced background doping is important to improve junction leakage in GeSn-based FET-devices. Trapping of dislocations in heterostructures and passivation of defects with *in-situ* carbon incorporation might be promising approaches for further growth optimization.

9 | Conclusion and Outlook

A comprehensive work on the physical characterization of GeSn semiconductor alloys for electronic application was provided from fundamental properties to advanced nanoelectronic devices. High Sn content direct bandgap GeSn alloys are only available since a few years. That is, the novelty of the GeSn material system allowed the initial study of material properties and electronic transport like Hall mobility, carrier concentration, Schottky barriers, high-κ interfaces, band to band tunneling and their dependencies on Sn content. On the other hand all necessary steps for GeSn device fabrication needed to be adapted, validated or redeveloped accordingly taking account of the reduced chemical and thermal stability of GeSn as compared to Si. The experimental demonstration of TFETs shows that these novel alloys can be technologically realized allowing the monolithical integration of direct bandgap group IV electronic devices on the Si platform. The individual building blocks for GeSn based electronic devices were studied consecutively.

First the GeSn surface was physically characterized *via* XPS in order to monitor the effectiveness of GeSn pre-high-κ cleaning and to identify the physical mechanism of selective Ge-*vs.*-GeSn etching. The removal of $GeSnO_x$ native oxide by use of a HF:HCl-last process, was validated. A highly selective dry etching process was developed utilizing CF_4 in a ICP process with a Farraday cage. The selective removal of Ge towards GeSn was ascribed to the formation of a solid Sn-rich $GeSnO_xF_y$ passivation layer as identified *via* XPS.

In terms of contact engineering very low hole Schottky barrier heights $< 0.15\,\mathrm{eV}$ were obtained with NiGeSn on p-type GeSn identifying NiGeSn as ideal metal-semiconductor alloy for low resistance contacts. The hole Schottky barrier height decreased with Sn content. Due a strong tunneling component low Schottky barrier heights could be also obtained for electrons in high *in-situ* n-doped GeSn. Dopant segregation was stud-

ied as a measure to tune the Schottky barrier height. The effective Schottky barrier height modification was evidenced by electrical measurements for B and As doping. A clear concentration peak was observed for these dopants in corresponding time-of-flight secondary ion mass spectroscopy measurements.

As essential element of a field-effect transistor the high-κ/GeSn interface was studied in detail. Interface trap densities in the $10^{12}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$-range were evidenced on HfO_2/GeSn stacks. High oxide capacitances of approx. $3\,\mu\mathrm{F/cm}^2$ were achieved while maintaining low gate leakage. The low bandgap of GeSn induced a strongly enhanced minority carrier response that increased with Sn content. The enhanced minority carrier response could be clearly correlated with the Sn induced bandgap shrinkage allowing easier carrier generation. Effects of the bandstructure on the capacitance-voltage characteristics were discussed.

Band-to-band tunneling was studied in (Ge)Sn *p*-*i*-*n* diodes. Negative differential resistance with peak-to-valley current ratios of 2.3 was observed at low temperatures as clear experimental sign of band-to-band tunneling. Direct tunneling was evidenced to provide the dominant contribution to the overall tunneling current demonstrating the advantage of the low and direct bandgap of high Sn content GeSn. The experimental analysis of different Sn contents in conjunction with compact modeling revealed enhanced band-to-band tunneling for direct bandgap GeSn as compared to Ge or Si.

This study was complemented by the realization of GeSn/Ge vertical heterojunction *p*TFETs. A numerical model was calibrated with temperature dependent electrical measurements. The modeling allowed the identification of trap-assisted tunneling as mechanism limiting the switching slope and degrading the off-state. Based on this calibrated model projections for improved electrostatics and reduced defect densities revealed potential sub-60 mV/dec operation over more than three orders of magnitude of drain current with a maximum sub-60 mV/dec current of $0.4\,\mu\mathrm{A}/\mu\mathrm{m}$.

Finally Hall measurements were performed on both *p* and *n*-type GeSn. Undoped (unintenionally doped) GeSn is *p*-type and showed comparably high background doping concentration in the mid $10^{16}\,\mathrm{cm}^{-3}$ to mid $10^{17}\,\mathrm{cm}^{-3}$ range that increased with Sn content. At room temperature hole mobilities comparable to those of Ge were observed. According to mobility calculations high electron mobilities $> 10^5\,\mathrm{cm}^2/\mathrm{Vs}$ were expected for direct bandgap GeSn when benefiting from the low effective mass of electrons in the direct Γ-valley and reduced scattering. Indeed temperature dependent Hall measure-

ments on 12.5 % Sn *in-situ* n-doped GeSn revealed a 2.3× increased electron mobility as compared to Ge at the respective doping level. However this observed peak mobility of 4600 $\mathrm{cm}^2/\mathrm{Vs}$ at $n = 2.9 \cdot 10^{17}\,\mathrm{cm}^{-3}$ and 50 K is limited by defect scattering at low temperatures compared to the projected mobility of ideal GeSn.

In conclusion, different aspects of GeSn material properties and GeSn based electronic devices were studied in detail and demonstrated that this novel material system to certain extend merges the benefits known from direct band gap III-V materials and mature Si-technology. The reduced thermal and chemical stability of GeSn compared to Si demanded process modification and precluded the use of ion implantation to achieve high doping levels. However, *in-situ* doping during growth was demonstrated to be suitable to achieve high p- and n-type carrier densities. The remaining key challenges are the improvement of material quality along with the reduction of the p-type background doping to achieve III-V material competitive mobilities, reduce TAT in TFETs and junction leakage in MOSFETs. Defect trapping in advanced heterostructures and the incorporation of carbon are possible approaches to address these issues. Significant advancements in the high-κ/GeSn interface density are expected based on the recent progress in related Ge-technology.

Acknowledgements

In this section I would like to use the opportunity to thank everybody who supported me within the course of my PhD thesis. I am deeply grateful for this time in which my life changed significantly. I learned a lot, gathered new experiences, gained new friends and a wonderful family.

First of all I would like to thank my doctoral adviser *Prof. Dr. Siegfried Mantl* for giving me the opportunity to conduct my PhD thesis in his group at the FZ-Jülich, for the exciting topic, for all the scientific support and advises and especially for the unique possibility he enabled me to conduct a part of my research at the University of Notre Dame, IN, USA. It was a great experience and a wonderful time for me and my little family. Thank you also very much for the support and the chances to present my results on international conferences. It is not something one can take for granted! Many thanks to *Prof. Dr. Detlev Grützmacher* for giving me the opportunity to work at his institute. I would like to thank *Prof. Dr. Matthias Wuttig* for undertaking the second review. Especially I am grateful to my supervisors *Dr. Dan Buca* and *Dr. Qing-Tai Zhao* for the daily support, encouragement and scientific advises. Thank you Dan for introducing me to the scientific community, the fruitful discussions and for the great trust and freedom you offered me.

Many thanks to *Dr. Simon Richter* for introducing me into TFET physics and technology as well as into the cleanroom work. My experimental work would not have been possible in this way without the growth of excellent GeSn epilayers by *Nils von den Driesch* and *Dr. Stephan Wirths*. Thank you so much for the numerous wafers you grew for me and for introducing me in the GeSn material system. In this regard also special thanks to the remaining members of the fabulous GeSn team, *Daniela Stange*, *Denis Rainko*, *Konstantin Mertens*, *Emily Hofmann* and *Thomas Lehndorff*. I would like to thank the latter two for the support with Schottky barrier and CV measurements,

respectively. Experimental and technical support is indispensable For an experimental work as present. To that end I gratefully acknowledge the Waldschlösschen team, *Andreas Tiedemann*, *Karl-Heinz Deussen* and *Patrick Bernardy*, the implanter team, *Christian Scholtysik*, *Andre Dahmen* and *Katja Palmen*, our TEM experts *Steffi Lenk*, *Fabian Wendt* and *Lidia Kibkalo* for numerous TEM preparations and analyses, as well as the complete HNF-team. Thank you *Dr. Gregor Mussler* for XRD measurements and support with their interpretation. Thank you *Keyvan Narimani* and *Dr. Sebastian Blaeser* for support with TCAD simulations. Thanks to *Alfred Fox* and *Benjamin Bennemann* for support with low temperature and Hall measurements, respectively. Also many thanks to the members of ZEA-3; *Dr. Uwe Breuer* and *Dr. Aleksei Savenko* for countless SIMS analyses and to *Dr. Astrid Besmehn* and *Dr. Heinrich Hartmann* for XPS measurements.

Furthermore I would like to express my special thanks to *Stefan Glass*, my office colleague and friend, for both private and scientific discussions. I very much appreciated your opinion! There was always a warm and friendly atmosphere in our group. In this regard I would like to thank the not yet named present and former members of PGI9-IT *Gia Vinh Luong*, *Dr. Anna Schäfer*, *Ulli Tromm*, *Qinghua Han*, *Dr. Chang Liu*, *Dr. Linjie Liu*, *Haitao Zhang*, *Jing Zhang*, *Dr. Anran Gao*, *Felix Krämer*, *Felix Rothe*, *Dr. Lars Knoll*, *Dr. Jürgen Schubert*, *Brigitte Modolo* and *Willi Zander*.

Special thank is dedicated to our external collaborators: *Prof. Dr. Valeri V. Afanas'ev* from the KU Leuven, Belgium for detailed explanations and great support with the interpretation of CV measurements, *Prof. Dr. Zoran Ikonic* from the University of Leeds, UK for band structure and mobility calculations including comprehensive discussions and comprehensible explanations, *Dr. Redwan N. Sajjad* from the group of *Prof. Dr. Dimitri Antoniadis*, MIT, Massachusetts, USA, for TFET modeling including countless comprehensible explanations, *Prof. Dr. Thomas Schröder* and *Dr. Peter Zaumzseil* from IHP, Frankfurt (Oder) for XRD measurements, *Dr. Jean-Michel Hartmann* from CEA-LETI, Grenoble, France for supply with excellent Ge virtual substrates, *Dr. Roger Loo* and *Anurag Vohra* from IMEC, Leuven, Belgium for the supply with the GeSn/Ge TFET stack and *Dr. Wilman Tsai* from TSMC, Taiwan for the supply with Ge *p-i-n* structures.

I spent four month of my PhD time at the University of Notre Dame, IN, USA. I would like to thank all those who were involved in enabling the stay and this unforgettable

experience. First of all I am especially grateful to *Prof. Dr. Suman Datta* for hosting me and my little family, for his ambition, undaunted motivation, encouragement and guidance to make the best of something. Also I would like to thank *Debrah Gillean* for managing all the bureaucracy. Great thanks to *Dr. Nikhil Shukla*, *Matt Jerry* and *Benjamin Grisafe* for welcoming us so warmly. Thank you *Dr. Rahul Pandey*, for the efficient, fruitful collaboration and for sharing your expertise in TFET fabrication. Also I would like to thank the not jet named group members *Dr. Ram Krishna Ghosh* and *Dr. Pankaj Sharma* for their support. Thanks to *Dr. Mike Barth* and *Bruce Rayner* from Pennstate University and Kurt Lesker Company, respectively, for the support and expertise with high-κ deposition and *in-situ* ellipsometry. Also many thanks to the NDNF and NDIIF, teams in Notre Dame.

Finally I dedicate my unlimited gratitude to my family and friends. Especially I would like to thank my wife Lena Janello, my children Hannes and Theo, my parents Brigitte and Rüdiger Schulte-Braucks and my sister Kathrin, my parents in law Achim Janello and Sabine Prinz-Janello and my sister- and brother-in-law Kira Janello and Maarten Potts for their unquestioned support, patience, encouragement and belief in me.

Thank you!

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A | Series resistance Correction of CV Measurements

Nicollian and Brews proposed [128] the following series resistance correction for CV measurements

$$C_{\mathrm{c}} = \frac{(G_{\mathrm{m}}^2 + \omega^2 C_{\mathrm{m}}^2) C_{\mathrm{m}}}{a^2 + \omega^2 C_{\mathrm{m}}^2} \quad \text{and} \quad G_{\mathrm{c}} = \frac{(G_{\mathrm{m}}^2 + \omega^2 C_{\mathrm{m}}^2) a}{a^2 + \omega^2 C_{\mathrm{m}}^2} \,, \tag{A.1}$$

where

$$a = G_{\mathrm{m}} - (G_{\mathrm{m}}^2 + \omega^2 C_{\mathrm{m}}^2) R_{\mathrm{s}} \quad \text{and} \quad R_{\mathrm{s}} = \frac{G_{\mathrm{ma}}}{G_{\mathrm{ma}}^2 + \omega^2 C_{\mathrm{ma}}^2} \,.$$

C_{c} and G_{c} are the corrected capacitance and conductance, respectively and $\omega = 2\pi f$. C_{ma} and G_{ma} denote the capacitance and conductance values measured in strong accumulation (negative bias for p-type). Series resistance should be avoided as much as possible. It can be done by proper selection of moderate substrate doping and low resistance metal electrodes. Furthermore the MOSCap area should be as small as possible [138]. Note that significant gate leakage can have a similar effect on the measured capacitance and should be taken into account when characterizing thin oxides [138].

B | Process Details

Table B.1.: *Etch rates of GeSn in various etchants*

Sn content	Equipment	Recipe	Etch rate (nm/s)
GeVS	wetbench	$H_2O_2 : H_2O$ *aq.* (1:10)	1.24
GeVS	Tepla Gigabatch 360	CF_4, 40 sccm, 35 W	2.6
GeVS	Oxford PLS 100/ICP (RIEV)	CSB_Marker1, SF_6:Ar	32.2
GeVS	Oxford PLS 100/ICP (RIEV)	CSB_Mesa2, Cl_2:Ar	17.4
5.5 %	wetbench	$H_2O_2 : H_2O$ *aq.* (1:10)	0.32
5.5 %	Tepla Gigabatch 360	CF_4, 40 sccm, 35 W	0.67
5.5 %	Oxford PLS 100/ICP (RIEV)	CSB_Marker1, SF_6:Ar	6.8
5.5 %	Oxford PLS 100/ICP (RIEV)	CSB_Mesa2, Cl_2:Ar	17.1
8.5 %	wetbench	$H_2O_2 : H_2O$ *aq.* (1:10)	0.22
8.5 %	Tepla Gigabatch 360	CF_4, 40 sccm, 35 W	0.34
8.5 %	Oxford PLS 100/ICP (RIEV)	CSB_Marker1, SF_6:Ar	4.1
8.5 %	Oxford PLS 100/ICP (RIEV)	CSB_Mesa2, Cl_2:Ar	17.1
12.5 %	wetbench	$H_2O_2 : H_2O$ *aq.* (1:10)	0.14
12.5 %	Tepla Gigabatch 360	CF_4, 40 sccm, 35 W	0.0067
12.5 %	Oxford PLS 100/ICP (RIEV)	CSB_Marker1, SF_6:Ar	1.7
12.5 %	Oxford PLS 100/ICP (RIEV)	CSB_Mesa2, Cl_2:Ar	16

Table B.2.: *Selected dry etch recepies*

Equipment	Recipe	Gas (sccm)	Pressure (mBar)	RF:ICP (W)	Application
Oxford PLS 100/ICP (RIEV)	CSB_Marker1	SF_6:Ar (100:8)	0.02	100:0	Ge etch, low anisotropy
Oxford PLS 100/ICP (RIEV)	CSB_Mesa2	Cl_2:Ar (8:20)	0.005	100:1000	vertical etch, high anisotropy
Oxford PLS 100/ICP (RIEV)	CSB_TiN etch neu	Cl_2:SF_6:Ar (12:2:60)	0.008	50:700	TiN etch , selective towards high-κ
Oxford PLS 100/ICP (RIEV)	CSB_O2-ICP	O_2 (60)	0.02	5:1000	Resist removal, cleaning
Oxford PLS 100/ICP (RIEV)	CSB_CHF3	CHF_3 (30)	0.02	200:0	SiO_2 etching
Tepla Gigabatch 360	CF4_35W_40sccm	CF_4 (40)	0.132	0:35	Selective etching of Ge towards GeSn
Oerlikon ICP-RIE (@ NDNF)	CSB_Cl10	Cl_2:Ar (8:20)	0.0067	5:1000	tapered etch, high anisotropy
Oerlikon ICP-RIE (@ NDNF)	CSB_Cl2	Cl_2:Ar (8:20)	0.0067	100:1000	vertical etch, high anisotropy
Oxford PLS 100/ICP (@ NDNF)	CSB_SF6 O2	SF_6:O_2 (100:8)	0.02	100:0	Mo etch
Oxford PLS 100/ICP (@ NDNF)	CSB_CF4 O2	CF_4:O_2 (20:80)	0.120	200:0	BCB etch

C | List of Publications

Journal Paper and Books

- C. Schulte-Braucks, R. Pandey, R. N. Sajjad, M. Barth, R. K. Ghosh, B. Grisafe, P. Sharma, N. Von Den Driesch, A. Vohra, G. B. Rayner, R. Loo, S. Mantl, D. Buca, C. C. Yeh, C. H. Wu, W. Tsai, D. A. Antoniadis, and S. Datta, "Fabrication, Characterization, and Analysis of Ge/GeSn Heterojunction p-Type Tunnel Transistors," *IEEE Transactions on Electron Devices*, vol. 64, pp. 2354–2362, oct 2017
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