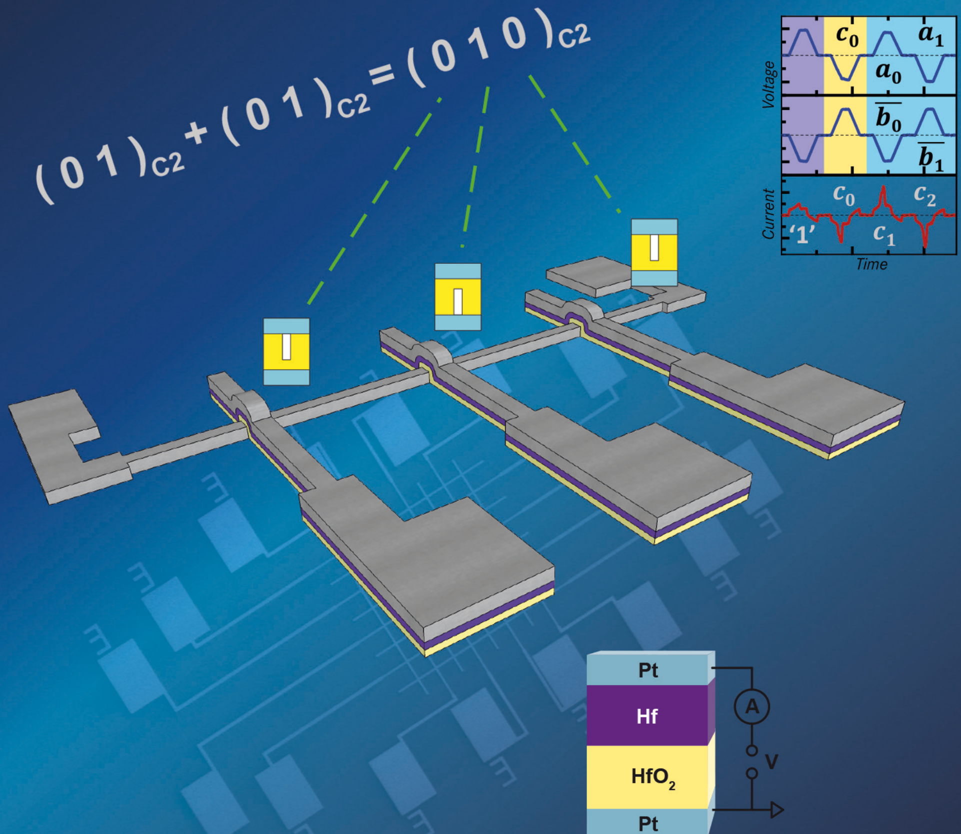
Development of ReRAM-based Devices for Logic- and Computation-in-Memory Applications

Thomas Breuer



Member of the Helmholtz Association

Information
Band / Volume 51
ISBN 978-3-95806-270-2

JÜLICH
FORSCHUNGSZENTRUM

Schriften des Forschungszentrums Jülich
Reihe Information / Information Band / Volume 51

Forschungszentrum Jülich GmbH
Peter Grünberg Institute (PGI)
Electronic Materials (PGI-7)

Development of ReRAM-based Devices for Logic- and Computation-in-Memory Applications

Thomas Breuer

Schriften des Forschungszentrums Jülich
Reihe Information / Information Band / Volume 51

ISSN 1866-1777 ISBN 978-3-95806-270-2

Bibliographic information published by the Deutsche Nationalbibliothek.
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available in the Internet at http://dnb.d-nb.de.

Publisher and Distributor:	Forschungszentrum Jülich GmbH Zentralbibliothek 52425 Jülich Tel: +49 2461 61-5368 Fax: +49 2461 61-6103 Email: zb-publikation@fz-juelich.de www.fz-juelich.de/zb
Cover Design:	Grafische Medien, Forschungszentrum Jülich GmbH
Printer:	Grafische Medien, Forschungszentrum Jülich GmbH
Copyright:	Forschungszentrum Jülich 2017

Schriften des Forschungszentrums Jülich
Reihe Information / Information, Band / Volume 51

D 82 (Diss., RWTH Aachen University, 2017)

ISSN 1866-1777
ISBN 978-3-95806-270-2

Vollständig frei verfügbar über das Publikationsportal des Forschungszentrums Jülich (JuSER) unter www.fz-juelich.de/zb/openaccess.

This is an Open Access publication distributed under the terms of the Creative Commons Attribution License 4.0, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

List of included own publications

Parts of the present work have been published in journals or on international conferences. The involvement of each topic (especially format and extent of citation and text) has been individually discussed and agreed with the coauthors. The respective publishers and copyright holders have been asked for reuse of each text or figure.

i) T. Breuer, L. Nielen, B. Roesgen, R. Waser, V. Rana, and E. Linn, "Realization of Minimum and Maximum Gate Function in Ta_2O_5-based Memristive Devices", *Scientific Reports*, vol. 6, p. 23967, 2016. (See [1] and Section 2.2 and 7.1.)

ii) T. Breuer, A. Siemon, E. Linn, S. Menzel, R. Waser, and V. Rana, "A HfO_2-Based Complementary Switching Crossbar Adder", *Advanced Electronic Materials*, vol. 1, no. 10, pp. n/a-n/a, 2015. (See [2], Abstract, Subsection 2.1.3, Section 7.3 and Chapter 8.)

iii) T. Breuer, A. Siemon, E. Linn, S. Menzel, R. Waser, and V. Rana, "Low-current operations in $4F^2$-compatible Ta_2O_5-based complementary resistive switches", *Nanotechnology*, vol. 26, no. 41, p. 415202, 2015. (See [3], Chapter 2 and 6.)

iv) T. Breuer, W. Kim, S. Menzel, V. Rana, A. Siemon, E. Linn, and R. Waser, "Low-Current and High-Endurance Logic Operations in $4F^2$-compatible TaO_x-based Complementary Resistive Switches", in *Silicon Nanoelectronics Workshop (SNW)*, IEEE, pp. 1-2, 2014. (See [4] and Subsection 7.2.2, © 2014 IEEE.)

v) A. Siemon, T. Breuer, N. Aslam, S. Ferch, W. Kim, J. van den Hurk, V. Rana, S. Hoffmann-Eifert, R. Waser, S. Menzel, and E. Linn, "Realization of Boolean Logic Functionality using Redox-based Memristive Devices", *Adv. Funct. Mater.*, vol. 25, no. 40, pp. 6414-6423, 2015. (See [5] and Subsection 7.2.2.)

vi) A. Schönhals, D. Wouters, A. Marchewka, T. Breuer, K. Skaja, V. Rana, S. Menzel, and R. Waser, "Critical ReRAM Stack Parameters Controlling Complimentary versus Bipolar Resistive Switching", in *IEEE International Memory Workshop (IMW)*, pp. 1-4, May 2015. (See [6], Subsection 2.1.3, Section 5.1 and Subsection 5.2.2, © 2015 IEEE.)

Abstract

Rapid growth of future information technology depends on energy-efficient computation and ultra-high density data storage. Non-volatile redox-based resistive switching memory (ReRAM) devices offer logic-in-memory and cognitive computing capabilities and can redefine von Neuman computer architecture. The Complementary Resistive Switch (CRS), where two bipolar switching cells are vertically stacked, is a promising candidate and enables integration of highly dense passive nano-crossbar arrays in $4F^2$ structure (with minimum feature size F). Due to the intrinsic non-linearity, the need for selector devices in the array is no longer required. Firstly, Ta_2O_5-based two-terminal devices (no access to the middle electrode (ME)) are considered, which facilitate simple integration and low fabrication cost. Their electrical characteristics are compared with switching of three-terminal devices (exhibiting access to the ME), in order to investigate the impact of single cell properties on the whole CRS. Initial electroforming process in the three-terminal devices is carried out by applying voltage stimuli to individual ReRAM cells. However, two-terminal devices require introduction of a novel procedure, which enables separate and controlled electroforming for low-current operations ($< 300\,\mu$A). Such devices (with improved endurance about 10^6 cycles) have been used to implement fuzzy logic in terms of MIN / MAX gates (concept suggested by Klimo *et al.* in [7], Nielen *et al.* in [8]), which could enable small-size sorting networks.
To reduce fabrication complexity, vertically stacked Pt|HfO_2|Hf|Pt ReRAM stacks are investigated, which offer similar *I-V* characteristics to the CRS, referred to as Complementary Switch (CS). The intrinsic complementary switching can be modified externally to eight-wise and counter-eight-wise bipolar switching. However, the Hf electrode thickness has also impact on the actual switching mode. Further process parameters, such as deposition rate of HfO_2, have much more of an impact on the initial device. Next, integration of the CS into 1×8 passive crossbar arrays is demonstrated. First, the implementation of all Boolean CRS-logic operations (concept suggested by Linn *et al.* in [9]) with the CS is proven, showing remarkable endurance (10^9 cycles). Afterward, two in-memory adders (concepts introduced by Siemon *et al.* in [10]) are experimentally demonstrated, which perform addition and subtraction operations.

Altogether, this could pave the way for next-generation information technology for parallel processing-in-memory architecture, which is implemented by ReRAMs embedded in energy-efficient, ultra-dense $4F^2$ passive crossbar arrays.

Kurzfassung

Die rapid ansteigende Nachfrage nach Lösungen für zukünftige Informationstechnologien lässt sich unmittelbar von dem enormen Bedarf an energieeffizienten Computersystemen und extrem hoher Datenspeicherdichte ableiten. Nichtflüchtige redox-basiserte resistive Speicher (ReRAM) können die derzeitige Datentechnologie mittels *cognitive computing* und der Möglichkeit, Logikoperationen direkt in der Speichereinheit durchzuführen (*logic-in-memory*), revolutionieren. Insbesondere der *Complementary Resistive Switch* (CRS), der aus zwei antiseriell angeordneten, vertikal gestapelten bipolar schaltenden ReRAM-Zellen besteht, ist für diese innovativen Anwendungen ein geeigneter Kandidat und ermöglicht zudem die Einbettung von $4F^2$-Strukturen (mit der minimalen Strukturgröße F) in enorm dichte passive *nano-crossbar arrays*. Aufgrund der intrinsischen Nichtlinearität muss nicht auf *selector devices* für die Ansteuerung einzelner Speicherelemente zurückgegriffen werden. Zunächst werden Ta_2O_5-basierte *two-terminal CRS* (ohne Zugang zur Mittelelektrode) betrachtet, die die Vorteile einer einfachen Integration in Schaltkreise und niedriger Produktionskosten aufweisen. Deren elektrische Kennlinien werden mit denen von *three-terminal devices* (mit Zugang zur Mittelelektrode) verglichen, um so den Einfluss der beiden einzelnen Zellen auf den gesamten CRS zu untersuchen. Die initiale *electroforming procedure* ist für die *three-terminal devices* sehr einfach zu realisieren, da sich hier, über den Zugang zur Mittelelektrode, die beiden einzelnen Zellen separat kontaktieren lassen. Dahingegen ist es für *two-terminal CRS* notwendig, eine neuartige Prozedur einzuführen, die ein separates und kontrolliertes *electroforming* für *low-current operations* ($< 300\,\mu$A) ermöglicht. Diese CRS devices, mit verbesserter *endurance* von über 10^6 Schaltzyklen, werden für die Implementierung von Fuzzy-Logik in Form von *MIN / MAX Gates* verwendet (Konzept vorgeschlagen von Klimo *et al.* in [7] und Nielen *et al.* in [8]), welche bei der Realisierung von Sortier-Netzwerken helfen könnten.

Um den Herstellungsprozess zu vereinfachen, werden simple vertikal gestapelte Pt|HfO_2|Hf|Pt ReRAMs genauer untersucht. Diese weisen unter bestimmten Bedingungen eine ähnliche I-V-Charakteristik zu der des CRS auf und werden in dem Fall als *Complementary Switch* (CS) bezeichnet. Das intrinsische komplementäre Schalten kann durch äußere Einwirkung ins *eight-wise* oder *counter-eight-wise* bipolare Schalten überführt werden. Darüber hinaus hat

ebenso die Hf-Elektrodendicke eine Auswirkung auf den intrinsischen *switching mode*. Weitere Prozessparameter, wie die Depositionsrate von HfO_2, haben dahingegen lediglich einen Einfluss auf die initialen Eigenschaften des Speicherelements. Die optimierten CS-Zellen (*endurance* von 10^9 Schaltzyklen, *operation current* $\sim 500\,\mu$A) werden in 1×8 passive *crossbar arrays* eingebettet. Anhand dieser *devices* wird zunächst die Umsetzbarkeit von Boolean-Logik-Funktionen demonstriert (Konzept vorgestellt von Linn *et al.* in [9]). Im Anschluss werden zwei in-memory adders experimentell getestet, welche Additionen und Subtraktionen durchführen (Konzept eingeführt von Siemon *et al.* in [10]). Diese Resultate belegen deutlich die funktionale Effizienz des *crossbar adder approach*, der einen wichtigen Weg für höchst fortgeschrittene ReRAM-basierte *computing-in-memory architecture* ebnet.

Contents

Contents **vii**

1 Introduction **1**

1.1 Scope of this work 4

2 Redox-based Resistive Switching Memory **7**

2.1 Switching Mechanisms 7

2.1.1 Bipolar Switching 7

2.1.2 Complementary Resistive Switching 10

2.1.3 Complementary Switching 11

2.2 Logic and Computation Properties (State of the Art) 12

2.2.1 Boolean Logic 12

2.2.2 Fuzzy Logic 13

3 Experimental Technology **15**

3.1 Analytical Methods 15

3.1.1 Thin Film Characterization 15

3.1.2 Electrical Characterization 20

3.2 Device Preparation 24

3.2.1 Plasma Ashing 24

3.2.2 DC / RF Sputtering 24

3.2.3 Lithography 25

3.2.4 (Reactive) Ion Beam Etching 28

4 Device Fabrication **29**

4.1 Thin Film Characterization 29

4.2 Bipolar / Complementary Switching Devices 37

4.3 Complementary Resistive Switching Devices 43
4.3.1 Three-Terminal Devices 44
4.3.2 Two-Terminal Devices 44

5 Resistive Switching in HfO_2-based Devices 51
5.1 Complementary vs. Bipolar Switching 51
5.2 Electroforming / SET / RESET 56
5.2.1 O_2 Sputtering Gas Flow Variation 56
5.2.2 Hf Electrode Thickness Variation 62
5.2.3 RF Sputtering Power Variation 65
5.3 Reliability 69
5.3.1 State Stability 69
5.3.2 Endurance 71
5.4 Conclusion 76

6 Ta_2O_5-based CRS Device Optimization 79
6.1 Low-Current Operation in CRS 79
6.1.1 Three-Terminal CRS 80
6.1.2 Two-Terminal CRS 81
6.2 Conclusion 92

7 ReRAM Device Application 95
7.1 Minimum / Maximum Gate 95
7.1.1 Basics 95
7.1.2 Proof-of-Concept 100
7.1.3 Discussion 107
7.2 Logic-in-Memory (CRS-Logic) 110
7.2.1 Basics 110
7.2.2 Proof-of-Concept 112
7.2.3 Discussion 127
7.3 Computation-in-Memory 128
7.3.1 Basics 128
7.3.2 Proof-of-Concept 133
7.3.3 Discussion 139

8 Conclusion and Outlook **143**
8.1 Device Improvement 143
8.2 Device Applications 145
8.3 Outlook 147

A Appendix A **149**
A.1 Electron Beam Lithography 149
A.2 Thin Film Surface Roughness 151
A.3 Material Stoichiometry 152
A.4 Statistical Definitions 152
A.5 Associative Capacitive Network 153

List of Figures **157**

List of Tables **161**

Bibliography **163**

Acknowledgement **181**

Chapter 1

Introduction

In the age of the Internet of Things, i.e. the internetworking of smart devices, electronic memories have become an integral part of humans, as personal electronic devices such as laptops, digital cameras, smart phones and tablets are equipped with memory devices. To have better consumer experience, these memory elements should be of higher capacity, faster access speed (read and write) and as well as economically obtainable.
Conventional memory technologies, Flash, SRAM and DRAM cannot satisfy the technological and commercial requirements (e.g. due to physical limitations). Therefore, emerging memory technologies have been actively pursued for the next generation of non-volatile data storage. The ideal characteristics for future memory device include fast programming speed ($<$ ns), low operation voltage ($< 1\,\mathrm{V}$), low power / energy consumption ($\sim$ fJ/bit for write), long retention time (> 10 years), high write / read endurance ($> 10^{16}$ cycles) and excellent scalability ($< 10\,\mathrm{nm}$).
New memory devices include Phase-Change RAM (PCRAM), Ferroelectric RAM (FeRAM), Magnetoresistive RAM (MRAM) and Resistive / Redox-based RAM (RRAM / ReRAM). Table 1.1 shows the comparison of the characteristics of current and future memory technologies. The ReRAM devices can be scaled down below the five nanometer-mark with $4F^2$ feature size.[11–13] Recently, write / erase time in sub-nanosecond range has been realized.[14] Additionally, the energy consumption for toggling the memory state can be reduced to a range of 0.1 fJ.[11] Having compatibility with CMOS, ultra-high dense integration capability, ReRAM has advantages over other memory tech-

nologies and is being pursued for different application domains such as neuromorphic and reconfiguration logic. Furthermore, these memristive devices (memory resistors) offer also the capability to merge logic and computation with memory units.[9, 10, 15–20] This approach avoids the data transfer between separated memory and computation units as in the conventional von Neumann computer architecture.
Beyond these application fields, the ReRAM is also a promising candidate for innovative artificial intelligence systems, which are modeled on the highly efficient human brain. In recent years, scientists have tried to imitate the human brain capabilities with current CMOS technology. However, the power consumption is one of the biggest drawbacks in these machines. For instance, Watson IBM supercomputer is capable of processing 80 trillion operations (teraflops) per second and consumes 2.3 MW.[21,22] It runs about 2,800 processor cores and has 16 terabytes of working memory. On other hand, the human brain, an example for artificial synapses and neuromorphic processor units, contains 100 billion neurons and consumes only 25 W. Therefore, new and innovative concepts / technologies have to be considered, which enable significantly more energy efficient memory and computation applications. Due to clear similarities to synapses[23–26] and promising switching properties, the ReRAM might be able to meet all requirements.

Table 1.1: Current baseline and prototypical memory technologies. Values in brackets depict best projected achievements. The data are based upon the International Technology Roadmap for Semiconductors (ITRS) from 2013.[13]

	ReRAM (Bipolar Switch)	DRAM	SRAM	NAND Flash	FeRAM	STT-MRAM	PCRAM
(Non-)Volatile	Non-Volatile	Volatile	Volatile	Non-Volatile	Non-Volatile	Non-Volatile	Non-Volatile
Feature size [nm]	$(<)5$	36 (9)	45 (10)	$16\ (>10)$	180 (65)	65 (16)	45 (8)
Cell Area (2D) [F^2]	4	6 (4)	140	4	22 (12)	20 (8)	4
Write/Erase Time [ns]	<1	<10	0.2 (0.07)	$10^6/10^5$	$65\ (<10)$	35 (1)	$100\ (<50)$
Retention Time	>10 yr	64 ms (refresh required)	as long as voltage is applied	>10 yr	>10 yr	>10 yr	>10 yr
Write Cycles	$(>)10^{12}$	$>10^{16}$	$>10^{16}$	10^5	$10^{14}\ (>10^{15})$	$10^{12}\ (>10^{15})$	10^9
Write Voltage [V]	$(<)1$	2.5 (1.5)	1 (0.7)	15	1.3-3.3 (0.7-1.5)	$1.8\ (<1)$	$3\ (<3)$
Read Voltage [V]	0.1	1.8 (1.5)	1 (0.7)	4.5	1.3-3.3 (0.7-1.5)	$1.8\ (<1)$	$1.2\ (<1)$
Write Energy [J/bit]	1×10^{-13} (1×10^{-16})	4×10^{-15} (2×10^{-15})	5×10^{-16} (3×10^{-17})	1×10^{-10}	3×10^{-14} (7×10^{-15})	2.5×10^{-12} (1.5×10^{-13})	6×10^{-12} (1×10^{-15})

1.1 Scope of this work

The present work is focused on material / device engineering and implementation of innovative application concepts for logic- and computation-in-memory operations on the ReRAM. Here, Ta_2O_5- and HfO_2-based devices are investigated, which are promising candidates for innovative memory technologies offering excellent switching properties.[27–34]
Chapter 2 gives an overview of fundamental mechanisms involved in the ReRAM, where the focus is on the Valance Chance Mechanism (VCM), which is responsible for resistance change in subsequently demonstrated binary metal oxide devices. The discussion includes the three switching modes (bipolar switching, complementary resistive switching and complementary switching) and the state of the art of logic / computation concepts enabling operations directly in memory units.
Subsequently, relevant experimental technologies are briefly described in Chapter 3, including analytical methods for material and device characterization / preparation and experimental setups. The detailed preparation and fabrication flow of the individual device types is given in Chapter 4. This also includes material characterization regarding stoichiometry, structure, film thickness and surface topography. For HfO_2-based devices, several fabrication parameters have been varied, e.g. Hf electrode thickness and sputtering power / growth rate. The impact of these parameters on device characteristics is investigated in Chapter 5, especially initial resistance, the electroforming process, state reliability and transition from bipolar to complementary switching mode.
In Chapter 6, the focus is on the optimization process of Ta_2O_5-based devices showing complementary resistive switching. Three- and two-terminal switches (offering an / no access to the middle electrode) are compared and a novel forming procedure, which implements low-current operations for micro- and nanometer scaled devices, is introduced.
Finally, three promising ReRAM applications are considered in Chapter 7: MIN / MAX gate (fuzzy logic; concept introduced by Klimo *et al.*[7] and Nielen *et al.*[8]), CRS-logic (logic-in-memory; concept introduced by Linn *et al.*[9]) and multi-bit crossbar adders (computation-in-memory; concept introduced

by Siemon *et al.*[10]) Relevant basics of these concepts are comprehensibly explained and pre-measurements and proof-of-concept experiments are presented. At the end, the summary of this research and the outlook for future efforts are given in Chapter 8.

Chapter 2

Redox-based Resistive Switching Memory

2.1 Switching Mechanisms

The redox-based random access memory, referred to as ReRAM, is one of the most auspicious emerging non-volatile memory (NVM) devices by reason of: low-voltage operating mode, brilliant capability of energy efficiency, outstanding scalability, compatibility to 3D fabrication and silicon technology and high endurance.[18, 19, 35–42] On the basis of switching properties, ReRAMs can be categorized into the unipolar switch, which can be programmed and erased with the same bias polarity, and the bipolar switch (BS) needing opposite bias polarities.[42, 43]

Different switching mechanisms for the resistive switching phenomena have been reported in literature. However, the most relevant ones are: Thermo-Chemical Mechanism (TCM)[44], Valence Change Mechanism (VCM)[42] and ElectroChemical Metallization (ECM)[45]. All of them are dominated by redox-related chemical processes. Due to higher endurance[27] and better uniformity, VCM-based bipolar ReRAMs are of most interest. These devices can be implemented by single layer or bi-layer structures with TiO_x[46], HfO_x[47] and TaO_x[27] etc.

2.1.1 Bipolar Switching

Bipolar switching is predominately observed in asymmetric stacks, the binary metal oxides are sandwiched between low work function and high work func-

tion metal electrodes. The device resistance can be changed reversibly from the high resistance state (HRS or '0', sometimes: 'OFF' state) to the low resistance state (LRS or '1', sometimes: 'ON' state) by external voltage or current stimuli. Both states are non-volatile, i.e. no further voltage needs to be applied to keep the actual state.
Figure 2.1 presents a typical *I*-*V* characteristic, which has been measured on a Pt|ZrO_x|Zr memory stack by applying quasi-static voltage ramps to the Pt electrode. Here, the resistance change is described by a filamentary switching model.[48] The conducting filament is ruptured and regrown during the switching as depicted by the inset sketches (A) to (D) in Figure 2.1. The filament consists of oxygen vacancies (green balls, $V_O^{\bullet\bullet}$ in Kröger-Vink notation[49, 50]) and reduced metal ions (purple balls). Here, "reduced" is relative to the ideal crystal and $^{\bullet}$ denotes a positive charge relative to the perfect lattice, i.e. the $V_O^{\bullet\bullet}$ is twice positively charged. At the beginning, the memory device is in the 'OFF' state (A) offering a gap (in the disc region) between the permanent filament (plug region) and the Pt electrode. Applying a negative voltage to the Pt electrode, the SET process starts (B), when positively charged oxygen vacancies are attracted into the gap increasing the local conductivity and closing the filamentary rupture. After the SET process, the memory cell is in the conductive 'ON' state (C), which is stable as long as the applied voltage does not change the polarity and the RESET process does not start (D).
The difference between HRS and LRS can be physically explained by considering the oxygen vacancy profile $[V_O^{\bullet\bullet}]$ and the energy-band model. The ZrO_x|Zr interface is assumed as ohmic contact and does not change significantly during the switching. However, the Pt|ZrO_x interface exhibits a Schottky barrier within the disc region, whose width depends on oxygen vacancy concentration as depicted in Figure 2.2. Oxygen vacancies, which are attracted into the disc region during the SET process, serve as dopants[48] and the barrier width is inversely proportional to root of the dopant concentration.[51] In the LRS, the barrier width is negligible and the contact serves as an ohmic resistor. Repelling the vacancies into the plug region (during RESET process) increases the barrier width and the current is vehemently reduced.

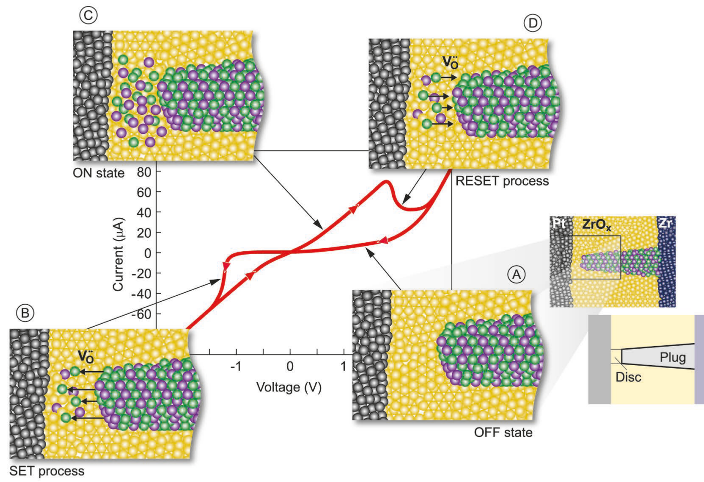


Figure 2.1: Valence Change Mechanism (VCM) switching scheme. The quasi-static I-V characteristic of a Pt|ZrO$_x$|Zr valence change memory. Consider, the displayed voltage is applied to the Pt electrode, whereas the Zr electrode is grounded. The sketches A to D present the switching stages. The oxygen vacancies are represented by green balls, whereas the purple ones indicate the Zr ions being in a lower valence state. (A) HRS (or 'OFF' state), (B) SET process, (C) LRS (or 'ON' state) and (D) RESET process.[48] (Reprinted with permission from the publisher.)

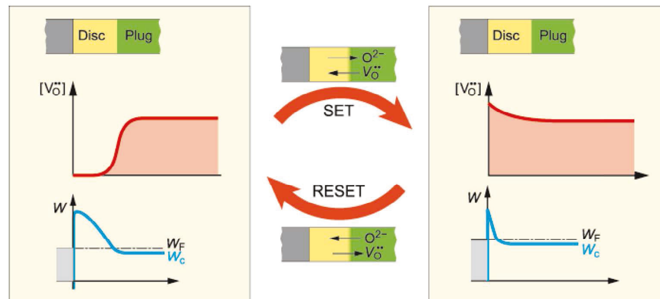


Figure 2.2: Sketch of oxygen vacancy profile $[V_O^{\bullet\bullet}](x)$ (red line), the conducting band diagram $W_c(x)$ (blue line) and the Fermi level W_F (black, dashed line) in the disc / plug region of the n-conducting filament in the HRS (left) and LRS (right). The illustration of the SET and RESET process considering the oxygen ion / vacancy movement (center).[48]) (Reprinted with permission from the publisher.)

2.1.2 Complementary Resistive Switching

For ultra-high dense NVM applications, the ReRAM-based devices feature integration in passive $4F^2$ (minimum feature size F) crosspoint arrays.[3, 52] Stacking of the crossbars enables further enhancing of the device embedding density to $4F^2/n$, where n is the number of stacks.[53] The memory elements arranged in rows and columns are highly inter-connected in this configuration. Therefore, the architecture suffers from intrinsic sneak paths.[12, 54] Furthermore, this issue is aggravated, if the accessed memory cell being in HRS is surrounded by cells being in LRS. As a consequence, the sensed read current does not only pass the accessed cell. Surrounding paths with potential lower resistance also contributes to the overall current. This additional current causes misinterpretation of the actual memory device state.
The sneak current issue scales up with the crossbar array size.[3, 12] Thus, the number of embedded devices in the array is limited.[54] In order to solve this problem, various types of selector devices are available, which enable dense integration: ovonic threshold switch [55], mixed ionic electronic conductors [56], rectifying based Pt|TiO_2|Pt[57–59], MOSFET integration [60, 61] and metal-insulator transition materials[62]. However, up to now, these devices are not capable of satisfying significant requirements in terms of scalability and device properties in large $4F^2$ crossbar arrays. For instance, MOSFET-based 1T1R architecture requires larger foot-print and in most cases the current density of available selectors is insufficient to drive ReRAMs.[12]
As an answer to this problem, Linn *et al.* have introduced the concept of the Complementary Resistive Switch (CRS).[12] This device is composed of two bipolar switching ReRAMs, which are referred to as top cell (TC) and bottom cell (BC). In the present thesis, both cells are partially vertically stacked and anti-serially connected (see Figure 2.3a).[3,12,63,64] The CRS inherently comprises a memory and selector element. Figure 2.3b demonstrates the schematical I-V switching curve of the CRS. The insets illustrate the resistance scheme of the CRS states. Independent of the concrete device state, below specific threshold voltages, the CRS offers a high resistance (cf. $V_{\mathrm{th},1}$, $V_{\mathrm{th},3}$). This enables reduction of general leakage currents. Furthermore, CRS crossbar arrays are capable to fulfill the fundamental requirements for parallel write / read operations in storage-class memories, in order to guarantee high-speed data

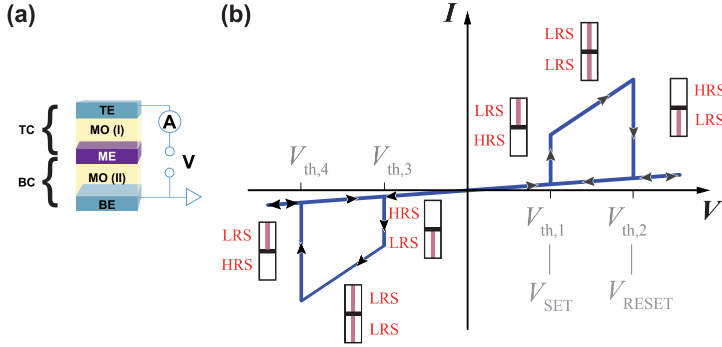


Figure 2.3: (a) CRS stack scheme. Two anti-serially stacked ReRAM cells, top cell (TC) and bottom cell (BC). Each cell consists of the middle electrode (ME), metal oxide (MO) and top electrode (TE) / bottom electrode (BE) layer. (b) *I*-*V* scheme of the CRS. For the switching process, the threshold voltages $V_{\mathrm{th},1}$ to $V_{\mathrm{th},4}$ have to be considered. The insets indicate the actual resistance state of the BC and TC. These cells are complementarily toggled between a low resistance state (LRS) and a high resistance state (HRS).[3] (Redrawn with permission from the publisher.)

processing.[65] Additionally, ReRAMs exhibit the capability of processing-in-memory operating mode (CRS-logic), which has been suggested in [8–10] and both experimentally demonstrated in [1, 2, 5] and Section 7.2. The two CRS states LRS/HRS (TC in LRS, BC in HRS) and HRS/LRS (TC in HRS, BC in LRS) are identified with the logical ‘0’ and ‘1’ and used for information storage.[3] The ‘ON’ state, where both cells are in the LRS is only a transition, whenever the device changes from ‘0’ to ‘1’ and contrariwise. The ‘OFF’ state, where BC and TC are highly resistive, does not occur during cycling. This state only exists for the initial non-electroformed CRS.[3] This promising CRS concept has been successfully proven for several metal oxides materials, e.g. HfO_2 ,Ta_2O_5 and TiO_2.[66–70]

2.1.3 Complementary Switching

Lately, the complementary switch (CS) has been reported, which is implemented by a single VCM-based ReRAM cell (e.g. TiN|HfO_x|TiN or Pd|TaO_x|Ta|Pd).[31, 69] These devices show similar *I*-*V* curves to the CRS device (cf. Figure 2.4), but offering a simpler stack structure.[31, 69] In con-

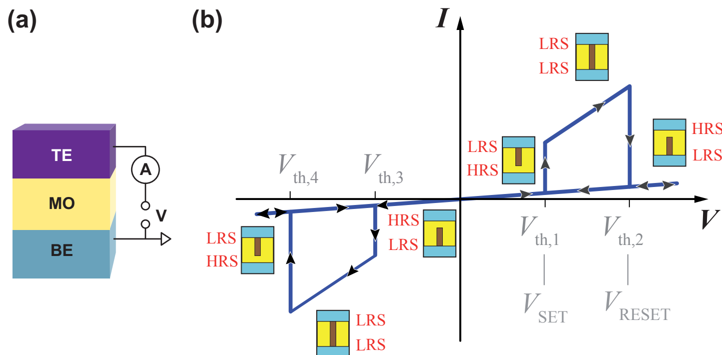


Figure 2.4: (a) CS stack scheme. The device consists of the top electrode (TE), the metal oxide (MO) and bottom electrode (BE) layer. (b) *I*-*V* scheme of CS device. For the switching process, the threshold voltages $V_{th,1}$ to $V_{th,4}$ have to be considered. The switching occurs at the two MO-electrode interfaces, which are complementarily toggled between a low resistance state (LRS) and a high resistance state (HRS). The insets indicate the actual CS state.

trast to the CRS, the CS is based on switching at two interfaces in the same cell.[6, 71] The individual switching stages are discussed for the HfO_2-based CS in Section 5.1. Since the CS features an inherent selector property, large crossbar arrays can be realized without the need of additional selector devices.

2.2 Logic and Computation Properties (State of the Art)

2.2.1 Boolean Logic

Performance of next-generation information technology depends strongly on the successful research on novel device materials as well as efficient circuit architecture and software.[2] For this progress, passive crossbar arrays composed of redox-based resistive switches (ReRAMs) are highly auspicious candidates for ultra-high dense data storage and energy-efficient processing applications.[9, 41, 42, 72]
The conventional von Neumann architecture is based upon separated units: central processing unit (CPU) and memory unit (MU).[2] Data are transferred

between MU and CPU via a connection line. However, the rate for data transfer is constrained. This issue is referred to as the von Neumann bottleneck.[73] In order to overcome this limitation, novel concepts have been proposed, where computations are performed directly within the memory (processing-in-memory). Such concepts have recently been presented for ReRAM technology.[17, 74, 75] In those concepts, the control unit (CU) and the MU are both on the same chip. The CU is based on CMOS and the MU on ReRAM technology, which are compatible. In opposition to the conventional approach, this CU does not control only the memory operating mode, but also the logic operating mode. Rosezin *et al.* have demonstrated that the CRS enables realization of elementary implication operations and can be considered as a finite state machine.[76] Figure 2.5 depicts the comparison of the CRS with a finite state machine. Recently, Linn *et al.* have proposed CRS-logic concept.[9]
The CRS-logic has several features: (1) The actual memory state is used as a third input variable for the next operation.[10] (2) The logic operations are processed by CS / CRS devices and (3) afterwards the information is directly / inherently stored in the final memory location.[9] Thus, this approach is a logic-in-memory concept designed for CS and CRS arrays, but can be used for all bipolar switching devices. Moreover, for this specific concept, two multi-bit crossbar adder schemes have been introduced by Siemon *et al.*[10] Proof-of-concept electrical measurements for logic- and computation-in-memory applications on crossbar arrays are presented in Section 7.2 and 7.3.

2.2.2 Fuzzy Logic

Considering fuzzy logic, the truth values are not restricted to 0 (completely false) and 1 (completely true), rather any real number between 0 and 1 is possible. Inspired by this idea, Šuch and Klimo have proposed a concept, where two-memristive circuits are applied to realize Maximum and Minimum (MAX / MIN) logic gates.[7] The suggested gate structure exhibits two anti-serially connected single ReRAMs, that means the device structure can be compared with the conventional CRS, but it offers an additional access to the middle electrode (ME).[3, 75, 77, 78] In general, one MIN / MAX gate exhibits two inputs and one output for sensing the lower or higher input potential.[79]

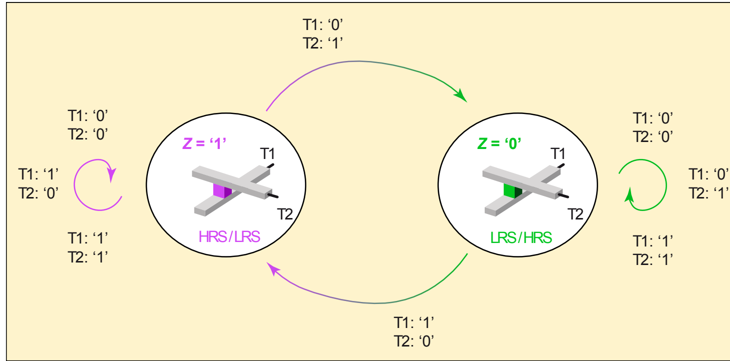


Figure 2.5: The CS / CRS as finite state machine. Depending on the actual device state Z ('0' or '1'), the state switches only for specific input signals at the terminals T1 and T2.

Concerning binary considerations, these devices corresponds to OR / AND logic gates.[79, 80] These elements can be applied for processing of analog signals and can enable implementation of sorting networks[81], while considering several constraining specifications.[1, 8, 79]
The corresponding three-terminal CRS devices are demonstrated and characterized in Chapter 6. Šuch *et al.* have demonstrated the characteristic of actual memristive devices differs strongly from the ideal memristor characteristic. Nonetheless, a reliable MIN / MAX gate operating mode is facilitated by considering few limitations regarding the input signal amplitude.[78, 79] Despite of these limitations, which are extensively discussed, the proposed structures are highly suitable to feature fuzzy logic operations.[1]

Chapter 3

Experimental Technology

3.1 Analytical Methods

3.1.1 Thin Film Characterization

3.1.1.1 X-Ray Reflectometry

X-ray reflectometry (XRR) is used to determine the thickness of thin films sputtered on substrates in order to determine the film growing rate. This method is based on reflection principle of the x-ray light and can fundamentally be described with Snell's law

$$n_0 \cos\theta = n_1 \cos\theta_1 \tag{3.1}$$

where θ is the angle of the incident beam (to the surface), which propagates through the medium of refractive index n_0, and θ_1 is the beam refraction angle in the medium with a refractive index n_1 (cf. Figure 3.1). The substrate thickness is assumed to be infinite in comparison to the thin film. Therefore, the intensity of the beam is neglected, which is refracted from the substrate and reflected back at the substrate-plate interface.
Figure 3.1 shows the optical path difference Δs between directly reflected wave and the refraction wave ($\Delta s = s_1 - s_0$). For constructive interference, Δs has to be a multiple integer n of the beam wavelength λ. Depending on the incident angle, both waves interfere constructively or destructively. The measured x-ray reflectivity shows oscillations (Kiessig oscillations[82]) as function of the

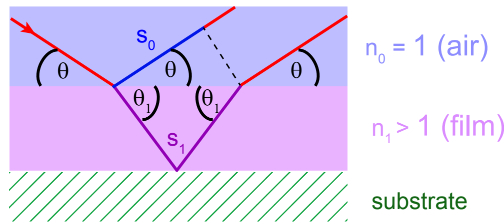


Figure 3.1: X-ray reflection at the thin single layer (deposited on substrate). The beam incides with the angle θ from air (refractive index $n_0 = 1$) and partially reflected from the surface and deflected in the film by the angle θ_1. At the film-substrate interface, the beam is reflected toward the surface, where it interferes with the directly reflected beam due to the path difference $(s_1 - s_0)$. The substrate thickness is assumed to be infinite. Therefore, the diffracted beam is neglected in the substrate.

wavelength, incident angle, refractive indices and the film thickness. The thin film thickness d can be estimated by

$$d = \frac{\lambda}{2\Delta\theta} \tag{3.2}$$

where $\Delta\theta$ is the distance between two neighboring intensity maxima.[83] An exemplary XRR measurement is presented in Figure 4.1. In the present work, the measurements have been performed by the Philips PW 3020 diffractometer, using a Cu-K$_\alpha$ x-ray tube ($\lambda_{K_{\alpha,1}} = 1.540598\,\text{Å}$ and $\lambda_{K_{\alpha,2}} = 1.544426\,\text{Å}$) in the Bragg-Brentano geometry. The thickness is calculated by XRR simulations, fitting film parameters (density, roughness, thickness) in a physically reasonable way.

3.1.1.2 X-Ray Diffraction

Applying the x-ray diffraction (XRD) mode by the Philips PW 3020 diffractometer enables one to investigate the structural quality of crystalline samples. Due to the periodic crystal lattice, Bragg reflections are observed for incident angles, where the diffracted waves interfere constructively, i.e. Bragg's equation

$$n\lambda = 2d_{hkl}\sin\theta \tag{3.3}$$

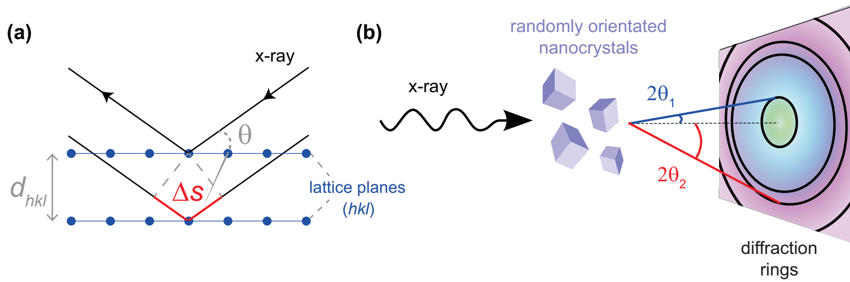


Figure 3.2: X-ray diffraction scheme. (a) Diffraction from two parallel crystal planes. The x-ray beam incides at angle θ. Scattering peaks are only observed, if the path distance $\Delta s = 2d \sin\theta$ is a multiple integer of the x-ray wavelength λ. (b) Schematic of the Debye-Scherrer method. The randomly orientated crystals generate diffraction rings without rotating the sample. Radial scanning enables the common 2θ-scan as shown in Figure 4.2 [84]

has to be fulfilled, where $n\lambda$ is a multiple integer of the used wavelength and d_{hkl} refers to the lattice distance of lattice planes (hkl) with the Miller indices h, k and l (cf. Figure 3.2a).

In the case of thin films, the observed reflections depend on the substrate / film orientation. In the present work, the grown thin films however become nanocrystalline by thermal annealing. Due to the random arrangement of such nanocrystals, the full diffractogram is visible without any additional rotation of the substrate (see Figure 3.2b), which is similar to the Debye-Scherrer method for powder diffraction.[84–86] This means that there is always a sufficient number of crystals, which are orientated properly to fulfill Equation 3.3 for each Bragg reflection. The full diffractogram is measured by a single 2θ-scan.

In order to reduce the signal contribution of the substrate, the grazing incidence X-ray diffraction (GIXRD) method is used. The x-ray beam penetration depth is limited to the upper layer due to the small incidence angle. Smaller angles cause less penetration into the substrate, but require longer observation time (due to a poor signal to noise ratio).[87]

3.1.1.3 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a surface sensitive measurement technique to determine the elemental composition of materials. The sample

is exposed to the x-ray beam with known wavelength (or photon energy). By absorbing photons, core electrons are excited, move toward the surface and leave the material. This is referred to as the photoelectric effect. The penetration depth (for investigations) is limited by the mean free path of electrons in solids: larger distance to the surface increases the probability of inelastic scattering and reabsorption of the excited electron. The loss ratio also depends on the kinetic energy of the electrons and the material composition (structure, density etc.)
The original depth of the non-scattered or elastically scattered electrons, which leave the surface, is up to few nanometers and can be controlled more accurately by the angle resolved XPS method. The kinetic energy E_{kin} of the free electrons is measured by an electron detector. The binding energy E_{b} of the electrons, which is typical for each element and the actual chemical bonding (causing chemical energy shift), is calculated by using the law of the conservation of energy

$$E_{\mathrm{b}} = E_{\mathrm{ph}} - E_{\mathrm{kin}} - \phi \tag{3.4}$$

where $E_{\mathrm{ph}} = h\nu$ is the x-ray photon energy (Planck's constant h, the photon frequency ν) and ϕ the work function of the material.

3.1.1.4 Atomic Force Microscopy

To investigate the surface topography with resolution in the sub-nanometer (atomic) range, atomic force microscopy (AFM) is used. A nanoscopic tip, which is fixed to a cantilever, scans the sample surface, where the cantilever movement is realized by piezo elements. The tip is deflected by inter-atomic forces, which are caused by quantum-mechanical effects and Coulomb repulsion. In the present work, the contact mode is used, i.e. there is always a mechanical contact between sample and tip. Measuring tip deflection as function of the location enables one to determine the mapped surface height profile. A laser beam is reflected off the back of the cantilever, where the direction of the reflection is recorded by a position-sensitive photodetector.

3.1.1.5 Electron Microscopy

Scanning Electron Microscopy The structural quality checks of the patterned samples are performed by a SU8000 scanning electron microscope (SEM). A Schottky cathode supplies electrons, which are accelerated by an anode voltage in the range of several kilovolts (typically $\sim 10\,\mathrm{kV}$). The electron beam is focused on the specimen by an electron-optical system (combination of different electrostatic and electromagnetic lenses).
The focused specimen area is scanned by deflection of the electron beam using the optics. The applied acceleration voltage defines the penetration depth of the primary electrons into the specimen. Therefore, the acceleration voltage is used to focus on a specific layer. The striking electrons lose energy by interacting with the specimen matter, which is caused by different mechanisms. X-ray emission, low-energetic secondary and high-energetic backscattered electrons are the main products of the interactions.[88] All these physical particles sensed with individual detectors (cf. Figure 3.3) carry information about the specimen, which are used to draw conclusions on structure and elemental composition.
Particular electron species and x-rays are measured by individual detectors. The specimen is mapped by the intensity variation of detected particles while scanning the investigated area and the observed structures are displayed by black-and-white contrast images. The SU8000 resolution limit is about few nanometers.

Transmission Electron Microscopy Further structural investigation of the layer / device cross-section is available by transmission electron microscopy (TEM). In contrast to the SEM technique, in the TEM, the accelerated electrons transmit the specimen and material information is only carried by these primary electrons (not by x-rays, backscattered or secondary electrons). Complete transmittance requires high acceleration voltages in the range of 100 kilovolts and electron transparency, i.e. the specimen has to be very thin (about $100\,\mathrm{nm}$ or thinner).
The specimen (lamella) is prepared by the focus ion beam technique, where the investigated cross-section is sliced from the sample by the ion beam. Thinner specimens reduce inelastic electron scattering and enable higher resolution.

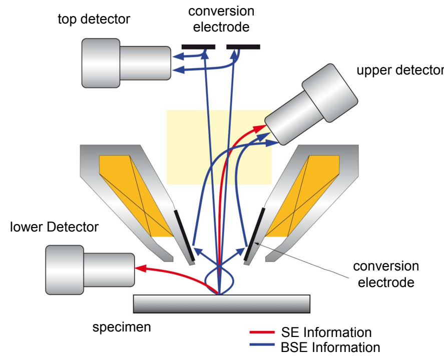


Figure 3.3: Schematic of electron detection for the SEM. Different detectors are used for low-energetic secondary electrons (SE) and high-energetic backscattered electrons (BSE), which are generated during individual processes and carry information about the specimen.[89]

The sample is not scanned by the electron beam, therefore only a fixed area is exposed by the broad beam and investigated. After leaving the specimen, the electrons pass electron-optics for magnification and are detected by a photosensor (CCD camera). Image resolution in the sub-nanometer range is possible. For quick investigation of the cross-section, a scanning transmission microscope is used, where the electron beam scans the specimen similar to the SEM and only the transmitted electrons are detected.

3.1.2 Electrical Characterization

In the present work, the electrical characterization of resistive switching elements is performed with various tools. The electrical measuring setups are used for applying quasi-static (DC) voltage sweeps with a ramp rate in the range of volt per second and voltage pulses (AC) down to the pulse width range of nanoseconds. Quasi-static means: the voltage ramp is slow to ensure the loading of parasitic capacitance in order to minimize the influence capacitive phenomena on the ReRAM device.[90] Additionally, the memory system has always sufficient time to react on the external driving force (applied voltage) and is nearly always in the quasi-equilibrium. Most of those setups are non-modified standard equipment and are not described in detail.

3.1.2.1 Quasi-static Measurement

The Keithley 2611A Sourcemeter is used for quasi-static measurements applying voltage or current ramps. Here, only voltage driven experiments have been performed, where the voltage can be increased from 1 μV up to 200 V. Depending on actual measuring range, the current is sensed from 1 pA up to 1.5 A. The sourcemeter supports contacting the device under test (DUT) by two probes. The signal can be only applied to one probe, whereas the second one is set to ground. For the resistive switching, the maximal device conductivity can be controlled by applying a current compliance (CC). This CC also protects the device against electrical voltage breakthrough. The sourcemeter exhibits an instrument CC. Whenever the measured current reaches the chosen CC level, the system switches to the current source mode and keeps the current constant. As long as the applied voltage is larger than actual voltage drop across the DUT, the system stays in the current source mode. If the actual voltage drop is equal to or smaller than the applied one, the system switches back to the voltage source mode. However, due to the slow response time of the instrument CC, it has to be checked that the timing is sufficient with respect to the experimental requirements (see Chapter 6).

The B1500A Semiconductor Parameter Analyzer (see Figure 3.4) enables both quasi-static voltage sweeps and the application of base voltage levels. The DUT is contacted minimally with two probes, but up to four can be used, where simultaneous signals are applied. This functionality is relevant for such applications as those mentioned in Section 7.1. Using the high resolution source monitoring units, voltages up to 100 V can be applied, where the resolution ranges from 25 μV up to 5 mV (depending on the actual voltage range). Currents up to 100 mA can be detected with resolution from 100 aA to 5 μA, which is sufficient for the present experiments. The analyzer also exhibits an instrument CC.

Additionally, the Keithley 4200-SCS is available for quasi-static measurements. This system supports an instrument CC and four probes for contacting the device. Additionally, toggling between the quasi-static and the pulse measure mode (without switching between special probes) is featured. Furthermore,

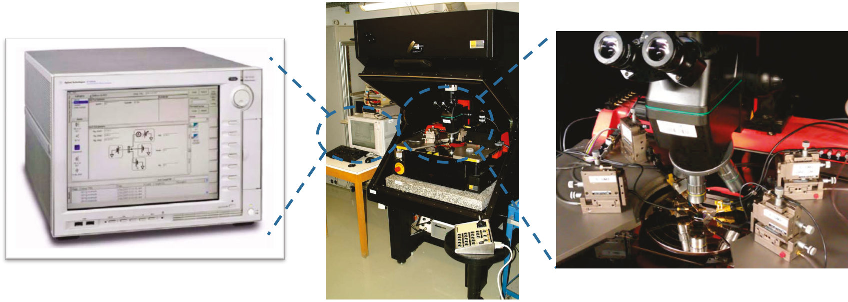


Figure 3.4: Overview of the experimental equipment (center), B1500A Semiconductor Parameter Analyzer (left) and optical microscope with four probes for contacting the sample.

applying simultaneous voltage stimuli is available by multiple probes.

3.1.2.2 Pulse Measurement Setup

Some endurance and retention experiments have been performed on the Keithley 2611A by applying long pulses in the micro- and millisecond range. However, better analysis regarding endurance and proof-of-concept tests for application is achieved by short pulses in the nanosecond range, which are supported by the Keithley 4200-SCS. Pulses down to few 10 ns can be applied to the DUT, if the response current level is sufficient. For instance, detecting the current by the 10 mA range requires a minimum pulse width of about 160 ns and a minimum pulse rising / falling time of about 20 ns.

Voltage Sensing Unit. In Section 7.1, three-probe measurements are demonstrated. The voltage is applied to two different probes. A part of the voltage drops across the device (depending on the actual device state). The remaining voltage is measured at the third probe. In the quasi-static setup, this is implemented by the current bias mode, where the current is kept at constant zero ampere by applying a counter voltage to the third probe. The inverse counter voltage is equal to the voltage, which has to be sensed at the third probe.
However, this method cannot work for pulsed signals, since instrumental regulation of the inverse voltage is too slow. To measure the resulting voltage at the third probe, a self-designed impedance converter has been connected

directly to the probe, which consists of an operational amplifier (OP27) and a monolithic unity gain buffer (EL2003), operating in the feedback configuration. This device combines features of the single units.[91] A simplified equivalent circuit diagram of the impedance converter is depicted in Figure 3.5. The OP27 offers a high input resistance ($\sim 3\,\mathrm{G\Omega}$) to avoid current flow through the probe, which could distort the voltage measurement.

The EL2003 acts as voltage follower and can supply higher output voltage as compared to the OP27. This is important to drive the $50\,\Omega$ terminating resistor, which suppresses signal reflections. The feedback signal of the EL2003 is transferred to the second input of the OP27. By using this feedback operation, the OP27 compares the difference between both inputs. The OP27 modifies the output signal as long as the difference disappears.[91, 92]

A further $50\,\Omega$ resistor (input resistance of the Keithley 4200) is serial to the terminating resistor of the impedance converter. Both serve as a voltage divider. The measured voltage at the Keithley 4200 has to be doubled to get the right values. The impedance converter is not an ideal device and additional resistors have to be added, to improve the device characteristics: $1\,\mathrm{k\Omega}$ between OP27 and EL2003 to prevent oscillations and $10\,\mathrm{M\Omega}$ at the input to avoid an offset-voltage, which has been up to $0.7\,\mathrm{V}$ and could destroy or at least change the present device state.[91]

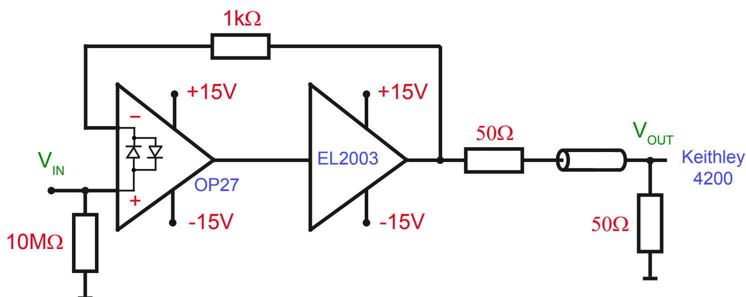


Figure 3.5: Simplified circuit of impedance converter for detecting pulse output signals in MIN / MAX gates.

3.2 Device Preparation

3.2.1 Plasma Ashing

Material structures and compositions have to be well known in order to understand effects and to tailor device properties. Minimal impurities in semiconductor manufacturing can cause huge impacts on the device characteristics. This might aggravate the explanation of the origin of the observed effects. Thus, the sample has to be cleaned sufficiently before starting the individual processing steps.
To remove organic impurities from the surface, especially rest of patterning or protection resist, the TePla 300 microwave plasma system is used. Oxygen plasma is generated by high-frequency radio waves, which ionize low pressure O_2 gas. To remove hardened resist, the plasma power is set to 600 W for 30 min. Reactive oxygen ions combine with the resist components and form volatile ash particles like CO_2, which are removed by vacuum pump.

3.2.2 DC / RF Sputtering

The Oerlikon Univex 450 C is available for metal and oxide thin film deposition. Figure 3.6 shows the sputtering equipment. The sample is loaded into the load lock and chamber atmosphere is pumped down to 10^{-7} mbar by both a turbopump and backing pump in order to achieve clean environmental conditions, avoiding sample contamination. The system offers six separated sputtering chambers (SC) with individual sputtering targets. In this way, mutual contamination of the target materials can be excluded.
In the present work, the following targets are used: Pt (SC5), Ta (SC4) and Hf (SC3). Depending on the particular chamber, the RF or the DC sputtering technique is applied and the target size is either 4 in or 2 in. For enabling physical or reactive sputtering, O_2, Ar or N_2 are available as process gases. The sample can be transferred by a handler-robot from chamber to chamber to deposit subsequently different material layers without breaking the vacuum. Individual sputtering recipes can be programmed with the control unit. This enables automatic execution of the processes and transfer between used chambers.

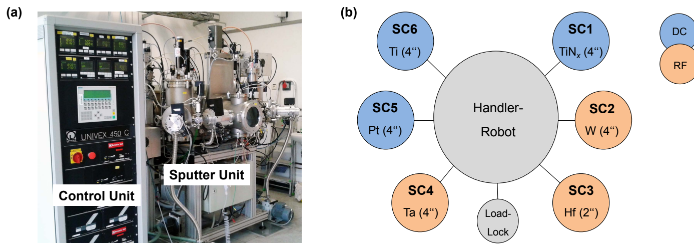


Figure 3.6: Sputtering equipment. (a) Overview about control unit and sputter unit. (b) Scheme of the sputter unit. Six separated sputtering chambers for individual (2″/4″) sputtering targets are available. Depending on the chamber, DC or RF sputtering technique is used. The handler-robot transfers the sample automatically from chamber to chamber.

For the sputtering, a static / high-frequency electrical field is applied between target and sample (DC / RF sputtering). The ionized gas particles are accelerated toward the target, where the surface is bombarded and target particles are ejected out. For reactive sputtering, the target material combines with the gas ions. The particles move toward the sample, where they are absorbed on the surface growing the deposition film. All sputtering processes in this work are performed at room temperature.

3.2.3 Lithography

Depending on the structure size, the deposited films are patterned by different lithography processes: photolithography (micrometer scaled devices) or electron beam lithography (nanometer scaled devices). However, in both cases the processes are similar. The samples are first coated with a lithography resist layer, which is exposed at selected regions to high-energetic particles (controlled by a lithography mask), whereby chemical bonds are changed. Afterwards, these regions are either soluble or insoluble (positive / negative lithography resist) by the used chemical developer and the mask pattern is transferred to the resist.

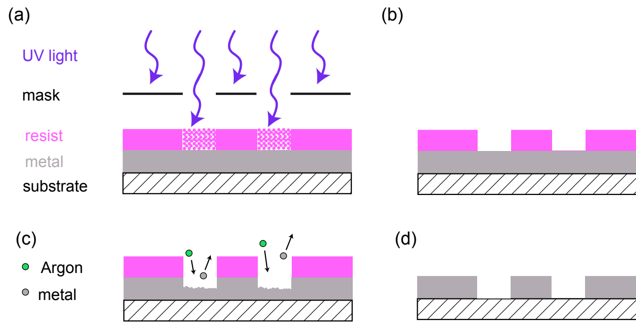


Figure 3.7: Process scheme of film patterning by photolithography. (a) Selective UV light exposure of the positive photoresist by optical mask. (b) Structured resist after development process. (c) Pattern transfer from resist to metal film by physical Ar ion beam etching. (d) Final metal structure on substrate after photoresist removal.

3.2.3.1 Photolithography

A simple process scheme for a particular sample is depicted in Figure 3.7, where the sample is spin coated with positive photoresist. This resist is highly sensitive to UV light. The lithography is performed by Karl Suss MA6 Mask Aligner using an optical mask, which enables selective exposure. The selective regions of the resist, which are exposed to UV light, become soluble and are removed by the chemical developer, whereby the mask layout is transferred to the resist.

3.2.3.2 Electron Beam Lithography

Nanometer scaled structures are realized by the electron beam (e-beam) lithography technique. The spin coated resist is sensitive to high-energetic electrons, which are focused to a fine beam to achieve high resolution. E-beam lithography does not require any optical mask. Using a CAD layout file, the e-beam is controlled for writing the desired pattern (see Figure A.1). Electrons show wave-like characteristics, which are described by the de Broglie hypothesis. The matter wavelength λ is given by

$$\lambda = \frac{h}{p} \tag{3.5}$$

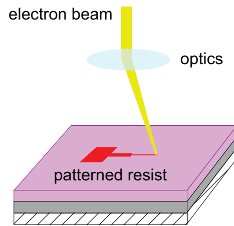


Figure 3.8: Diagram showing the e-beam writing process. Selective exposure of the lithography resist is controlled by electron optics using a CAD layout file.

where h is the Planck's constant and p the electron momentum. Relativistic effects are negligible at acceleration voltages about 50 kV and the momentum is given by

$$p = \sqrt{2 m_\mathrm{e} E_\mathrm{kin}} \tag{3.6}$$

with the electron mass m_e and the kinetic energy $E_\mathrm{kin} = eV_\mathrm{acc}$ (electron charge e, acceleration voltage V_acc). The wavelength is about 5 pm and does therefore not limit the writing resolution (concerning device size from 20 nm to 100 nm).[90, 93] The rather dominant limitation effects are forward scattering within the resist, widening the beam and backscattering caused by the substrate.[94] The backscattered electrons expand the effective beam width, which can cause increased total exposure dose and ultimately damage the desired patterning. This is resolved by using the proximity correction, i.e. the beam base dose is modulated by a mapped correction factor.[94] Exemplary mapping of the correction factor for used nanostructures is presented in Figure A.2.
Here, the Vistec EBPG 5000plus is used as e-beam writer system, whose setup is in principle equivalent to a SEM. In the present work, a negative e-beam resist is used. Therefore, the regions, which are exposed to the e-beam (cf. Figure 3.8), will remain after the developing process. After writing, the post exposure bake is performed, which is required for crosslinking of the exposed resist regions. These regions become insoluble in the chemical developer. Next, the resist patterning is transferred to the deposited films by the etching process.

3.2.4 (Reactive) Ion Beam Etching

The Oxford Ionfab 300 plus, a reactive ion beam etching (RIBE) system, is used to transfer resist patterning into the deposited thin films. The sample surface is etched by ion bombardment (physical dry etching), which is shown schematically in Figure 3.7c. The process gas is ionized by a high-frequency generator (13.56 MHz) and the ions are accelerated toward the sample by ion optics.[95] After passing the optics, the ions are neutralized by a perpendicular electron beam, otherwise the sample would be positively charged.
The etching is performed in a high-vacuum chamber to avoid any surface contamination and undesired interactions of the gas ions with other particles. Due to nature of ion beam, the etching process is anisotropic. However, depending on the etching gas composition, chemical (reactive) etching processes also occur, which are rather isotropic. Tilting the sample during etching is beneficial to remove redeposited material on the substrate or at the resist mask. Here, the RIBE process enables sufficient etching rates (range: nanometer per second) to control structuring of films precisely, which are several nanometers thick.

Chapter 4

Device Fabrication

4.1 Thin Film Characterization

In the present work, resistive switching phenomena in HfO_2- and Ta_2O_5-based ReRAMs are investigated. In order to understand and to explain these effects, the device and material systems have to be clearly defined. Especially fabrication process and device / material development require detailed knowledge of material properties and the impact of individual process steps on the device characteristics. Only the consideration of all relevant correlations enables systematic tuning of device characteristics for successful and efficient memory and computation applications. For example, in Section 5, the influence of the Hf electrode thickness on the resistive switching in HfO_2-based devices is investigated. The experimental data can only be interpreted successfully, if film thickness / deposition rate is known.

Growth Rate The thickness of the grown films is determined by the XRR measurement, which is shown exemplary for Ta_2O_5 in Figure 4.1. The wavelength of the intensity oscillation (the distance between to neighboring intensity maxima) corresponds to the Ta_2O_5 film thickness d, which can be estimated by Equation 3.2. This estimation is possible due to the simple stack structure, since the Si substrate and the SiO_2 thickness are infinite in comparison to the sputtered thin film. Therefore, the sample can be considered as single layer system and Equation 3.2 can be applied. A more accurate result is enabled by the XRR simulations (red curve). In order to reduce the

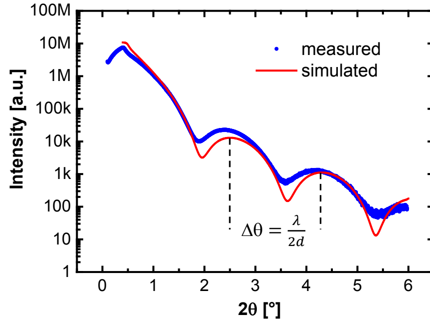


Figure 4.1: X-ray reflectometry (XRR) measurement and simulation of the as-deposited Ta_2O_5 thin film. Period length of the Kiessig oscillations indicates 5 nm film thickness.

parameters, which have to be fit, the film roughness has been measured by AFM. Knowing the sputtering time t_{sp}, the growth rate r_{sp} is determined in the linear regime by Equation 4.1.

$$r_{\mathrm{sp}} = \frac{d}{t_{\mathrm{sp}}} \tag{4.1}$$

Similar measurements have been performed for all used materials and growth parameters, which are used for the present work. Table 4.1 summarizes the calculated growth rates. Considering these growth rates are verified only for films in the thickness range of several nanometers ($d \leq 30\,\mathrm{nm}$), the same need not be valid for thicker films. Under same sputtering conditions (equal parameters), deposition rate of the Ta_2O_5 and the HfO_2 thin films are different, since the sputtering target size is different (Hf target: 2 in, Ta target: 4 in).

Surface Roughness Surface roughness of the thin film is an important parameter, which might affect the switching properties of the devices. For example, a rough Pt surface might promote short circuits in the memory stack, which directly connects the bottom electrode with the top one while bypassing the oxide layer. Therefore, surface roughness investigation of each individual material (including the sputtering conditions) is carried out by the AFM (see Appendix Section A.2). For each case, the surface roughness is negligible in comparison to the used film thicknesses ($d \geq 5\,\mathrm{nm}$).

Table 4.1: Growth rates for the sputter deposition of the used materials and sputtering parameters.

Material	RF / DC* Power [W]	rel. O_2 flow [%]	growth rate [nm/min]
Hf	116	0	24
Hf	58	0	11
Ta	116	0	9.2
Pt	375*	0	106
HfO_2	116	13	3.0
HfO_2	116	23	3.0
HfO_2	116	30	3.0
HfO_2	58	23	1.2
HfO_2	174	23	5.5
HfO_2	232	23	6.7
Ta_2O_5	232	23	3.2

Material Structure Next, the thin film structure of the switching oxides is investigated by GIXRD analysis. Figure 4.2 shows the summarized experimental results for HfO_2 and Ta_2O_5. Both oxides have been sputtered using the relative 23 % O_2 gas flow. The RF sputtering power is 116 W for HfO_2 and 232 W for Ta_2O_5. The absolute signal intensity is not considered and measurement results are shifted on the intensity axis for the better comparison. The used grazing incident angle α for the x-ray beam is 1.5 °. Each measurement has been performed over several days in order to improve the statistics, especially for low intensity peaks.

At the beginning, the blank non-treated and the blank annealed thermally oxidized Si substrates (about 430 nm of SiO_2 on top) are investigated (see Figure 4.2a) to identify possibly visible substrate peaks. The thermal treatment has been performed at 750 °C for 5 min in nitrogen gas atmosphere. Generally, the x-ray penetration into the substrate is low that substrate x-ray reflexes are not visible or very reduced in intensity. Due to the substrate orientation the Si (311) peak (space group $F\,d\,\overline{3}\,m$ (No. 227); diamond structure) is still visible. The peak observation could be avoided by rotation of the substrate.

Nevertheless, the Si substrate diffractogram is not changed by the thermal annealing procedure. Only the Si (311) intensity is lowered for the annealed sample, which can be attributed to a slight difference in the substrate orienta-

tion. The as-deposited HfO_2 does not differ significantly in the x-ray intensity distribution (Figure 4.2a, red data points) from blank substrates, excluding the slight intensity uprising in the 2θ range from 25 ° to 35 °. This effect indicates an additional amorphous film on the substrate. Next, the as-deposited HfO_2 film is annealed (same parameters as for the blank substrate).
The GIXRD measurement on the annealed HfO_2 film (Figure 4.2(a,b), green data points) shows several reflection peaks. The HfO_2 exhibits a structure transition from the amorphous to a nanocrystalline phase, which is indicated by the peak broadness. The peak positions are compared with experimental data from the Inorganic Crystal Structure Database (ICSD) to identify the crystal structure. The annealed HfO_2 offers the monoclinic crystal structure (space group $P\ 2_1/c$ (No. 14); cf. Figure 4.2b). Detailed information about the space groups are presented in the International Tables for Crystallography.[96]
The same experiment has been performed for Ta_2O_5 (see Figure 4.2c). The as-deposited film does not show any diffraction peak, whereas annealing at 800 °C for 5 min in nitrogen gas atmosphere causes a phase transition from the amorphous state to the nanocrystalline orthorhombic structure (space group $A\ m\ m\ 2$ (No. 38); see Figure 4.2d).

Material Composition To determine the material composition or rather the metal cation and oxygen anion ratio, XPS analysis has been performed. HfO_2 and Ta_2O_5 are in the same way sputtered as the samples used for the XRD experiments. The sputtered films are exposed to a monochromatic Al-K_α ($h\nu = 1486.6$ eV) beam in the large area mode (spot size: 1.4 mm × 200 μm). The survey scan of HfO_2 in Figure 4.3a shows the relevant core levels of O-1s, C-1s and Hf-4f, which are highlighted by dark blue labeling.
For quantification of the survey scan, the MultiPak analysis software is used. The peak fitting using a mixed Gaussian-Lorentz function and the calculation of Shirley background is performed by the software UNIFIT 2014. First, the energy level has to be calibrated by shifting the C-1s peak to 285.0 eV (see Figure 4.3d), which is typical for common surface contamination by carbon.[97] Subtraction of the Shirley background is a correction method. This includes the background intensity enhancement by inelastically scattered elec-

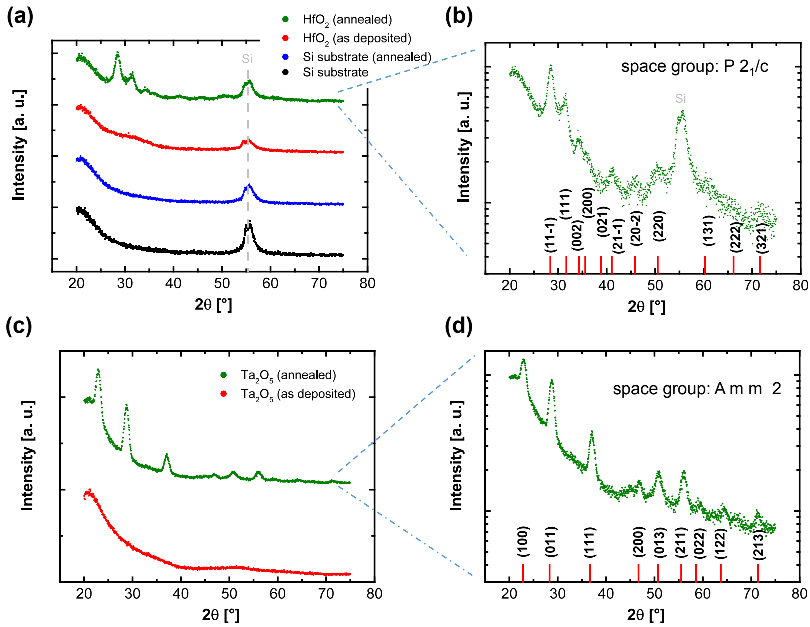


Figure 4.2: GIXRD analysis for as-deposited (a) HfO_2 and (c) Ta_2O_5. As comparison, the films have been annealed (b, d). Additionally, the blank non-treated and the blank annealed Si substrate have been considered (a) to identify the substrate peaks (vertical dashed line). The as-deposited films are GIXRD-amorphous. The annealed films are nanocrystalline and the corresponding space group is identified by the diffraction peaks (b, d). Only the peaks with the largest energy are labeled.

Table 4.2: Determined parameters from the XPS analysis of as-deposited HfO_2 with 23 % O_2 sputtering gas flow and 116 W RF sputtering power. (With kind approval of A. Besmehn, ZEA-3, FZ Jülich)

Peak	Compound	E_B [eV]	Area [cps · eV]	RSF	corr. Area	C_{at} [At.-%]
O1s	HfO_2	530.10	14765.9150	0.773	20143.131	51.41
O1s	OH-, O+C	531.94	2400.0978	0.773	3274.349	8.36
C1s	C-C, C-H	285.00	999.17416	0.314	3182.083	8.12
C1s	C-OH	286.18	346.0040	0.314	1101.924	2.81
C1s	COOH	288.98	225.8021	0.314	719.115	1.84
Hf4f	HfO_2	16.67	31227.6010	2.901	10764.426	27.47

trons, which are caused by the photoelectron peaks.[97] Figure 4.3b depicts the Hf-4f spectrum. The peak is split into a doublet due to spin-orbital interaction[97]: the higher energetic $Hf^{4+}_{4f5/2}$ peak (18.3 eV) and the lower energetic $Hf^{4+}_{4f7/2}$ peak (16.7 eV).[2] Furthermore, the spectrum proves hafnium shows a single chemical state (as expected for hafnium oxide). The peak energy positions are consistent with values published for HfO_2 in literature.[98, 99] The O^{2-}_{1s} spectrum at 530.1 eV is presented in Figure 4.3c. The main peak exhibits a shoulder around 532 eV, which is explained by surface contamination of hydrogen-oxygen compounds.[99, 100] All relevant parameters extracted by the XPS spectra are summarized in Table 4.2. The composition ratio of Hf : O is about 1 : 1.9, which is determined by the area ratio of the corresponding peaks, i.e. the oxide might be slightly reduced. However, this difference is still within the measurement accuracy.[2]

The variation of the relative O_2 sputtering gas flow has no impact on the XPS spectrum and therefore the Hf : O ratio remains unchanged (cf. Figure 4.4). The tabular results are presented in Appendix Section A.3. RF sputtering power variation does also not influence the composition ratio.

XPS analysis of the Ta_2O_5 film is depicted in Figure 4.5. The survey includes the relevant core levels of O-1s, C-1s and Ta-4f. The C-1s peak position is used for energy level calibration. Similar to the HfO_2 spectrum, the Ta-4f peak is split into a doublet.[2, 3] The two peaks (26.8 eV, 28.2 eV) correspond to the Ta-$4f_{5/2}$ and Ta-$4f_{7/2}$ orbitals, indicating Ta^{5+} in Ta_2O_5.[101] The atomic percentage ratio of Ta to O (of Ta-O compounds) is around 0.4. This result verifies the correct stoichiometry of Ta_2O_5 within the experimental accuracy.[3]

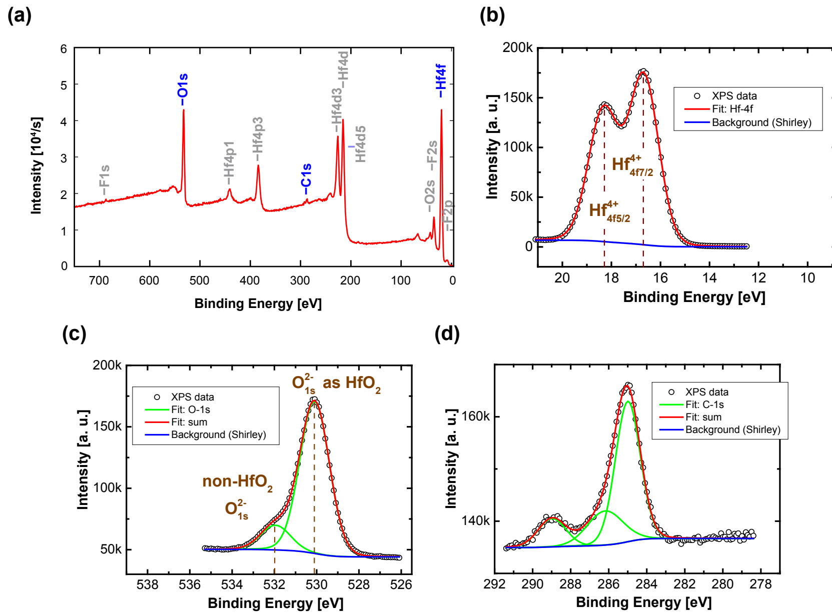


Figure 4.3: XPS analysis of as-deposited HfO_2. (a) Survey scan with highlighted core levels (blue labeled), which are further investigated. (b) Detailed scan of the Hf-4f peak, which is split into a doublet. (c) Detailed scan of the O-1s spectrum. (d) Detailed scan of C-1s peak caused by typical surface contamination by carbon, which is used for the energy level calibration. (With kind approval of A. Besmehn, ZEA-3, FZ Jülich)

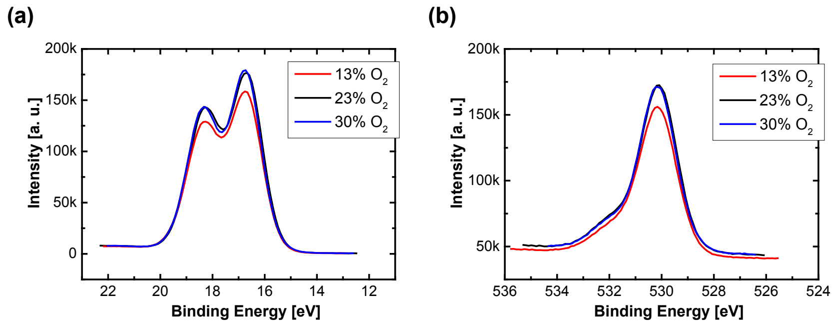


Figure 4.4: XPS of as-deposited HfO_2 for different relative O_2 sputtering gas flow. (a) Hf-4f spectra and (b) O-1s spectra. The variation of relative O_2 sputtering gas flow does not change the composition ratio of Hf and O. (With kind approval of A. Besmehn, ZEA-3, FZ Jülich)

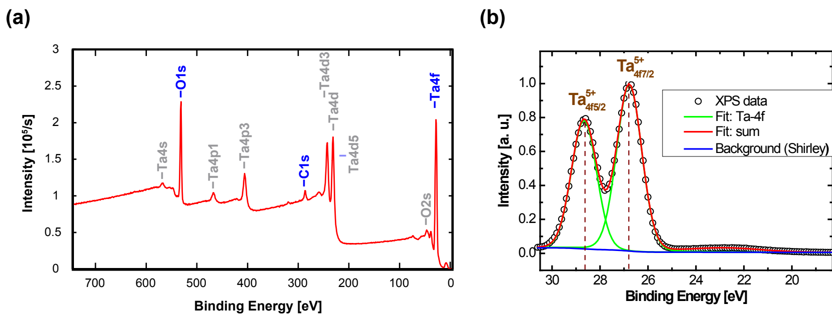


Figure 4.5: XPS of as-deposited Ta_2O_5. (a) Survey scan with highlighted core levels (blue labeled), which are further investigated. (b) Detailed scan of the Ta-4f peak, which is split into a doublet. (With kind approval of A. Besmehn, ZEA-3, FZ Jülich)

4.2 Bipolar / Complementary Switching Devices

In this thesis, all biploar / complementary switching devices have been fabricated on thermally oxidized silicon wafers.[2] The thickness of the SiO_2 is about 430 nm. Next, 5 nm thick Ti (as adhesive layer) and 30 nm thick Pt are deposited.

Figure 4.6 depicts the subsequent fabrication flowchart. The fabrication procedure is separated into two steps (bottom electrode (BE) and top electrode (TE) layer patterning). At the beginning, the substrate is covered by a protection resist layer for dicing the wafer into 1 in × 1 in samples. The resist is removed by cleaning the sample in the acetone ultrasonic bath for 5 min. That is followed by another ultrasonic treatment in isopropanol in order to avoid residues of the highly volatile acetone. Then, the sample is dried with a nitrogen gas pistol. In order to remove the possible organic impurities, the sample is exposed to oxygen plasma by a plasma asher at 600 W for 30 min. Next, the sample is pre-baked at 120 °C for 5 min to remove adhesive water molecules, which could debase the adhesion between substrate and resist.

Afterwards, AZ 5240E (positive photoresist) is spin coated using 4000 rpm for 30 s (pre-spin coating: 1000 rpm for 5 s). This step generates a 400 nm photoresist (PR) thickness, which is confirmed by the profilometry measurement in Figure 4.7. Thinner photoresist enables smaller structures, but it should exhibit a sufficient thickness to endure the later etching procedure. That has to be checked by the photoresist etching rate and the required etching time to transfer the resist patterning into the layer stack. Afterwards, the PR is dried (softbake) at 90 °C for 5 min. Next, the substrate is covered with the optical mask in the vacuum contact mode and exposed to UV light (313 nm) for 25 s. The exposed resist regions are removed by immersing the sample into AZ 326 MIF (resist developer) with continuous stirring for 120 s. The development process is stopped by rinsing in ultrapure water for 5 min. Finally, the mask pattern is transferred into the PR layer.

Then, the PR pattern is transferred with the help of the (reactive) ion beam etching process into the Pt and Ti layer. Here, the metals are etched by Ar particles at −10 ° (beam incident angle) for 120 s. An additional Ar etching at

$-50°$ for 30 s is required in order to reduce fences and redeposited material. The etching rate of AZ 5204E is around 9 nm/min and the total etching time is not critical for the 400 nm thick resist layer. Finally, remaining photoresist is stripped by putting the substrate into acetone overnight. On the next day, the sample is polished gently in acetone using a swabbing stick. Figure 4.8 shows the effect of wiping the sample in acetone, observed under an optical microscope and SEM. Compared to the polished sample (cf. Figure 4.8(c,d)), the non-treated one (cf. Figure 4.8(a,b)) shows fences at the structural edges. After the swapping step, the sample is cleaned in an ultrasonic bath in fresh acetone and isopropanol for 5 min.

In the following, Pt|HfO_2|Hf|Pt stacked devices are considered. The switching oxide and the electrode material(s) are deposited by sputtering process. The HfO_2 layer is sputtered reactively by applying a RF electrical field and the Hf target is used as a metal source in combination with a gas mixture of Ar and O_2. The process pressure is around 2.3×10^{-2} mbar. For the HfO_2 device fabrication, the argon-oxygen gas mixture and the RF sputtering power is varied (see Chapter 5). The Hf metal layer is deposited with 116 W RF power using the Hf target in 100 % Ar gas ambiance (2.3×10^{-2} mbar). In Chapter 5, the impact of the Hf electrode thickness on the switching characteristics is presented. At last, the Pt capping metal layer is sputtered using a DC power generator at 375 W with Ar sputtering gas (1.44×10^{-2} mbar). All depositions are carried out at room temperature and without breaking the vacuum.

Next, the top electrode structure is transferred into the last three deposited layers by using the photolithography and RIBE processes. In general, the individual steps are identical to the BE layer pattering process, except for the applied optical mask and the RIBE parameters. The oxide is etched reactively by CF_4 at $0°$ (beam incident angle), whereas the metals are etched by pure Ar at $0°$. Here, the redeposition is not that critical as for the previous etching, since no further film will be deposited. Etching the oxide layer with Ar should be avoided, since the Ar ambiance reduces the oxide layer. Furthermore, etching of the oxide with CF_4 provides a higher selectivity between the HfO_2 and the subsequent Pt bottom electrode. This protects the Pt BE against huge damage by slight over-etching. The etching rate of AZ 5204E is around 29 nm/min with CF_4 and also not critical (regarding used etching time

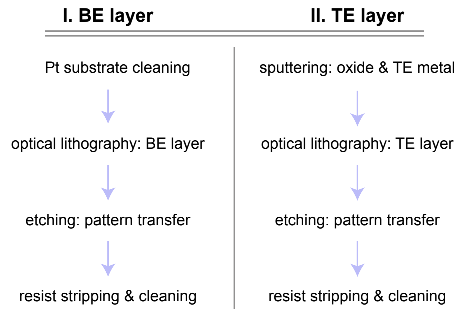


Figure 4.6: Flowchart of bottom electrode (BE) and top electrode (TE) layer for micrometer scaled BS and CS devices.

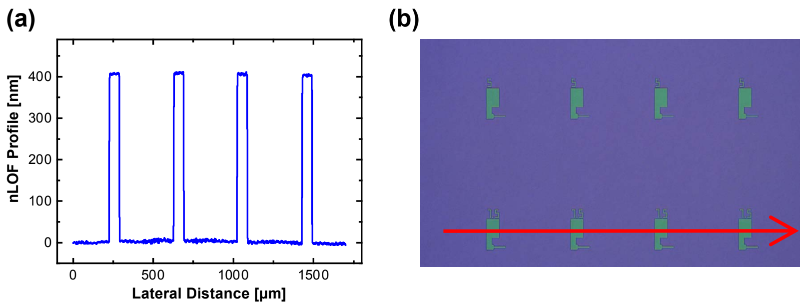


Figure 4.7: (a) Profilometry of patterned AZ 5204E photoresist by the Dektak 150 Surface Profiler. (b) Optical microscopy of the scanned path.

and PR thickness). After patterning the device, any plasma cleaning treatment in asher should be avoided, because the oxygen plasma will increase the device resistance (further oxidation), which could result in higher forming voltages or even damage the resistive switching properties. In the end, the crosspoint of the bottom and top electrode layer forms the complete Pt|HfO_2|Hf|Pt cell stack. All device parameters are summarized in Table 4.3.
The SEM image (topview) of ReRAM devices with the Pt|HfO_2|Hf|Pt crosspoint stack is demonstrated in Figure 4.9.[2] The complete device structure (see Figure 4.9a), especially the cross-junction (see Figure 4.9b), which represents the memory cell, is well defined. In Section 7.3, the proof-of-concept for computation-in-memory applications is performed, which requires crossbar arrays of ReRAM cells. The used 1×8 crossbar array is presented in Figure 4.9c.

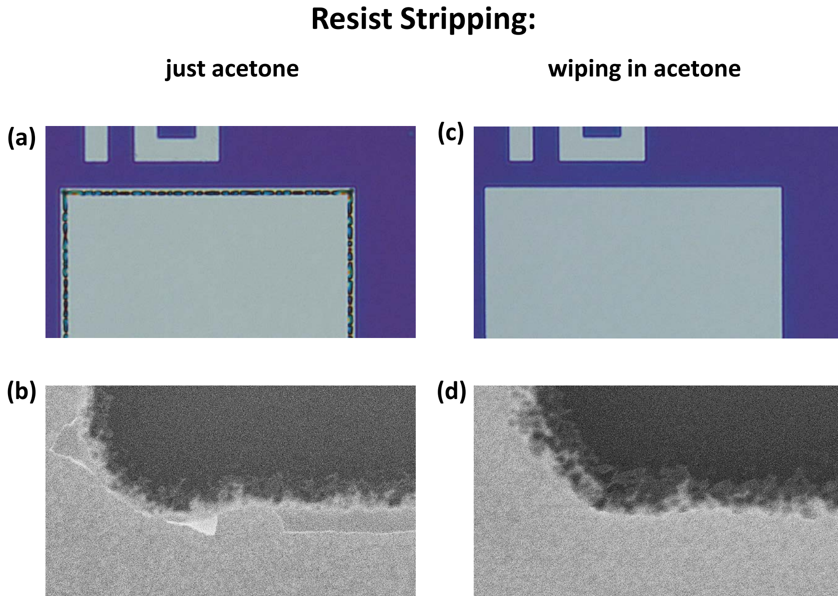


Figure 4.8: Optical and SEM image about the impact of photoresist stripping (a,b) without and (c,d) with swabbing in acetone.

Table 4.3: Deposition parameters of the HfO_2-based device fabrication processes. Parameter variations are highlighted by red lettering.

#	d_{HfO_2} [nm]	d_{Hf} [nm]	Ar-O_2 sputtering gas ratio	RF Power [%}
1	5	5	90 : 10	20
2	5	5	83 : 17	20
3	5	5	77 : 23	20
4	5	5	77 : 23	20
5	5	10	77 : 23	20
6	5	15	77 : 23	20
7	5	30	77 : 23	20
8	5	15	77 : 23	10
9	5	15	77 : 23	20
10	5	15	77 : 23	30
11	5	15	77 : 23	40

For the switching properties, the view of a cross-section of the cell stack is interesting in the same way.[2] Therefore, a TEM lamella has been cut from the cross-junction by FIB preparation (as-deposited stack: 30 nm Pt | 5 nm HfO_2 | 5 nm Hf | 25 nm Pt). Figure 4.10a shows a STEM overview of the considered cell area. The orange arrow indicates the scanning path, which is investigated in detail by an EDX line profile scan. Figure 4.10b presents the detected counts for the individual elements on a logarithmic scale as function of the EDX line scan. The significant Pt signal originates from the BE and TE region. The top Pt has penetrated into the lower stack, since the Pt atoms strike with high kinetic energy on the sample during sputtering process.
In spite of the low intensity, the O signal is quite symmetric and congruent with the Hf signal, i.e. oxygen ions have diffused from the HfO_2 into the Hf layer. The Hf here serves as an oxygen getter and extracts oxygen out of the HfO_2 layer, which becomes reduced, resulting in the oxidized Hf layer. The total oxide thickness has thus increased from 5 nm to 10 nm. This effect has an important impact on the ReRAM switching properties as demonstrated in Chapter 5. Due to the low oxygen signal (concerning the noise level), the EDX measurement does not provide detailed information about the oxygen profile (e.g. homogeneous or gradual oxygen concentration profile), which could be investigated further by long term experiments. The HRTEM image in Figure 4.10c confirms the oxygen diffusion, since the Hf and HfO_2 regions are not distinguishable. The entire oxide layer seems to be amorphous in accord with the GIXRD experiment in Section 4.1.

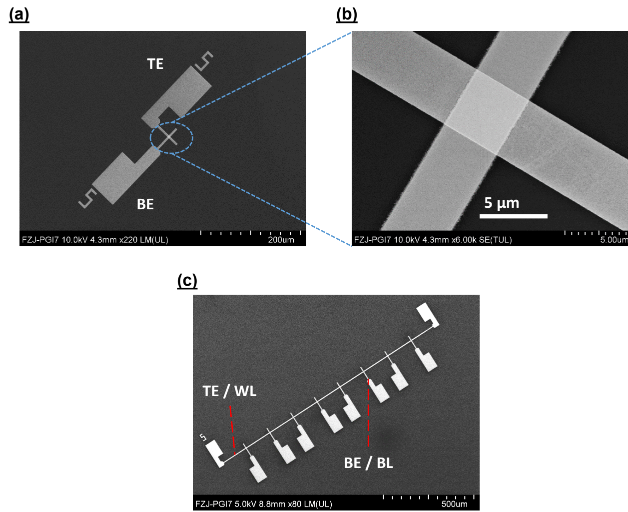


Figure 4.9: SEM images of micrometer scaled devices. Line width of the BE and TE is 5 μm, which are referred to as wordline (WL) and bitline (BL) in Section 7.3.

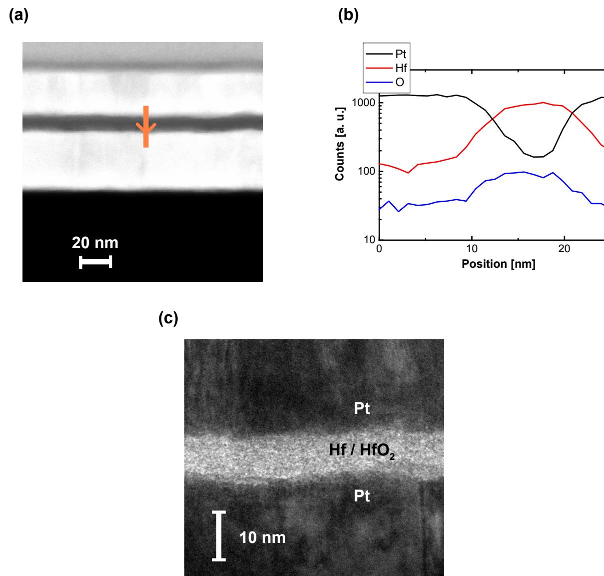


Figure 4.10: (a) STEM image of cell stack (30 nm Pt | 5 nm HfO_2 | 5 nm Hf | 25 nm Pt as-deposited). The orange arrow indicates the path used for EDX line profile scan in (b). (c) HRTEM image. The as-deposited Hf film is fully oxidized.

4.3 Complementary Resistive Switching Devices

In this work, two types of complementary resistive switching (CRS) device configurations have been fabricated.[3] One configuration is designed with access to the middle electrode (ME), which is called structure A for further discussion (three-terminal device). That allows one to investigate the impact of the ME (see Chapter 6). Furthermore, the physical third terminal becomes also interesting for specific devices application (cf. Section 7.1) The second configuration, referred to as structure B, does not exhibit any access to the ME (two-terminal device).
The starting point for each device preparation is a thermally oxidized Si substrate wafer deposited with 5 nm thick Ti and 30 nm thick Pt on top. The Ti film acts as adhesive layer between SiO_2 and Pt. Table 4.4 gives an overview about the different types of CRS device structures.
Required material layer deposition has been performed under the following conditions: Ta_2O_5 is reactively sputtered by using a Ta target as metal source. The gas mixture of oxygen (23 %) and argon (77 %), at chamber pressure of 2.3×10^{-2} mbar, serves as sputtering gas and oxygen source.[3] The applied RF sputtering power is about 116 W. Elementary Ta films are deposited using the RF power generator (116 W) with pure argon (100 %) sputtering gas. The sputtering process for Pt and the used etching gases for patterning the individual layers are identical to the processes used for the BS / CS ReRAMs (see Section 4.2).

Table 4.4: Comparison of available CRS device design specifications. Consider, micro-BC and nano-BC refer to the size scaling dimension of the bottom cell (BC).

Name	structure A	structure B	
No. of terminals	3	2	
Type	micro-BC	micro-BC	nano-BC
Ta_2O_5 thickness	10 nm	10 nm	5 nm
Ta thickness	10 nm	5 nm	5 nm
Ta_2O_5 thickness	10 nm	10 nm	5 nm

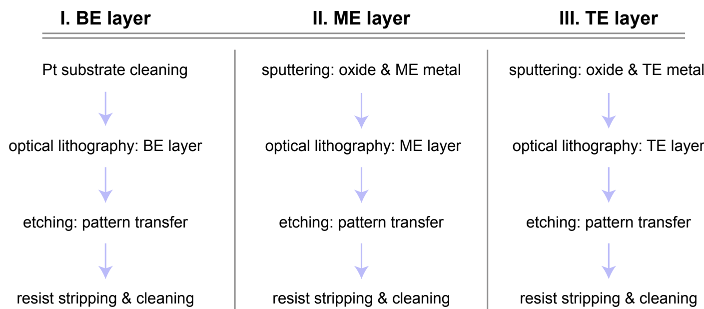


Figure 4.11: Flowchart for the three-terminal micro-BC CRS device, referred to as structure A. The complete process requires three processing steps: bottom electrode (BE), middle electrode (ME) and top electrode (TE) layer patterning.

4.3.1 Three-Terminal Devices

The fabrication process of the three-terminal micrometer scaled CRS device is separated into three main steps, which are only distinguishable in in some parameters: BE, ME and TE layer. The non-detailed process flow is summarized in Figure 4.11. The BE layer structuring is absolutely identical to the one used for BS / CS ReRAMs. Subsequently, Ta_2O_5 (as first active oxide) and Ta (as ME metal) are deposited. The ME patterning is transferred to both films by optical lithography and dry etching by the RIBE system.
After the removal of remaining photoresist, Ta_2O_5 (as second active oxide) and Pt as TE metal are grown by sputtering. These two films are structured by the TE layer. The BC is defined by the intersection of the BE and ME layer ($Pt|Ta_2O_5|Ta$), whereas the TC by the crossing area of the ME and TE layer ($Ta|Ta_2O_5|Pt$). The final structure is presented by SEM images (overview and magnification of cross-junction) in Figure 4.12.

4.3.2 Two-Terminal Devices

The two-terminal CRS device is preferred for the integration in passive crossbar arrays for memory and computing applications. Here, both micrometer and nanometer scaled devices have been realized.

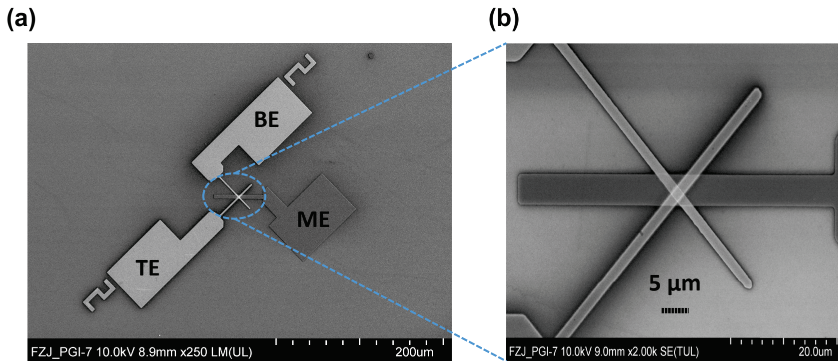


Figure 4.12: SEM images of three-terminal micro-BC CRS device. (a) Device overview and (b) magnification of the cross-junction region.

4.3.2.1 Micrometer Scaled Devices

The two-terminal micrometer scaled CRS device requires processing of two layers. Thus, the fabrication flow (see Figure 4.13) is equivalent to the one used for micrometer scaled BS / CS devices.[3] The Ti|Pt layer is patterned by BE layer, whereas Ta_2O_5|Ta|Ta_2O_5|Pt stack is structured by the TE layer. Due to the simple structure, the two-terminal CRS device looks identical to CS / BS device (cf. Figure 4.9).

4.3.2.2 Nanometer Scaled Devices

Starting point for the nano-BC CRS device is the thermally oxidized Si substrate.[3] The nanometer scaled Pt bottom electrodes have already been structured by a UV nanoimprint process, developed and optimized by Lentz.[90] These steps are therefore not shown in the process flowchart in Figure 4.14. At the beginning, the substrate is covered with protection resist from the wafer dicing into 2 cm × 2 cm samples. The resist is removed as described for the BS / CS devices in Section 4.2.
On the patterned BE, the Ta_2O_5|Ta|Ta_2O_5|Pt stack is deposited in-situ by using the sputtering process.[3] The sample is heated to 120 °C for 5 min in order to remove adhesive water molecules. Next, the AZ nLof 2020 (negative e-beam resist), which has been mixed with AZ EBR (thinner) (resist : thinner = 1 : 2), is spin coated on the substrate with 3000 rpm for 30 s (pre spin coating:

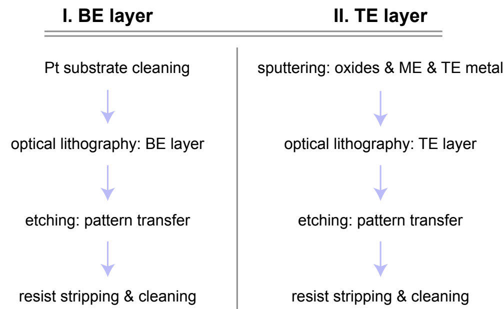


Figure 4.13: Flowchart for two-terminal micro-BC CRS device. The complete process requires two processing steps: bottom electrode (BE), middle electrode (ME) and top electrode (TE) layer patterning.

1000 rpm for 5 s). The resist thickness of 280 nm is verified by the profilometer scan presented in Figure 4.15. The resist is then dried on a hot plate at 100 °C for 3 min (softbake).
The TE layer (cf. Appendix Figure A.1) is patterned by e-beam writer (Vistec EBPG 5000plus), using the parameters as depicted in Table 4.5. For alignment of the top electrode to the bottom electrode layer, the tool is switched to SEM mode and the alignment markers on the sample are captured. After writing, a post exposure bake (PEB) is performed at 110 °C for 3.5 min, which is required for the cross-linking process of the exposed resist. The resist is developed by AZ 726 MIF for 50 s. The development is stopped in ultrapure water by the overflow rinse.
The sample is etched in the RIBE system. In order to remove any residue, i.e. undeveloped part of the e-beam resist (between the desired structures), the sample is treated with a low-current oxygen beam. This generates a sharper structure profile as is demonstrated by the comparison of two samples (with and without low-current oxygen beam treatment) in Figure 4.16.
After the completion of the etching process, the residual e-beam resist is removed by TechniStrip NI555 (resist stripper) overnight. The next day, the stripper is heated up to 80 °C for 2 h and the sample is polished gently using a swabbing stick in warm TechniStrip NI555. Afterward, the sample is cleaned by ultrasonic bath in acetone and isopropanol, for 5 min, followed by drying with the nitrogen gas pistol.

Table 4.5: E-beam writing parameters for the nano-BC CRS device (top electrode layer).

	coarse structure	fine structure
beam current	20 nA	200 pA
resolution	50 nm	5 nm
dose	28 μC/cm^2	33 μC/cm^2

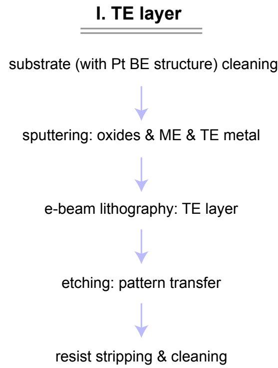


Figure 4.14: Flowchart for two-terminal nano-BC CRS device. Starting point is the substrate with structured Pt bottom electrode (BE) and only the top electrode (TE) layer processing is required

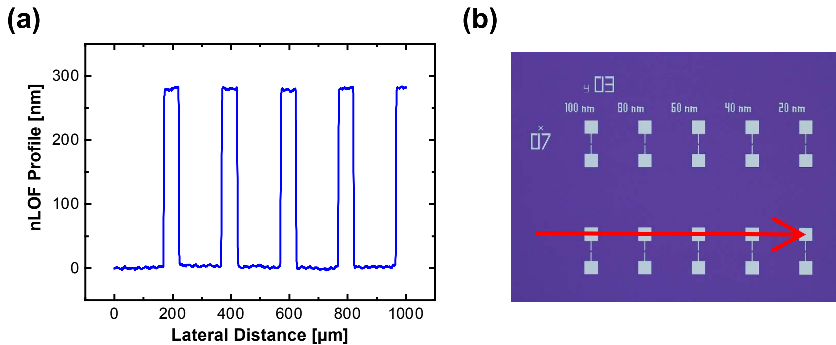


Figure 4.15: (a) Profilometry of patterned AZ nLOF 2020 e-beam resist, thinned with AZ EBR (ratio resist : thinner = 1 : 2). (b) Optical microscopy image of the sample. The scan area is marked with the red arrow.

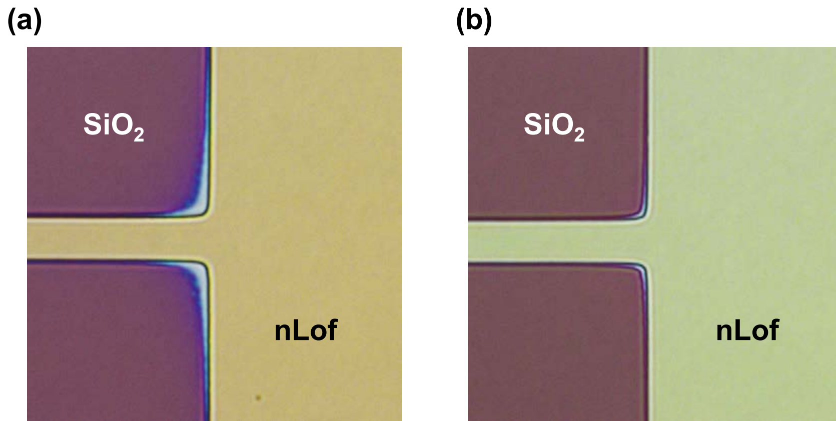


Figure 4.16: Effect of the low-current oxygen beam treatment with subsequent profile etching. (a) With and (b) without low-current oxygen beam. The oxygen treatment enables sharper profiles.

Figure 4.17 shows SEM images of the 1×4 nano crossbar array with one BE and four TE lines, where each cross-junction represents an individual CRS device.[3] A deeper view on the device stack is given by the TEM image in Figure 4.18. The cross-section does not show the full stack. Due to a miss cut, only the TE line on the SiO_2 substrate is present. All material layers are clearly distinguishable. As deposited, both Ta_2O_5 films should offer the same thickness. However, the top oxide layer is slightly thicker, which is attributed to the fabrication process. Whenever the top Ta_2O_5 film is reactively sputtered, the Ta layer is exposed to the oxygen sputtering gas and oxidizes.

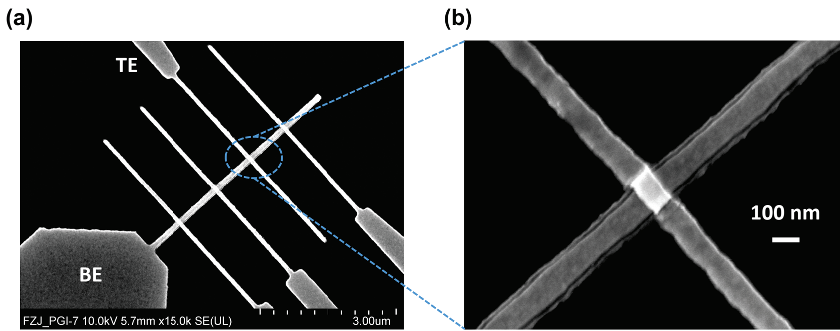


Figure 4.17: SEM image of the two-terminal nano-BC CRS device. (a) overview of the 1×4 crossbar array and (b) magnification of a cross-junction representing an individual CRS device.

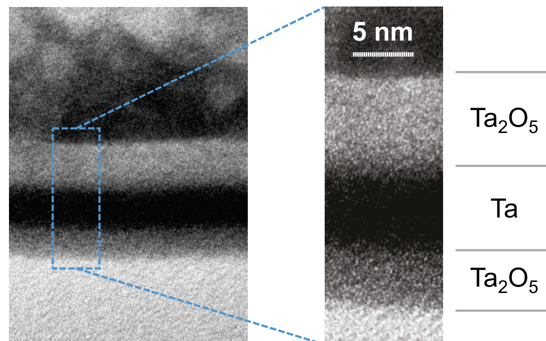


Figure 4.18: TEM cross-section image of two-terminal nano-BC CRS device. Metal and oxides are clearly resolved.

Chapter 5

Resistive Switching in HfO_2-based Devices

5.1 Complementary vs. Bipolar Switching

ReRAM switching characteristics can be controlled and optimized by numerous fabrication parameters. Material engineering is as important as device designing. In this chapter, the influence of fabrication process parameters on switching properties of HfO_2-based ReRAMs is investigated. Here, the focus is on the sputtering process (e.g. sputtering rate and Hf electrode thickness). The fabrication process of the HfO_2-based stack (see Figure 5.1) is described in Section 4.2.
First, the cell stack 30 nm Pt | 5 nm HfO_2| 5 nm Hf | 25 nm Pt is considered.[2] The electrical measurements have been performed on the Agilent B1500A parameter analyzer. Figure 5.1 depicts the used measurement scheme for the two-terminal ReRAM devices. The sweeping voltage signal is applied to the top electrode (TE), whereas the bottom electrode (BE) is on ground.
In general, the micrometer scaled cells exhibit an initial highly resistive state.[2] Therefore, an electroforming procedure is required to grow a conductive filament, which is partially ruptured and subsequently regrown during the subsequent switching. In order to protect the device from over-voltage and to limit the operation current, a current compliance (CC) is applied during the forming process, since the cell toggles abruptly from a high resistance state (HRS) to a low resistance state (LRS).

Figure 5.2 shows the electroforming I-V characteristic (red curve). The virgin device is highly resistive around few MΩ (at 0.2 V read voltage).[2] For the electroforming procedure, positive voltage sweep is applied (1). Around 2.3 V, the current increases abruptly, but is limited to 500 μA by the instrument CC. Finally, the device is formed and its state is set to Z = HRS/LRS (2). In the following, the device is switched without using the instrument CC. The device shows the symmetric complementary switching (CS) (blue I-V curve).[2]
The CS characteristic is explained by alternating rupture and regrowth of the conducting filament at the two interfaces Hf|Pt (A) and Pt|HfO_2 (B).[2, 71] Any filamentary rupture at one interface causes local high resistivity (HRS), whereas an non-ruptured filament region is related to local low resistivity (LRS). For example: in the CRS state Z = HRS/LRS, interface A offers the HRS, whereas interface B shows the LRS.
After electroforming procedure, a negative ramped voltage is applied. The CS changes via transition state 'ON' (see Figure 5.2 (3), non-broken filament) to the Z = LRS/HRS state (4), where the conduction path is ruptured at interface B. Subsequently, a positive voltage sweep is applied resulting in regrowth of the filament at interface B and 'ON' transition state (5). Next, the filament ruptures again at interface A (6) and the CS switches to Z = HRS/LRS.
The self-limiting current characteristic is attributed to interactive switching at the two interfaces. A lower LRS (higher conductivity) of interface A would work as a higher current compliance for switching at interface B. That would result lower LRS at interface B. The same applies to the opposite case. This is referred to as the self-compliance behavior of the CS device. 95 % of the tested devices works properly and show the complementary switching.
However, the complementary switching is not the only switching mode which is offered by the HfO_2-based stack. Figure 5.3 illustrates the feasibility of the bipolar switching (BS) in (a) the eight-wise and (b) the counter-eight-wise switching mode. By applying the current compliance during the voltage sweep for one polarity, the bipolar switching is established. An instrument CC for the positive voltage polarity suppresses the switching at interface A resulting in the eight-wise mode. The additional switching at interface A would be required for the CS behavior as indicated by the pale, light purple color.
To realize the counter-eight-wise switching mode, the CC is applied during

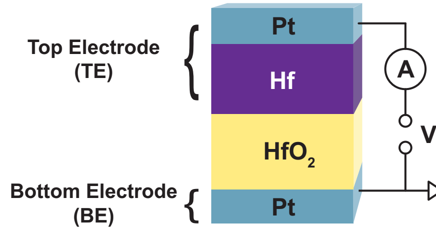


Figure 5.1: Measurement scheme for HfO_2-based devices. The sweeping voltage stimulus is applied to the Hf|Pt top electrode (TE), whereas the Pt bottom electrode (BE) is grounded.

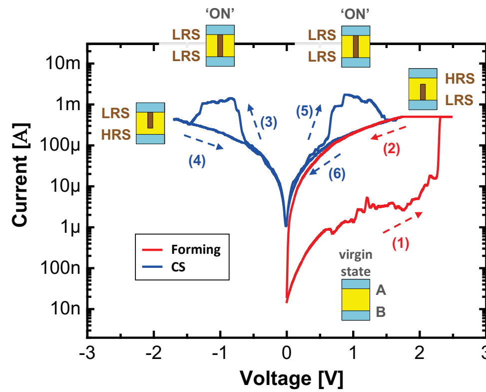


Figure 5.2: Electroforming I-V characteristic (red curve) and subsequent CS cycle (blue I-V curve) in HfO_2-based devices. The insets indicate the resistance scheme at the electrode interfaces A and B.[2] (Redrawn with permission from the publisher.)

the negative voltage sweep. That allows the switching at interface A but not at interface B (see Figure 5.3b). The RESET process requires high current for the Joule heating effect to rupture the filament. Therefore, no CC is used for the RESET process, since that would be counterproductive and the device would not function properly.

All three switching modes are experimentally achievable in the same device as a function of the CC as depicted in Figure 5.4. However, the cell prefers the symmetric complementary switching as long as it is not influenced by an extrinsic factor (e.g. external CC). The symmetric CS I-V curve gives a clear indication that the device does not anymore offer an asymmetric stack, which is contradictory to the as-deposited layers. This presumption is confirmed by TEM and EDX analysis demonstrated in Figure 4.10. The Hf and the oxide region cannot be distinguished in the HRTEM image. The EDX line profile scan indicates clearly the oxygen scavenging effect by the Hf electrode. Oxygen has partially diffused from the as-deposited HfO_2 region into the as-deposited Hf layer, which is completely oxidized and the overall oxide thickness $d_{\mathrm{HfO}x}$ increases from 5 nm to 10 nm. This results in the rather symmetric oxide distribution profile.

The initial cell offers a rather asymmetric I-V characteristic, since the actual electroforming voltage values differ for positive and negative voltage polarity. Devices formed by positive polarity, requires the forming voltage V_{FORM} around 2.1 V (see Section 5.2), whereas such devices formed by negative polarity requires $V_{\mathrm{FORM}} \approx -2.7$ V and the current increase is less abrupt. Consider, the negative forming does not change the switching polarity in the BS mode, the cell is rather electroformed to the high resistance state, which is switched to LRS by applying a positive voltage.

The asymmetric characteristic arising in the initial device can be explained by a model, using the modulation of TE cap work function by oxygen incorporation.[6] During the electroforming process, where the conductive oxygen vacancy filament is grown, the hafnium oxide work function becomes symmetric at both Pt interfaces, resulting in the symmetric complementary switching.

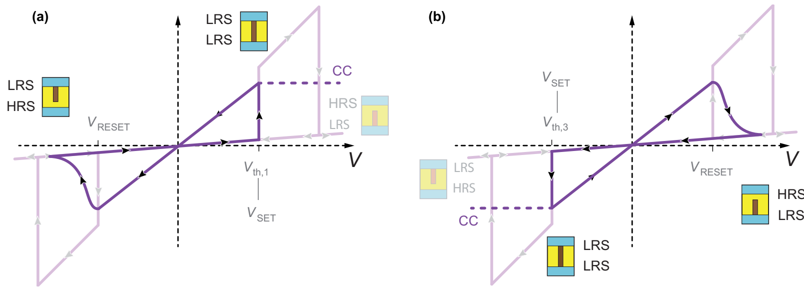


Figure 5.3: Complementary switching (CS) vs. bipolar switching (BS) in HfO_2-based devices. BS *I*-*V* characteristic (a) in the eight-wise switching mode and (b) in the counter-eight-wise switching mode. The insets show the resistance scheme at the electrode interfaces. Switching at the second interface is suppressed by the instrument current compliance (CC). The pale curve indicates the CS *I*-*V* characteristic without CC.

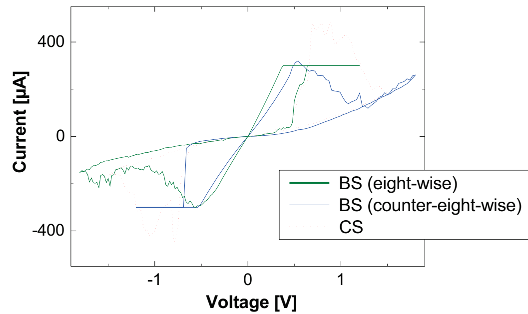


Figure 5.4: Measured *I*-*V* characteristic of the Complementary Switch (CS) vs. Bipolar Switch (BS) implemented by the same devices. By applying the instrument current compliance (CC) to the positive / negative voltage polarity, the BS mode is set to eight-wise / counter-eight-wise switching.

5.2 Electroforming / SET / RESET

5.2.1 O_2 Sputtering Gas Flow Variation

For deposition of a HfO_2 layer, a Ar-O_2 sputtering gas mixture is used (reactive sputtering). The relative oxygen O_2 sputtering gas flow has been varied for the fabrication of different devices (10 % ("10 %-O_2"), 17 % ("17 %-O_2") and 23 % ("23 %-O_2"). Consider, the relative sputtering gas flow should not be confused with the oxygen ratio in the deposited hafnium oxide film. XPS measurements have shown that the three sputtering conditions result in the same O:Hf ratio (see Section 4.1). However, that does not mean there is not any impact on the device properties.

The comparison of the initial resistance R_{ini} is summarized in Figure 5.5. The resistance has been evaluated at $V_{\text{read}} = 0.2\,\text{V}$. The definition of the box diagram plot and the relation to the experimental data are depicted in Appendix Figure A.3. Here, for a clear view, the measured data points are not included. A broad scattering by several orders of magnitude in the initial cell resistance is observed in each case. However, devices, where the HfO_2 film has been deposited at less relative O_2 sputtering gas flow, exhibit the lower R_{ini}. Independent of the sputtering process parameters, all types of devices require the electroforming procedure. It is presumed that the initial resistance affects the forming procedure, but the coefficient of determination with $R^2 = 0.03$ does not indicate any relevant correlation between initial resistance and forming voltage (see Figure 5.6a). The definition of R^2 is given in Appendix Section A.4.

The forming *I*-*V* curves for three exemplary devices with an initial resistance of 10 kΩ, 260 kΩ and 30 MΩ are summarized in Figure 5.6b. In spite of the different initial resistance, all devices show the forming event around 2 V. The forming voltage does not show any trend and is equal for the three sputtering gas conditions (see Figure 5.7).

The electroforming experiment has been performed on devices with electrode line width of 2 μm and 10 μm, which defines the square cell area size ($2 \times 2\,\mu\text{m}^2$ and $10 \times 10\,\mu\text{m}^2$). It is observed that the influence of the sell size is not significant and can be negligible within the root mean square deviation. Therefore, the results for all sizes are merged (cf. Figure 5.7b). The same behavior is also

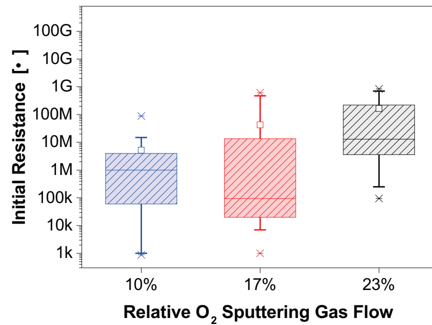


Figure 5.5: Initial resistance as function of relative O_2 sputtering gas flow, evaluated at read voltage about 0.2 V.

observed for subsequent SET and RESET investigations (bipolar switching) and in the following only devices with $5 \times 5\,\mu m^2$ cell size are considered.

To perform experiments on the bipolar switching mode, a proper CC has to be applied for the SET process, which prevents switching at the second interface. The RESET voltage V_{RESET} and the SET voltage V_{SET} are two relevant measurands. In the following, V_{SET} is defined by the voltage, where the abrupt current increase reaches the CC level (see Figure 5.3). By this definition, V_{SET} could depend on the CC level (depending on the abruptness degree of current increase). However, it enables one to include devices, which do not offer a single dominant SET event (also observed in [102]), but a multi-step SET process (cf. Figure 5.4, green curve). This might be attributed to multi filamentary growth or quantized switching.
V_{RESET} is defined as the voltage, where the RESET process starts. At that point, the I-V curve starts to change from the ohmic behavior to a non-linear characteristic (see Figure 5.3). In general, the current reaches the maximum absolute value at the RESET voltage. By this definition, V_{RESET} does not depend on the maximal applied voltage $V_{\mathrm{RESET,Stop}}$, since the RESET process is more gradual. Increasing $V_{\mathrm{RESET,Stop}}$ enables one to switch the BS device into a deeper HRS.[29, 103, 104]
The focus of subsequent measurements is on the bipolar eight-wise switching. Unless stated otherwise, a dual-voltage ramp of ±1.5 V has been applied to tog-

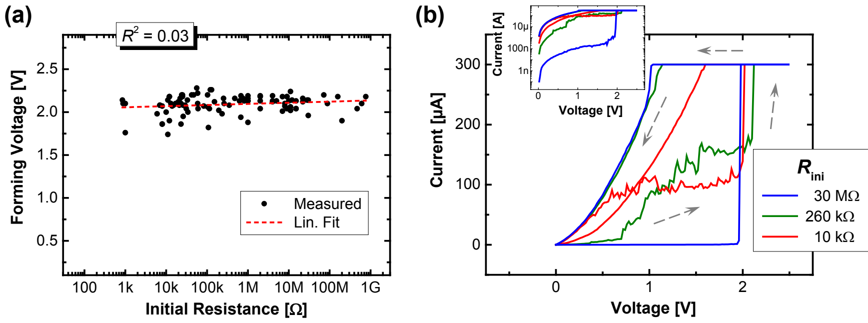


Figure 5.6: Initial resistance R_{ini} does not impact the forming voltage V_{FORM}. (a) Forming voltage vs. initial resistance. The coefficient of determination with $R^2 = 0.03$ indicates there is no significant linear relationship between V_{FORM} and R_{ini}. (b) Forming I-V curves of three devices with different R_{ini}.

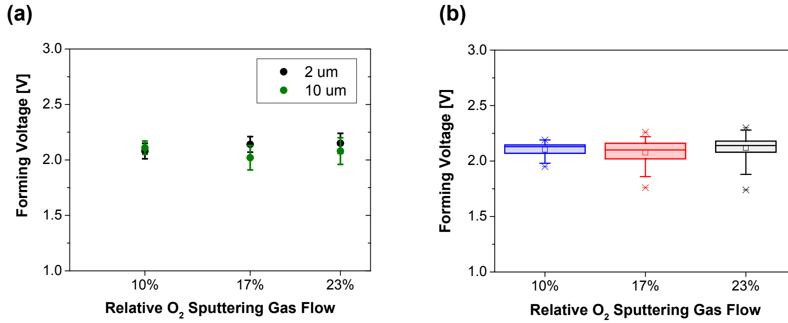


Figure 5.7: Forming voltage in complementary switching HfO_2-based devices as function of relative O_2 sputtering gas flow. (a) The variation of the forming voltage as function of the cell size is negligible within the scattering. Therefore, the results for all cell sizes are merged in (b).

gle the devices. Figure 5.8 demonstrates the results of the quasi-static (a) SET and (b) RESET experiments regarding the switching voltages. The statistics include cycle-to-cycle and device-to-device variations. V_{SET} and V_{RESET} are quite symmetric, both are around $\pm 0.7\,\mathrm{V}$. The relative O_2 sputtering gas flow (within the investigated regime) does not show any significant influence on the switching voltages. Since shape and conductivity of the conductive filament is well defined by the applied CC, the RESET voltage shows the lower scattering. The stronger SET voltage variation from device to device and from cycle to cycle seems to be an inherent property of the HfO_2-based cells.

Figure 5.9a depicts the Weibull plot about the resistance distribution in LRS and HRS. Here, the cell has been switched by voltage pulse stimuli, where the pulse width is about 0.05 s. The SET voltage amplitude is about $2.0\,V$ or $2.2\,V$, respectively, whereas RESET voltage amplitude is $-1.1\,\mathrm{V}$ or $-1.8\,\mathrm{V}$ to realize two different high resistance states (HRS-1 or HRS-2). The LRS offers a narrow distribution around $1\,\mathrm{k}\Omega$ due to the CC, whereas both HRS show the larger resistance scattering.

The deeper RESET is achieved by increasing the voltage pulse $V_{\mathrm{RESET,Pulse}}$. Variation of $V_{\mathrm{RESET,Pulse}}$ enables multi-level switching, which facilitates to store more than one bit in a single memory cell, resulting in a data storage density improvement.[29, 32] However, the deeper HRS exhibits larger resistance scattering in the HfO_2-based devices[102], which is attributed to a random generation of defects in the switching volume.[48] This leads to more randomness in the SET process. The LRS is less random, since the number of generated oxygen vacancies in the switching region, which are involved for regrowing the conductive filament, is better determined by the CC. The HRS and SET voltage spreading problem can be solved by using state-correction algorithms.[105, 106]

The cell conductance is decreased by rupturing the filament at the oxide-electrode interface (here: interface B). The deeper the RESET is, the larger is the gap between filament plug and the electrode, resulting in the higher HRS resistance. The stronger ruptured filament requires more power for the

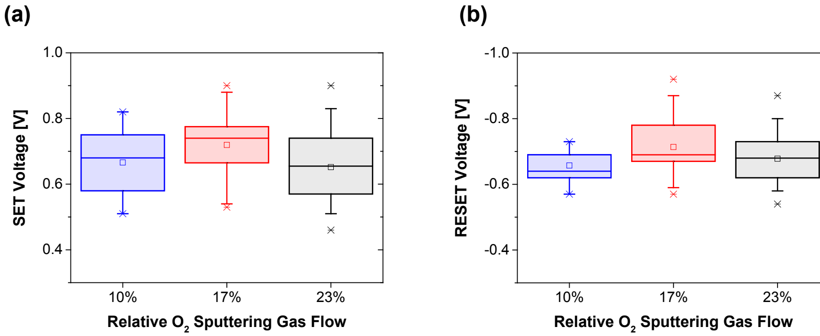


Figure 5.8: (a) SET and (b) RESET voltage as function of relative O_2 sputtering gas flow.

regrowing (SET process). The switching power P is given by

$$P = \frac{1}{T} \int_{t_0}^{t_0+T} V(t) \cdot I(t)\, \mathrm{d}t \qquad (5.1)$$

where T is the switching time. Figure 5.9b shows SET voltage dependence on the previous HRS resistance. V_{SET} increases nonlinearly with the HRS resistance. Since the HRS resistance depends on $V_{\mathrm{RESET,Stop}}$, the required SET voltage is also a function of the maximal applied voltage for the RESET process (see Figure 5.9c). The deeper the RESET process leads to higher V_{SET}. Hence, the scattering in the V_{SET} also increases. The latter observation is in accordance with the result of Figure 5.9a. Most devices show an increased V_{SET} or larger scattering for a smaller $V_{\mathrm{RESET,Stop}}$ ($V_{\mathrm{RESET,Stop}} < 1.5\,\mathrm{V}$). Additionally, the HRS resistance becomes closer to the Pt line resistance, which is about $500\,\Omega$, and the HRS-LRS resistance window almost vanishes. This is due to an insufficient RESET process.

Low switching power P (cf. Equation 5.1) is of interest for device integration and its application. One approach is to reduce the switching current, which is determined by the conductivity of the filament. For this purpose, geometry and composition of the conductive filament should be controlled precisely. The switching current in the single ReRAM device is considered to be dependent on the current compliance during the electroforming / SET pro-

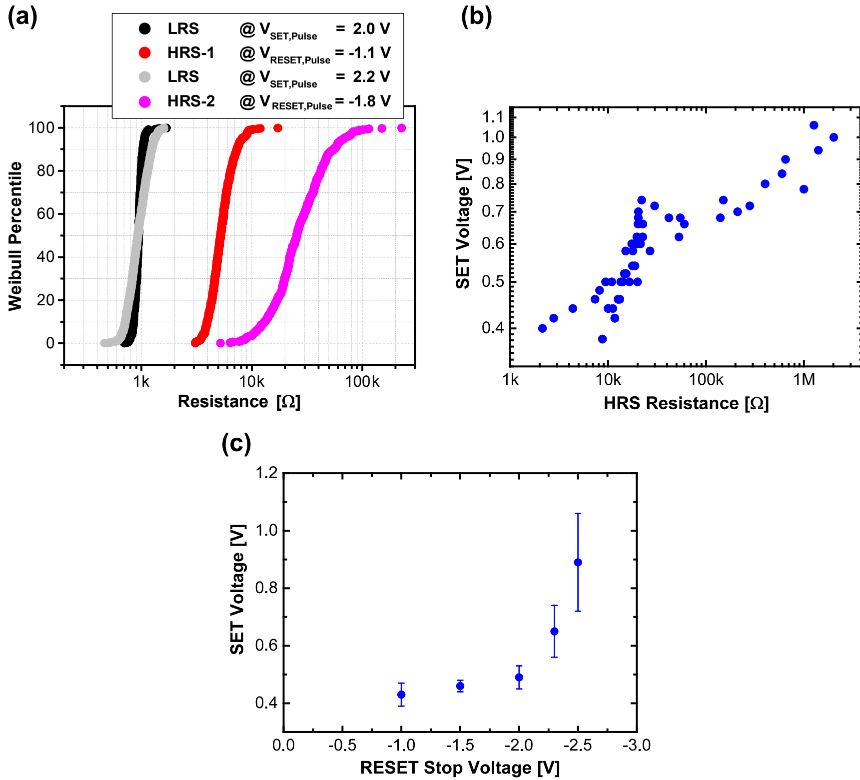


Figure 5.9: Variation of the LRS and HRS resistance and the SET voltage. (a) Weibull plot showing the resistance distribution as function of $V_{\mathrm{RESET,Stop}}$. (b) SET voltage dependence vs. HRS resistance. (c) SET voltage as function of $V_{\mathrm{RESET,Stop}}$.

cedure.[107] Therefore, the reduced current compliance could help to realize low-current switching ReRAM devices. The CC does not only limit the SET current, but it also reduces the RESET current, since the conductivity of the filament is defined during the SET process. During the RESET process the high current generates local Joule heating, which causes the rupture of the filament.[108, 109]

Figure 5.10 summarizes the distribution of the maximal RESET current ($I_{\mathrm{max,RESET}}$). The experiment has been performed by applying different CC levels during the SET process. All samples show clearly the same trend: the maximal current during the RESET process is linearly proportional to the CC level used for the previous SET process. "17 %-O_2" features a slightly lower operation current at a given CC level, in comparison to "23 %-O_2". For "10 %-O_2" the comparison is not performed due to insufficient number of data points.

5.2.2 Hf Electrode Thickness Variation

It has been observed that the as-deposited 5 nm thick Hf film is completely oxidized due to the partial oxygen diffusion from the as-deposited HfO_2 layer. In the next experimental step, the influence of the as-deposited Hf electrode thickness d_{Hf} is investigated, while the relative O_2 sputtering gas flow is fixed at 23 %. If the as-deposited Hf film is thinner ($d_{\mathrm{Hf}} < 5\,\mathrm{nm}$), the final overall oxide thickness will be thinner ($d_{\mathrm{HfO}x} < 10\,\mathrm{nm}$). But, if the as-deposited Hf film is thicker the oxide could penetrate deeper into electrode metal and change the material and device properties. Nevertheless, the diffusion depth should be limited in the thermal equilibrium.

Five samples with different Hf electrode thickness have been prepared: 0 nm ("0 nm-Hf"), 5 nm ("5 nm-Hf"), 10 nm ("10 nm-Hf"), 15 nm ("15 nm-Hf") and 30 nm ("30 nm-Hf"). Figure 5.11 depicts R_{ini} as function of the Hf electrode thickness. All samples offer a highly resistive initial state and require the electroforming procedure. The sample "0nm-Hf" exhibits a broad scattering about six orders of magnitude. These devices can be electroformed, but they do not show resistive switching over more than few cycles.[110] Devices with the thicker Hf electrode show scattering over less orders of magnitude in the initial resistance, especially "15 nm-Hf" and "30 nm-Hf" with R_{ini} about a few

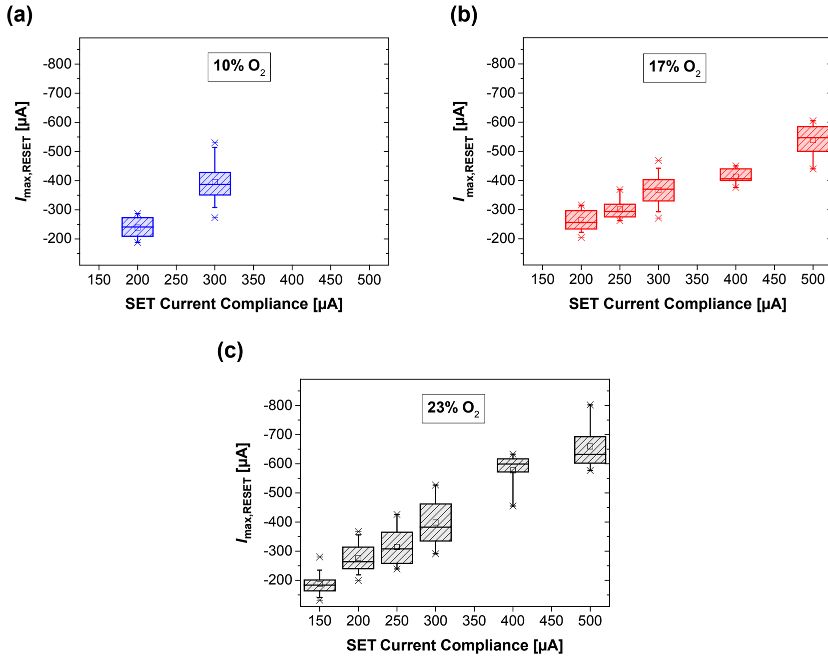


Figure 5.10: Maximal RESET current as function of applied current compliance for SET process. Independent of the relative O_2 sputtering gas flow for the HfO_2 deposition, all devices follow the same trend.

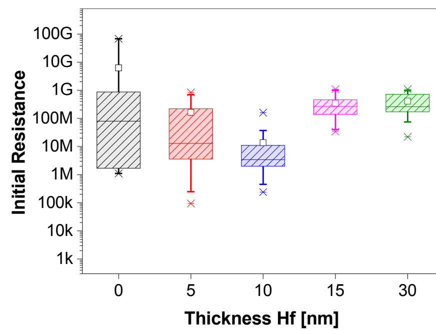


Figure 5.11: Initial resistance as function of Hf capping metal thickness in HfO_2-based devices.

hundred MΩ. The difference from "10 nm-Hf" to "15 nm-Hf" cannot be explained. At least, for all samples, the resistance median and the interquartile range meet the megaohm range.

A clear nonlinear trend is given by the comparison of the forming voltage in Figure 5.12a. The thicker Hf electrode causes the lower forming voltage: the thicker Hf layer enables more oxygen ions to diffuse out of the as-deposited HfO_2 film and generates a higher amount of oxygen vacancies there, benefiting for the conductive filament growth. Thus, the forming voltage decreases. V_{FORM} meets the saturation level of 1.4 V for devices with a 10 nm thick or thicker Hf cap layer. That means the oxidation depth of Hf is saturated and no further oxygen vacancies are generated by thicker Hf films.

Chen *et al.* have demonstrated higher oxygen scavenging from HfO_2 with the thicker Hf electrode by using XPS analysis.[110] This characteristic is not limited to the Hf capping metal, since the Ti electrode also shows the increase of V_{FORM} by decreasing the layer thickness.[111] The same trend is observed for Ta_2O_5-based ReRAMs as depicted in Figure 5.12b.[6] This confirms that the oxygen scavenging by the active electrode is a common effect and not restricted to one specific material.

Figure 5.13 depicts the (a) SET and (b) RESET voltage dependence on the Hf electrode thickness. More than 80 % of the devices without a Hf electrode do not show any bipolar switching. The remaining 20 % switch less than 10 cycles, offering only very abrupt RESET and SET events with a difference

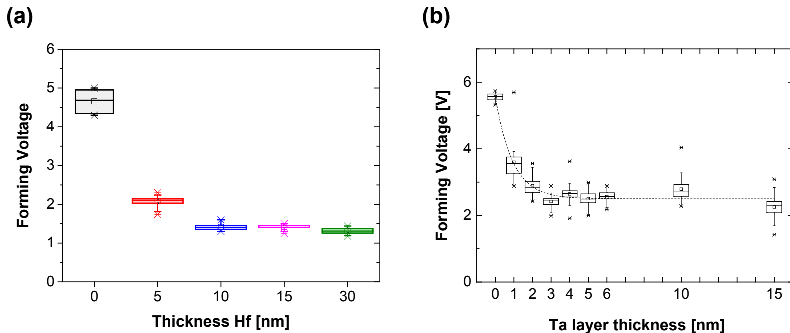


Figure 5.12: Forming voltage as function of capping metal thickness in (a) HfO_2- and (b) Ta_2O_5-based devices.((b) from [6], reprinted with permission from the publisher, © 2015 IEEE.)

between R_{HRS} and R_{LRS} around five orders of magnitude and large scattering in V_{SET} (0.96 V...3.18 V) and $V_{\mathrm{RESET}}(-1.98\,\mathrm{V}...-0.54\,\mathrm{V})$. Therefore, these data are not considered for analysis. Devices with the 5 nm thick Hf layer offer the highest RESET and SET voltages. As observed for the variation of the relative O_2 sputtering gas flow, the SET voltage exhibits more scattering than the RESET voltage.
Due to the demonstrated correlation between V_{SET} and previous HRS resistance (cf. Figure 5.9), one can derive: the HRS is not defined as well as the LRS and offers more variation in the resistance value. From 5 nm to the thicker Hf layer, SET and RESET voltage decrease, indicating that the switching behavior changes. This is the point, where the devices change from naturally preferred CS to BS behavior. The switching voltages do not change anymore by further increase of the Hf electrode thickness.

5.2.3 RF Sputtering Power Variation

In the following experiment, the impact of the HfO_2 sputtering rate is investigated, while the relative oxygen sputtering gas flow is fixed at 23 % and the Hf electrode thickness at 15 nm. The growing rate is directly controlled by RF sputtering power (see Section 4.1). The RF power conditions of 10 % (58 W), 20 % (116 W), 30 % (174 W) and 40 % (232 W) are considered.
Figure 5.14 summarizes the statistical distributions of the electroforming pro-

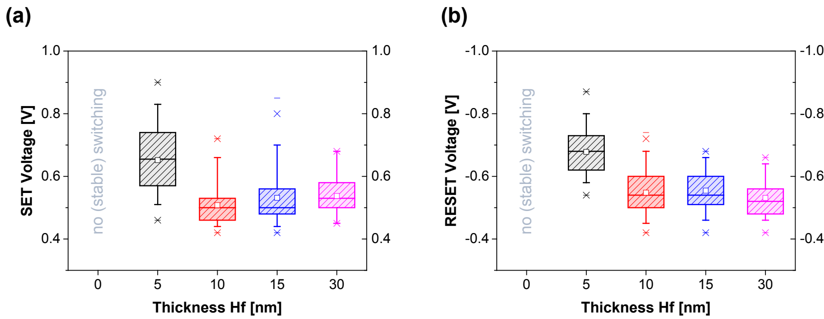


Figure 5.13: (a) SET and (b) RESET voltage as function of capping metal thickness in HfO_2-based devices.

cess. At least the initial cell characteristics are influenced by the sputtering power. From 20 % to 30 % RF power, R_{ini} is reduced by two orders of magnitude. Further increase of the sputtering rate decreases the resistance slightly. Exactly the same trend is observed for the forming voltage. Here, a clear correlation exists between V_{FORM} and R_{ini}. This is contrary to the experiment of the variation of the relative O_2 sputtering gas flow. It seems that the higher-energetic particles (stronger accelerated by the higher electrical field) generate more defects in the switching oxide film. However, a minimal threshold RF power has to be exceeded in order to observe that effect. Unfortunately, the RF power cannot be increased more than 40 % to avoid a damage of the 2 inch Hf sputtering target.

The subsequent bipolar switching (V_{SET} and V_{RESET}, see Figure 5.15) does not differ for the devices with the four fabrication conditions. Nevertheless, the HRS resistance and therefore also the SET voltage again show broader scattering than LRS resistance and RESET voltage. The RF sputtering power influences only the initial behavior.

Once the conductive filament is formed, the memory cells exhibit almost the same bipolar switching characteristic. That is also visible in the maximal current (during the RESET process). Figure 5.16 shows the $I_{\text{max,RESET}}$ dependence on the applied SET CC level for devices, where the HfO_2 films have been grown with the 10 % and 30 % RF power conditions. The samples do not distinguish significantly. $I_{\text{max,RESET}}$ runs into a lower limit around 200...300 μA at the CC level of 100...200 μA. That is attributed to low HRS resistance (for

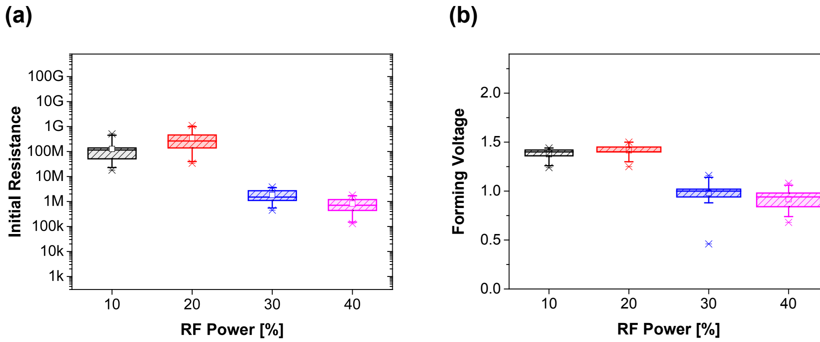


Figure 5.14: (a) Initial resistance and (b) forming voltage as function of RF sputtering power in HfO_2-based devices.

$V_{\mathrm{RESET,Stop}} = -1.5\,\mathrm{V}$) resulting in a minimal pre-SET current (current level immediately before the SET process) in the range of several $10\,\mu\mathrm{A}$, which does not allow further decreasing of maximal operation current. Additionally, the RESET process seems to be incomplete causing the low HRS resistance.
Using the deeper RESET could be a promising approach to enable switching while applying lower CC level, in order to decrease further $I_{\mathrm{max,RESET}}$. The deeper HRS enables lower pre-SET currents, that is beneficial for the clear abrupt SET process in order to achieve a suitable HRS-LRS resistance window.
$I_{\mathrm{max,RESET}}$ exhibits an upper saturation of $900...1000\,\mu\mathrm{A}$ at the CC level of $900...1000\,\mu\mathrm{A}$. For the lower LRS resistance, the Pt line resistance (connection line from contact pad to memory cell) becomes more dominant in device characteristics. That serial Pt line resistance is about $500\,\Omega$ and works below a certain LRS level as a current compliance (see also Chapter 6). If the line resistance becomes comparable or even larger than the cell resistance, the voltage drop across the contact line is not negligible anymore. That means a large amount of the applied voltage drops across the Pt line and not across the cell stack. Therefore, during the SET process, the filamentary regrowth is limited, resulting in a lower LRS conductance (than expected) and a limited $I_{\mathrm{max,RESET}}$.

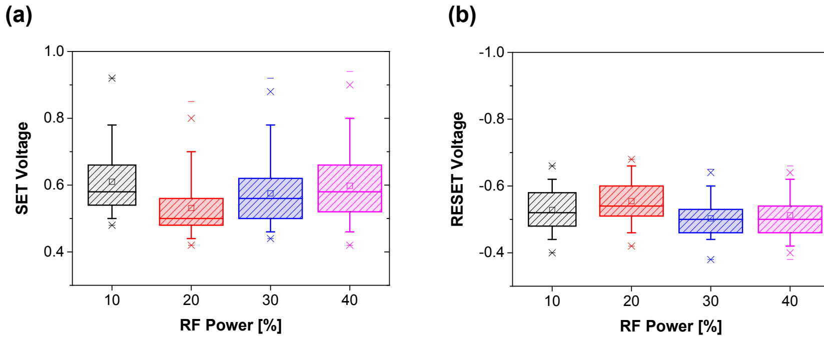


Figure 5.15: (a) SET and (b) RESET voltage as function of RF sputtering power in HfO_2-based devices.

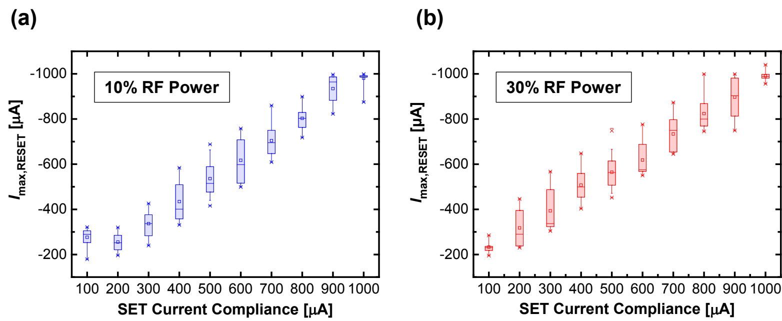


Figure 5.16: Maximal RESET current as function of the used RF sputtering power for growing HfO_2 films.

5.3 Reliability

5.3.1 State Stability

Bipolar switching experiments compare in the previous section the SET and RESET processes. The HRS exhibits a broader resistance distribution, whereas the LRS resistance is clearly defined and offers little scattering. The deeper the RESET is, the larger the resistance scattering (cf. Figure 5.9).
Since the devices prepared under different conditions do not distinguish substantially after the electroforming treatment (excluding devices inherently preferring the complementary switching mode), the samples are not differentiated anymore. The low variation in the LRS resistance can be attributed partly by the instrument CC, which controls size and geometry of the conductive filament and finally the maximal operation current (see also Section 6.1). However, the broad HRS spreading might indicate a kind of non-stability. Due to the nature of the redox-based resistive switching, there can only be maximal one state, which is thermodynamically stable.[48] This means the HRS or the LRS has to be non-stable or at least metastable.
To investigate the thermal stability of the resistance states, some temperature dependence experiments have been performed to accelerate the redox reactions involved in resistive switching, that avoids long observation times (long-term experiments). At the beginning, the device is switched to HRS by a quasi-static voltage sweep with negative polarity. Subsequently, the resistance state is monitored by pulses with an amplitude of $V_{\mathrm{read}} = 0.1\,\mathrm{V}$ for every 0.5 s. Simultaneously, the temperature is increased by linear temperature ramp from 22 °C to 210 °C. The results are presented in Figure 5.17a (purple circles). The progress of the resistance is depicted in steps of 10 K, where ±3 consecutive resistance values around $T = n \cdot 10\,°\mathrm{C}$ ($n = 2...21$) have been averaged in order to include temperature drift. The initial HRS resistance is about 90 kΩ. Up to 70 °C the state does not show any degradation. Further increasing the temperature results in a linearly decreasing trend of the resistance down to around 20 kΩ (at 210 °C).
During the experiment the temperature ramp has been paused several times in order to observe the resistance change at a fixed temperature (not shown here). While keeping the temperature on a constant level, the resistance does

not significantly change. Therefore, it is able to exclude dramatic temperature drift and progressive state degradation, which is not caused by temperature increase but by relaxation or the reading process. This fact excludes the possibility that the memory cell could exhibit a gradual state degradation due to intrinsically caused retention problems.

During the next step, the heating system is switched off followed by slow temperature decrease. The resistance values have been averaged in the same way as mentioned above. The HRS resistance keeps on the same level during the cooling progress (see Figure 5.17b, purple circles), i.e. the state has changed irreversibly. Here, irreversibility means the system does not return to the initial state although the temperature is reset to the primary condition. Nevertheless, the device still shows reversible bipolar switching by applying SET and RESET voltage stimuli.

Lastly, at room temperature, the cell is switched to the low resistance state by the quasi-static voltage sweep with positive polarity, in order to investigate the LRS stability. Neither heating (Figure 5.17a, black circles) nor cooling process (Figure 5.17b, black circles) effect the degradation of the LRS, where the resistance maintains at 1 kΩ.

Since the temperature does not affect the LRS up to 210 °C, the LRS seems to be thermodynamically stable (over the experimental period). Furthermore, since no CC is used (excluding during the SET event, conducted at room temperature at the beginning), the CC cannot have any further impact on the state stability during the heating experiment. This means the device is set to the well-defined LRS by the CC. However, the continuing state stability is not determined by the CC: if another arrangement of ions (different resistance state / LRS) exhibited the lowest free energy, the system would change (accelerated by thermal heat) to that arrangement[48] (independent of any previously used CC).

A similar characteristic is observed for retention tests. At first, the sample is heated up to a target temperature, at which the experiment will be conducted. Then the device is switched by the quasi-static voltage sweep to the HRS or LRS, depending on which state is tested. During the retention test the state is monitored by applying the read voltage pulses of 0.1 V in 20 s time steps. The results are summarized in Figure 5.18. The reduced data points are plotted

on a logarithmical time scale to make trends clearer. The LRS is very well defined. For the most part, the state is stable and does not show any significant degradation. Even at 200 °C, the LRS is stable for more than 1×10^6 s (> 11 days) (Figure 5.18a). After that time period, the device state has not been failed, but the experiment has been stopped.
After the retention measurement, the cell functions properly and can be reversibly switched. This has always been checked in order to exclude non-functionality / damage of the device, which might be stable in the actual resistance state.
The same experiment is conducted for the HRS. At 200 °C the RESET process is performed by applying the negative voltage sweep. The resistance monitoring process is identical to the previous experiment. For the HRS resistance, two different temporal progressions are observed: gradual degradation (Figure 5.18b) or abrupt degradation (Figure 5.18c); a mixture of both cases is also possible. This indicates the HRS degeneration could be determined by two different mechanisms. In a few cases the HRS is stable for more than 1×10^5 s (> 1 day) at 200 °C, but many of them fail within the time range of 1×10^4 s (> 2.5 hours) at 150 °C. Oxygen diffusion from the rupture region of the conductive filament, which involves oxygen vacancy generation at the disc region, is supposed as a retention failure mechanism for the HRS.[112–114] The fact, which resistance state, LRS or HRS, shows the higher stability, might originate from the actual filament geometry.[115] For larger filaments, the oxygen vacancy incorporation into the filament disc region might be energetically more favorable and therefore the LRS might be more stable. However, for smaller filaments, their dissolving by removal of oxygen vacancies might be energetically more favorable and therefore the HRS might be more stable.

5.3.2 Endurance

Bipolar Switch At the end, some endurance experiments have been performed to test the LRS and HRS stability by the number of switched cycles. Consider, in general, the endurance test is an extensive topic on its own. It requires well known switching properties. There are many parameters, which can be optimized (e.g. pulse width / amplitude, pulse rising / falling time etc.), in order to determine the best endurance conditions.

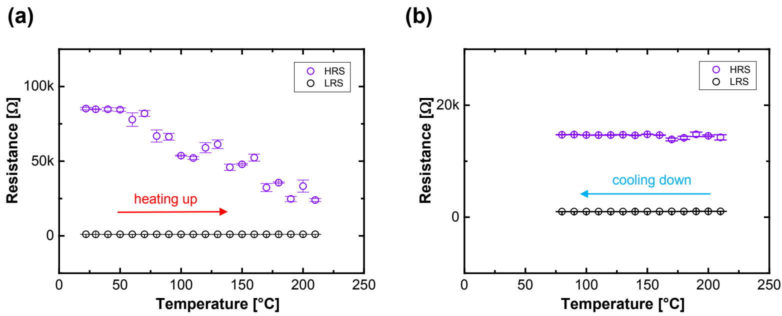


Figure 5.17: Thermal stability of HRS / LRS for HfO_2 devices. The resistance change of HRS / LRS for (a) heating up and (b) cooling down conditions.

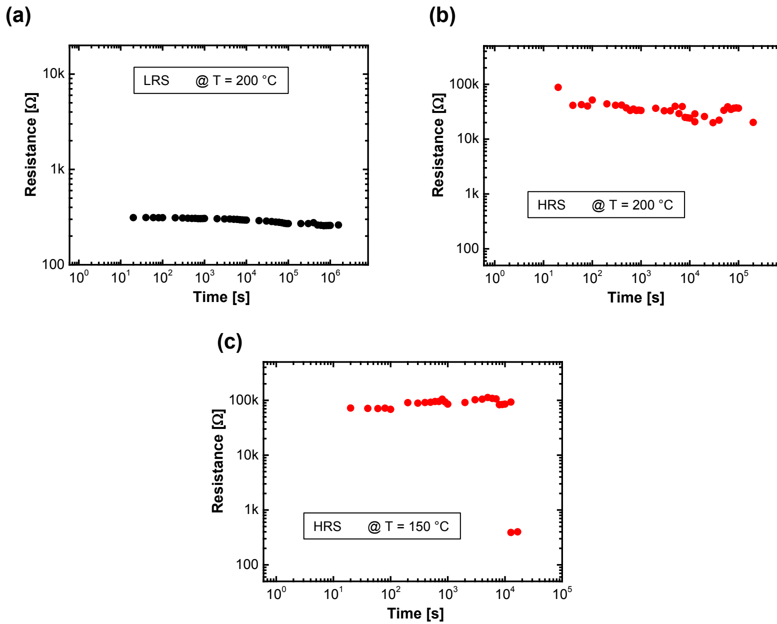


Figure 5.18: Retention test of the LRS (a) and the HRS (b, c) under enhanced thermal heat stress for HfO_2 devices. The LRS does not change the resistance level significantly, whereas the HRS shows gradual and abrupt degradation.

Ideal cycling requires (beyond suitable HRS-LRS resistance window) an invariant rupture and regrowth of the conductive filament in the switching volume. This means, the filamentary geometry and size and the number of involved oxygen vacancies keep equal for the HRS and the LRS respectively.[48]
Mismatching parameters result in an endurance failure. If the amount of generated and degenerated oxygen vacancies is unequal for the SET and the RESET process, the device will suffer from over-SET or over-RESET, i.e. the LRS or the HRS (or both) change the resistance level.[48,116] State-correction algorithms are a suitable solution for over-SET / -RESET and state spreading problems.[105, 106] Due to the complexity of the endurance issue, here, just pre-measurements are performed using long voltage pulses in the range of micro- and milliseconds. Figure 5.19 depicts the pulsed driven endurance measurement on the HfO_2-based device under different cycling conditions. While the LRS resistance is well controlled by the CC, the HRS exhibits resistance spreading, whose broadness correlates directly with the averaged HRS resistance level.
The switching parameters affects strongly the switching characteristics and the device endurance. Figure 5.19a shows the effect of unbalanced RESET pulses (over-RESET). In spite of the large scattering, the gradual degradation is visible. After 10^3 cycles, the cell fails completely and ends up in a low resistance state. However, this does not mean the device is completely broken. By applying the quasi-static voltage sweep, the cell is regenerated and can again be reversibly switched.
In contrast, too large SET pulse amplitudes are detrimental for higher endurance (see Figure 5.19b). The LRS resistance increases gradually (over-SET). This might be attributed to an insufficient response time of the instrument CC. After 7×10^4 cycles the LRS fails, resulting in a very high ohmic resistance. But this does also not imply the total device breakdown. In general, the switching can be restored by a quasi-static RESET procedure (maybe requiring increased $V_{\mathrm{RESET,Stop}}$) followed by the re-electroforming step.
Using matched pulsing parameters results in stable switching and clear HRS-LRS resistance window as presented in Figure 5.19c, which allows the implementation of multi-level switching (see Figure 5.9a and 5.19d)

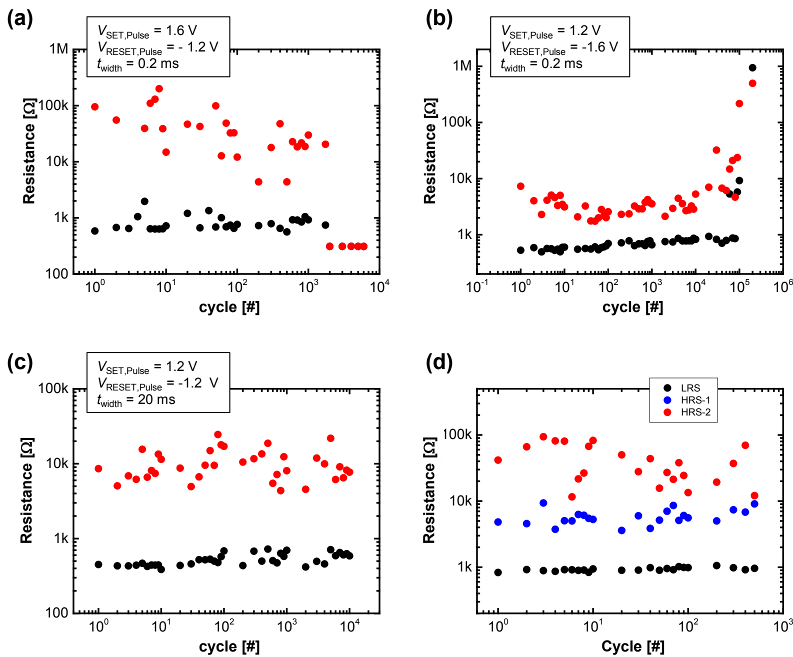


Figure 5.19: Endurance measurements on HfO_2 devices using milli- and microsecond pulses. Unmatched pulse parameters cause (a) the over-RESET or (b) over-SET issue intensifying the endurance RESET or SET failure. (c) Suitable switching parameters promote high endurance and stable HRS-LRS resistance window, enabling (d) multi-level implementation.

Complementary Switch Stable switching properties and endurance of HfO_2-based CS devices are essential for implementation of application concepts.[2] In opposite to single bipolar ReRAMs, only a destructive current based readout is provided for CS devices by the present experimental setup. Since the two CS states are highly resistive in the same range, they cannot be distinguished at low voltages by (non-destructive) current readout. The required reading voltage should be at least equal to the threshold voltage $V_{\text{th},1}$ or $V_{\text{th},3}$ (see Figure 2.4), causing change of the CS state.
For the endurance test n positive and negative alternating pulses (width 500 ns, pulse amplitude 2 V, $n = 1, 10, 100...$) are applied.[2] Afterwards, the CS operating mode is confirmed by quasi-static voltage sweep. The recorded switching I-V plots are depicted in Figure 5.20(a). The CS shows stable complementary switching properties up to 10^9 cycles. Certainly, the hysteresis loops indicate overall a slight current decrease with increasing number of cycles, but the resistance window between the CS 'OFF' state (HRS/LRS or LRS/HRS) and the CS 'ON' state (LRS/LRS) is rather constant. Subsequent to the endurance test, positive and negative spike responses have been recorded to confirm the general operability under pulse conditions (see Figure 5.20c).
Next, the read selectivity is extracted from the recorded endurance data.[2] For this purpose, the currents at $V/2 = 0.5\,\text{V}$ and $V = 1\,\text{V}$ are compared (see Figure 5.20(b)). Feasible size of the crossbar array depends (among other parameters) on the read selectivity. Hence, improving this factor is a crucial challenge in CS engineering. Most notably, advancing the electroforming process is a promising method for CS current reduction and low-power operation. The desired CS 'ON' resistance is in the range from $10\,\text{k}\Omega$ to $100\,\text{k}\Omega$. This would cause current spikes in the lower microampere regime. Therefore, the required energy per operation could be as low as several femtojoules, due excellent switching speed feasibility ($< 200\,\text{ps}$).[14]
Devices, failing earlier complementary switching, remains in the highly resistive state (LRS/HRS or HRS/LRS). Normally, they are not completely broken. The switching can again be restored by the re-electroforming procedure (same conditions as used for the initial electroforming).

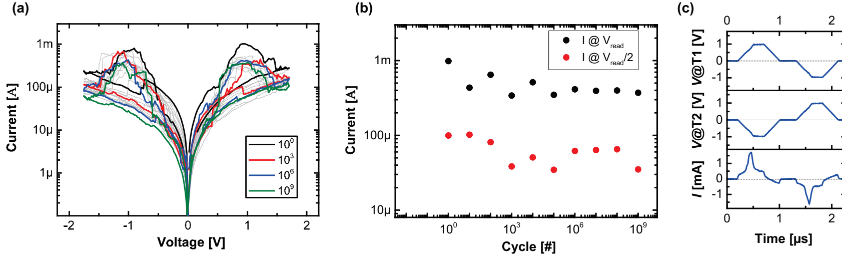


Figure 5.20: Endurance experiment of the HfO_2-based CS. (a) I-V-characteristic for quasi-static voltage ramps after n pulsed cycles (alternating positive and negative pulses). Consider, fluctuations in the highly resistive CS states are observed (i.e. cycle 10^3 for positive polarity), which might be caused by atomistic nature of the conductive filament.[117] (b) Read selectivity extracted from the recorded endurance data (at read voltages $V_{\text{read}} = 1\,\text{V}$ and at $V_{\text{read}}/2$). (c) Transient response current after the endurance experiment.[2] (Redrawn with permission from the publisher.)

5.4 Conclusion

The switching characteristics of samples with different fabrication process parameters have been investigated (relative O_2 sputtering gas flow, Hf electrode thickness, RF sputtering power for HfO_2 deposition). Independent on the parameters, the initial HfO_2 cell has to be electroformed. The forming is feasible by applying a sufficient positive or negative stimulus. However, electroforming into the LRS using the positive polarity requires the lowest voltage in each case. Furthermore, the forming voltage is reduced for devices with the thicker Hf electrode. The negative forming does not influence the switching polarity, the cell is rather switched to the high resistance state.

The cell stack 30 nm Pt | 5 nm HfO_2| 5 nm Hf | 25 nm Pt exhibits different switching modes depending on the instrument CC for the SET process: complementary switching, eight-wise and counter-eight-wise bipolar switching. Naturally, that device prefers the complementary switching, since the CS characteristics are sometimes visible on the RESET side despite of the used CC.[2] That means, before the RESET process starts for applying a negative voltage sweep, the LRS shows clearly a non-linear current rise. Increasing the Hf electrode thickness to 10 nm or more, the device prefers the bipolar switching and the LRS is more linear.

Variation of the remaining fabrication parameters (RF sputtering power, relative O_2 sputtering gas flow) has an impact on the initial resistance and the forming process, but once the conductive filament is grown, the samples do not distinguish in the subsequent bipolar switching. The switching power of the memory device has to be as low as possible for energy efficient data storage and computation applications. Reducing the maximal operation current is one approach. Decreasing the CC level during the SET process results in lower RESET currents for all different samples.
Additionally, the HfO_2-based ReRAM enables multi-level switching by the deep RESET, which allows storing more than one bit per memory cell in order to enhance the data storage density. However, the HRS seems to be less well defined as the LRS. The deeper the HRS is, the larger the resistance spreading. That issue could be tackled by state correction algorithms. Further, experiments conducted under thermal stress shows the HRS degrades to a low resistance state, while the LRS is more stable. Failing the resistance state does not mean the total devices breakdown. In general, the functionality is recoverable by adjusted voltage stimuli.

Chapter 6

Ta_2O_5-based CRS Device Optimization

6.1 Low-Current Operation in CRS

The promising CRS concept has been successfully proven for several metal oxides materials, e.g. HfO_2[70], Ta_2O_5[27, 67, 69, 118] and TiO_2[68].[3] Among these candidates, the best properties, relating to reliability (low variations) and endurance, are featured in Ta_2O_5-based devices. For instance, highly reliable CRS switching up to 3×10^4 cycles has been presented by Schmelzer *et al.* in [67]. It should be mentioned that these devices are of few micrometer size and require large switching current ($\sim$ mA), maybe causing enhanced power consumption. To decrease the CRS operation current, elementary composition and shape of the conductive filament in the ReRAMs should be tailored. It is assumed that the current compliance (CC) during the electroforming / SET process determines the overall switching current in the single device.[107] Thus, decrease of the CC level, for the electroforming procedure, could enable low-current operations in the CRS.

For common single bipolar switches (e.g. Pt|Ta_2O_5|Ta), the electroforming process is quite straightforward: to switch the device from virgin highly resistive state (vHRS) to the LRS, a positive voltage is applied to the top electrode (here: Ta).[3] Commonly, the use of a CC is the best approach in order to constrain the maximal current and to avoid any device damage.[61] Certainly, this approach is not practicable for integrated (two-terminal) CRS, since they do

not offer any access to the middle electrode (ME) in the passive crossbar array configuration. However, this access would be required to address separately the bottom cell (BC) and the top cell (TC). Hence, an innovative process, which ensures in-situ electroforming of completely embedded (two-terminal) CRS, has been introduced.[3]
In the following subsections, the systematic behavior of Ta_2O_5-based two- and three-terminal CRS devices (i.e. without / with access to the middle electrode) from μm to nm-scale are discussed and a novel electroforming method is proposed. This controlled forming process enables low-current operation ($< 300\,\mu$A) for Pt|Ta_2O_5|Ta|Ta_2O_5|Pt CRS devices without the need to access the middle electrode.[3] Table 4.4 gives an overview about the different types of CRS structures, which are investigated.

6.1.1 Three-Terminal CRS

The complete forming procedure includes three steps (see Figure 6.1).[3] The three-terminal micro-BC CRS (structure A) devices exhibit access to the ME, which enables straightforward and individual electroforming of the TC and BC. That means a positive voltage is applied to the ME, while the top electrode (TE) or the bottom electrode (BE) is set to ground (see 1st and 2nd step in Figure 6.1). During this procedure the instrument CC controls the switching current, enabling precise generation of a conducting filament in the two cells.[3] Next, the RESET process on the TC or BC has to be performed (by the 3rd step), where the CRS is switched to the HRS/LRS or LRS/HRS state. The electroforming *I*-*V* characteristics of the individual cells are demonstrated in Figure 6.2.[3] The applied CC level is about $100\,\mu$A. Around 2.2 V, the TC is electroformed (cf. Figure 6.2a). Afterwards, the cell shows the bipolar switching mode. However, the BC requires an electroforming voltage (V_{FORM}) of about 1.0 V (cf. Figure 6.2b). The deviation is attributed to non-projected different Ta_2O_5 thicknesses in the TC and BC, as indicated by the TEM image of the CRS stack cross-section (see Figure 4.18).[3] This issue is caused by the device fabrication process, where the Ta-ME is exposed to air for patterning (cf. process flowchart in Figure 4.11). Due to the exposure to atmosphere, the Ta layer partly oxidizes on top and causes a thicker Ta_2O_5 layer in the TC.
After electroforming of the BC and TC, one cell is switched to HRS and the

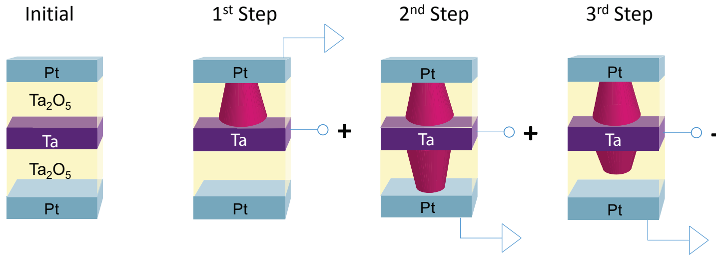


Figure 6.1: Forming procedure of three-terminal CRS device consists of three steps. Bottom cell (BC) and top cell (TC) are formed separately. Step 1 is the formation of the TC. Step 2 is the formation of the BC, resulting in the LRS/LRS state. This is followed by the RESET on one cell to switch the device to the HRS/LRS or LRS/HRS state (step 3).

other one remains in LRS.[3] Henceforth, the experimental setup is changed to CRS contact configuration, where the BE is set to ground and the driving voltage is applied to the TE. The CRS I-V characteristics are presented Figure 6.2c. The maximal switching current is below 300 μA, the lowest CRS operation current for micrometer scaled CRS up to now.[3] Consider, the threshold voltages for positive and negative polarity (HRS/LRS $\rightarrow$ LRS/LRS and LRS/HRS $\rightarrow$ LRS/LRS, respectively) show a slight deviation (asymmetry). This observation might be attributed to the Ta_2O_5 thickness asymmetry in BC and TC.
The typical CRS I-V characteristics, as demonstrated in Figure 6.2c, is the superposition of the BC and TC switching properties.[3] For instance, the CRS RESET events indicate clear similarities to the corresponding BC and TC RESET processes in Figure 6.2(a,b). The TC offers the more abrupt RESET process and the subsequent current does no increase further for higher driving voltage. On the other hand, the BC RESET event is more gradual and afterwards the current increases further by enhancing applied voltage.

6.1.2 Two-Terminal CRS

Next, the ME is embedded in the CRS for intergration in ultra high-dense passive crossbar arrays.[3] In this two-terminal device configuration, the ME does not exhibit an external connection line for addressing. However, in or-

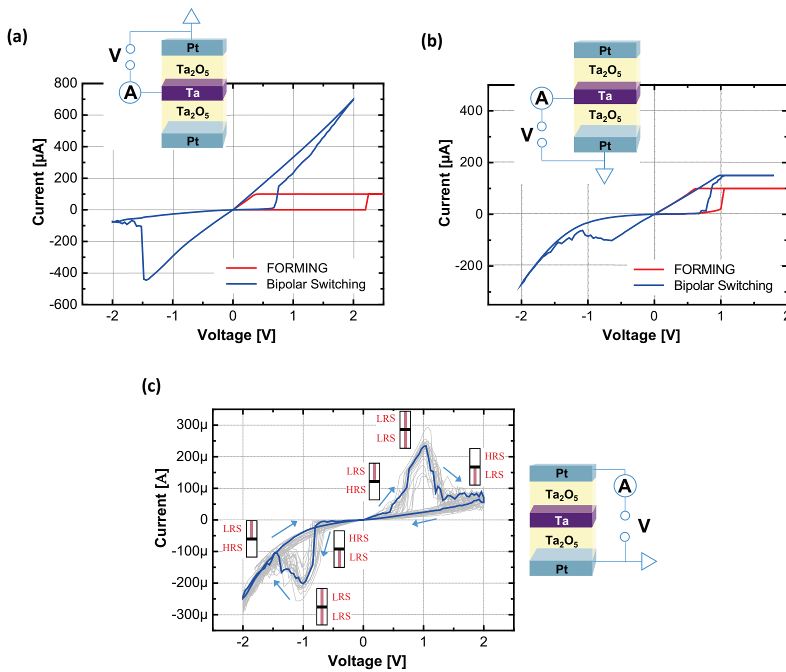


Figure 6.2: Different switching modes of the three-terminal-CRS depend on the used contact mode, which is given by the insets in (a, b, c). The separate electroforming of (a) TC and (b) BC and (a, b) consecutive bipolar switching of individual cells. Contacting the top and bottom Pt electrode enables the CRS mode (c). The arrows in (c) indicate the switching direction, whereas the added resistance schemes show the actual CRS state.[3] (Reprinted with permission from the publisher.)

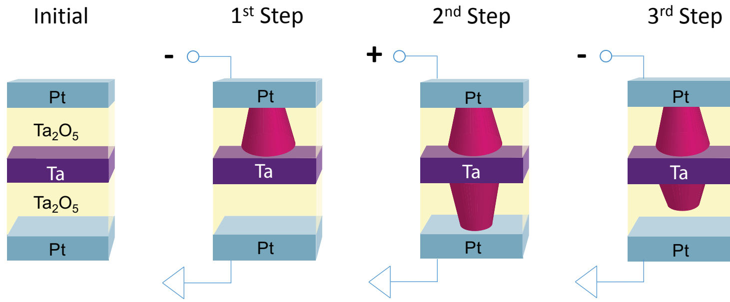


Figure 6.3: Novel forming procedure of two-terminal CRS device, which does not require access the middle Ta electrode. Step 1 is the formation of the TC. Step 2 is the formation of the BC, resulting in the LRS/LRS state. This is followed by the RESET process on one cell to switch the device to the HRS/LRS or LRS/HRS state (step 3).

der to generate initially well-defined conducting filaments, a novel three-step electroforming process is applied. Therefore, two electroforming routes are considered, which distinguish in the virgin states of TC and BC. Nevertheless, the presented electroforming procedure is universally applicable, since both routes are enabled by the same steps. Initially both cells show either a low resistance or a high resistance. If the CRS stack is initially in the vHRS/vHRS, an electroforming of the two cells is required.[3] This is realized by the first two steps followed by the RESET event of one cell (see Figure 6.3). The last step requires either a negative or a positive voltage applied to the top Pt, resulting in the CRS state LRS/HRS or HRS/LRS respectively. However, if the CRS stack of Pt|Ta_2O_5|Ta|Ta_2O_5|Pt exhibits a virgin low resistance (vLRS/vLRS), the first two electroforming steps do not have any impact (due to the applied CC) and only the final RESET process of one cell is the essential step.[3]

6.1.2.1 Micro-BC CRS

The electroforming procedure of the two-terminal micro-BC CRS is depicted in Figure 6.4a. Initially the device is in the vHRS/vHRS state.[3] First of all, a negative voltage sweep is applied to the TE. The TC is electroformed around $-3.5\,V$, where the current compliance level is about $I_{CC} = 500\,\mu$A ((1) and (2) in Figure 6.4a). Unexpectedly, the complete stack is now highly conductive.

The hypothesis: the BC offers a virgin high resistance state (vHRS), but is simultaneously electroformed with the TC. Next, a reference measurement for the three-terminal CRS is conducted to confirm the idea[3]: In the beginning, it has been confirmed that BC and TC show the vHRS, initially. Afterwards, the identical electroforming procedure (as used for the two-terminal CRS) has been performed. This experiment confirms the made hypothesis: in the first step, the forming voltage is about -3.5 V. This value is higher than the voltage, which is required to electroform the single TC (2.5 V) and single BC (1 V).[3] That means BC and TC are initially in the vHRS/vHRS state, because the two- and three-terminal CRS require a forming voltage around -3.5 V. Thus, the resulting lowly resistive state is attributed to simultaneous electroforming of TC an BC.
The non-separated electroforming might be ascribed to the applied CC.[3] The instrument CC automatically decreases the actual applied voltage, which drops over the device under test, if the detected current reaches the selected CC level. However, the instrument CC is insufficient in terms of response time.[60] Therefore, the TC forming voltage is minimally applied longer to the CRS, although the TC has been electroformed yet, causing the immediate BC electroforming. Interestingly, in opposition to the TC, the BC is electroformed with inverse polarity (due anti-serial stacking of both cells). Electroforming processes with negative and positive polarity on single ReRAMs (based on several materials), have been reported and simulated.[119–121] The second forming procedure step (see (3-4) in Figure 6.4a) has no impact on the device. Finally, one cell has to be switched to HRS by the RESET process to activate the CRS characteristic (see (5) in Figure 6.4b).[3] Here, the BC is switched to the HRS, achieved by applying a negative voltage sweep to the TE (without CC). That means the CRS state changes to LRS/HRS. One must take into consideration that there is a strong indication that only the BC is affected by the RESET process (see (5) in Figure 6.4b), because regular complementary resistive switching is observed afterwards (see (6) in Figure 6.4b and Figure 6.4c).

To solve the limitation issue of the instrument CC, in the following, the current regulation is implemented by inserting a series resistor with 82 kΩ.[3] This

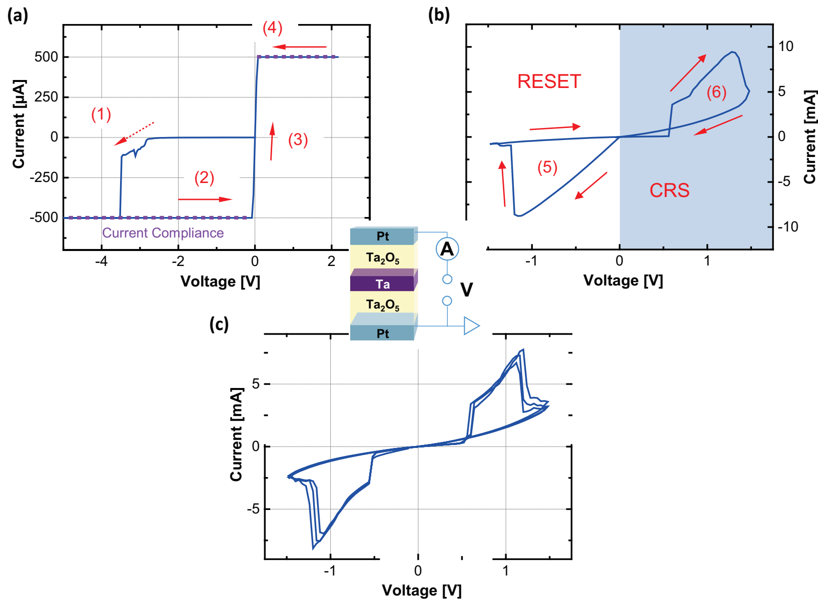


Figure 6.4: (a, b) Electroforming procedure of the top cell (TC) and bottom cell (BC) and (b, c) complementary resistive switching of the two-terminal micro-BC CRS device. During the electroforming process, BC and TC switch simultaneously to the LRS (a, (1-4)), since the response time of the instrument current compliance is insufficient. Afterwards, the RESET process on the BC (b, (5)) is performed to implement the complementary resistive switching mode (b, (6)).[3] (Reprinted with permission from the publisher.)

resistor is mounted directly at the probe tip, which is connected to the TE (to which the voltage signals are forced), in order to avoid overshoots induced by parasitic capacitance.[60] Figure 6.5a presents the electroforming procedure. In the first step, the voltage drops almost completely over CRS, since its initial resistance is about few GΩ, i.e. the serial resistance is negligible. Around -4 V the TC is electroformed (cf. (1) in Figure 6.5a). As a consequence, the CRS conductivity is enhanced abruptly, but the series resistor instantly limits the electrical current.[3]
After this first step, the CRS is rectifying regarding the *I*-*V* characteristic (see Figure 6.5a, (1-2)). This property is similar to a diode, where positive polarity is in the reverse direction. The observation is ascribed to superposed *I*-*V* characteristics of the serial resistor and the unformed rectifying BC. After the TC is electroformed, nearly all voltage instantly drops across the series resistor instantly. Therefore, an uncontrolled electroforming (with wrong polarity) of the BC is prevented.
Next, the BC is electroformed, requiring 2 V (2).[3] After which, the CRS offers linear *I*-*V* characteristic, until the RESET of one cell (cf. Figure 6.5b) is conducted without CC (3). Finally, the micro-BC CRS shows the complementary resistive switching mode (see (4) and Figure 6.5c). The operation current is below 300 μA. In fully embedded CMOS/CRS arrays, line access transistors could control the current on-chip for a successful electroforming procedure. Thus, no further series resistors need to be added to the circuitry, featuring $4F^2$ cell size.

For the two-terminal micro-BC CRS devices, which are not separately electroformed, the CC level does not affect the CRS operation current.[3] If TC and BC are simultaneously electroformed, the process is rather uncontrolled. Therefore, the conducting filament size is also undefined. The same is observed for CRS, which show the vLRS/vLRS state. Considering, this is the most frequent case for non-electroformed, large area ($> 2 \times 2\,\mu\text{m}^2$) CRS.[3] Remember that structural defects, especially oxygen vacancies, are essential for the switching mechanism in VCM-based ReRAMs.[122,123] Large area devices offer an enhanced defect probability. These additional defects could generate a conducting path or, at least, cause a higher leakage current.[124] Therefore,

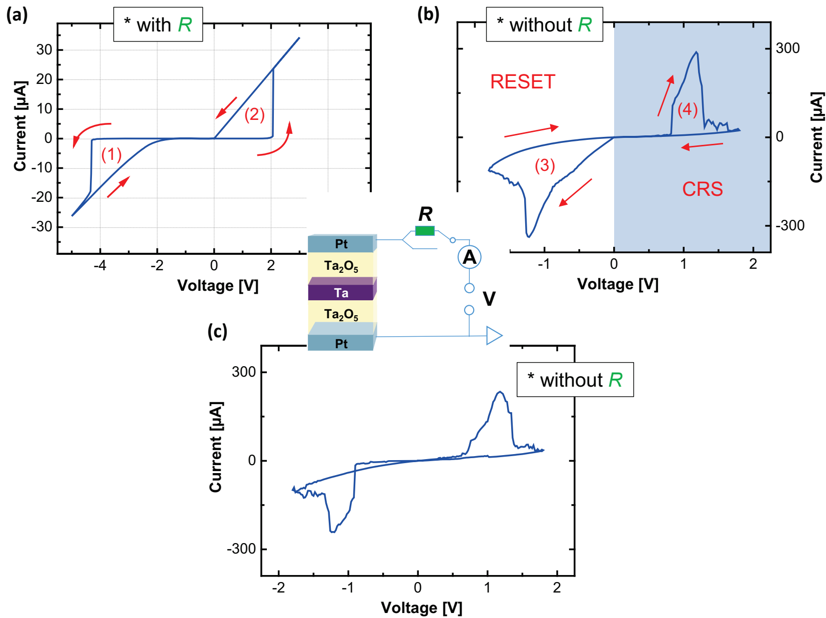


Figure 6.5: (a, b) Electroforming process of top cell (TC) and bottom cell (BC) and (b, c) complementary resistive switching of two-terminal micro-BC CRS device. The centered sketch shows the measurement scheme with optional external serial resistor. For the first two forming steps (a, (1-2)), the additional series resistor ($R = 82\,\mathrm{k}\Omega$) is applied in order to prevent simultaneous electroforming of TC and BC. Subsequently, RESET of BC without an external resistor is performed (b, (3)). Finally, the device offers CRS currents below $300\,\mu\mathrm{A}$ (c, (4)).[3] (Reprinted with permission from the publisher.)

the initial vLRS/vLRS state conductivity is already so high that low switching currents cannot be implemented anymore.

Nevertheless, it is worth studying the properties of those high-current devices.[3] The I-V characteristic of the $2\times2\,\mu\mathrm{m}^2$ micro-BC CRS stack is demonstrated in Figure 6.6a. The I-V cycles are performed after n sweeps, where the ramping rate is about $1\,\mathrm{V/ms}$.

The maximal operation current is rather high, since, for controlled conditions, TC and BC (in structure B devices) are not separately electroformed. In spite of the enhanced operation current, device structure B endures more than

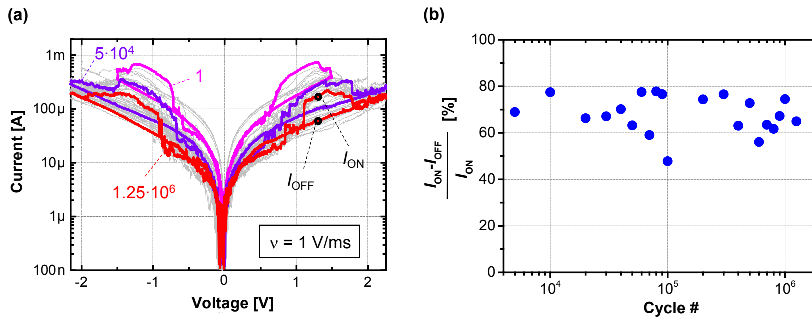


Figure 6.6: (a) I-V characteristics of the two-terminal micro-BC CRS device with a voltage ramp of 1 V/ms. The device endures up to 1.25×10^6 cycles. Exemplary cycles are highlighted in individual colors (1st cycle: pink; 5×10^4 cycles: purple; 1.25×10^6 cycles: red). (b) Normalized current window between I_{ON} (LRS/LRS) and I_{OFF} (HRS/LRS), read at $V_{\text{read}} = 1.3\,\text{V}$.[3] (Reprinted with permission from the publisher.)

1.25×10^6 cycles, excelling the highest reported[67] performance for CRS. Additionally, the experiment shows a slight overall current degradation with increasing number of cycles; for instance ON and OFF current (I_{ON} and I_{OFF}; cf. definition in Figure 6.6a).[3] This degradation might be attributed to the asymmetric TC / BC geometry, especially regarding cell area and oxide thickness, and the slightly non-symmetric I-V characteristic. If this irregularity causes unbalanced RESET / SET processes, i.e. the RESET process is stronger than the SET process, the current will decrease continuously (from cycle to cycle). However, the normalized window between I_{ON} and I_{OFF} (read voltage $V_{\text{read}} = 1.3\,\text{V}$) is fairly constant (see Figure 6.6b).

6.1.2.2 Nano-BC CRS

The I-V characteristic of the nano-BC CRS stack is presented in Figure 6.7, in order to test the electroforming procedure efficiency with this structure.[3] First, the TC is electroformed by forcing negative voltage to the TE (1), then the BC with positive polarity (2). For the TC, a $V_{\text{FORM}} = -2.2\,\text{V}$ and a CC level of about $100\,\mu\text{A}$ are required. In the first step, the nano-BC CRS is not completely electroformed to a highly conductive state, in opposition to the micro-BC CRS, (cf. Figure 6.4a). The CRS offers a rather non-ohmic

state, which shows the rectifying I-V property, similar to a diode with the reverse direction for positive polarity. This characteristic corresponds to the unformed BC. The subsequent electroforming of the BC occurs around 1.3 V (2). Consider: (i) Initially, TC and BC have offered the vHRS state and the voltage has dropped equally over both cells. (ii) Only the voltage drop across the complete CRS stack is sensed. Therefore, the real forming voltage of the single TC cannot be determined by the used experimental setup.
After the first electroforming step, the TC shows the LRS. Thus, in the second step, almost all voltage drops over the BC. Therefore, a lower V_{FORM} is observed for the BC.[3] The cells of the investigated nano-BC devices offer thinner oxide films (5 nm as deposited) compared to the micro-BC CRS (10 nm as deposited). The metal-oxide thickness affects the forming voltage as reported in literature.[124, 125] Hence, lower voltage is sufficient to electroform the thinner nano-BC CRS. Furthermore, the separate electroforming procedure is reliable with the instrument CC and does not need an external serial resistor. The small-dimension conductor line (width 100 nm), from the BE contact pad to the BC, is the reason for this achievement.[3] As comparison, the micro-BC CRS conductor line is several micrometers broad. Smaller lines act as a higher inbuilt series resistor (here: 100 Ω...400 Ω). Of course, the actual value depends on the material (resistivity) and line length. However, for the successful separate electroforming procedure, the TC resistance after forming ($\sim$ 20 kΩ in LRS), which is considered as additional serial resistor CC, is crucial.
After the second forming step, the instrument CC is deactivated and, by forcing a negative voltage sweep to the TE, the RESET process of the BC is performed (see (3) in Figure 6.7b).[3] Thus, the BC is switched to the HRS and the TC remains in the LRS. Since the probability of defects, which could induce an initial vLRS/vLRS state is reduced, due to the small cell size of the nano-BC CRS, most devices show the vHRS/vHRS state at the beginning. That means the initial CRS resistance (1.4 MΩ at read voltage of -0.2 V) is sufficient to electroform the individual cells separately.
Thirty consecutive switching cycles of the nano-BC CRS are demonstrated in Figure 6.7c. The maximal operation current is below 300 μA. The present device has been electroformed with the $I_{\mathrm{CC}} = 200\,\mu$A CC level. The low current level indicates that the separate electroforming process can be well controlled

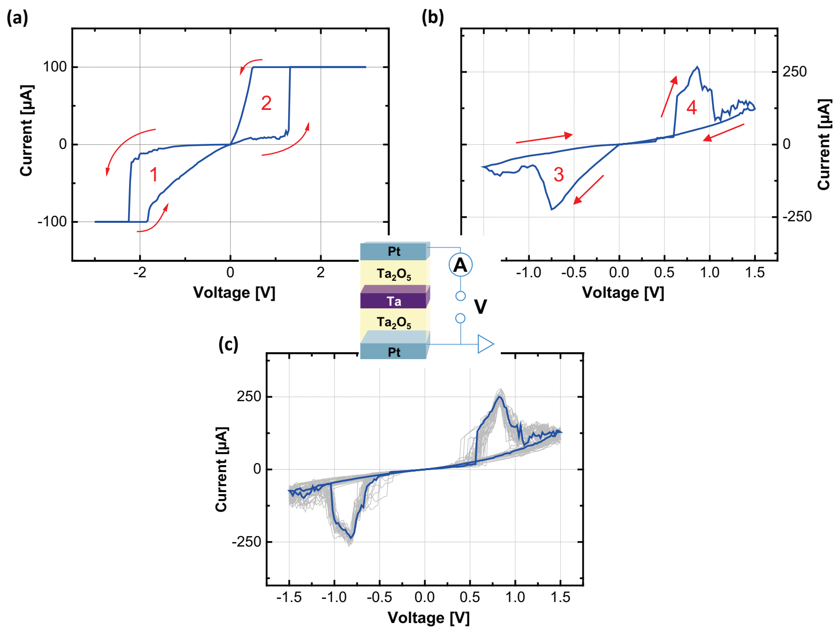


Figure 6.7: (a, b) Electroforming process of top cell (TC) and bottom cell (BC) and (b, c) complementary resistive switching of the two-terminal nano-BC CRS device. The TC is electroformed by forcing negative voltage stimulus to the top Pt (a, (1)). Afterwards, positive voltage stimulus is applied to generate the conductive filament in the BC (2). Subsequently, the RESET process is performed on the BC and thus the CRS stack is switched to the LRS/HRS state (b, (3)). Finally, the device offers stable complementary resistive switching (c).[3] (Reprinted with permission from the publisher.)

without the use of an external serial resistor. At next, the effect of the I_{CC} level on the operation current is investigated. For this purpose, the devices have been electroformed for several CC levels ($I_{CC} = 100\,\mu A$, $200\,\mu A$ and $500\,\mu A$).[3] The dependence of the maximal operation current (I_{max}@CRS) on I_{CC} is summarized in Figure 6.8.

Both cells have been electroformed with equal I_{CC}. It is remarkable that the switching current decreases by lowering I_{CC}. However, this observation is not unexpected, since the diameter of the conducting filament, which is generated by the electroforming process, depends on I_{CC}.[107] Higher I_{CC} might induce

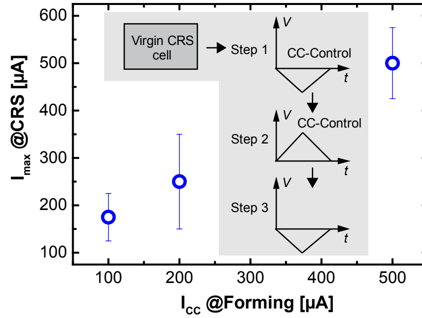


Figure 6.8: Maximal CRS switching current (I_{max}@CRS) as function of current compliance level I_{CC}, which is applied during the separate electroforming procedure. The procedure consists of three steps as demonstrated by the inset scheme. The CRS current is reduced with I_{CC}.[3] (Reprinted with permission from the publisher.)

thicker filament diameter in each cell, including higher conductivity. However, once the two conducting cell paths are generated by the electroforming process, the CRS characteristic is dominated by the current self-limitation feature.[3] The cell being in HRS limits the current, which passes the second cell being in LRS. This intrinsic alternating CC feature is caused by the dynamic CRS system.
This suggestion has been confirmed by a dynamic simulation model.[126] Thus, both cells can be operated at lower current ($< 300\,\mu$A).[3] The maximal current might be decreased more by further lowering the I_{CC} (during electroforming) or material and device engineering. For instance, BC and TC could base upon inhomogeneous oxygen vacancy profiles in the oxide layer (e.g. realized by bilayer structure[122]) or different materials. By this means, the Schottky barrier height (at the Pt-oxide interface) could be tailored in order to decrease the overshoot current, which occurs for the electroforming procedure.

Furthermore, endurance experiments have been performed. In the beginning, the nano-BC CRS have been electroformed with $I_{\text{CC}} = 500\,\mu$A.[3] For the endurance test, quasi-static driven I-V cycles are measured after n pulsed cycles (see Figure 6.9a). The applied pulses show a width of 2 ms and an amplitude of ±2.5 V. For more than 10^4 cycles, the CRS switches reliably and shows a stable normalized current window of I_{ON} to I_{OFF} (cf. Figure 6.9b).

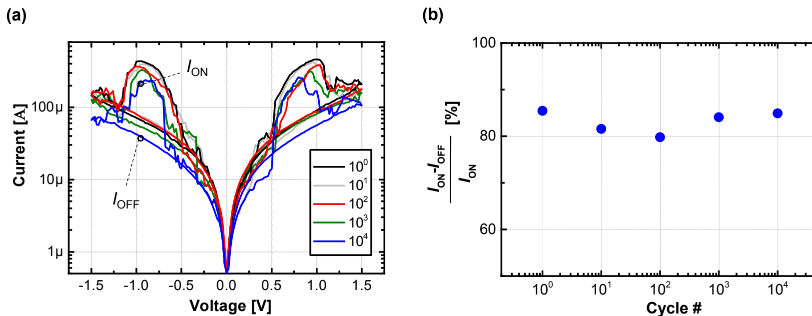


Figure 6.9: Endurance measurement of the two-terminal nano-BC CRS. (a) I-V characteristic for quasi-static voltage ramps after n pulsed cycles (alternating positive and negative pulses). The overall current decrease with the number of cycles is less distinct than for micro-BC CRS devices. (b) Normalized current window between I_{OFF} and I_{ON} is very stable.[3] (Reprinted with permission from the publisher.)

Nonetheless, a slight decrease of the overall current with increasing number of cycles is recognized, which might be caused by unbalanced RESET / SET events, i.e. the RESET process is stronger the SET process.

6.2 Conclusion

Three differently structured CRS devices are considered.[3] Each device is implemented by two vertically and anti-serially stacked single bipolar switching ReRAM cells. The final CRS layer sequence is for all CRS types identical: Pt|Ta_2O_5|Ta|Ta_2O_5|Pt.

For the three-terminal micro-BC CRS (with access to the ME), TC and BC are separately electroformed via the conventional way (individual contacting).[3] The switching current of the CRS depends highly on the electroforming process of the individual cells and can be reduced by the applied CC level. This enables low-current operation ($< 300\,\mu$A) in the CRS.

The two-terminal micro-BC CRS device (with embedded ME) offers higher switching current than the three-terminal structure.[3] This is ascribed to the uncontrollable / non-separated electroforming process and the simultaneous breakdown of both cells, as consequence of insufficient response time of the

instrument CC. The separate electroforming of the single cells is achieved by use of a proper external serial resistor, which controls the forming current and enables low-current CRS operation. Regarding the state-of-the-art technology, the two-terminal CRS shows improved endurance performance ($> 10^6$ cycles). For the two-terminal nano-BC CRS, the separate electroforming process is well controlled without the need of an external series resistor.[3] Therefore, low CRS current is achieved, which is proportional to the I_{CC} during the forming process. Based on this approach, the switching current of the nano-BC CRS is reduced down to $\sim 200\,\mu$A. Additionally, these devices switch up to 10^4 cycles. The investigations suggest that CRS devices with embedded ME, which are electroformed by the novel forming procedure, are promising memory elements for future low-current applications in passive nano-crossbar structures.[3]

Chapter 7

ReRAM Device Application

7.1 Minimum / Maximum Gate

7.1.1 Basics

The complementary resistive switch (CRS) is based upon two single ReRAM, which are integrated in an anti-serial configuration and referred to as top cell (TC) and bottom cell (BC).[1] Each of them can be switched from a highly resistive state (HRS) to a lowly resistive state (LRS) and vice versa. Here, the focus is on Ta_2O_5-based ReRAMs as illustrated in Figure 7.1. The resistive switching Ta_2O_5 films of the TC and BC are stacked between Ta and Pt electrodes. The complete device film stack is symmetric. Hence, the *I*-*V* characteristic is also symmetric and does not depend on which side, i.e. bottom electrode (BE) or top electrode (TE), the voltage is applied. In the CRS, BC and TC switch always complementarily as consequence of the anti-serial stacking.

Figure 7.1 demonstrates the two configurations for vertical stacking of single ReRAMs to generate a CRS device.[1] The CRS *I*-*V* characteristics for both configurations are not distinguishable. Certainly, the polarities for the SET and RESET process of the BC and TC, differ for both cases. The more conventional layer sequence (Pt|Ta_2O_5|Ta|Ta_2O_5|Pt) of the CRS is illustrated in Figure 7.1a. Beginning with the state configuration, where the TC is in LRS and BC in HRS (referred to as the CRS state LRS/HRS): To the top Pt electrode, positive voltage is applied, while the bottom one is set to ground. The

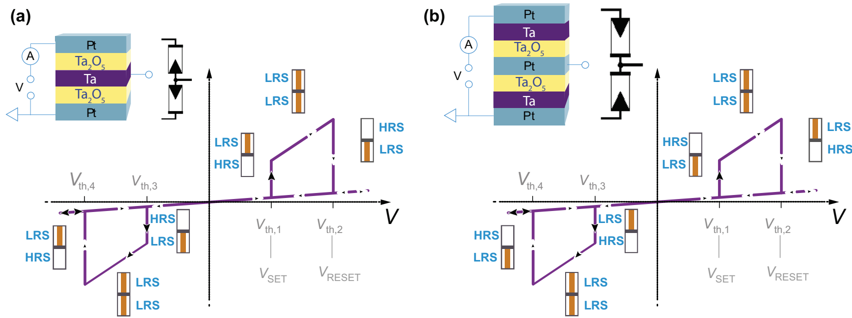


Figure 7.1: (a) CRS stack with equivalent circuit and related *I*-*V* scheme of the MIN logic gate. (b) The inverse CRS stack with corresponding equivalent circuit and *I*-*V* switching scheme of the MAX logic gate. Beside the ideal *I*-*V* curve (purple colored), the respective CRS state is indicated by resistance scheme. Corresponding RESET and SET events of BC / TC occur at the respective threshold voltages $V_{\mathrm{th},1}$ to $V_{\mathrm{th},4}$.[1] (Reprinted with permission from the publisher.)

BC state changes to LRS at threshold voltage $V_{\mathrm{th},1}$, i.e. the CRS switches to the LRS/LRS transition state (cf. Figure 2.3). By enhancing voltage to $V > V_{\mathrm{th},2}$, the TC becomes highly resistive, that means the CRS state changes to HRS/LRS. The CRS does not switch anymore and remains in the state HRS/LRS as long as no positive voltage is applied. Only for sufficiently negative voltage amplitude, the device switches to the LRS/LRS transition state, because the TC becomes lowly resistive at $V_{\mathrm{th},3}$. At $V_{\mathrm{th},4}$, the CRS switches to the original state (LRS/HRS) by rupturing the conductive BC filament. The second stacking configuration for the CRS is depicted in Figure 7.1b. In comparison to Figure 7.1a, this device exhibits inverse switching of the TC and BC. However, this difference is not visible in the *I*-*V* characteristic.

For the logic operations, the non-transition states, LRS/HRS and HRS/LRS, are of main interest.[1] Crucial prerequisites for realization of the Maximum (MAX) and Minimum (MIN) logic are:

- The two stacked cells offer always complementary and reversible switching with two resistive states. That means one cell is always (after each performed operation) in the high resistance state, whereas the other one is in the low resistance state.

- The LRS resistance is always negligible in comparison to the HRS resistance.

As depicted in Figure 7.2 the CRS is used as three-terminal (T1, T2 and T3) gate, in order to implement the MIN / MAX feature. T1 and T2 correspond to the top and bottom Pt electrode. For sensing the resulting signal the middle electrode (ME) is used, which is referred to as the third terminal T3. The input signal q is applied to terminal T1, whereas p is the input signal applied to terminal T2. The resulting signal, which is sensed at T3, is referred to as *out*.
For any MIN / MAX logic operation, T1 and T2 are either set to high potential 'H' or low potential 'L'. As an initial and simpler approach, instead of TC and BC, two static resistors with corresponding resistances R_1 and R_2 are considered, to understand the MIN / MAX logic concept. The sensed signal *out* is determined by

$$out = \frac{R_1}{R_1 + R_2} p + \frac{R_2}{R_1 + R_2} q \tag{7.1}$$

Since the LRS resistance is negligible in comparison to the HRS one, $R_1 \gg R_2$ is assumed without limiting the generality. This simplifies Equation 7.1 to $out \approx p$.[1] That means, the voltage applied to T1 drops completely over the resistor R_1. Therefore, the sensed voltage at T3 is always equal to the applied voltage to T2.
However, this result does not depend on the voltage configuration, which is a drawback of the static resistor consideration.[1] Due to this reason, the MIN / MAX gate logic cannot be realized by classical resistors. However, the CRS on the other hand consists of two dynamic resistors, which show complementary change of resistance. The CRS is capable of fulfilling all the requirements for the MIN / MAX operating mode, since it toggles between HRS/LRS and LRS/HRS, as function of the actual state and the applied voltages to T1 and T2.
The truth tables for the MIN / MAX function are depicted in Figure 7.2b.[1] The device dynamics are illustrated for all configurations of the input signals q and p. The 4th and 6th table column describe the MIN operation, by means

of device behavior and expected result. At the beginning, the initialization is performed by applying p = 'L' and q = 'H' to the corresponding terminals. This is equivalent to applying positive potential to the top Pt electrode, while setting the bottom one to ground (cf. Figure 7.1).
For the experimental part, consider two points: The initialization procedure is not a requirement for the logic concept and only performed once.[1] It sets the device to a defined state. This facilitates to follow and verify the device dynamics from the beginning. Secondly, observation of any switching event depends on the time resolution of experimental setup and the previous CRS state. Nonetheless, the resulting CRS states and thus the corresponding *out* results are clear for all q and p configurations.
The CRS stack shown in Figure 7.1a is used to implement the MIN function.[1] By initialization, the stack is switched to the HRS/LRS state. In the first configuration, q = 'L' and p = 'L' are applied. Here, no voltage drops across the CRS stack. Hence, the BC remains in LRS and the TC in HRS. As consequence, the signal, which is applied to T1, drops completely over the TC (being in HRS), but there is almost no voltage drop across the BC and therefore $out = p$ = 'L'. Afterwards, the asymmetric configuration q = 'H' and p = 'L' are used. This configuration is equivalent to the initialization. The CRS state does not switch, therefore, $out = p$ = 'L' is sensed. Now, the polarities at the input terminals are flipped to q = 'L', p = 'H'. This configuration is equal to grounding T2 and applying negative voltage polarity to T1 (see Figure 7.1a). The BC shows transition from LRS to HRS, whereas the TC switches from HRS to LRS ($\rightarrow$ LRS/HRS). Afterwards, the applied voltage to T2 drops completely over the BC (being in HRS), but nearly no voltage drop over the TC (being in LRS) occurs. Therefore, $out = q$ = 'L'. For the last configuration, q = 'H' and p = 'H', which is symmetric, there is no voltage drop over the CRS. Thus, the device remains in the present state (LRS/HRS) and $out = q$ = 'H' is detected. Thence, the MIN logic gate device always provides the minimum value as output for all possible input configurations.[1]

The CRS stack, which is used for generating the MAX operation, is demonstrated in Figure 7.1b.[1] The resistive dynamics of the gate device and the

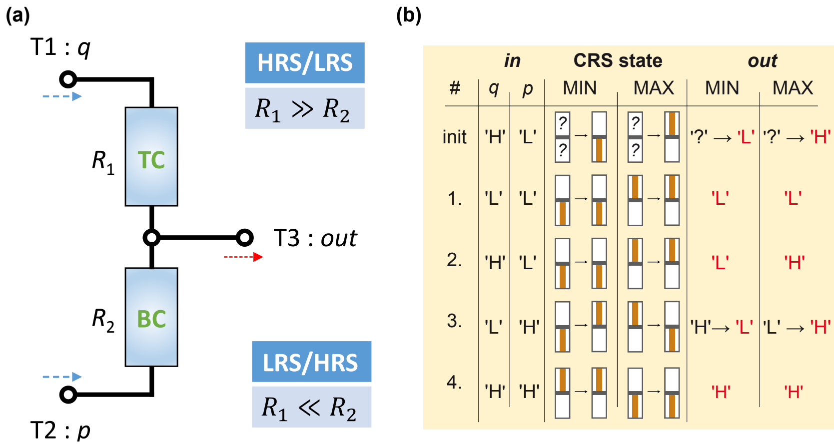


Figure 7.2: (a) General measurement concept for the MIN / MAX function. (b) Truth table: MIN / MAX gate operation for all q and p depending input configurations (2nd and 3rd table column). q is applied to terminal T1, whereas p to terminal T2. The logic concept does not require any initialization process, but here, the step is used to predict the device dynamics from the beginning (4th and 5th table column). Both, the previous device state and the present input configuration determine the actual switching process, but the result (6th and 7th table column, red labeled) is clear and does not depend on the previous state.[1] (Reprinted with permission from the publisher.)

sensed *out* signal are summarized by the 5th and 7th table column in Figure 7.2b. The initializing procedure, setting T1 to q = 'H' and T2 to p = 'L', defines the CRS state as LRS/HRS, different to the MIN gate, which has been set to the HRS/LRS state by the same input configuration. That is attributed to the inverse CRS stack. For the symmetric input configuration q = 'L' and p = 'L', no resistance change at all occurs and thus $out = q$ = 'L' is detected. Using the configuration q = 'H' and p = 'L' does not switch the CRS and $out = q$ = 'H' sensed. The next configuration with q = 'L' and p = 'H', i.e. reversed voltage polarity in comparison to the previous one, changes the device state to HRS/LRS so that $out = p$ = 'H' is received. Finally, q = 'H' and p = 'H' are used. No voltage drop over the device occurs due to the symmetric input potentials. Thus, the CRS state remains unchanged (HRS/LRS) and out = 'H' is sensed. In total, the MAX logic gate provides the maximum value as output for all possible input configurations.[1]

7.1.2 Proof-of-Concept

7.1.2.1 Checking of Device Requirements

Three-terminal CRS devices facilitate the ME access using terminal T3.[1] Therefore, the feature of individual electroforming and bipolar switching on the BC / TC is enabled. The TC is accessed by grounding T1 and forcing voltage to T3. For controlling the BC, the terminals T3 and T2 are used.
Electrical investigations of both cell types are demonstrated in Figure 7.3(a,b), where (a) is related to the TC and (b) to the BC.[1] The illustration is divided into the upper figure showing the linear I-V curves and the lower figure demonstrating the logarithmical R-V curves. The required electroforming procedure on individual cells is represented by the dotted, gray curve. For unformed devices, the initial resistances vary from some hundred kΩ to a few MΩ. By applying positive voltage, the conductive filament is generated and the current increases abruptly around $1.7\,V$. The instrument current compliance (CC) level at about $500\,\mu A$ stops the SET process and limits the conductivity, in order to avoid any damage. Furthermore, it has been demonstrated that the CC level has a direct impact on the maximal operation current.[3] A lower CC level reduces the current in single ReRAMs and as a result, also in the CRS.

Around 1 kΩ, BC and TC are electroformed to LRS and show ohmic current-voltage-characteristics.[1] The final bipolar switching is represented by the blue curves: By using negative voltage polarity, the gradual RESET process becomes visible below $-0.6\,V$ and the devices are switched to non-ohmic HRS, where resistances vary around $R_{\mathrm{HRS}} \approx 100\,\mathrm{k}\Omega ... \mathrm{M}\Omega$. Applying a positive voltage, the SET event occurs around $1\,V$, where the current rises abruptly. The LRS shows a resistance R_{LRS} of about 1 kΩ. The resistances of the individual states have been determined by ramping the reading voltage in the range of $\pm 0.5\,V$ (red / green, dashed line). The data displays a symmetric resistance ratio (for negative and positive reading polarity) with $R_{\mathrm{HRS}}/R_{\mathrm{LRS}} \approx 100...1000$. With respect to the prerequisites summarized in Subsection 7.1.1, this result is satisfying for implementation of fuzzy gate logic.
Furthermore, endurance measurements on individual bottom and top cells have been conducted. However, BC and TC do not distinguish regarding the endurance performance and only one representing measurement is demonstrated in Figure 7.3(c,d). For the experiment, microsecond pulses have been applied. Device resistance has been recorded for the HRS and LRS by applying $V_{\mathrm{read}} = 0.2\,V$. The complete data record up to 10^4 cycles is presented in (c). Although no algorithm for controlling the target resistance has been applied, the resistance window is clear and larger than one order of magnitude. The extended endurance test up to 10^6 cycles is demonstrated in (d). In order to reduce the needed measuring time, reading has not been performed after each cycle, i.e. the data has been recorded on logarithmical time scale.

Next, the CRS contact mode is used. This means T3 is not considered and forcing voltage is applied to T1 and / or T2, respectively. Thereby, the device shows non-linear complementary resistive switching (see Figure 7.1).[1] The current response of the CRS stack measured as function of quasi-static voltage sweep is plotted in Figure 7.4a. Here, T2 is set to ground and the voltage stimuli is forced to T1.
MIN and MAX gates show similar *I*-*V* curves and only one representative measurement is depicted. The intrinsic feature of the CRS is self-limitation of the operation current, which is reduced below $500\,\mu A$. This low-current operation is achieved by individual electroforming procedure of the BC and

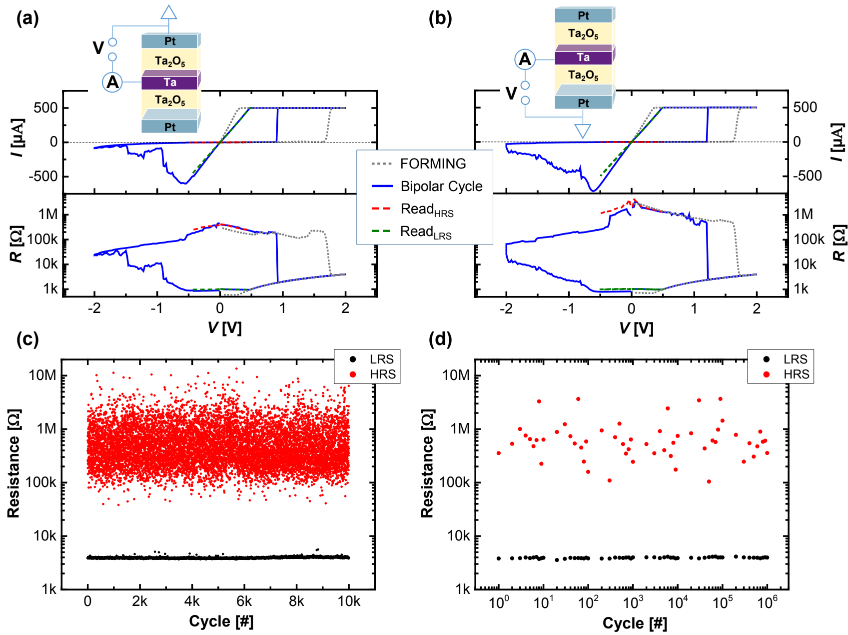


Figure 7.3: Individual quasi-static investigation of (a) TC and (b) BC. The upper insets show the applied experimental setup. The top graph demonstrates the I-V characteristic, the lower one represents the R-V curve. After the required, separate electroforming procedure (dotted, gray curve), TC and BC show the bipolar resistive switching (blue curve). Analysis of the HRS and LRS resistances (green / red, dashed curve) depicts the symmetric resistance window. (c) and (d) summarize endurance test on the BC / TC. (c) Non-reduced data recorded up to 10^4 cycles, (d) reduced endurance data recorded up to 10^6 cycles by sensing on logarithmical time scale.[1] (Reprinted with permission from the publisher.)

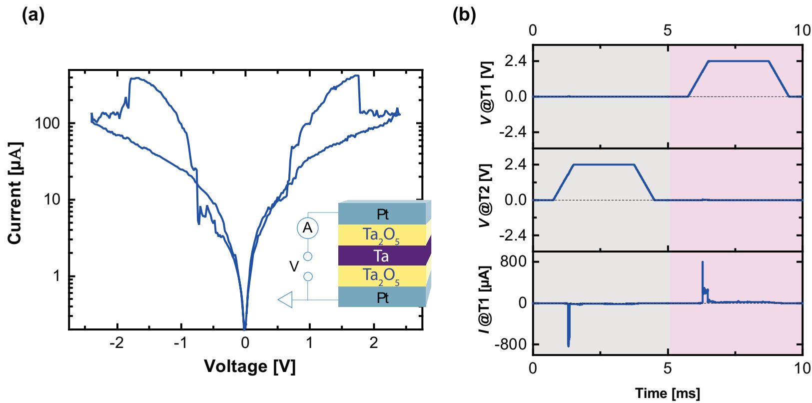


Figure 7.4: Electrical investigation of the CRS device. (a) quasi-static I-V curve with experimental setup as inset and (b) μs-pulse driven measurement with transient current response.[1] (Reprinted with permission from the publisher.)

TC, while using low CC level.[3]
The symmetric current-voltage characteristic offers clear SET and RESET events for negative / positive polarity.[1] However, pulse driven experiments are of more interest for applications. Therefore, transient response currents as function of voltage pulse stimuli (amplitude: 2.4 V; width: 3 ms) are plotted in (b). Switching of the CRS state is detected as a current spike, which is more relevant for the CRS-logic presented in Section 7.2. Recent investigations prove these CRS devices show reliable switching for more than 10^6 cycles.[3]

7.1.2.2 MIN Gate Function.

For all demonstrated electrometric experiments on the MIN / MAX gate, either the Keithley 4200-SCS or the Agilent B1500A parameter analyzer have been used.[1] In case of quasi-static experiments, the *out* signal at T3 is sensed by using the current bias mode (voltage sensing unit). That means the current level for T3 is fixed to zero. For sensing the voltage, a counter voltage is automatically applied at T3, in order to keep the current on the fixed level. This is only possible, if both voltages have the same absolute value. However, this concept cannot be applied for pulse driven experiments due to an insufficient response time of the instrument to regulate the counter voltage. Hence, the

resulting voltage at T3 is sensed by a self-designed impedance converter (IC), whose simplified circuit is illustrated in Figure 3.5. The bandwidth of the IC is about 8 MHz and it supports slew rates up to 2.8 V/μs. Additionally, the IC offers high input resistance about 3 GΩ, that ensures nearly no current passes T3.

Figure 7.5 demonstrates representative experimental realizations of the MIN function by means of three voltage modes: (a) quasi-static voltage sweep, (b) base voltage (applying constant voltage levels) and (c) voltage pulse.[1] In order to prove the device flexibility, the experiments also differ in values for ‘L’ and ‘H’. The voltage, which drops over the CRS, is determined by the difference of the signals at T1 and T2. The maximal absolute value, which is given for $q \neq p$, has to be sufficient for toggling the CRS.
Static and dynamic characteristics of the MIN gate are plotted as function of time and, above the graph, the corresponding final states are illustrated by the familiar resistance scheme.[1] The first two upper signal lines represent applied voltages to T1 and T2. The third line in (a,c) is related to the current response. The lowest signal line represents *out* at T3. Whenever a switch of CRS is directly recorded by the instrumental setup, i.e. an abrupt drop of *out* or a current spike is observed, the change of the CRS state is clearly highlighted by means of the resistance sketch below the graph.
At the beginning, the gate device is initialized by setting T1 to ‘H’ T2 to ‘L’.[1] This step is not needed for the MIN function and thus not demonstrated in Figure 7.5 ,but it enables confirmation of the CRS response for the first input configuration. The sequence of configurations for q and p is identical to the one depicted in the previous truth table (cf. Figure 7.2b). It should be noted that the used sequence has no impact on the final logic state and therefore not on final result. Nonetheless, the sequence has an impact on possible detected switching events in the *out* signal, which are not considered to interpret the result.[1] The result is clear for a certain configuration of q and p and is always independent of the used voltage mode. In total, the logic device always displays the minimal value of q and p, as expected for the MIN gate.

The experiment, which has been performed by the base voltage mode, is demonstrated Figure 7.5b.[1] Here, the switching is not visible in the *out* signal line, since the instrument time resolution is insufficient for detecting the abrupt voltage drop / current response. Thus, the current signal is not shown. Nonetheless, the CRS state switches for the configuration $q =$ 'L' and $p =$ 'H', but it is not visible by the recorded data. However, for the voltage sweep and the pulsed mode, the switching dynamic is detected by current and *out* responses (see Figure 7.5(a,c)). For the quasi-static mode (a), when q is swept to $0.6\,V$ and p to $3\,V$, the CRS does not switch directly. That is attributed to the fact that the voltage is slowly increased and is insufficient at the beginning. Firstly, *out* increases first to $3\,V$ instead of $0.6\,V$, since BC is in LRS and TC in HRS (LRS/HRS). Once the voltage drop across the CRS stack is sufficient, the state switches to LRS/HRS. Simultaneously, the voltage at T3 decreases spontaneously to $0.6\,V$. For the pulse driven mode, a similar abrupt voltage decrease is detected (c), once the CRS state is switched.
For the configuration $q = p =$ 'H' with 'H' $= 3\,V$ in (a), the sweeping time is significantly enhanced in comparison to the other configurations. However, this is just an artifact caused by the measurement equipment, since the measured current level has a direct impact on instrumentally adjusted speed of the voltage sweep. For $q = p$, no voltage drops over the CRS and thus only current noise is sensed. The same is given for the configuration $q = p =$ 'L' with 'L' $= 0.6\,V$). However, here the timing for sweeping is five times quicker. This is not remarkable, since the input signal amplitude is lowered by the inversed factor. Further representative experiments are demonstrated in the supplementary information of [1].

7.1.2.3 MAX Gate Function

The MAX gate device is composed of the inversed CRS stack as demonstrated in Figure 7.1b.[1] The MAX gate device is initialized at the beginning, similar to the MIN gate, even though the procedure is not needed for the logic functionality. The experimental results for three voltage operation modes are presented in Figure 7.6: (a) the voltage sweep, (b) the base voltage and (c) the pulse driven voltage mode. Several values for the high and low potentials are used to show the MAX gate flexibility. The structure of the figure

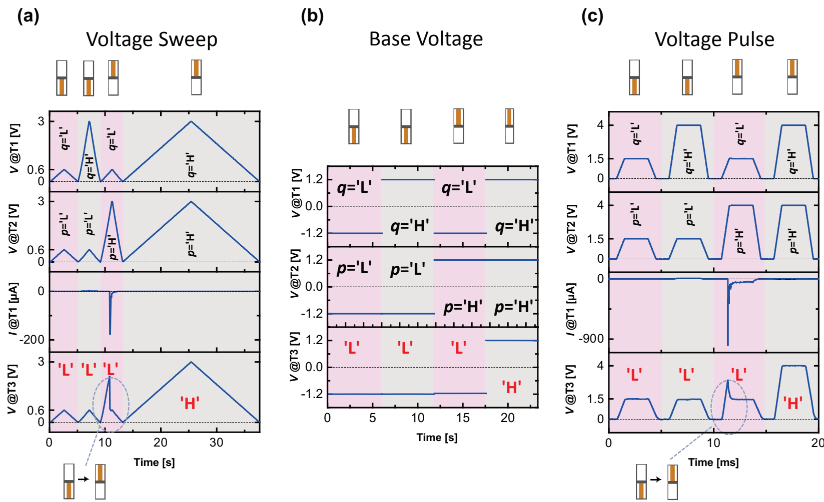


Figure 7.5: MIN gate logic implementation by means of three voltage modes: (a) quasi-static voltage sweep, (b) base voltage (applying constant voltage levels) and (c) voltage pulse. Resistance scheme above the graphs shows the resulting CRS state. A change of state, which is detected in the recorded data, is highlighted by the resistance scheme below the plots. The graphs include from top to bottom: voltage signal at T1 and T2, current signal (only a, c) and sensed voltage at T3. The base voltage experiment (b) does not show the current signal, since switching is not explicitly observed due to insufficient instrumental time resolution. 'L' (low potential) and 'H' (high potential) are related to applied input and detected output signals, respectively. Values for 'L' and 'H' are varied to prove the flexibility of the gate device.[1] (Reprinted with permission from the publisher.)

is equal to the one, which has been used to discuss the MIN operation above. *out* always displays the maximal value for all configurations of the inputs q and p, as expected for the MAX gate. Further representative experiments are demonstrated in the supplementary information of [1].

7.1.3 Discussion

Depending on the experimental conditions, the results of MIN and MAX operations are not directly available in the *out* signal, i.e. a specific settling time constant of the gate device has to be respected.[1] Essentially, the voltage amplitude applied to T1 and T2 has an impact on this settling time. That means, for ramp signals with a slow slew rate or low amplitude, the MIN and MAX logic function requires more time than for short voltage pulses with larger amplitudes.

For the pulse driven experimental application, the IC is the limiting factor, which supports a slew rate up to 2.8 V/μs and 8 MHz bandwidth.[1] Here, in order to guarantee sensing of abrupt voltage drops, which are the result of the CRS switching dynamics, the gate devices are driven in the millisecond pulse range. Indeed, if the CRS runs reliably, it will not be required to measure the current response and to detect switching events. The reason (for showing the current signal) is clearer evidence for the device logic functionality. The MIN / MAX gate is not limited in relation to the operation time, since ReRAMs feature write operations below 200 ps.[14] Thus, the optimization process for sensing and filtering the *out* signal is a major challenge.

The optimal approach for a sensor unit would be an IC with a high slew rate, high input resistance and wide bandwidth.[1] Certainly, for integrated sense amplification, the circuitry quality is rather unusual. More commonly, stages with reduced input impedances are mainstream.[79] Hence, the current stage depends on the input impedances of the subsequent logic stage elements. Thence, for actual circuit design, loading of the *out* signal is very significant issue.[79] Operating speed in the order of microseconds would be sufficient for many applications (i.e. audio signal processing or signal sorting). Therefore, the timing constraint is not at all critical.[79]

'L' or 'H' are not limited in theory relating to their individual values. Rather, the voltage (*out*), which is supplied by the IC, is limited (here: $\pm 12\,V$).[1] Cer-

tainly, there is a second limitation regarding the minimal difference of 'L' and 'H', as discussed in Subsection 7.1.1: this difference should be at least equal to the threshold voltages $V_{\text{th},2}$ and $V_{\text{th},4}$ (cf. Figure 2.3). If this requirement is not satisfied, the CRS will never switch and cannot meet the specifications for the MIN / MAX logic concept. Moreover, the potential difference determines the switching kinetics, which are generally dominated by the (voltage-time) non-linear property of ReRAMs.[124, 127–129] That means shorter pulses require higher amplitudes to switch the device. Therefore, it should be ensured that the voltage drop is sufficient for the used pulse width. The input signal difference could be more optimized by modifying several pulse parameters, such as rising / falling time.[1] The second approach is reduction of the threshold voltages ($V_{\text{th},2}$ and $V_{\text{th},4}$, cf. Figure 2.3). This could be achieved by engineering of used materials and device design.

Regarding concatenability, it should be noted that the demonstrated logic gates provide restricted performance due to the lack of signal restoration within the CRS device.[1, 8] One option, in order overcome this issue: analog buffers are integrated in the electric circuit.[8] Though, small-size circuitry blocks without any buffer will also work, for instance, realization of memristive sorting networks enabling high energy and area efficiency. Otherwise, timed transistor-based systems for cascading can also be used.[8, 130] The benefits of using the last scheme enable the use of the separated and controlled electroforming procedure.[8]

The presented ReRAM-based approach enables a smaller unit array and excellent facilities of scaling in comparison to conventional CMOS-based approaches (cf. Table 1.1).[1] Furthermore, the use of the CRS keeps the power consumption to a minimal level, since these devices exhibit highly resistive states and short switching times (HRS/LRS $\leftrightarrow$ LRS/HRS). Nevertheless, to enable ReRAM-based logic applications, further investigations concerning performance improvement (such as endurance, reliability and cycle-to-cycle variation) still have to be done.[1] Even though ReRAMs facilitate low-energy operations,[131] the more relevant consideration is the direct comparison of ReRAM-based and CMOS-based circuitries, in the sense of energy efficiency. However, this can only be answered precisely, if the actual application area and circuitry are known.[132]

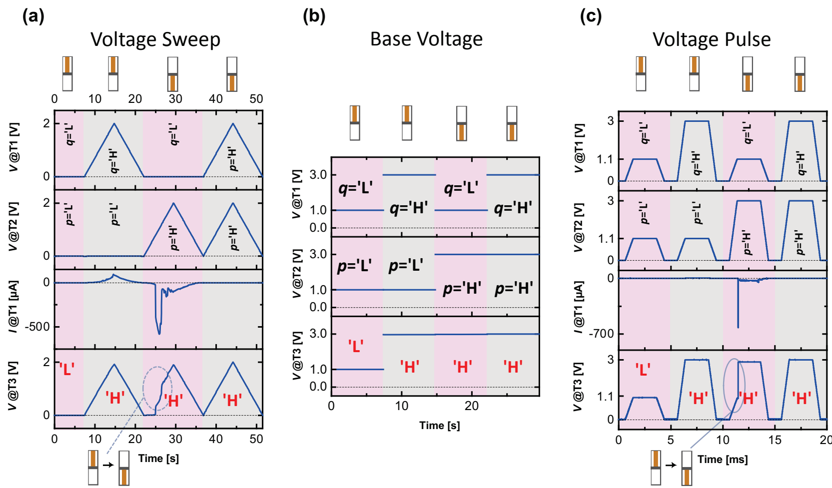


Figure 7.6: MAX gate logic implementation by means of three voltage modes: (a) quasi-static voltage sweep, (b) base voltage (applying constant voltage levels) and (c) voltage pulse. Resistance scheme above the graphs shows the resulting CRS state. A change of state, which is detected in the recorded data, is highlighted by resistance scheme below the plots. The graphs includes from top to bottom: voltage signal at T1 and T2, current signal (only a, c) and sensed voltage at T3. The base voltage experiment (b) does not show the current signal, since switching is not explicitly observed due to insufficient instrumental time resolution. 'L' (low potential) and 'H' (high potential) are related to applied input and detected output signals, respectively. Values for 'L' and 'H' are varied to demonstrate the gate device flexibility.[1] (Reprinted with permission from the publisher.)

7.2 Logic-in-Memory (CRS-Logic)

Basic logic functions are fundamental elements for more complex processing-in-memory operations (see section 7.3) and therefore discussed first. As a starting point the CRS-logic concept, which has been suggested by Linn *et al.* in [9], is explained in brief. Single bipolar switching ReRAMs are capable of performing 14 (out of 16) two-input Boolean operations by applying this logic concept. The remaining two logic functions, XOR and XNOR, are realized by the modified CRS-logic concept with a standard readout scheme but using two memory devices[9] or the extended logic concept with a conditional readout scheme.[5, 133]
In spite of the name, the CRS-logic concept is not only compatible with the CRS (based on VCM or ECM), but also to all types of bipolar resistive switching memory devices (based on VCM or ECM), threshold switching-based ReRAM and CS (based on VCM).[5, 9, 76]

7.2.1 Basics

Due to multi-compatibility of the CRS-logic to each bipolar resistive switching device, the principles are simply demonstrated on the CRS, representatively for each bipolar ReRAM device. Concerning computation and logic applications, it is more common to identify the device state Z by the two binary logic states '0' and '1'. It does not matter, what CRS state is related to which logic state, as long as it is done consequently. Here, HRS/LRS (TC in HRS, BC in LRS) is identified with the logical '1' (Z = '1') and LRS/HRS (TC in LRS, BC in HRS) by the logical '0' (Z = '0'). The less important transition state LRS/LRS is called 'ON'.
The common CRS device offers two terminals (T1 and T2) for applying the input signals, which can be identified with the TE and the BE respectively (cf. Figure 2.3 and 7.7b topmost draft). Binary logic operations require the two input variables q and p, which are either '0' or '1'. All applied voltage signals to the terminals are either high potential (input: '1') or low potential (input '0'). For instance, the CRS offering the initial state Z' = '1' will only flip to the subsequent state Z = '0', if '0' is applied to terminal T1 and '1' to T2. The remaining voltage conditions do not affect the initial state, that means

$Z = Z' =$ '1' is the consequence. However, if the cell is initially in $Z' =$ '0' only the condition, where '1' is applied to T1 and '0' to T2, will flip the device state to $Z =$ '1'. For the remaining voltage conditions, the expression $Z = Z' =$ '0' is valid.
The subsequent state Z can be interpreted as logic operation result. That means, if the initial state Z' is known, the device implements the reversed implication (RIMP) operation for $Z' =$ '1' or the inverse implication (NIMP) operation for $Z' =$ '0' (cf. logic truth table in Figure 7.7a and signal sequence table for logic functions in Figure 7.8).[9] As a direct consequence, the resulting state Z is described by the equation

$$Z = (T_1 \text{ RIMP } T_2) \cdot Z' + (T_1 \text{ NIMP } T_2) \cdot \overline{Z'} \tag{7.2}$$

which has been introduced by Linn *et al.*[9] " $\cdot$ " denotes a conjunction of two variables, whereas "+" represents a disjunction. T_1 and T_2 are the respective voltage signals applied to terminals T1 and T2. The bar indicates a negation. All logic functions can be derived from Equation 7.2 and implemented by CRS (cf. [9]). Therefore, a defined sequence of voltage signals need to be applied for each function. In every step, one signal is applied to each terminal, T1 and T2. Furthermore, Equation 7.2 requires that the previous CRS state Z' is known, since the actual logic function depends on Z'. Hence, the first step of all logic functions is an initialization. Some logic functions require an initialization by the TRUE operation (setting Z' to '1'), whereas other functions need the FALSE operation (setting Z' to '0'; cf. Figure 7.8). This step is followed by zero, one or two logic steps, as a function of the inputs p and q. The count of actual required steps depends on the individual logic operation. After these steps, the result is inherently stored in the memory cell, where the logic operation has been conducted, what gives the naming 'logic-in-memory' to the concept.
In Figure 7.7a and 7.8, the truth table and sequence schemata for 14 two-input logic Boolean functions are depicted. The applied signals to terminals T1 and T2 define the state of the device. The stored result of the individual logic operation can be readout anytime by performing a reading step. Here, a kind of $V/2$ scheme (cf. [9, 134, 135]) is applied for the logic implementation. Assuming the CRS operation voltage is V ($V > V_{\text{th},2}$ and $V > V_{\text{th},4}$), the

high potential is represented by the logical ‘1’ and means applying $+V/2$, whereas the low potential is identified by ‘0’ and means applying $-V/2$. In total the full operation voltage V drops across the device. For the readout, ‘1’ ($+V/2$) is applied to terminal T1 and ‘0’ ($-V/2$) to T2 (see Figure 7.7b). Take into consideration that this step is not required for the CRS-logic, but for the readout of memory. Depending on the stored CRS state Z, two different responses can be observed in the transient current behavior:

Z = ‘1’: The reading step does not change the device state (cf. Figure 2.5). Only a leakage current is detected.

Z = ‘0’: The reading step changes the device state (cf. Figure 2.5). A current spike (caused by the state flip) is detected and superposes a leakage current (cf. Figure 7.7b, undermost draft).

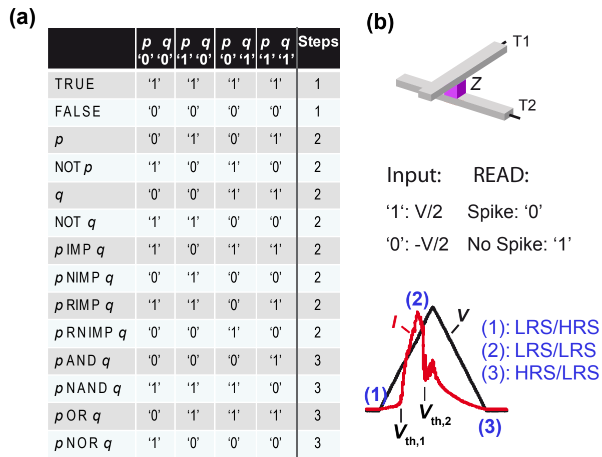
More precisely: the detection of a current spike is interpreted as reading of ‘0’, whereas the absence of a current spike is taken as reading of ‘1’ (cf. Figure 7.7b). Consider, the readout schema is destructive, since the CRS cell always ends up in state ‘1’ (HRS/LRS). However, a non-destructive readout is preferred regarding an improved endurance. Some interesting concepts for a non-destructive reading have been demonstrated.[136–138]

7.2.2 Proof-of-Concept

7.2.2.1 HfO_2-based CS

The quasi-static operation on the HfO_2-based CS is already demonstrated in Chapter 5. However, with respect to applications, voltage pulse driven experiments are more relevant than quasi-static measurements, since pulse conditions are closer to real input signals in integrated circuitries.[2] By sensing the electrical current as functions of the applied voltage stimuli and time, the actual device resistance state is determined and also switching kinetics / events are observed. For this reason, the current spike response concept is discussed and investigated.

All demonstrated electrometric experiments have been conducted by the Keithley 4200-SCS. For experiments under pulse conditions, voltage pulses offering a well-defined amplitude ($\pm V/2$) and a width of 500 ns are applied to the device



(a)

	p *q* '0' '0'	*p* *q* '1' '0'	*p* *q* '0' '1'	*p* *q* '1' '1'	Steps
TRUE	'1'	'1'	'1'	'1'	1
FALSE	'0'	'0'	'0'	'0'	1
p	'0'	'1'	'0'	'1'	2
NOT *p*	'1'	'0'	'1'	'0'	2
q	'0'	'0'	'1'	'1'	2
NOT *q*	'1'	'1'	'0'	'0'	2
p IMP *q*	'1'	'0'	'1'	'1'	2
p NIMP *q*	'0'	'1'	'0'	'0'	2
p RIMP *q*	'1'	'1'	'0'	'1'	2
p RNIMP *q*	'0'	'0'	'1'	'0'	2
p AND *q*	'0'	'0'	'0'	'1'	3
p NAND *q*	'1'	'1'	'1'	'0'	3
p OR *q*	'0'	'1'	'1'	'1'	3
p NOR *q*	'1'	'0'	'0'	'0'	3

Figure 7.7: Logic-in-Memory functionality. The concept has been introduced by Linn *et al.* in [9]. (a) Logic truth table with all input conditions of the variables p and q, the individual logic results and the number of required operation steps for implementation. (b) Input and spike read scheme with exemplary current spike response (for quasi-static voltage sweep).[4] (Reprinted with permission from the publisher.)

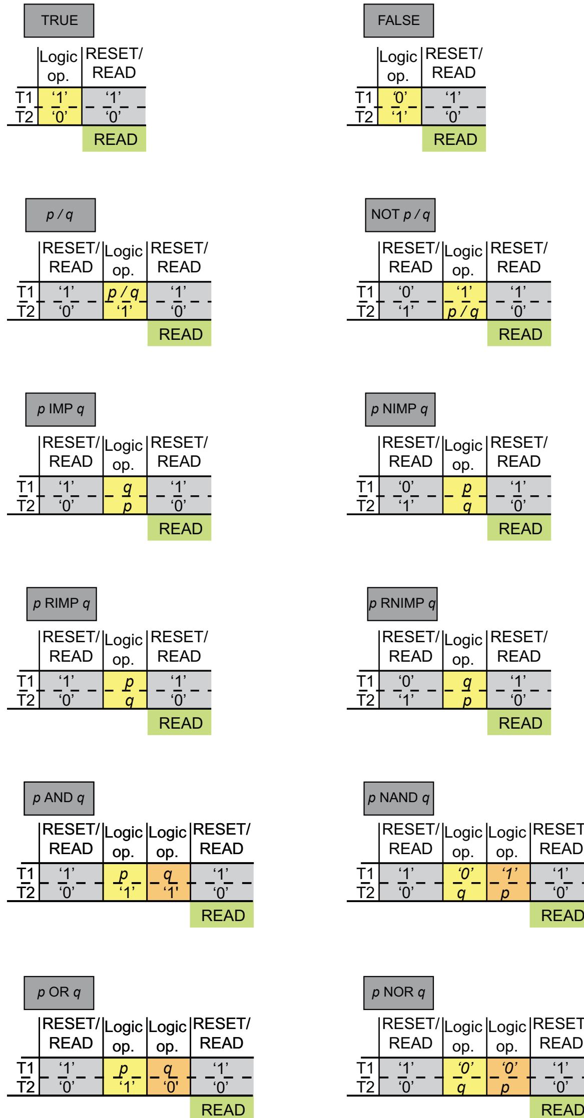


Figure 7.8: Logic table for 14 out of 16 two-input Boolean logic functions, implemented by one to three cycles. The signal sequence is applied to the device terminals T1 and T2. The concept has been introduced by Linn *et al.* in [9]. Consider, the READ step is only required to read the result, but it is not included in any logic function.

terminals T1 and T2, simultaneously, with write voltage V, which should be equal to / larger than the threshold voltages $V_{\mathrm{th},2}$ and $V_{\mathrm{th},4}$ (cf. Figure 2.4).[2] The input signals $T1$ and $T2$ are applied to the corresponding terminals T1 and T2. The responding transient current is detected as function of time.
Figure 7.9 gives an overview of all possible voltage / state configurations of the device and the distinguishable current responses (depending on the previous state Z').[2] Z' is the current state of the cell before applying the voltage pulses.
First, the cell is in the state Z' = '0'. If $+V$ drops across the device ($T1 = +V/2$, $T2 = -V/2$) the switching from state '0' to '1' will be expected (1st cycle).[2] For the transient current, a positive spike is observed, which indicates the switching from '0' to '1'.
Applying the same signals does not change the state of the cell anymore (2nd cycle).[2] Therefore, no current spike is visible, only the area-type leakage current of the highly resistive state. Thus, both states Z' = '0' and Z' = '1' can be distinguished by applying a positive write voltage and so enabling a destructive readout procedure called "Spike Read".
However, if in total $-V$ ($T1 = -V/2$, $T2 = +V/2$) drops across the device being in state Z' = '1', the device state will change from '1' to '0' (3rd cycle).[2] As a consequence, a negative current spike is measured. In the 4th cycle, the CS state does not change and no current spike event is detected, since the voltage configuration has not been changed. Whenever the same / symmetric potentials are forced to T1 and T2 at once, no voltage drops over the device and only (dis-)charging current is sensed (see 5th and 6th cycle). Thus, the measured transient currents of the last two cycles do not depend on Z' and confirm the expected CS characteristic.

Figure 7.10 to 7.21 demonstrate the experimental implementation of the 14 two-input Boolean logic functions listed in Figure 7.7a.[2] The realization has been performed on HfO_2-based CS devices under quasi-static and pulsed conditions using a single CS. Here, the CS operation voltage is about 2 V for quasi-static / pulse measurements and the efficient pulse width is 500 ns. Nevertheless, quasi-static operation is already achievable by $V = 1.5$ V as shown in Figure 5.2.

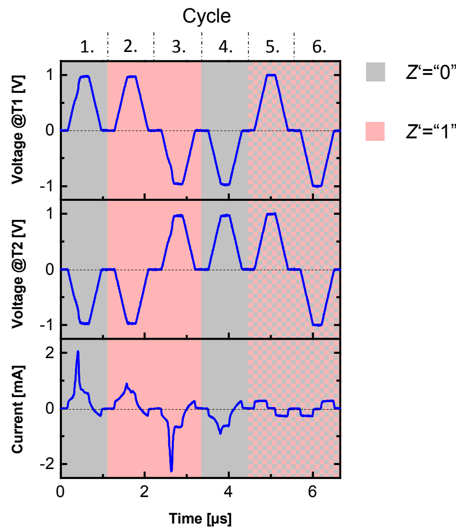


Figure 7.9: Feasible pulsed voltage / state configurations of the CS device with related transient current response. The difference of potentials applied to the terminals T1 and T2 determines the overall voltage drop ($V_{\mathrm{tot}} = V_{\mathrm{T1}} - V_{\mathrm{T2}}$). Z' is the CS state before applying signals to T1 and T2, with Z' = '0' (gray) or Z' = '1' (rose). If the signals are equal, only (dis-)charging current is observed (independent of Z'). For all configurations, the transient current responses are unique. Consider, the switching current depends on the electroforming procedure and the applied pulse parameters. For example, steep rising and falling ramps of voltage pulses result in larger current levels (in comparison to quasi-static experiments), since the CS is not able to respond quasi-statically to the voltage drop. Rather, it shows an instantaneous switching via the 'ON' transition state, causing the typical current spike.[2] (Reprinted with permission from the publisher.)

The actual minimal operation voltage amplitude for the pulse mode depends on pulse parameters, especially on the pulse width.[2] This relation is attributed to the non-linear switching kinetics in ReRAM devices.[128, 129, 139, 140] To exemplify the CRS-logic on CS devices, the realizations of the NIMP and RIMP functions are explained. The experimental results for both logic functions are presented in Figure 7.15 for the NIMP and Figure 7.16 for the RIMP function. Both operations are verified by the READ results for all different combinations of the two input signals p and q. To quantify the individual steps clearly, all different step types are highlighted by individual colors: initialization (rose), logic step (green), reading (yellow).
Overall, two steps are required for each case, the RIMP (or NIMP) function: initialization and one logic step, where the inputs are applied. Consider, in the case of the RIMP operation, initialization and reading are equivalent. Therefore, this step is performed only once. For the logic RIMP operation, only for the input signal configuration with $p =$ ‘0’ and $q =$ ‘1’, the output is equal to ‘0’, whereas for the logic NIMP operation, the output is ‘0’ excluding the configuration with $p =$ ‘1’ and $q =$ ‘0’ (cf. Figure 7.7).
In order to conduct the RIMP operation, the device needs to be initialized to the state ‘1’ in advance. This is achieved by T1 to ‘1’ and T2 to ‘0’ (cf. Figure 7.8). However, for implementation of the NIMP operation, the device requires an initialization procedure to the state ‘0’ by forcing ‘0’ to T1 and ‘1’ to T2. The second step is identical for the NIMP and RIMP operation. p is forced to T1 and q to T2. For both logic operation implementations, all response currents, i.e. the cell area depending on leakage current and the current spike, show expected characteristics.
The implementation of the remaining 12 logic functions is similar to the RIMP and NIMP operation. The way, how the experimental data are presented, is identical.

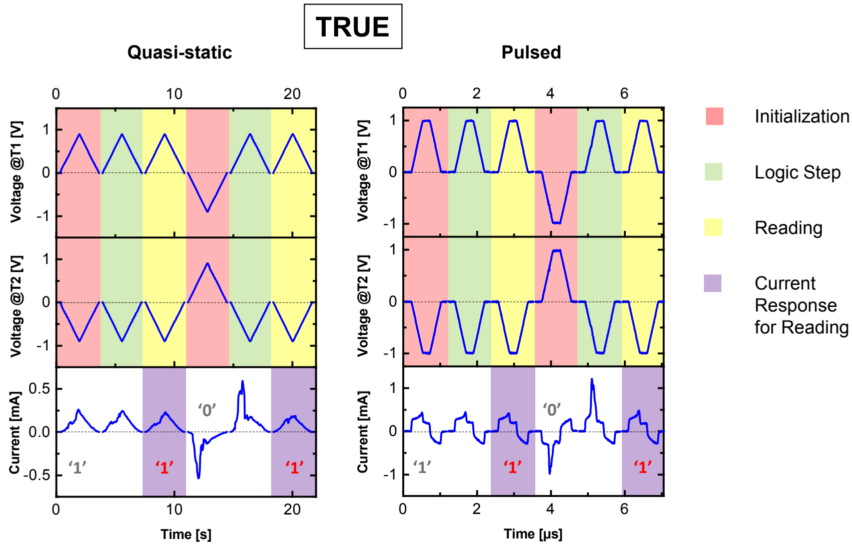


Figure 7.10: The CRS-logic TRUE function performed by one step under quasi-static and pulse conditions. READ results are highlighted by red labeling. Note that the initialization step is redundant and not essential for common implementation. However, it is proven the TRUE function works for both initial states, $Z' =$ '1' and $Z' =$ '0'. In general, the single logic step fulfills the TRUE function (cf. Figure 7.8).[2] (Reprinted with permission from the publisher.)

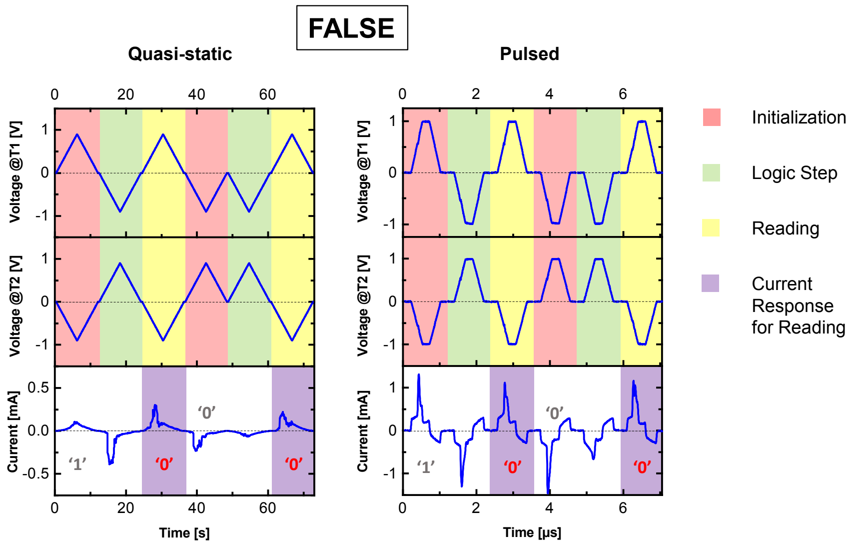


Figure 7.11: The logic FALSE function performed by one step under quasi-static and pulse conditions. READ results are highlighted by the red labeling. Note that the initialization step is redundant and not essential for common implementation. However, it is proven the FALSE function works for both initial states, Z' = '1' and Z' = '0'. In general, the single logic step fulfills the TRUE function (cf. Figure 7.8).[2] (Reprinted with permission from the publisher.)

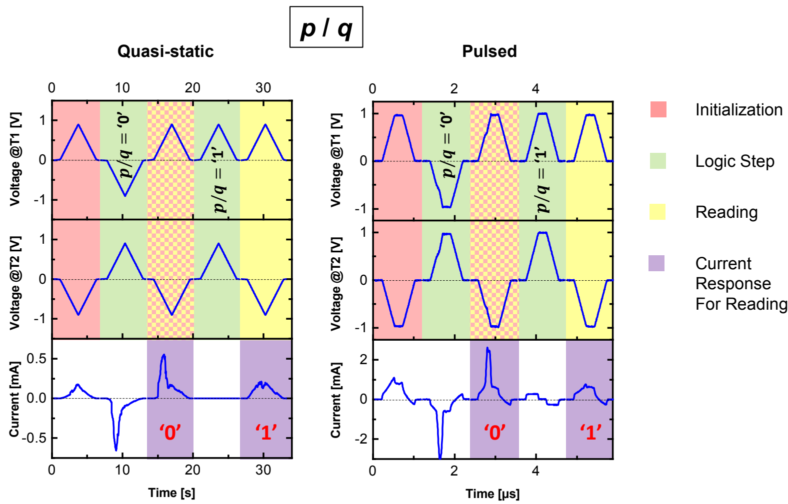


Figure 7.12: The CRS-logic p / q function performed by two steps under quasi-static and pulse conditions. It should be noted this logic operation depends only on one input variable (either p or q) and overall only two input configurations are available.[2] (Reprinted with permission from the publisher.)

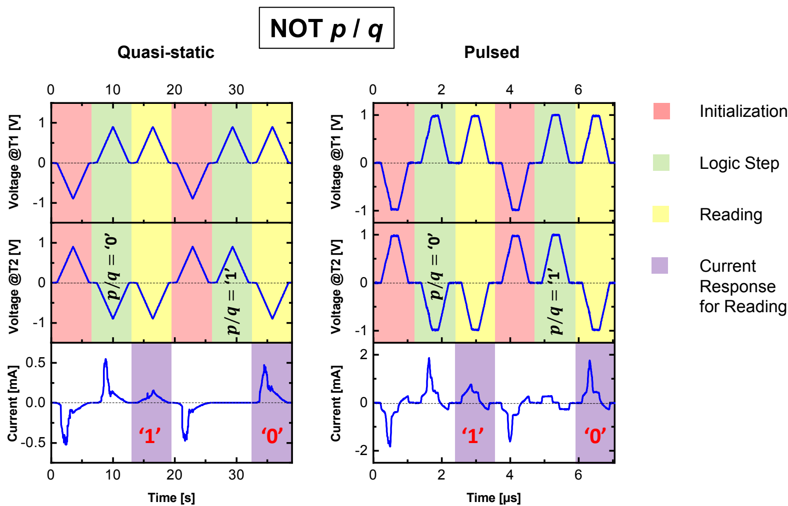


Figure 7.13: The CRS-logic NOT p / q function performed by two steps under quasi-static and pulse conditions. It should be noted this logic operation depends only on one input variable (either p or q) and overall only two input configurations are available.[2] (Reprinted with permission from the publisher.)

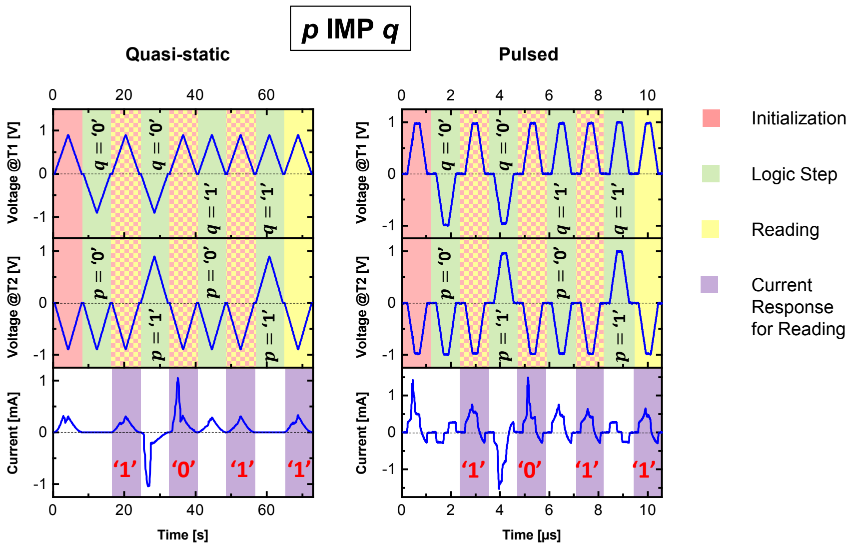


Figure 7.14: The CRS-logic IMP function is performed by two steps under quasi-static and pulse conditions.[2] (Reprinted with permission from the publisher.)

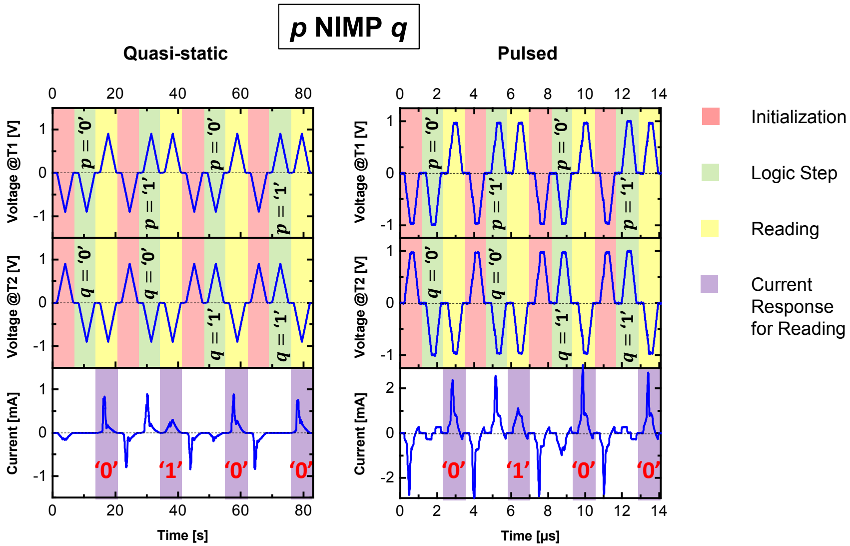


Figure 7.15: The CRS-logic NIMP function is performed by two steps under quasi-static and pulse conditions.[2] (Reprinted with permission from the publisher.)

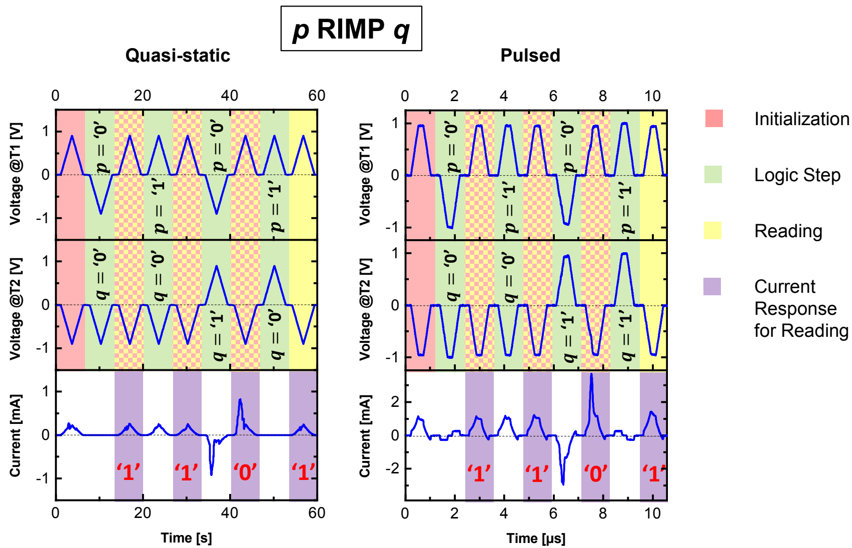


Figure 7.16: The CRS-logic RIMP function is performed by two steps under quasi-static and pulse conditions.[2] (Reprinted with permission from the publisher.)

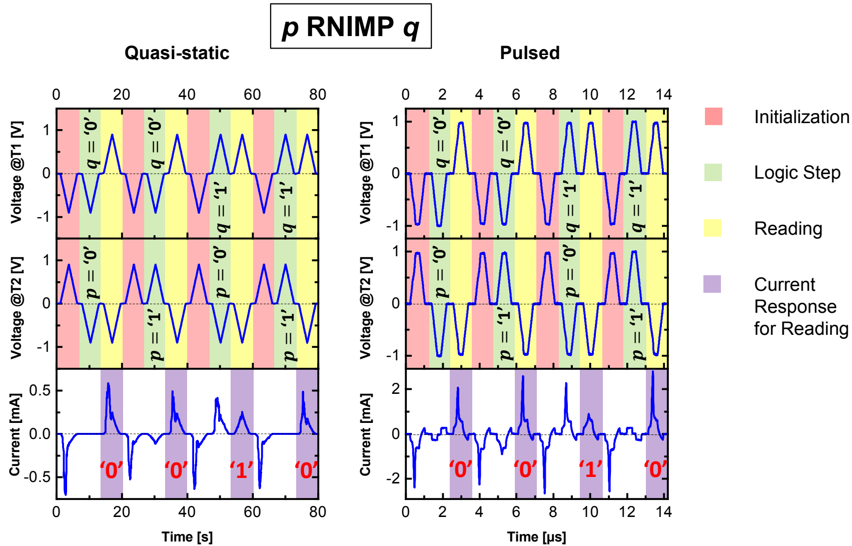


Figure 7.17: The CRS-logic RNIMP function is performed by two steps under quasi-static and pulse conditions.[2] (Reprinted with permission from the publisher.)

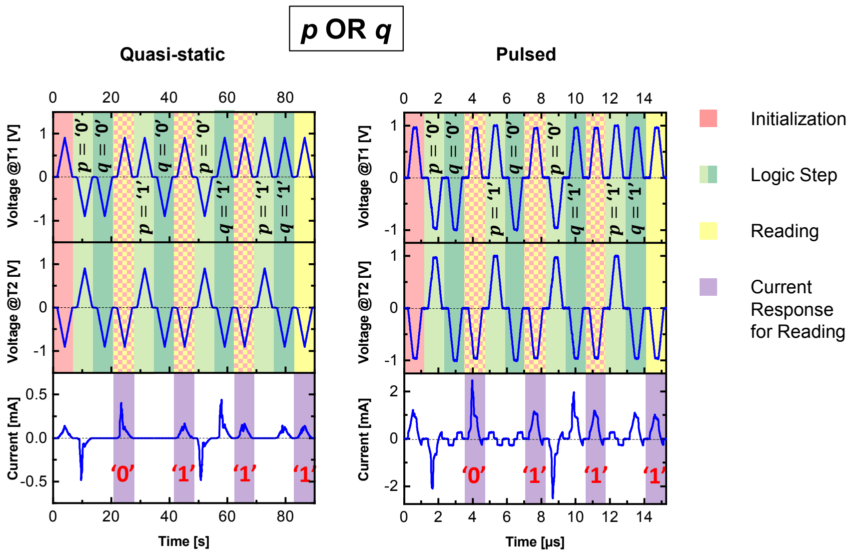


Figure 7.18: The CRS-logic OR function is performed by three steps under quasi-static and pulse conditions.[2] (Reprinted with permission from the publisher.)

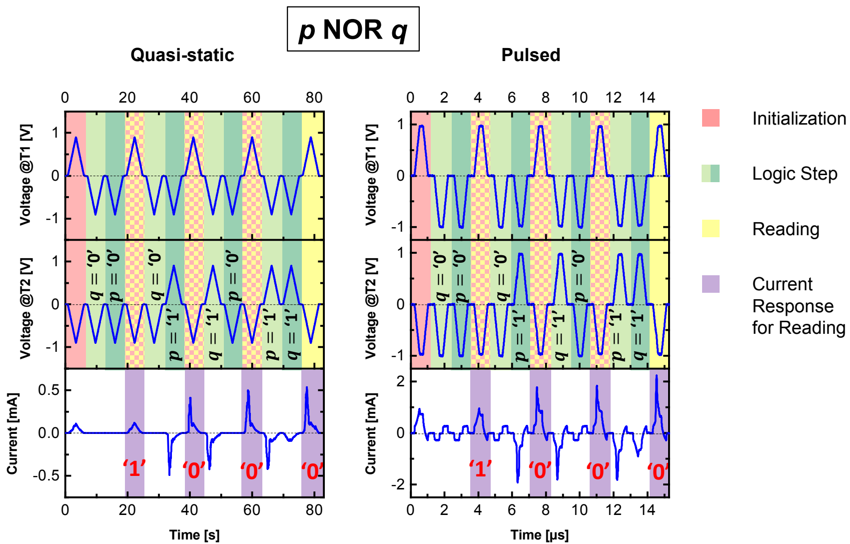


Figure 7.19: The CRS-logic NOR function is performed by three steps under quasi-static and pulse conditions.[2] (Reprinted with permission from the publisher.)

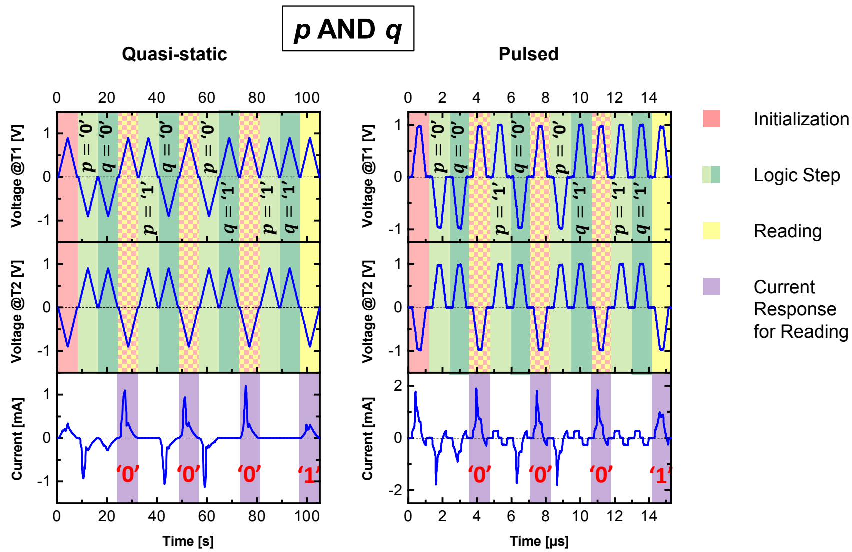


Figure 7.20: The CRS-logic AND function is performed by three steps under quasi-static and pulse conditions.[2] (Reprinted with permission from the publisher.)

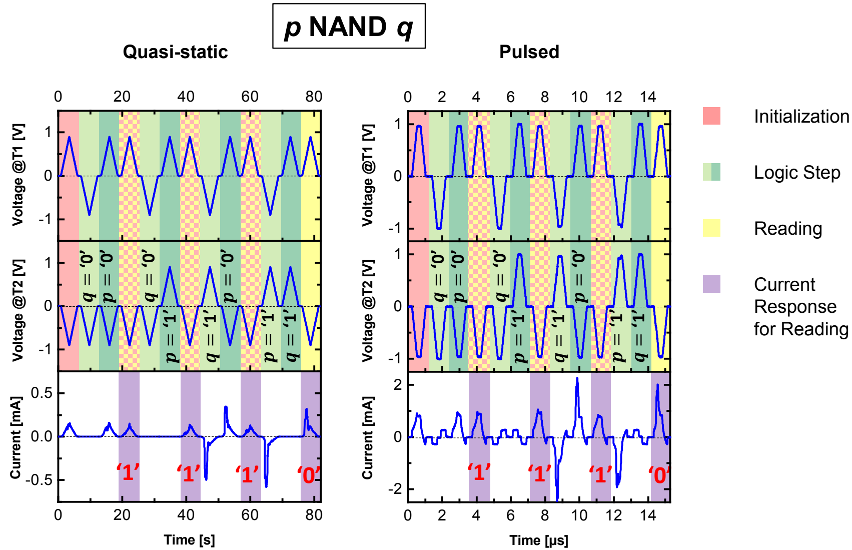


Figure 7.21: The CRS-logic NAND function has been performed by three steps under quasi-static and pulse conditions.[2] (Reprinted with permission from the publisher.)

7.2.2.2 Ta_2O_5-based CRS

The CRS-logic has also been implemented successfully on the two-terminal Ta_2O_5-based CRS devices.[4, 5] The way the concept is realized, including the used measurement equipment, is identical to the HfO_2-based CS devices. Therefore, just two functions are depicted here.
Figure 7.22 (left) shows the three-step AND function in the quasi-static operation mode on the nano-BC-CRS. On the right hand side, the AND operation in pulse mode on the micro-BC-CRS device is demonstrated. The applied pulses are 500 ns wide. Due to the separate forming procedure (see Subsection 6.1.2) the nano-BC structure supports the low-current operation in the microampere range. The two-terminal micro-BC CRS has not been formed separately by adding a serial resistor (cf. Subsection 6.1.2) and offers operation currents in the milliampere range. Figure 7.23 (left) depicts the low-current IMP operation for nano-BC structured CRS with 5 μs pulses.

For verification, a dynamical Ta_2O_5-based circuit model is applied, which has been suggested by Siemon *et al.* in [141]. The schema is shown in Figure 7.24a. One bipolar switching cell consists of an active oxide (Ta_2O_5) sandwiched between two different electrode materials (Pt and Ta). It is assumed that the oxide offers an ionic and electronic current branch at the disc region, in addition a leakage current over the whole cell area is considered. Moreover, a Schottky diode at the Pt interface and a plug resistance are implicit. The interface at $Ta|Ta_2O_5$ is assumed as ohmic, since the Schottky barrier height is negligible due to partial oxygen interdiffusion between the oxide layer and the Ta electrode.
In order to simulate the *I*-*V* characteristic of the CRS (see Figure 7.24b), two of those model constructs have to be connected anti-serially. The present simulations have been performed by A. Siemon. Figure 7.23 shows the comparison between a pulse driven measurement (left) and a simulation (right) of the IMP operation for the nano-BC CRS. The suggested model seems to be auspicious, since the measurement results are well reflected.[4]

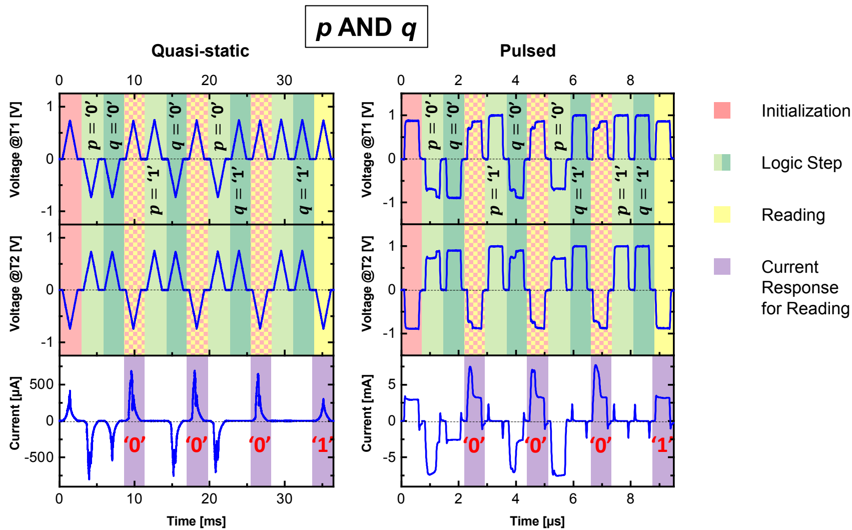


Figure 7.22: Measurement of the logic AND operation by two steps for (left) the nano-BC CRS under quasi-static conditions and (right) for the micro-BC CRS under pulse conditions.[4] (Redrawn with permission from the publisher.)

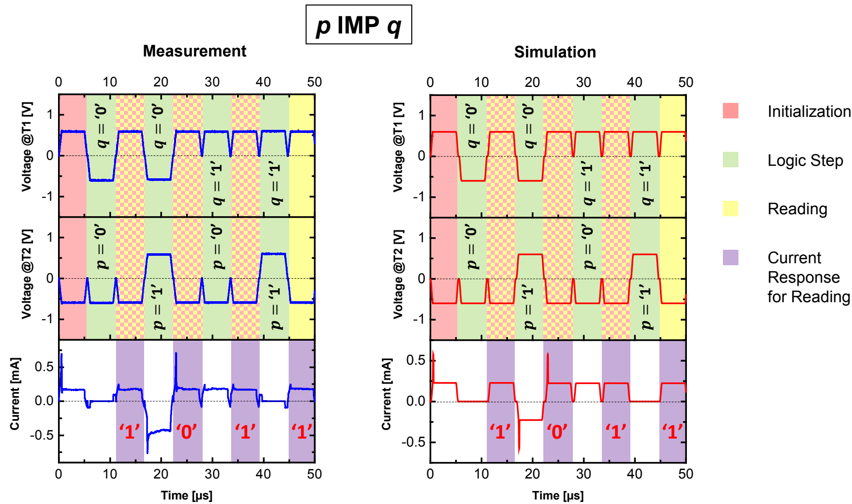


Figure 7.23: Measurement (left) and simulation (right) of the logic IMP function by two steps for the nano-BC CRS under pulse conditions. Simulations have been performed by A. Siemon.[4] (Redrawn with permission from the publisher.)

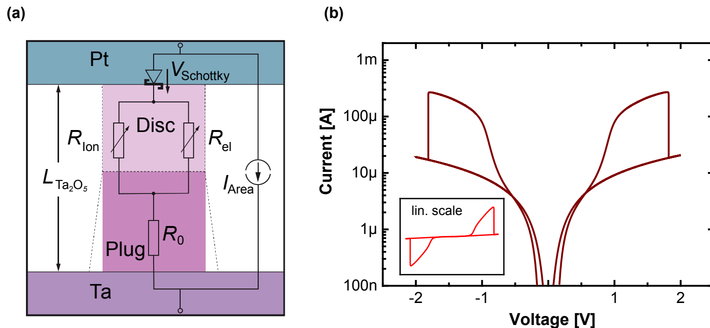


Figure 7.24: Dynamical simulation model for Ta_2O_5-based CRS device suggested by Siemon *et al.* in [141]. (a) Assumed equivalent circuit for a single ReRAM cell. To simulate *I*-*V* sweeps of the CRS device as shown in (b), two equivalent circuits have to be combined anti-serially. The simulation has been performed by A. Siemon.[4] (Reprinted with permission from the publisher, © 2014 IEEE.)

7.2.3 Discussion

In this section, proof-of-concept measurements for the CRS-logic, a novel logic-in-memory concept suggested in [9], have been performed.[2, 4, 5] 14 Boolean two-input logic operations have been realized under quasi-static and pulse conditions. The CRS-logic is based on the intrinsic behavior of the ReRAM, whose final state is clearly described by logic terms (see Equation 7.2).

Each logic function requires a defined sequence of applied voltage signals. The number of steps depends on the individual function, but the maximal number is limited by three. The implementation is successfully proven on single HfO_2-based micrometer scaled CS[2] and single Ta_2O_5-based nano- / micrometer scaled CRS[4, 5] devices. Both types support the capability for low-power operation, since they offer a sub-mA operation current.

During pulsed measurements some parasitic (dis-)charging current is observed.[2] To avoid these undesired effects, normally the voltage would only be applied to one electrode and the current would be measured by the PMU at the second electrode which is connected to ground. However, this is not possible here due to the applied voltage scheme, where the operation voltage is split to BE and TE. It is observed that the (dis-)charging current is affected by some pulse parameters, especially the pulse rising and falling time. The

shorter these timings are the larger the parasitic effects. The challenge is to realize short pulses, while keeping the (dis-)charging current below a compatible level to identify clearly the current spike response.
Using a dynamical circuit model the bipolar and complementary resistive switching properties of the Ta_2O_5-based cells are described very well.[141] Even the experimentally measured data for logic operations are fitted consistently.[4]

7.3 Computation-in-Memory

7.3.1 Basics

Figure 7.25 illustrates a schematic sketch of the passive crossbar array.[2] Each crosspoint of a bitline (BL) and a wordline (WL) represents one individual memory device. Here, CS devices are integrated as memories, since they offer an inherent selector characteristic. The CRS could also be a possibility, however, the CS requires a simpler fabrication procedure. This array structure is used in the following, such that T1 terminals are connected to each other by WLs and the T2 terminals to BLs. For instance: the term A0-WL1-BL2 is referred to the CS cell which is located at the crosspoint of WL1 and BL2 in array A0.

The present adder concept has been introduced by Siemon *et al.* in [10]. The adder enables addition or subtraction operations of two binary input words, referred to as a and b.[2, 10] The input words consist of input word bits a_i and b_i with significance i. Unlike basic two-input CRS-logic, a full adder needs three inputs: word bits a_i, b_i and carry bit c_i.
In [10] a simple method has been used for the carry computation to calculate intermediate results, which are merged afterwards in a final operation. Three inputs, the bits a_i and b_i and the previous carry c_i, determines the next higher significant carry c_{i+1}. This relation is given by the expression

$$c_{i+1} = (a_i + b_i) \cdot c_i + (a_i \cdot b_i) \cdot \overline{c_i}, \tag{7.3}$$

where "+" denotes a disjunction of two variables and " · " a conjunction. Negation of a bit is indicated by the bar symbol on top. For two configurations,

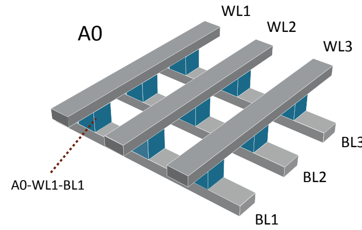


Figure 7.25: Illustration of the crossbar array (A0). Each cross-junction of wordline (WL) and bitline (BL) is comprised of an individually addressable CS cell. The different WLs and BLs are consecutively numbered. For instance, the cell in the array A0 at the crosspoint of WL1 and BL1 is referred to as A0-WL1-BL1.[2] (Reprinted with permission from the publisher.)

the next significant carry c_{i+1} is '1': (i) The previous carry c_i = '1' and a_i or / and b_i is / are also '1'. (ii) Whenever c_i = '0', $a_i = b_i = 1$ has to be fulfilled. However, the approach of straightforward implementation of these interlaced logic operations (described by Equation 7.3) is inefficient by means of CRS-logic, since an extensive number of steps are required for only one carry bit calculation (cf. Figure 7.8): "$(a_i + b_i) \cdot c_i$" requires 3 steps for the disjunction and 3 additional steps for the conjunction. "$(a_i \cdot b_i) \cdot \overline{c_i}$" requires also 6 steps, i.e. 3 steps per disjunction. Afterwards, a last disjunction of both partial expressions is conducted (3 steps). In total, this unsophisticated approach would require 15 steps to compute a single carry bit.
However, Siemon *et al.* have shown that the partial expression "$(a_i + b_i) \cdot c_i$" is equivalent to "$\left(a_i \text{ RIMP } \overline{b_i}\right) \cdot c_i$" and "$(a_i \cdot b_i) \cdot \overline{c_i}$" to "$\left(a_i \text{ NIMP } \overline{b_i}\right) \cdot \overline{c_i}$".[10] As consequence, the carry equation c_{i+1} (Equation 7.3) can be modified to

$$c_{i+1} = \left(a_i \text{ RIMP } \overline{b_i}\right) \cdot c_i + \left(a_i \text{ NIMP } \overline{b_i}\right) \cdot \overline{c_i} \tag{7.4}$$

Equation 7.4 shows the general form of the CRS-logic function, which has been introduced by Linn *et al.* That means the computation of c_{i+1} is significantly simplified by considering the initial device state Z' (here: c_i) as additional (third) input.[2,10] The operation is realized by only one step by means of the CRS-logic: a_i is the input signal forced to the WL, $\overline{b_i}$ is the input at the BL, c_i is the previous device state before the signals are applied and c_{i+1} is the resulting device state.[9] That means the computation of the next significant

Carry	Cycle	Z'	WL	BL	Z
	1.	c_i	a_i	$\overline{b_i}$	c_{i+1}

Sum	Cycle	Z'	WL	BL	Z
	1.	c_i	a_i	b_i	s'_i
	2.	s'_i	b_i	c_{i+1}	s_i

c_i	a_i	$\overline{b_i}$	c_{i+1}	read
'0'	'0'	'0'	Z = '0'	'0'
'0'	'0'	'1'	Z = '0'	'0'
'0'	'1'	'0'	Z = '1'	'1'
'0'	'1'	'1'	Z = '0'	'0'
'1'	'0'	'0'	Z = '1'	'1'
'1'	'0'	'1'	Z = '0'	'0'
'1'	'1'	'0'	Z = '1'	'1'
'1'	'1'	'1'	Z = '1'	'1'

c_i	a_i	b_i	c_{i+1}	s'_i	s_i	read
'0'	'0'	'0'	'0'	Z = '0'	Z = '0'	'0'
'0'	'0'	'1'	'0'	Z = '0'	Z = '1'	'1'
'0'	'1'	'0'	'0'	Z = '1'	Z = '1'	'1'
'0'	'1'	'1'	'1'	Z = '0'	Z = '0'	'0'
'1'	'0'	'0'	'0'	Z = '1'	Z = '1'	'1'
'1'	'0'	'1'	'1'	Z = '0'	Z = '0'	'0'
'1'	'1'	'0'	'1'	Z = '1'	Z = '0'	'0'
'1'	'1'	'1'	'1'	Z = '1'	Z = '1'	'1'

Z = '0' (LRS/HRS)   Z = '1' (HRS/LRS)

Figure 7.26: Adder truth table for carry and sum bit computation. The concept has been introduced by Siemon *et al.* in [10]. All carry and sum bits are determined by Equation 7.4 to 7.6. The calculation of the carry bit c_{i+1} (of significance $i+1$) is performed by one step. c_i is required as former state (Z'), a_i is applied to the WL, whereas the negated b_i to the BL. The sum bit s_i is computed by two steps. First, the intermediate sum bit s'_i is determined. For this purpose, c_i is used as previous state Z' and a_i is applied to the WL, whereas b_i to the BL. Finally, the previous result $Z = s'_i$ is used as new former state Z' and b_i is applied to the WL and c_{i+1} to the BL, in order to compute the sum bit.[2] (Reprinted with permission from the publisher.)

carry bit is an inherent feature of all bipolar switching ReRAMs.
For computation of the sum bit s_i, similar considerations can be performed, but two process steps are required.[2, 10] First, the intermediate sum bit s'_i is computed by

$$s'_i = (a_i \text{ RIMP } b_i) \cdot c_i + (a_i \text{ NIMP } b_i) \cdot \overline{c_i}. \tag{7.5}$$

In the second step, the sum bit is finally calculated by the expression

$$s_i = (b_i \text{ RIMP } c_{i+1}) \cdot s'_i + (b_i \text{ NIMP } c_{i+1}) \cdot \overline{s'_i} \tag{7.6}$$

The concept scheme of the carry and sum bit computation is depicted in Figure 7.26 by means of corresponding truth tables.[2]
The realization of the carry c_{i+1} by the CS device is shown in Figure 7.27 as

proof for the experimental feasibility.[2] The several operation steps are represented by individual background colors: (light green) programming of c_i, (dark green) calculation of c_{i+1} and (yellow) reading. All relevant reading currents are indicated by a purple background color. Consider, the configurations with c_i = '1' corresponds to the CRS-logic RIMP operation (see Equation 7.4 and Figure 7.16), where the device is programmed to '1' at the beginning. Hence, further initialization steps are not needed here. Comparably, the configurations with c_i = '0' represent the CRS-logic NIMP function (see Equation 7.4 and Figure 7.15), where the device state is initialized to '0'. Therefore, the initial device state Z' acts as third input. Further, this result confirms that the RIMP and NIMP functions are subsets of the CRS-logic concept.
For the computation of the next significant carry c_{i+1}, the input carry c_i does not need to be written into the cell by an additional process step, since the value is already available as result of the former calculation step.[2] Therefore, considering the non-volatile ReRAM state as third input is a major benefit of the present computation-in-memory concept.

Two's Compliment Inclusion of negative numbers (in the binary system) in arithmetic operations is achieved by applying the complementary notation.[2] One approach is given by means of the one's compliment. To generate a negative number for the binary system, the bits of the corresponding positive binary notation are negated. Certainly, a doubled notation for the zero (± 0) is the direct consequence of the one's compliment notation. This can be avoided by applying the two's complement: first, similar to the one's compliment, a bitwise negation is performed, subsequently, 1 is added the number. However, this implicates that the positive number range is one value shorter than the negative one.
The presented multibit adders enable processing of subtraction and addition operations by means of the two's complement.[2,10] For the addition operation $a + b$, the computation of all required carries and (intermediate) sum bits is straightforward by using Equation 7.4 to 7.6, starting with the first carry bit $c_0 = 0$. Similarly, the subtraction $a - b'$ (with minuend a and subtrahend b')

can be interpreted as addition of a with the additive inverse of b':

$$a - b' = a + (-1) \cdot b' = a + (-b') \tag{7.7}$$

The additive inverse of b' is implemented by generating the two's compliment as described above. This generation requires the addition of 1 in the second step. However here, 1 is not added to $\overline{b'}$ but to c_0. That means $a - b'$ is realized by the addition of a and $\overline{b'}(= b)$ with modified $c_0 = 1$.

Adder Schemes Two adder schemes are considered, which are predicted based on the explanations above: the Pre-Calculation (PC) Adder and the Toggle-Cell (TC) Adder.[2, 10] The first scheme is based upon two different arrays, one for auxiliary calculations and a second to compute the sum word. Furthermore,
$2(N + 1) + 2$ operation steps are required for the PC Adder concept, with the bit length N of a and b. This includes $N + 1$ memory read accesses, which are required, since the computed carries c_{i+1} are subsequently used (i.e. applied to corresponding BLs) to generate the sum bits s_i (cf. Equation 7.6).
Different to the first concept, the TC Adder operates in one array, where the Toggle-Cell performs all carry bit calculations.[2, 10] In addition, this is the only cell, which is readout for the computation process (excluding the read of the final sum word). For the TC Adder, less device resources are needed, but requires more processing steps $(4N + 5)$. The number of memory read accesses is for both adder concepts identical $(N + 1)$.[10]. Considering, the present work is focused on the experimental proofs by means of exemplary arithmetic operations. For further specifications of the adder concepts, general cycle flows and a suggested concept of hybrid CMOS/ReRAM architecture, the reader is referred to [10, 15]. For proving the two adder schemes, two calculation examples are performed by using the two's complement, these are one addition (on the PC Adder) and one subtraction operation (on the TC Adder).

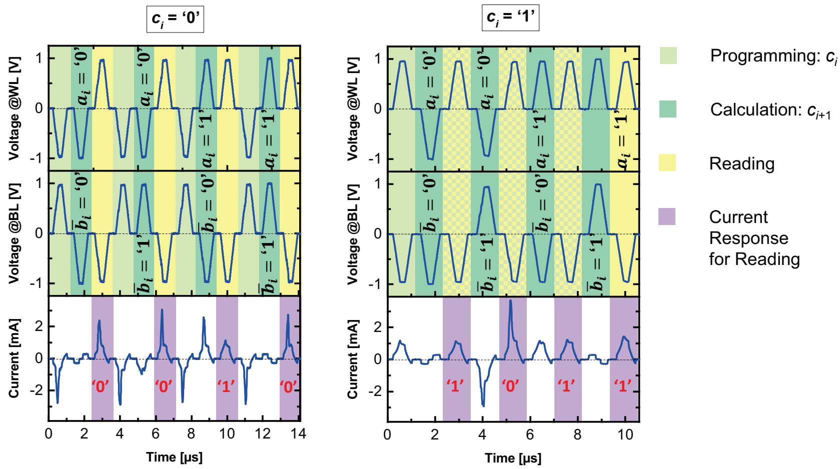


Figure 7.27: Implementation of the carry as defined by Equation 7.4. c_{i+1} depends on the inputs (a_i and $\overline{b_i}$) and the previous carry (c_i): c_i = '0' (left) or c_i = '1' (right). Background colors of the graph highlight the different operations. Reading results are displayed by red lettering.[2] (Reprinted with permission from the publisher.)

7.3.2 Proof-of-Concept

7.3.2.1 Pre-Calculation Adder

Here, the addition $a + b$ with the two operands $a = (01)_{\mathrm{C2}} = (1)_{\mathrm{dec}}$ and $b = (01)_{\mathrm{C2}} = (1)_{\mathrm{dec}}$ (C2: two's complement, dec: decimal system) is presented.[2] $s = (010)_{\mathrm{C2}} = (2)_{\mathrm{dec}}$ is the expected result.

The Pre-Calculation Adder computes required auxiliary carries and the sum separately in two different arrays.[2, 10] The here demonstrated example requires two arrays, which offer in each case one WL and three BLs. The bitlines are named BL1, BL2 and BL3 from right to left (cf. sketch of the used array in Figure 7.28) and the single wordline is labeled by WL. Note, on both arrays the processes would be generally conducted in parallel. However, due to an insufficient number of available probes, auxiliary and main computation operations are performed subsequently on a single array. Nonetheless, processing on both arrays is presented as parallel implementation due to straightforwardness. For the adder concept, this way of presentation does not cause any loss of generality.

Figure 7.28 depicts the eight required steps of the demonstrated addition experiment.[2] The several operations are indicated by individual background colors: (rose) initialization, (light green) programming of c_0, (dark green) calculation, (yellow) read. The graphs includes the applied inputs to the particular WLs and BLs (black lettering) and the present stored information in the individual CS device (gray lettering). The light brown background color in the transient current graph highlights the steps, where the actual cell information is purposely kept unchanged.

1st step – Initialization: At the beginning, all CS devices are initialized to avoid undefined states. This is similar to the Boolean CRS-logic operations (see Section 7.2) By forcing the WLs to '1' and the BLs to '0', all CS states switches to '1'. This is required for the subsequent programming step (especially in the case subtraction with c_0 = '1').[2]

2nd step – Programming of c_0: Afterwards, c_0 is written into all cells. For this purpose, c_0 is forced to the WLs and '1' to the BLs. In case of the addition, c_0 is equal to '0'.[2]

3rd step – Calculation of c_1 and s'_0: The information c_1 is required to compute higher significant carries and (intermediate) sum bits. Therefore, c_1 is computed in each device of the two arrays, excluding the least significant cell in array A0 (A0-WL-BL1). That means a_0 = '0' is forced to the WLs and $\overline{b_0}$ to the relevant BLs. In A0-WL-BL1, the intermediate sum bit s'_0 is in parallel determined by applying b_0 to corresponding BL1.[2]

4th step – Calculation of c_2 and s'_1: Now, the next carry c_2 is calculated in A0-WL-BL3 and in the two most significant cells of array A1. Thus, a_1 is forced to the associated WLs and $\overline{b_1}$ to the associated BLs. In parallel, the intermediate sum bit s'_1 is determined in A0-WL-BL2. The states of the least significant cells of both arrays is preserved, since this information is used later as a third input. To achieve this, the relevant BLs are set to the same potential as used for the WLs.[2]

5th step – Calculation of c_3 and s'_2: Here, the most significant bits of a and b (a_1, b_1) are doubled (i.e. $a_2 \equiv a_1$, $b_2 \equiv b_1$) and used to compute c_3 and s'_2 (according to Equation 7.4 and 7.4), otherwise the final result could be incorrect / misinterpreted (see remark below). In case of applying the two's compliment, doubling of the highest significant bit does not change value or sign of the operands a and b. The calculating of s'_2 and c_3 is performed in the highest significant cells of both arrays and is similar to the 4th step. a_1 is forced to the WLs and b_1 or $\overline{b_1}$ to the corresponding BLs, respectively. The states of the remaining cells are intentionally kept unchanged in order to save c_1, c_2, s'_0 and s'_1.[2]

6th step – Read of c_1 and Calculation of s_0: Next, the sum bit computation is started. For this purpose, c_1 is read from A1 by setting the related WL to '1' and the relevant BL to '0'. The read information is used to calculate the first sum bit s_0 in A0-WL-B1 by applying b_0 to WL and c_1 to BL1. The readout is conducted. The information of the remaining devices is maintained for the subsequent steps.[2]

7th and 8th step – Read of c_1 and c_2 and Calculation of s_1 and s_2: In the same way, the read of c_2 and c_3 and the computation of s_1 and s_2 are performed (cf. step 6). The operations are simply shifted to the next significance. Finally, the sum word is stored in A0 until the information needs to be read.[2]

To prove the adder functionality, the result is read in the subsequent (but not required) step: $s = (010)_{\mathrm{C2}}$, which is converted to the decimal system $(2)_{\mathrm{dec}}$ as expected.[2]

Remark to step 5 (origin of doubling):
If the sum word was limited to the same bit length as the input words (here: two bits) by ignoring carry c_2, the result would be $s = (10)_{\mathrm{C2}} = (-2)_{\mathrm{dec}}$ and thus incorrect. The correct value +2 is not included in the present codomain, since it cannot be represented by two bits using the two's compliment (at least three bits are required). To avoid an incorrect result, the potential overflow PO needs to be detected considering c_1 XOR c_2. Only if the overflow was '0',

the sum would be valid, but neither is the case here. Another possibility (to obtain the valid result) could be interpreting the carry $c_2 = 0$ as s_3. For the present example, this approach provides the correct result $s = (010)_{\mathrm{C2}}$. Consider, this step is equivalent to filling the input words with a leading zero. However, this operation is not allowed for negative values, since in the two's compliment, the highest significant bit also indicates the algebraic sign. The best approach is doubling the most significant bit of the input words a and b. This step does not change algebraic sign and value of the input words but ensures the correct result.[2] Here, the doubled bits are used to compute s_2 in the ordinary way. Afterwards, the most significant carry c_3 does not need to be considered anymore, since, by doubling the most significant bit, c_2 is equal to c_3. Therefore, the PO is '0' and the result is valid. Doubling the most significant bit is not limited to the present example, it is a rather general approach.

7.3.2.2 Toggle-Cell Adder

Here, the subtraction operation $b - a$ of the two operands $a = (1)_{\mathrm{C2}} = (-1)_{\mathrm{dec}}$ and $b = (0)_{\mathrm{C2}} = (0)_{\mathrm{dec}}$ (C2: two's complement, dec: decimal system) is presented.[2] $s = (01)_{\mathrm{C2}} = (1)_{\mathrm{dec}}$ is the expected result.
The TC Adder operates with one array. In contrast to the PC-Adder, each auxiliary calculations is performed in the least significant cell, the Toggle-Cell (A0-WL-BL1).[2, 10] Certainly, this costs an enhanced number of processing steps. For the demonstrated example, one array is needed, which offers one WL and three BLs. The several devices and contact lines are labeled identically to the previous PC-Adder example.[2] Figure 7.29 shows the nine operation steps. The identical background / lettering color code is applied as for the PC Adder (cf. Figure 7.28).

1st step – Initialization: The WL is set '1' and all BLs to '0' in order to initialize every cell to the defined state '1'.[2]

2nd step – Programming of c_0: c_0 is written into each cell. For this purpose, c_0 is applied to the WL and '1' to the BLs. Here, c_0 is equal to '1', since a subtraction operation is performed.[2]

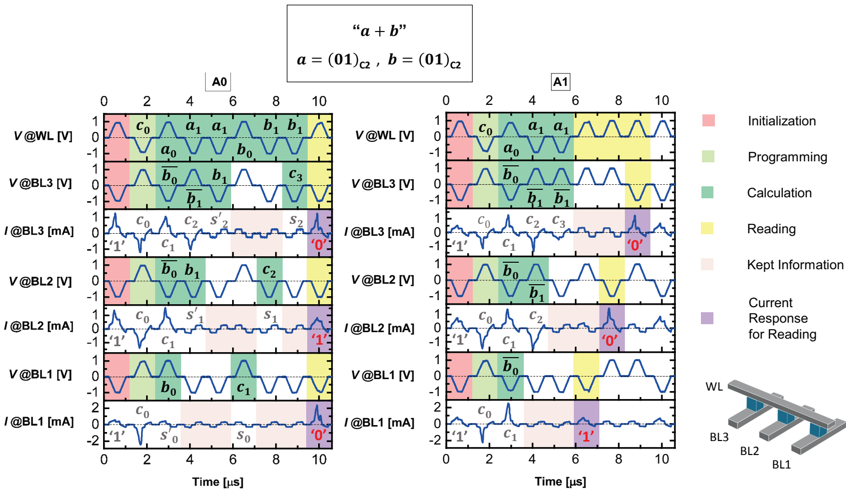


Figure 7.28: Pre-Calculation (PC) Adder: proof-of-concept experiment for the operation "$a + b$" with $a = (01)_{\mathrm{C2}}$ and $b = (01)_{\mathrm{C2}}$, where C2 indicates the two's complement notation. The main / auxiliary calculations are conducted in the array A0 / A1. Reading results are displayed by red labeling. Background colors of the graphs highlight the different operations. Significant bits, which are applied WLs and BLs, are pointed by black lettering. Actual stored cell information is displayed once in the current response line (gray labeling). The lower right illustration depicts the used 1×3 crosspoint array with the terminals WL and BL1 to BL3 for the input signals.[2] (Reprinted with permission from the publisher.)

3$^{\text{rd}}$ step – Calculation of c_1 and s'_0: Due to the subtraction, the WL is set to $\overline{a_0}$ and corresponding BLs to $\overline{b_0}$ to compute c_1 in all cells, excluding (A0-WL-BL2) the least significant bit cell. On this CS device, the first intermediate sum bit s'_0 is calculated by forcing b_0 to BL2.[2]

4$^{\text{th}}$ step – Read of c_0: Next, the carry c_1 has to be read from the TC, since this information is needed to determine the first sum bit in the following step. The information of the remaining cells is maintained by setting the associated BLs to the same potential as applied for WL.[2]

5$^{\text{th}}$ step – Calculation of s_0: The sum bit s_0 is computed in A0-WL-BL2 by forcing b_0 to WL and c_1 to BL2. The remaining information / device states is intentionally preserved.[2]

6$^{\text{th}}$ step – Rewriting of c_1: c_1 needs to be written back to the TC, because this information is required as a third input to determine c_2. The other CS states are untouched.[2]

7$^{\text{th}}$ step – Calculation of c_2 and s'_1: Similar to the PC Adder, the highest significant operand bits are doubled to guarantee the correct sum word. Again, $\overline{a_0}$ is applied to the WL and the carry c_2 is calculated in the TC by setting BL1 to $\overline{b_0}$. s_0 is still preserved in in A0-WL-BL2 by setting BL2 also to $\overline{a_0}$. BL3 is set to b_0 and the cell A0-WL-BL3 is used to compute the second intermediate sum bit s'_1.[2]

8$^{\text{th}}$ step – Read of c_2: c_2, the last carry, has to read from the TC to compute the sum bit s_1 in the following step. The remaining cell information is untouched.[2]

9$^{\text{th}}$ step – Calculation of s_1: s_1, the last sum bit, is determined by setting WL to b_0 and BL3 to c_2. The WL potential is also applied to the remaining BLs to maintain the states / information. Finally, the sum word is stored in the array until the information needs to be read.[2]

To prove the adder functionality, the result is read in the subsequent (but

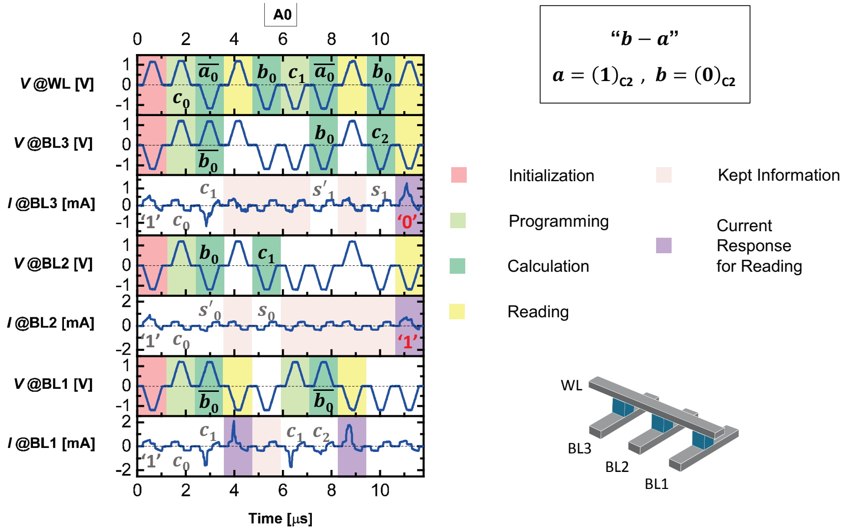


Figure 7.29: Toggle-Cell (TC) Adder: proof-of-concept experiment for the operation "$b-a$" with $a=(1)_{C2}$ and $b=(0)_{C2}$, where C2 indicates the two's complement notation. The TC Adder is based on a single array. Auxiliary calculations are conducted in the TC, which is represented by the least significant cell (A0-WL-BL1). Background colors of the graph highlight the different operation steps. Significant bits, which are applied WLs and BLs, are pointed by black lettering. Actual stored cell information is displayed once in the current response line (gray labeling). The lower right illustration depicts the used 1×3 crosspoint array with the terminals WL and BL1 to BL3 for the input signals.[2] (Reprinted with permission from the publisher.)

not required) step: $s=(01)_{C2}$, which is converted to the decimal system $(1)_{dec}$ as expected.[2]

7.3.3 Discussion

Experimental proving of a highly attractive multi-functionality-in-memory concept is a major milestone: For the first time, a CRS-adder is realized physically, which helps to overcome the von Neumann bottleneck. Achieving this target, ReRAM-based Pt|HfO_2|Hf|Pt CS devices have been embedded in $1 \times n$ crossbar structure.[2]

Beyond simple memory functionality, the ReRAM, considered as two-terminal

device, can be used as logic unit, which enables logic-in-memory operations. All CRS-logic functions are feasible under quasi-static and pulse conditions. Including the present state as third input, the ReRAM becomes a kind of three-terminal device working with three input signals. Based on this, arithmetic operations (addition and subtraction) have been demonstrated on a small-size passive crossbar array by applying the PC / TC Adder scheme.[2] The concept has been proven for pulsed input conditions. These results confirm the general feasibility of the multibit full adder technology. Altogether, this could pave the way for next-generation information technology for parallel processing-in-memory architecture, which is implemented by ReRAMs embedded in energy-efficient, ultra-dense $4F^2$ passive crossbar arrays.[2]

By way of example, a small application is considered, which converts a MP3 file with a high sample rate to a MP3 file with a low sample rate. In the first step of a conventional computer architecture, the MP3 file is read from HDD and stored in the working memory.[142] After that, the data are pushed in the cache and to the registers. Next, the calculation starts in the arithmetic unit. Here, the algorithm needs to coordinate the intermediate results between adders, multipliers etc. which also store intermediate results in clocked pipeline registers. When the calculation is over, the new file is stored back to the HDD.

However, in case of the CRS-logic, the MP3 file is saved in the ReRAM memory. Therefore, read processes can directly be performed in this area of memory. Then either the information is written back, or if the data are not needed anymore, the memory is left as it is. With the read information the conversion / calculation is started in a different area of the array, where no data are stored, or in the same area (depending on what needs to be done with this information), if the memory space is sufficient. A more complex calculation is not performed in one cycle, so some intermediate results are calculated in between and are stored in the devices until they become required for further processes. When all intermediate states are merged and the final result is calculated, one can consider either leaving it stored in this area, where the calculation has been performed, or copy it to another region in the array, where it can be stored.

All steps in this example are performed on the array and in the memory area.

The intermediate steps need to be read out and are needed as inputs in other steps. This costs some energy. However, the additional power consumption induced by these readouts might be overcompensated by the reduction due to data transfer avoidance. The organization of the control unit (CU) has a huge impact of the complexity of these architectures and needs to be adjusted to the purpose of application. One can trade the CU's complexity against the calculation time. For example, by using a lightweight logic-in-memory controller (see [143]) the complexity of the CU is kept small, but the calculation time of the circuit gets much higher. By using a more complex CU or more advantaged calculation concepts the calculation time could be reduced.

The CS device requires further engineering to enable the paradigm shift from conventional CMOS circuits toward hybrid CMOS/CS architectures.[132] Reducing and controlling the CS operation current is one main issue, which still needs to be addressed. A device to device variation of the spike current is observed ($0.5\,\mu$A up to few milliamperes). High leakage currents especially, cause incorrect readouts, if the amplitude is not too far from the spike current. The problem could be aggravated considering these unavoidable device variations. Thus, reducing this leakage is an important engineering task for this type of CS device. The most auspicious approach to decrease the currents is to reduce the cell size, since area-type leakage will scale with the device size. The devices, which are used to prove the CS adder functionality, have an area of $5 \times 5\,\mu\text{m}^2$ which must be scaled down to the low nanometer regime in the future. Furthermore, a more sophisticated forming procedure may lead to a tighter distribution of the initial HRS states, which would also help to reduce the HRS leakage.
In Chapter 6, it is shown for Ta_2O_5-based CRS devices that the forming process has a significant impact on the operation current and that reduction of currents for nanoscale devices is feasible. Therefore, this approach should also possible for CS switching devices. The ON resistance target is in the range of $10..100\,\text{k}\Omega$.[2] Hence, the spike currents could be in the low microampere range. That means the energy consumption per operation / logic function could be as low as few femtojoules, because the feasible ReRAM write / read speed is below 200 ps[14]. However, the actual energy consumption decisively

depends on the applied computer architecture which differs considerably for hybrid CMOS/CS architectures, compared to conventional CMOS-only architectures.[132] Since hybrid CMOS/CS architectures will try to overcome the memory wall, the reduction of energy consumption due to memory access avoidance could be substantial.

Another issue, which should be considered: there may be a significant voltage dividing effect in the array operation because of the line resistance. Here, the Pt WL resistance is in the range of $500\,\Omega$ for CS devices being in the array center. This causes a slight increase of the required RESET. Consider, Pt is not the ideal available conductor material. Therefore, the line resistance and its impact on the device switching properties could be considerably reduced by applying Cu wires. Thus, the write voltage can be reduced by using a different material, achieving more energy efficient procedures.

Chapter 8

Conclusion and Outlook

The present thesis deals with binary-oxide-, redox-based resistive switches (ReRAM). This includes the investigation of crucial impact factors on the ReRAM characteristics, device integration and proof-of-concept experiments for novel application concepts. For HfO_2-based devices, fabrication process parameters have been varied, in order to evaluate the effect on device properties and the intrinsic switching mode. Furthermore, the vertically stacked complementary resistive switch (CRS) based on Ta_2O_5 has been designed and fabricated, which enables simple integration of $4F^2$ structure in ultra-dense, passive nano-crossbar arrays. Beyond process and device improvement (e.g. operation current), investigations are focused on the determination of significant parameters of the complementary resistive switching.
The optimized devices are used to realize logic operations directly in memory units. Based on this CRS-logic, proof-of-concept measurements are performed to achieve crossbar adders with a computation-in-memory feature. The outcome of individual experiments has been summarized in the following sections.

8.1 Device Improvement

HfO_2-based Switches

Pt|HfO_2|Hf|Pt micrometer scaled stacks offer several switching modes: complementary switching and (counter-)eight-wise bipolar switching. The actual preferred switching is directly determined by the Hf electrode thickness. For

5 nm thick Hf film, the device offers symmetric, non-linear and self-limiting *I-V* characteristic, which is referred to as the complementary switch (CS). Since the two used switching states are highly resistive, the CS is inherently comprised of a selector and memory element, making it an ideal candidate for integration in passive crossbar arrays, in order to implement high-dense data storage. Measurements by voltage pulses (500 ns pulse width) show an improved endurance for 10^9 cycles. Furthermore, switching in 500 μA current regime might enable low-power operations for CS applications.
TEM and EDX analyses of the device cross-section show evidence that the Hf film serves as an oxygen getter. The oxygen is taken out of the HfO_2 layer, which becomes reduced, resulting in oxidation of the complete Hf film. The complementary switching can be explained by a rupturing and regrowing of the conductive filament at the two electrode interfaces, as well as using a model of modulation of top electrode cap work function by oxygen incorporation.[6, 71]
Applying an instrument current compliance (CC) for the positive or negative voltage polarity suppresses switching at the second interface and the device shows eight-wise or counter-eight-wise bipolar switching (BS).
By increasing the Hf electrode thickness to 10 nm or even larger, only bipolar switching is observed, where multi-level resistance states are feasible by tuning the maximal applied voltage for the RESET process (deep RESET). Further variation of device fabrication parameters as sputtering power or O_2 sputtering gas flow has impact only on the initial device properties. However, after electroforming, the samples no longer differ.
For BS devices, low-current operations (200..300 μA) are feasible, since the maximal switching current is proportional to the CC level of the electroforming / SET process. Due to all these excellent characteristics, the HfO_2-based devices are promising candidates for proof-of-concept measurements for innovative applications.

Ta_2O_5-based Complementary Resistive Switches

Three vertically stacked CRS structures (anti-serial combination of two bipolar switches) have been fabricated: (1) three-terminal micrometer scaled CRS, (2, 3) two-terminal micro- / nanometer scaled CRS.[3] The CRS *I-V* is similar to the CS characteristic. Therefore, the CRS is also a promising candidate for

designing passive crossbar memories without the need of selective elements. CMOS circuitry is only required for addressing and readout.
The three-terminal devices offer access to the middle electrode (ME) enabling a straightforward electroforming and investigation of the individual cells.[3] Lowering the switching current is one approach for low-power operations. The CRS operation current is determined by the LRS conductance of the individual top cell (TC) and bottom cell (BC), which is controlled by the CC during the electroforming process.
The two-terminal devices feature an embedded ME, enabling simple integration in passive crossbar arrays. However, a novel electroforming technique, which facilitates the separate electroforming procedure of the TC and BC, without the need of access to the ME, has been presented in this work.[3] Furthermore, the operation current decreases by lowering the CC level. Reduction of the switching current of the CRS below 300 μA has been demonstrated. Further electrical measurements show an improved endurance for more than 10^6 cycles, considering the present state-of-the-art technology. Therefore, the embedded ME CRS devices formed by the novel forming procedure are excellent candidates for future low-current elements in passive crossbar arrays.

8.2 Device Applications

Three-terminal Pt|Ta_2O_5|Ta|Ta_2O_5|Pt CRS stacks and reversed stacked CRS devices (Pt|Ta|Ta_2O_5|Pt|Ta_2O_5|Ta|Pt) have been used for fuzzy-logic implementation.[1] Top and bottom electrode serve as input terminals (T1 and T2), whereas the resulting output signal is read at the ME terminal (T3). Quasi-static measurements of the single cells show highly bipolar resistive switching. The TC / BC endurance is more than 10^6 cycles.
Due to the large LRS-HRS resistance ratio of about 100..1000, the voltage, applied to the terminal of the cell being in the HRS, is estimated to drop completely across this cell.[1] Therefore, at T3, only the voltage is detected, which is applied to the terminal of the second cell (being in LRS). This interesting characteristic, combined with the switching dynamics of those devices, enables the realization of MIN and MAX gate logic operations on single CRS elements, whose concept has been introduced by Šuch and Klimo in [7] and Nielen *et al.*

in [8]. These elements can be applied for processing of analog signals and can enable implementation of small-size sorting networks.[81]
The implementation has been demonstrated using different input voltage modes (voltage sweep, base voltage and voltage pulse) and diverse voltage amplitudes.[1] Operation speed in the order of microseconds would be sufficient for many applications (i.e. audio signal processing or sorting). Therefore, the timing constraint is not at all critical.[79]

Beside the three-terminal CRS, more simple two-terminal CRS and CS devices have been presented, in order to realize proof-of-concept experiments of logic-in-memory operations (referred to as CRS-logic), which have been suggested by Linn *et al.* in [9]. Logic operations are performed in the memory unit, where the results are directly stored until the information readout is required. This concept enables one to overcome the von Neumann bottleneck, which is the data transfer limitation between the separated memory and processing unit in conventional computer architecture.
14 two-input Boolean functions are shown by using single CRS or CS devices.[2,5] The logic functions are realized by applying specific signal sequences to the two input terminals and the stored information is read out by a destructive current spike response method. Proof-of-concept measurements have been performed by applying quasi-static voltage sweeps and pulses, where pulse width has been down to 500 ns. The operation currents are always in the microampere / milliampere regime for quasi-static / pulse conditions.

Based on the CRS-logic and the intrinsic carry computation feature of CRS and CS devices, Siemon *et al.* have introduced two multi-bit crossbar adder schemes: Pre-Calculation (PC) Adder and Toggle-Cell (TC) Adder.[10] For both schemes, the previous device state is considered as third input variable, in addition to the two input signals applied to the device terminals.
The proof-of-concept has been performed on 1×8 crossbar arrays (1 wordline, 8 bitlines), where each cross-junction represents a single HfO_2-based CS cell.[2] Due to non-linear CS *I-V* characteristics, no additional selector devices have to be integrated. For the experiment, specific sequences of voltage pulses (in the 500 ns range) have been applied for the required initialization, program-

ming, calculation and reading steps. By using the two's compliment, several arithmetic calculations (addition and subtraction operations) have been realized. Altogether, this could pave the way for next-generation information technology for parallel processing-in-memory architecture, which is implemented by ReRAMs embedded in energy-efficient, ultra-dense $4F^2$ passive crossbar arrays.[2]

8.3 Outlook

Beyond the important results of the present thesis, further investigations are still required to understand physical and chemical switching mechanism in redox-based resistive switches, in order to tailor device properties. This includes construction and experimental proof of an improved model, which explains in detail the change of intrinsic switching modes from bipolar to complementary switching, as well as their origin. (HR)TEM, EDX, atom probe tomography (ATP) and Rutherford backscattering spectrometry (RBS) might be powerful analyzing techniques, in order to investigate the difference of CS and BS in locally resolved physical and chemical structures. Here, the oxygen distribution profile inside the reactive electrode could provide a key role, since the intrinsic switching mode is a direct consequence of the thickness of the reactive electrode, which serves as an oxygen getter. Oxygen is taken out of the active oxide layer, generating oxygen vacancies, which are essential for resistive switching phenomena.[48] Simulations and experimental results should be compared with devices based on different oxides and electrode materials. So far, it seems that the change from CS to BS is not limited to one specific material, but rather a material independent effect.
Additionally, the investigation of the impact of further device and process parameters on initial and subsequent switching characteristics should be continued and extended in detail. The results might be useful for understanding switching properties and to improve the ReRAM characteristics regarding: efficiency, low-power operation, non-linearity (for larger crossbar arrays), endurance and state stability (retention), which are crucial for any device application.

Furthermore, several proof-of-concept experiments of promising computation-in-memory approaches have been demonstrated in the present work. However, implementation of other innovative technology concepts on here presented developed and optimized devices is an ongoing process. Recently, Tappertzhofen *et al.* have suggested a capacitance based non-destructive readout for CRS, composed of asymmetric stacks.[136] The concept is explained in Appendix Section A.5, especially by the equivalent circuit in Appendix Figure A.4. Based on the capacitive non-destructive readout, Kavehei *et al.* have introduced in [144] an Associative Capacitive Network (ACN) concept. This provides a full parallel search for the Hamming distance (i.e. difference) between input and stored templates.[144] Therefore, the ACN is a promising technology for applications in memory-intensive and cognitive computing, stochastic learning and intelligent data processing.[144]

Due to intrinsic characteristics, the CRS devices can be embedded in passive crossbar arrays so that the ACN unit does not require any selector device. For this purpose, a proper 8×16 crossbar structure and single test devices have been designed, based on the optimized Ta_2O_5 CRS (cf. Appendix Figure A.5). The devices show complementary resistive switching *I*-*V* characteristics. Capacitive measurements, which have been performed as demonstrated in Appendix Figure A.6, fulfill all requirements. However, due the limitation of time for the present thesis, further results are not available to date and a lot of research has still to be done, in order to realize the basic ACN features, e.g. a content addressable memory (CAM) for full parallel pattern recognition.

Appendix A

A.1 Electron Beam Lithography

Digital Mask for Nanostructures

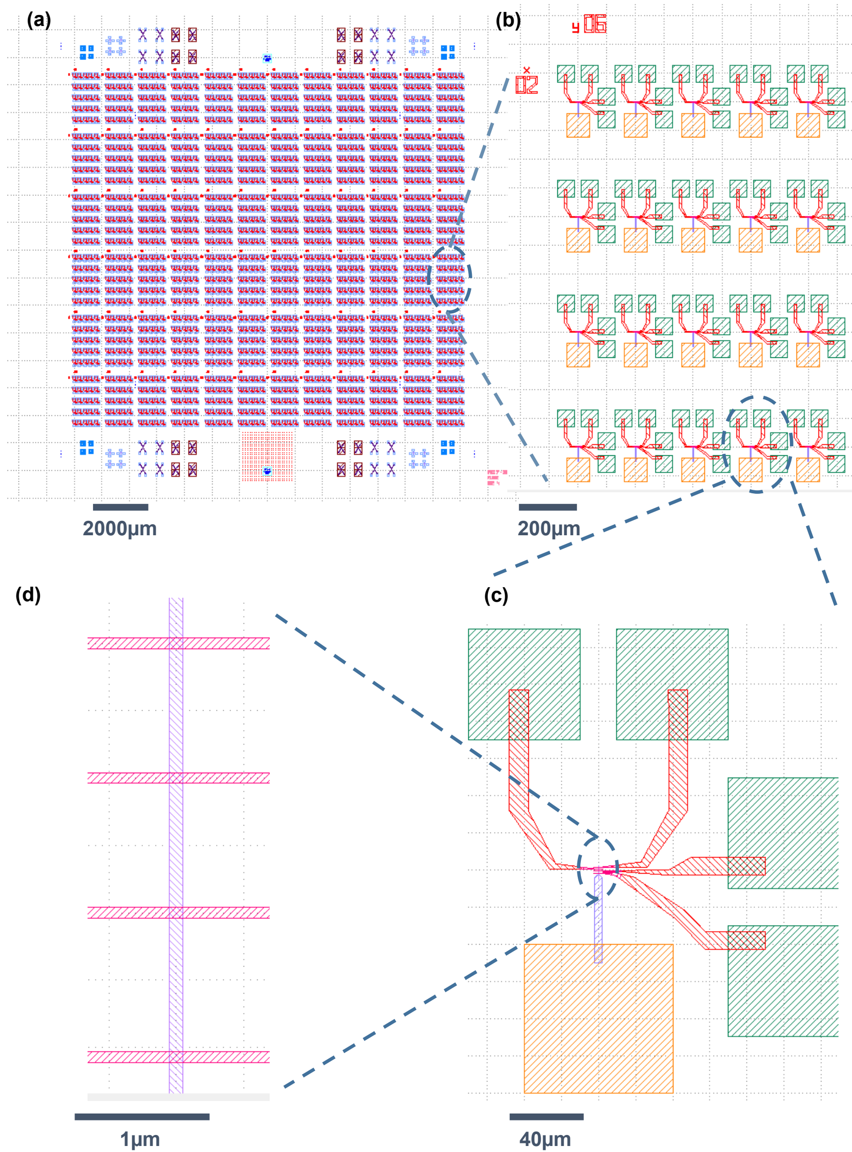


Figure A.1: E-beam process mask. E-beam is controlled by a CAD layout file in order to define the patterning by selective exposure.

Proximity Correction Factor

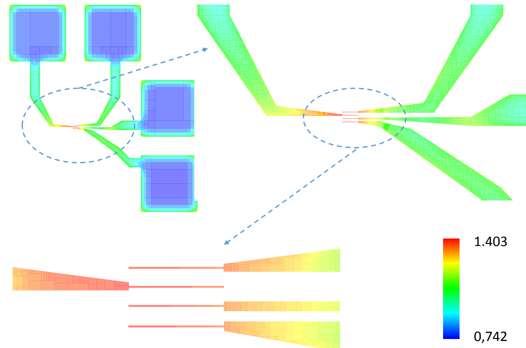


Figure A.2: E-beam proximity correction. The beam base dose is modulated by the mapped proximity correction factor in order to respect the impact of back scattered electrons. Omitting this correction method causes increased exposure dose under which the structure would suffer.

A.2 Thin Film Surface Roughness

Table A.1: Surface roughness analysis of sputtered thin films and used growing parameters. Parameter variations are highlighted by red labeling.

Material	RF / DC* Power [W]	rel. O_2 gas flow [%]	Roughness [nm]
Si	(as substrate)		0.1
SiO_2	(as substrate)		0.2
Hf	116	0	0.6 - 0.8
Hf	58	0	0.4 - 0.5
Ta	116	0	0.3 - 0.6
Pt	375*	0	0.3 - 0.4
HfO_2	116	13	0.2
HfO_2	116	23	0.2
HfO_2	116	30	0.2
HfO_2	58	23	0.2
HfO_2	174	23	0.2
HfO_2	232	23	0.2
Ta_2O_5	232	23	0.2

A.3 Material Stoichiometry

Table A.2: XPS analysis of as deposited HfO_2 with 13 % O_2 sputtering gas amount. (With kind approval of A. Besmehn, ZEA-3, FZ Jülich)

Peak	Compound	E_B [eV]	Area [cps · eV]	RSF	corr. Area	C_{at} [At.-%]
O1s	HfO_2	530.10	13508.824	0.773	18429.501	50.76
O1s	OH-, O+C	531.96	2110.510	0.773	2879.277	7.93
C1s	C-C, C-H	285.00	1097.989	0.314	3496.781	9.63
C1s	C-OH	286.42	303.316	0.314	965.975	2.66
C1s	COOH	289.01	212.893	0.314	678.001	1.87
Hf4f	HfO_2	16.7	28589.857	2.901	9855.173	27.15

Table A.3: XPS analysis of as deposited HfO_2 with 30 % O_2 sputtering gas amount. (With kind approval of A. Besmehn, ZEA-3, FZ Jülich)

Peak	Compound	E_B [eV]	Area [cps · eV]	RSF	corr. Area	C_{at} [At.-%]
O1s	HfO_2	530.10	14803.171	0.773	20195.323	51.41
O1s	OH-, O+C	532.06	1957.822	0.773	2670-971	6.8
C1s	C-C, C-H	285.00	1169.459	0.314	3724.393	9.48
C1s	C-OH	286.3	364.716	0.314	1161.516	2.69
C1s	COOH	289.11	237.19493	0.314	755.395	1.92
Hf4f	HfO_2	16.73	31250.816	2.901	10772.429	27.42

A.4 Statistical Definitions

Coefficient of Determination

In the case of a simple linear regression, the coefficient of determination R^2 is defined by the square of the correlation coefficient ρ, which is defined by

$$\rho\left(x,y\right)=\frac{\operatorname{cov}\left(x,y\right)}{\sigma\left(x\right)\sigma\left(y\right)}=\frac{\sum\limits_{i=1}^{n}\left(x_i-\overline{x}\right)\left(y_i-\overline{y}\right)}{\sqrt{\sum\limits_{i=1}^{n}\left(x_i-\overline{x}\right)^2\sum\limits_{i=1}^{n}\left(y_i-\overline{y}\right)^2}} \tag{A.1}$$

with the random variables x and y, the covariance $\operatorname{cov}(x,y)$ (of x and y), the standard deviations $\sigma(x)$ and $\sigma(y)$, the mean values $\overline{x}$ and $\overline{y}$ and the number data point n. The coefficient of determination ($0 \leq R^2 \leq 1$) is a

quality measure of the linear regression model. “1” indicates a perfect linear relationship, whereas “0” means no linear relationship between x and y.

Box Diagram Plot

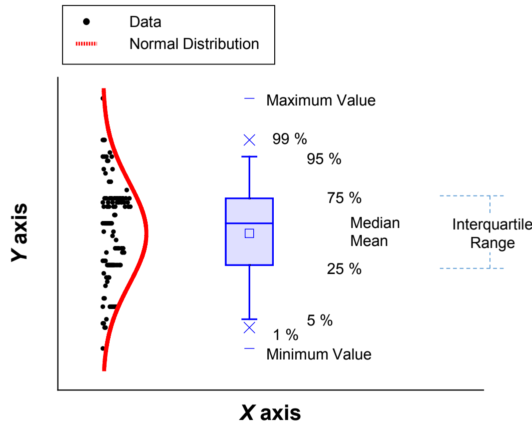


Figure A.3: Definition of the box diagram plot. Measured data points (black), fitted normal distribution curve (red) and derived box diagram (blue) with declaration.

A.5 Associative Capacitive Network

Lately, Tappertzhofen *et al.* have suggested a capacitance based non-destructive readout for CRS composed of asymmetric stacks.[136] The concept is given by the equivalent circuit in Appendix Figure A.4. The two CRS states, LRS/HRS and HRS/LRS, always offer one cell in the HRS, whereas the second cell is in the LRS. The cell being in the LRS is considered as a resistor and the cell being in the HRS is equivalent to a capacitor.

If the TC and the BC differ in the capacitance, both CRS states can be distinguished by capacitive read procedure. This can be implemented by oxide materials with different permittivity or different cell thickness / area for BC and TC (cf. Appendix Equation A.2). Based on the capacitive non-destructive readout Kavehei *et al.* have introduced in [144] an Associative Capacitive Network (ACN) concept. The ACN technique provides the capability of weighting synaptic-like contribution on a shared line, basically realized by bit-by-bit

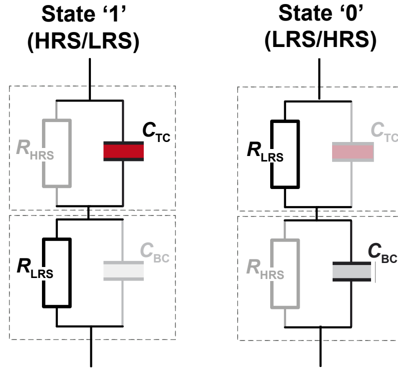


Figure A.4: Associative capacitive network (ACN) scheme. The concepts have been introduced by Tappertzhofen *et al.* in [136] and by Kavehei *et al.* in [144]. Bottom cell (BC) and top cell (TC) distinguish in capacitance for the individual high resistance state. Therefore, total device capacitance is different for the two CRS states (‘1’ and ‘0’ or rather HRS/LRS and LRS/HRS).[144] (Redrawn with permission from the publisher.)

XNOR operations.[144] This enables a full parallel search for the Hamming distance (i.e. difference) between input and stored templates.[144] Due to these capabilities, the ACN is a promising technology for applications in memory-intensive and cognitive computing, stochastic learning and intelligent data processing.[144] Due to intrinsic characteristics, the CRS devices can be embedded in passive crossbar arrays so that the ACN unit does not require any selector device.

In the next step, a proper passive crossbar array structure has been designed as demonstrated in Appendix Figure A.5. For complete fabrication process, three lithography steps combined with back etching are required: (1) bottom electrode line pattern (Pt), (2) middle electrode pattern (Ta_2O_5|Ta) and (3) top electrode line pattern (Ta_2O_5|Pt). The finally patterned array is depicted in Appendix Figure A.5. At each crosspoint, one vertically stacked CRS device (Ta_2O_5|Ta|Ta_2O_5) with embedded ME is sandwiched between bottom and top Pt contact. The devices show complementary resistive switching *I*-*V* characteristic. Capacitive measurements for the two CRS states (LRS/HRS, HRS/LRS) have been performed as demonstrated in Appendix Figure A.6.

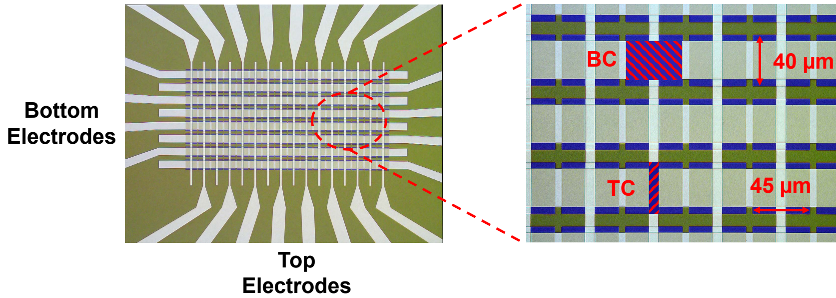


Figure A.5: Optical microscopy of the Associative Capacitive Network (ACN) array. Bottom cell (BC) and top cell (TC) are stacked on each other. The CRS stack is asymmetric due to the different cell area (BC: $45 \times 30\,\mu\text{m}^2$; TC: $7.5 \times 40\,\mu\text{m}^2$).

The cell being in the HRS is assumed as parallel-plate capacitor, whose capacitance C is given by

$$C = \epsilon \frac{A}{d} \tag{A.2}$$

with the material dependent permittivity ϵ, the dielectric (oxide) thickness d and capacitor (cell) area A. As expected, the capacitance of the LRS/HRS state is around four times larger than the capacitance of the HRS/LRS state, since the bottom cell area is also four times larger than the top cell area (cf. Appendix Equation A.2). This difference is sufficient to distinguish both states clearly. Currently, a multiplexer setup demonstrated by Nielen *et al.* in [145] has to be optimized for the 8×16 Ta_2O_5-based ACN array, in order to realize the basic ACN features (cf. Appendix Figure A.7), e.g. a content addressable memory (CAM) for full parallel pattern recognition.

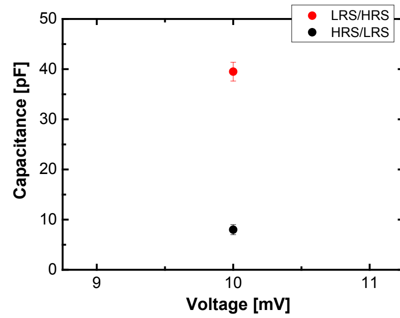


Figure A.6: Capacitance measurement of asymmetric CRS stack. The LRS/HRS capacitance is around four times larger than the HRS/LRS capacitance.

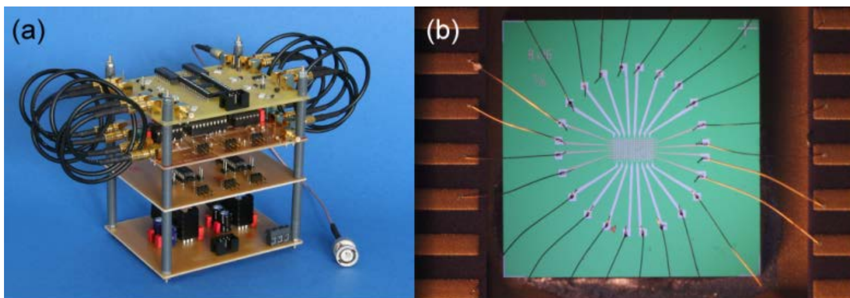


Figure A.7: (a) Multiplexer setup developed by Lutz *et al.* (b) Microscope image of the 8×16 micrometer structure ACN array bonded to a 28-pin chip carrier.[145] (Reprinted with permission from the publisher, © 2015 IEEE.)

List of Figures

2.1 Valence Change Mechanism switching scheme. 9
2.2 Sketch of oxygen vacancy concentration profile. 9
2.3 Device stack and *I*-*V* scheme of CRS device. 11
2.4 Device stack and *I*-*V* scheme of CS device. 12
2.5 CRS as finite state machine. 14

3.1 X-ray reflection at the thin single layer. 16
3.2 X-ray diffraction crystals. 17
3.3 SEM: detection of information. 20
3.4 Probe station and B1500A Semiconductor Parameter Analyzer. 22
3.5 Simplified circuit of impedance converter. 23
3.6 Sputtering equipment. 25
3.7 Process scheme of thin film patterning by photolithography. . . 26
3.8 E-beam writing process. 27

4.1 XRR measurement of Ta_2O_5 thin film. 30
4.2 GIXRD. 33
4.3 XPS analysis of HfO_2. 35
4.4 XPS of HfO_2 vs. relative O_2 during gas flow. 36
4.5 XPS of Ta_2O_5. 36
4.6 Flowchart for BS and CS devices. 39
4.7 Profilometry of patterned photoresist. 39
4.8 Photoresist stripping. 40
4.9 SEM: two-terminal micrometer scaled BS / CS. 42
4.10 TEM - EDX: HfO_2-based cell stack. 42
4.11 Flowchart for three-terminal micro-BC CRS device. 44
4.12 SEM: three-terminal micro-BC CRS device. 45

4.13 Flowchart for two-terminal micro-BC CRS device. 46
4.14 Flowchart for two-terminal nano-BC CRS device. 47
4.15 Profilometry of patterned e-beam resist. 47
4.16 Effect of the low-current oxygen beam treatment with subsequent profile etching. 48
4.17 SEM: two-terminal nano-BC CRS device. 49
4.18 TEM cross-section: two-terminal nano-BC CRS device. 49

5.1 Measure scheme for HfO_2-based devices 53
5.2 Forming and CS cycle in HfO_2-based devices. 53
5.3 CS vs. BS in HfO_2-based devices. 55
5.4 CS vs. BS in HfO_2-based devices. 55
5.5 Initial Resistance vs. relative O_2 sputtering gas flow in HfO_2-based devices. 57
5.6 Forming voltage vs. Initial Resistance in HfO_2-based devices. . . 58
5.7 Forming voltage vs. cell size and relative O_2 sputtering gas flow and in HfO_2-based devices. 58
5.8 SET / RESET voltage vs. relative O_2sputtering gas flow in HfO_2-based devices. 60
5.9 Variation of SET voltage and 'OFF' resistance in HfO_2-based devices. 61
5.10 RESET current vs. current compliance in HfO_2-based devices (by variation of relative O_2 sputtering gas flow). 63
5.11 Initial resistance vs. Hf capping metal thickness in HfO_2-based devices. 64
5.12 Forming voltage vs. capping metal thickness in HfO_2- and Ta_2O_5-based devices. 65
5.13 SET / RESET voltage vs. capping metal thickness in HfO_2- and Ta_2O_5-based devices. 66
5.14 Initial resistance / forming voltage vs. RF sputtering power in HfO_2-based devices. 67
5.15 SET / RESET voltage vs. RF sputtering power in HfO_2-based devices. 68
5.16 RESET current vs. RF sputtering power in HfO_2-based devices. 68
5.17 Thermal stability of HRS / LRS for HfO_2 devices. 72

5.18 Retention test of HRS / LRS for HfO_2 devices. . . . 72
5.19 Endurance tests on HfO_2-based CS device. . . . 74
5.20 Endurance test of HfO_2-based CS device. . . . 76

6.1 Forming procedure of three-terminal device. . . . 81
6.2 Electrical characterization of three-terminal CRS device. . . . 82
6.3 Forming procedure of two-terminal micro-BC CRS device. . . . 83
6.4 Electroforming of two-terminal micro-BC CRS device. . . . 85
6.5 Electrical characterization of two-terminal micro-BC CRS device. 87
6.6 Endurance test of two-terminal micro-BC CRS. . . . 88
6.7 Electrical characterization of two-terminal nano-BC CRS device. 90
6.8 CRS Switching Current vs. Current Compliance. . . . 91
6.9 Endurance test of two-terminal nano-BC CRS. . . . 92

7.1 *I*-*V* scheme for MIN / MAX gate. . . . 96
7.2 MIN / MAX Truth Table. . . . 99
7.3 Single cell characteristic for MIN / MAX gate. . . . 102
7.4 Electrometric characterization of MIN / MAX gate. . . . 103
7.5 Proof-of-concept measurement for MIN Gate. . . . 106
7.6 Proof-of-concept measurement for MAX Gate. . . . 109
7.7 Logic-in-Memory functionality. . . . 113
7.8 Logic-in-Memory functionality. . . . 114
7.9 Pulsed voltage configurations on CS depending on previous state Z'. . . . 116
7.10 Logic TRUE function in HfO_2-based CS device. . . . 118
7.11 Logic FALSE function in HfO_2-based CS device. . . . 119
7.12 Logic p / q function in HfO_2-based CS device. . . . 120
7.13 Logic NOT p / q function in HfO_2-based CS device. . . . 120
7.14 Logic IMP function in HfO_2-based CS device. . . . 121
7.15 Logic NIMP function in HfO_2-based CS device. . . . 121
7.16 Logic RIMP function in HfO_2-based CS device. . . . 122
7.17 Logic RNIMP function in HfO_2-based CS device. . . . 122
7.18 Logic OR function in HfO_2-based CS device. . . . 123
7.19 Logic NOR function in HfO_2-based CS device. . . . 123
7.20 Logic AND function in HfO_2-based CS device. . . . 124

7.21 Logic NAND function in HfO_2-based CS device. 124
7.22 Logic AND function in Ta_2O_5-based CRS device. 126
7.23 Logic IMP function in Ta_2O_5-based CRS device. 126
7.24 Dynamical simulation model for Ta_2O_5-based CRS device. 127
7.25 Schematic sketch of the crossbar array. 129
7.26 Adder truth table for carry and sum operation. 130
7.27 Implementation of the carry operation 133
7.28 Pre-Calculation Adder with "$a + b$", $a = (01)_{C2}$ and $b = (01)_{C2}$. 137
7.29 Toggle-Cell Adder with "$b - a$", $a = (1)_{C2}$ and $b = (01)_{C2}$. . . . 139

A.2 Box diagram definition 151
A.3 Box diagram definition 153
A.4 Associative capacitive network scheme. 154
A.5 Associative capacitive network array. 155
A.6 Capacitance measurement of asymmetric CRS stack. 156
A.7 Multiplexer setup. 156

List of Tables

1.1 Current baseline and prototypical memory technologies. 3

4.1 Growth rates for sputtering. 31

4.2 XPS analysis: as-deposited HfO_2 (23 % O_2 sputtering gas). . . . 34

4.3 Deposition parameters of the HfO_2-based device fabrication processes. 40

4.4 Listed types of CRS devices. 43

4.5 E-beam writing parameters for nano-BC CRS devices. 47

A.1 Surface roughness analysis of sputtered thin films. 151

A.2 XPS analysis: as deposited HfO_2 (13 % O_2 sputtering gas). . . . 152

A.3 XPS analysis: as deposited HfO_2 (30 % O_2 sputtering gas). . . . 152

Bibliography

[1] T. Breuer, L. Nielen, B. Roesgen, R. Waser, V. Rana, and E. Linn, “Realization of Minimum and Maximum Gate Function in Ta_2O_5-based Memristive Devices,” *Scientific Reports*, vol. 6, p. 23967, 2016.

[2] T. Breuer, A. Siemon, E. Linn, S. Menzel, R. Waser, and V. Rana, “A HfO_2-Based Complementary Switching Crossbar Adder,” *Advanced Electronic Materials*, vol. 1, no. 10, pp. n/a–n/a, 2015.

[3] T. Breuer, A. Siemon, E. Linn, S. Menzel, R. Waser, and V. Rana, “Low-current operations in $4F^2$-compatible Ta_2O_5-based complementary resistive switches,” *Nanotechnology*, vol. 26, no. 41, p. 415202, 2015.

[4] T. Breuer, W. Kim, S. Menzel, V. Rana, A. Siemon, E. Linn, and R. Waser, “Low-Currenturrent and High-Endurance Logic Operations in $4F^2$-compatible TaO_x-based Complementary Resistive Switches,” in *Silicon Nanoelectronics Workshop (SNW)*, pp. 1–2, 2014.

[5] A. Siemon, T. Breuer, N. Aslam, S. Ferch, W. Kim, J. van den Hurk, V. Rana, S. Hoffmann-Eifert, R. Waser, S. Menzel, and E. Linn, “Realization of Boolean Logic Functionality using Redox-based Memristive Devices,” *Adv. Funct. Mater.*, vol. 25, no. 40, pp. 6414 – 6423, 2015.

[6] A. Schönhals, D. Wouters, A. Marchewka, T. Breuer, K. Skaja, V. Rana, S. Menzel, and R. Waser, “Critical ReRAM Stack Parameters Controlling Complimentary versus Bipolar Resistive Switching,” in *IEEE International Memory Workshop (IMW)*, pp. 1–4, May 2015.

[7] M. Klimo and O. Šuch, “Memristors can implement fuzzy logic,” *arXiv:1110.2074v1 [cs.ET]*, pp. 1–11, 2011.

[8] L. Nielen, S. Ohm, O. Such, M. Klimo, R. Waser, and E. Linn, “Memristive Sorting Networks Enabled by Electrochemical Metallization Cells,” *Int. J. Unconv. Comput.*, vol. 12, no. 4, pp. 303–317, 2015.

[9] E. Linn, R. Rosezin, S. Tappertzhofen, U. Böttger, and R. b. Waser, “Beyond von Neumann - Logic operations in passive crossbar arrays alongside memory operations,” *Nanotechnology*, vol. 23, no. 30, 2012.

[10] A. Siemon, S. Menzel, R. Waser, and E. Linn, “A Complementary Resistive Switch-based Crossbar Array Adder,” *IEEE J. Emerging Sel. Top. Circuits Syst.*, vol. 5, no. 1, pp. 64 –74, 2015.

[11] C. Tsai, F. Xiong, E. Pop, and M. Shim, “Resistive Random Access Memory Enabled by Carbon Nanotube Crossbar Electrodes,” *ACS Nano*, vol. 7, no. 6, pp. 5360–5366, 2013.

[12] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, “Complementary Resistive Switches for Passive Nanocrossbar Memories,” *Nature Materials*, vol. 9, no. 5, pp. 403–406, 2010.

[13] ITRS, “International Technology Roadmap for Semiconductors.” http://www.itrs2.net/itrs-reports.html, 2015.

[14] A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams, “Sub-nanosecond switching of a tantalum oxide memristor,” *Nanotechnology*, vol. 22, p. 485203, 2011.

[15] A. Siemon, S. Menzel, A. Chattopadhyay, R. Waser, and E. Linn, “In-Memory Adder Functionality in 1S1R Arrays,” *ISCAS*, pp. 1338–1341, 2015.

[16] E. Linn, “Memristive Nano-Crossbar Arrays Enabling Novel Computing Paradigms,” *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2596–2599, 2014.

[17] E. Linn and R. Waser, “Complementary Resistive Switches for Logic-in-Memory Applications,” in *CMOSET 2013 Vol. 3: Circuits and Wireless Track Presentation Slides* (C. E. T. Research, ed.), pp. 241–280, Google Books, CMOS Emerging Technologies, 2013.

[18] J. J. Yang, D. B. Strukov, and D. R. Stewart, “Memristive devices for computing,” *Nat. Nanotechnol.*, vol. 8, no. 1, pp. 13–24, 2013.

[19] F. Pan, S. Gao, C. Chen, C. Song, and F. Zeng, “Recent progress in resistive random access memories: Materials, switching mechanisms, and performance,” *Mater. Sci. Eng. R-Rep.*, vol. 83, pp. 1–59, 2014.

[20] H. Li, B. Gao, Z. Chen, Y. Zhao, P. Huang, H. Ye, L. Liu, X. Liu, and J. Kang, “A learnable parallel processing architecture towards unity of memory and computing,” *Scientific Reports*, vol. 5, p. 13330, 2015.

[21] J. Kelly and S. Hamm, *Smart Machines: IBM’s Watson and the Era of Cognitive Computing.* Columbia Business School Publishing, Columbia University Press, 2013.

[22] S. Baker, *Final Jeopardy: Man vs. Machine and the Quest to Know Everything.* Boston, MA, USA: Houghton Mifflin Co., 2011.

[23] S. Park, H. Kim, M. Choo, J. Noh, A. Sheri, S. Jung, K. Seo, J. Park, S. Kim, W. Lee, J. Shin, D. Lee, G. Choi, J. Woo, E. Cha, J. Jang, C. Park, M. Jeon, B. Lee, B. H. Lee, and H. Hwang, “Rram-based synapse for neuromorphic system with pattern recognition function,” in *2012 International Electron Devices Meeting*, pp. 10.2.1–10.2.4, Dec 2012.

[24] S. Park, A. Sheri, J. Kim, J. Noh, J. Jang, M. Jeon, B. Lee, B. R. Lee, B. H. Lee, and H. Hwang, “Neuromorphic speech systems using advanced ReRAM-based synapse,” in *2013 IEEE International Electron Devices Meeting*, pp. 25.6.1–25.6.4, Dec 2013.

[25] S. Yu, R. Jeyasingh, Y. Wu, and H.-S. Philip Wong, “AC conductance measurement and analysis of the conduction processes in HfO_x based resistive switching memory,” *Applied Physics Letters*, vol. 99, no. 23, 2011. cited By (since 1996)5.

[26] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, “Nanoscale Memristor Device as Synapse in Neuromorphic Systems,” *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, 2010.

[27] M.-J. Lee, C. Lee, D. Lee, S. Lee, M. Chang, J. Hur, Y.-B. Kim, C.-J. Kim, D. Seo, S. Seo, U.-I. Chung, I.-K. Yoo, and K. Kim, "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta_2O_{5-x}/TaO_{2-x} bilayer structures," *Nature Materials*, vol. 10, no. 8, pp. 625–630, 2011.

[28] J. J. Yang, M.-X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro, and R. S. Williams, "High switching endurance in TaOx memristive devices," *Applied Physics Letters*, vol. 97, no. 23, 2010.

[29] W. Kim, S. Menzel, D. J. Wouters, R. Waser, and V. Rana, "3-Bit Multi Level Switching by Deep Reset Phenomenon in Pt/W/TaO_x/Pt-ReRAM Devices," *IEEE Electron Device Lett.*, vol. PP, no. 99, 2016.

[30] X. Lian, E. Miranda, S. Long, L. Perniola, M. Liu, and J. Suñe, "Three-state resistive switching in HfO_2-based RRAM," *Solid-State Electronics*, vol. 98, pp. 38 – 44, 2014. Selected Papers from {ULIS} 2013 Conference.

[31] F. Nardi, S. Balatti, S. Larentis, and D. Ielmini, "Complementary switching in metal oxides: toward diode-less crossbar RRAMs," in *IEEE International Electron Devices Meeting - IEDM '11*, pp. 31.1.1 − 31.1.4, IEEE, 2011.

[32] W. Ma, L. Liu, Y. Wang, Z. Chen, B. Chen, B. Gao, X. Liu, and J. Kang, "Multilevel resistive switching in $HfO_x/TiO_x/HfO_x/TiO_x$ multilayer-based RRAM with high reliability," in *Solid-State and Integrated Circuit Technology (ICSICT), 12th IEEE International Conference on*, IEEE, 2014.

[33] J. H. Yoon, S. J. Song, I.-H. Yoo, J. Y. Seok, K. J. Yoon, D. E. Kwon, T. H. Park, and C. S. Hwang, "Highly Uniform, Electroforming-Free, and Self-Rectifying Resistive Memory in the $Pt/Ta_2O_5/HfO_{2-x}/TiN$ Structure," *Advanced Functional Materials*, vol. 24, no. 32, pp. 5086–5095, 2014.

[34] T. Diokh, E. Le-Roux, S. Jeannot, M. Gros-Jean, P. Candelier, J. F. Nodin, V. Jousseaume, L. Perniola, H. Grampeix, T. Cabout,

E. Jalaguier, M. Guillermet, and B. D. Salvo, "Investigation of the impact of the oxide thickness and RESET conditions on disturb in HfO_2-RRAM integrated in a 65 nm CMOS technology," in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, pp. 5E.4.1–5E.4.4, April 2013.

[35] J. Zahurak, K. Miyata, M. Fischer, M. Balakrishnan, S. Chhajed, D. Wells, H. Li, A. Torsi, J. Lim, M. Korber, K. Nakazawa, S. Mayuzumi, M. Honda, S. Sills, S. Yasuda, A. Calderoni, B. Cook, G. Damarla, H. Tran, B. Wang, C. Cardon, K. Karda, J. Okuno, A. Johnson, T. Kunihiro, J. Sumino, M. Tsukamoto, K. Aratani, N. Ramaswamy, W. Otsuka, and K. Prall, "Process integration of a 27nm, 16Gb Cu ReRAM," in *IEEE International Electron Devices Meeting*, pp. 6.2.1–6.2.4, IEEE, 2014.

[36] "Panasonic Starts World's First Mass Production of ReRAM Mounted Microcomputers," press release, Panasonic Corporation, 2013.

[37] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nat. Mater.*, vol. 6, no. 11, pp. 833–840, 2007.

[38] A. Sawa, "Resistive switching in transition metal oxides," *Materials Today*, vol. 11, no. 6, pp. 28 – 36, 2008.

[39] F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux, and D. J. Wouters, "Control of filament size and reduction of reset current below 10 mu A in NiO resistance switching memories," *Solid-State Electron.*, vol. 58, no. 1, pp. 42–47, 2011.

[40] J. Hutchby, *ITRS Emerging Research Devices International Technology Working Group*, ch. 1.5. Wiley, 2015.

[41] ITRS, "International Technology Roadmap for Semiconductors." http://www.itrs2.net/2013-itrs.htm, 2013.

[42] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges," *Adv. Mater.*, vol. 21, no. 25-26, pp. 2632–2663, 2009.

[43] R. Waser, R. Bruchhaus, and S. Menzel, *Redox-Based Resistive Random Access Memories*, ch. 30. Wiley, 3 ed., 2012.

[44] D. Ielmini, R. Bruchhaus, and R. Waser, “Thermochemical resistive switching: materials, mechanisms, and scaling projections,” *Phase Transit.*, vol. 84, no. 7, pp. 570–602, 2011.

[45] M. N. Kozicki, M. Mitkova, and I. Valov, *Electrochemical Metallization Memories*, ch. 17, pp. 483–514. Wiley-VCH Verlag GmbH & Co. KGaA, 2016.

[46] J. Park, K. P. Biju, S. Jung, W. Lee, J. Lee, S. Kim, S. Park, J. Shin, and H. Hwang, “Multibit Operation of TiO_x-Based ReRAM by Schottky Barrier Height Engineering,” *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 476–478, 2011.

[47] P. Chen, Y. Chen, H. Lee, T. Wu, K. Tsai, P. Gu, W. Chen, C. Tsai, F. Chen, and M. Tsai, “Impacts of device architecture and low current operation on resistive switching of HfOx nanoscale devices,” *Microelectronic Engineering*, vol. 105, pp. 40–45, 2013.

[48] R. Waser, R. Bruchhaus, and S. Menzel, “Redox-based Resistive Switching Memories,” in *Nanoelectronics and Information Technology (3rd edition)* (R. Waser, ed.), pp. 683–710, Wiley-VCH, 2012.

[49] F. Kröger and H. Vink, “Relations between the Concentrations of Imperfections in Crystalline Solids,” vol. 3 of *Solid State Physics*, pp. 307 – 435, Academic Press, 1956.

[50] F. Kröger, “Defect Chemistry in Crystalline Solids,” *Annual Review of Materials Science*, vol. 7, no. 1, pp. 449–475, 1977.

[51] H. Ibach and H. Lüth, *Festkörperphysik: Einführung in die Grundlagen.* Springer-Lehrbuch, Springer Berlin Heidelberg, 7 ed., 2008.

[52] S. Menzel, E. Linn, and R. Waser, “Redox-based Resistive Memory,” in *Emerging Nanoelectronic Devices* (A. Chen, J. Hutchby, V. Zhirnov, and G. Bourianoff, eds.), vol. 1, ch. 8, pp. 137–161, Wiley, 2015.

[53] C. Kügeler, M. Meier, R. Rosezin, S. Gilles, and R. Waser, “High density 3D memory architecture based on the resistive switching effect,” *Solid State Electron.*, vol. 53, no. 12, pp. 1287–1292, 2009.

[54] A. Flocke and T. G. Noll, “Fundamental analysis of resistive nano-crossbars for the use in hybrid Nano/CMOS-memory,” in *ESSCIRC 2007: Proceedings of the 33rd European Solid-State Circuits Conference*, pp. 328–331, Proceedings of the 33rd European Solid-State Circuits Conference, 2007.

[55] D. Kau, S. Tang, I. Karpov, R. Dodge, B. Klehn, J. Kalb, J. Strand, A. Diaz, N. Leung, J. Wu, S. Lee, T. Langtry, K. Chang, C. Papagianni, J. Lee, J. Hirst, S. Erra, E. Flores, N. Righos, H. Castro, and G. Spadini, “A stackable cross point phase change memory,” *IEEE International Electron Device Meeting (IEDM)*, pp. 571–574, 2009.

[56] K. Gopalakrishnan, R. S. Shenoy, C. T. Rettner, K. Virwani, D. S. Bethune, R. M. Shelby, G. W. Burr, A. Kellock, R. S. King, K. Nguyen, A. N. Bowers, M. Jurich, B. Jackson, A. M. Friz, T. Topuria, P. M. Rice, and B. N. Kurdi, “Highly-Scalable Novel Access Device based on Mixed Ionic Electronic Conduction (MIEC) Materials for High Density Phase Change Memory (PCM) Arrays,” in *Symposium on VLSI Technology (VLSIT), Honolulu, HI*, pp. 205–206, 2010.

[57] C. Nauenheim, C. Kuegeler, A. Ruediger, R. Waser, A. Flocke, and T. Noll, “Nano-crossbar arrays for nonvolatile resistive RAM (RRAM) applications,” in *Nanotechnology, 2008. NANO ’08. 8th IEEE Conference on, 18-21 Aug. 2008 Arlington, TX, USA*, pp. 464–467, Nanotechnology, 2008. 8th IEEE Conference on, 18-21 Aug. 2008 Arlington, TX, USA, 2008.

[58] J. J. Yang, J. Borghetti, D. Murphy, D. R. Stewart, and R. S. Williams, “A Family of Electronically Reconfigurable Nanodevices,” *Adv. Mater.*, vol. 21, no. 37, pp. 3754–3758, 2009.

[59] G. Burr, R. Shenoy, K. Virwani, P. Narayanan, A. Padilla, B. Kurdi, and H. Hwang, “Access devices for 3D crosspoint memory,” *J. Vac. Sci. Technol. B*, vol. 32, no. 4, p. 040802, 2014.

[60] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, “Reduction in the reset current in a resistive random access memory consisting of NiO_x brought about by reducing a parasitic capacitance,” *Appl. Phys. Lett.*, vol. 93, no. 3, p. 033506, 2008.

[61] F. Lentz, B. Roesgen, V. Rana, D. J. Wouters, and R. Waser, “Current Compliance-Dependent Nonlinearity in TiO_2 ReRAM,” *IEEE Electron Device Lett.*, vol. 34, no. 8, pp. 996–998, 2013.

[62] M. Son, J. Lee, J. Park, J. Shin, G. Choi, S. Jung, W. Lee, S. Kim, S. Park, and H. Hwang, “Excellent Selector Characteristics of Nanoscale VO_2 for High-Density Bipolar ReRAM Applications,” *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1579–1581, 2011.

[63] R. Rosezin, E. Linn, L. Nielen, C. Kügeler, R. Bruchhaus, and R. Waser, “Integrated Complementary Resistive Switches for Passive High-Density Nanocrossbar Arrays,” *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 191–193, 2011.

[64] ITRS, “International Technology Roadmap for Semiconductors,” 2012.

[65] C. Lo, M. Chen, J. Huang, and T. Hou, “On the potential of CRS, 1D1R, and 1S1R crossbar RRAM for storage-class memory,” in *2013 International Symposium on VLSI Technology, Systems and Application, VLSI-TSA 2013*, International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), 2013.

[66] K. J. Yoon, S. J. Song, J. Y. Seok, J. H. Yoon, T. H. Park, D. E. Kwon, and C. S. Hwang, “Evolution of the shape of the conducting channel in complementary resistive switching transition metal oxides,” *Nanoscale*, pp. 2040–3364, 2013.

[67] S. Schmelzer, E. Linn, U. Böttger, and R. Waser, “Uniform Complementary Resistive Switching in Tantalum Oxide Using Current Sweeps,” *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 114–116, 2013.

[68] Y. C. Bae, A. R. Lee, J. B. Lee, J. H. Koo, K. C. Kwon, J. G. Park, H. S. Im, and J. P. Hong, “Oxygen Ion Drift-Induced Complementary Resistive Switching in Homo $TiO_x/TiO_y/TiO_x$ and Hetero $TiO_x/TiON/TiO_x$

Triple Multilayer Frameworks," *Adv. Funct. Mater.*, vol. 22, no. 4, pp. 709–716, 2012.

[69] Y. Yang, P. Sheridan, and W. Lu, "Complementary resistive switching in tantalum oxide-based resistive memory devices," *Appl. Phys. Lett.*, vol. 100, no. 20, pp. 203112/1–4, 2012.

[70] D. Wouters, L. Zhang, A. Fantini, R. Degraeve, L. Goux, Y. Chen, B. Govoreanu, G. Kar, G. Groeseneken, and M. Jurczak, "Analysis of Complementary RRAM Switching," *Electron Device Letters, IEEE*, vol. 33, pp. 1186–1188, Aug 2012.

[71] F. Nardi, S. Balatti, S. Larentis, D. Gilmer, and D. Ielmini, "Complementary Switching in Oxide-Based Bipolar Resistive-Switching Random Memory," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 70–77, 2013.

[72] J. J. Yang and R. S. Williams, "Memristive Devices in Computing System: Promises and Challenges," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 9, no. 2, p. 11, 2013.

[73] J. Backus, "Can Programming Be Liberated from the Von Neumann Style?: A Functional Style and Its Algebra of Programs," *Commun. ACM*, vol. 21, pp. 613–641, Aug. 1978.

[74] H. Mahmoudi, T. Windbacher, V. Sverdlov, and S. Selberherr, "Implication logic gates using spin-transfer-torque-operated magnetic tunnel junctions for intrinsic logic-in-memory," *Solid-State Electron.*, vol. 84, pp. 191–197, 2013.

[75] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'Memristive' switches enable 'stateful' logic operations via material implication," *Nature*, vol. 464, no. 7290, pp. 873–876, 2010.

[76] R. Rosezin, E. Linn, C. Kügeler, R. Bruchhaus, and R. Waser, "Crossbar Logic Using Bipolar and Complementary Resistive Switches," *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 710–712, 2011.

[77] M. Tada, T. Sakamoto, M. Miyamura, N. Banno, K. Okamoto, N. Iguchi, T. Nohisa, and H. Hada, "Highly reliable, complementary atom switch

(CAS) with low programming voltage embedded in Cu BEOL for Nonvolatile Programmable Logic," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, pp. 30.2.1–30.2.4, 2011.

[78] O. Šuch, E. Linn, M. Klimo, P. Jancovic, M. Frátrik, and K. Fröhlich, "On Passive Permutation Circuits," *IEEE J. Emerging Sel. Top. Circuits Syst.*, vol. 5, no. 2, pp. 173–182, 2015.

[79] L. Nielen (IWE II, RWTH Aachen University), "private communication," 2016.

[80] S. Kvatinsky, N. Wald, G. Satat, A. Kolodny, U. C. Weiser, and E. G. Friedman, "MRL - Memristor Ratioed Logic," in 13th *International Workshop on Cellular Nanoscale Networks and their Applications*, pp. 1–6, Aug 2012.

[81] M. Fratrik, M. Klimo, O. Šuch, and O. Skvarek, "Memristive sorting networks," *Phys. Status Solidi C*, vol. 12, no. 1-2, pp. 233–237, 2015.

[82] H. Kiessig, "Interferenz von Röntgenstrahlen an dünnen Schichten," *Annalen der Physik*, vol. 402, no. 7, pp. 769–788, 1931.

[83] M. Reiners, *Integration and Characterization of Atomic Layer Deposited TiO_2 Thin Films for Resistive Switching Applications.* PhD thesis, RWTH Aachen University, 2014.

[84] T. Breuer, "Gemischt valente Orthoferrite $La_1/3Sr_2/3FeO_3$: Targetpräparation für Dünnfilme und Bestimmung der Ordnungsphänomene." Diploma thesis, RWTH Aachen University, 2012.

[85] P. Meuffels (PGI-7, Forschungszentrum Jülich), "private communication," 2015.

[86] P. Debye and P. Scherrer, "Interference on inordinate orientated particles in x-ray light," *Physikalische Zeitschrift*, vol. 18, pp. 291–301, 1917.

[87] J. Schubert (PGI-9, Forschungszentrum Jülich), "private communication," 2014.

[88] J. Friedrich (PGI-7, Forschungszentrum Jülich), "private communication," 2014.

[89] Hitachi, *Ultra-high Resolution Scanning Electron Microscope - SU8000 Series*, August 2011.

[90] F. Lentz, *Integration of Redox-Based Resistive Switching Memory Devices.* PhD thesis, RWTH Aachen University, 2014.

[91] M. Gerst (PGI-7, Forschungszentrum Jülich), "private communication," 2015.

[92] B. Roesgen (PGI-7, Forschungszentrum Jülich), "private communication," 2015.

[93] C. Nauenheim, *Integration of resistive switching devices in crossbar structures.* PhD thesis, RWTH Aachen University, 2009.

[94] S. Trellenkamp (PGI-8-PT, Forschungszentrum Jülich), "private communication," 2014.

[95] R. Borowski (PGI-7, Forschungszentrum Jülich), "private communication," 2016.

[96] T. Hahn, ed., *International Tables for Crystallography (Volume A) - Space-Group Symmetry.* 2002.

[97] A. Besmehn (ZEA-3, Forschungszentrum Jülich), "private communication," 2014.

[98] H. Kim, H. Jung, J. Jang, J. Park, T. Park, S. Lee, and C. Hwang, "Dependence of optimized annealing temperature for tetragonal phase formation on the Si concentration of atomic-layer-deposited Hf-silicate film," *J. Appl. Phys.*, vol. 110, no. 11, 2011.

[99] D. Triyoso, R. Liu, D. Roan, M. Ramon, N. Edwards, R. Gregory, D. Werho, J. Kulik, G. Tam, E. Irwin, X. Wang, L. La, C. Hobbs, R. Garcia, J. Baker, B. W. Jr., and P. Tobin, "Impact of deposition and annealing temperature on material and electrical characteristics of ALD HfO_2," *J. Electrochem. Soc.*, vol. 151, no. 10, pp. F220–F227, 2004.

[100] L. Chen and R. W. Hoffman, “Angle-resolved x-ray photoelectron spectroscopy method for the thickness measurement of metal oxide/metal ultrathin films,” *Journal of Vacuum Science & Technology A*, vol. 11, no. 4, pp. 2303–2307, 1993.

[101] O. Kerrec, D. Devilliers, H. Groult, and P. Marcus, “Study of dry and electrogenerated Ta_2O_5 and Ta/Ta_2O_5/Pt structures by XPS,” *Materials Science and Engineering: B*, vol. 55, pp. 134–142, 1998.

[102] A. Fantini, L. Goux, R. Degraeve, D. J. Wouters, N. Raghavan, G. Kar, A. Belmonte, Y. Chen, B. Govoreanu, and M. Jurczak, “Intrinsic Switching Variability in HfO_2 RRAM,” in *5th IEEE International Memory Workshop (IMW), Monterey, CA*, pp. 30–33, 2013 5th Ieee International Memory Workshop (imw), 2013.

[103] W. Kim, D. J. Wouters, R. Waser, and V. Rana, “Effect of Ohmic Electrode (Ta, W, Ti, Hf) in TaOx ReRAM devices,” in *E-MRS 2015 Spring Meeting*, E-MRS 2015 Spring Meeting, 2015.

[104] L. Zhao, H. Chen, S. Wu, Z. Jiang, S. Yu, T. Hou, H. P. Wong, and Y. Nishi, “Multi-level control of conductive nano-filament evolution in HfO_2 ReRAM by pulse-train operations,” *Nanoscale*, vol. 6, pp. 5698–5702, 2014.

[105] F. Alibart, L. Gao, B. D. Hoskins, and D. B. Strukov, “High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm,” *Nanotechnology*, vol. 23, no. 7, pp. 75201/1–7, 2012.

[106] H. Manem, J. Rajendran, and G. S. Rose, “Design Considerations for Multilevel CMOS/Nano Memristive Memory,” *ACM J. Emerg. Technol. Comput. Syst.*, vol. 8, no. 1, pp. 6/1–22, 2012.

[107] B. Butcher, S. Koveshnikov, D. Gilmer, G. Bersuker, M. Sung, A. Kalantarian, C. Park, R. Geer, Y. Nishi, P. Kirsch, and R. Jammy, “High endurance performance of 1T1R HfO_x based RRAM at low (20 μA) operative current and elevated (150 °C) temperature,” in *IEEE International Integrated Reliability Workshop Final Report*, pp. 146–150, IEEE International Integrated Reliability Workshop Final Report, 2011.

[108] D. Ielmini, “Modeling the Universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven Filament Growth,” *IEEE Trans. Electron. Devices*, vol. 58, no. 12, pp. 4309–4317, 2011.

[109] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer, and D. Ielmini, “Resistive Switching by Voltage-Driven Ion Migration in Bipolar RRAM-Part II: Modeling,” *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2468–2475, 2012.

[110] Y. Y. Chen, G. Pourtois, S. Clima, L. Goux, B. Govoreanu, A. Fantini, R. Degraeve, G. S. Kar, G. Groeseneken, D. J. Wouters, and M. Jurczak, “Hf cap thickness dependence in bipolar-switching TiN/HfO_2/Hf/TiN RRAM device,” in *Symposium on Nonvolatile Memories held during the PRiME Joint International Meeting of the Electrochemical-Society and the Electrochemical-Society-of-Japan, Honolulu, HI*, pp. 3–9, Nonvolatile Memories, 2013.

[111] Z. Fang, X. P. Wang, J. Sohn, B. B. Weng, Z. P. Zhang, Z. X. Chen, Y. Z. Tang, G. Lo, J. Provine, S. S. Wong, H. . P. Wong, and D. Kwong, “The Role of Ti Capping Layer in HfO_x-Based RRAM Devices,” *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 912–914, 2014.

[112] Z. Wei, T. Takagi, Y. Kanzawa, Y. Katoh, T. Ninomiya, K. Kawai, S. Muraoka, S. Mitani, K. Katayama, S. Fujii, R. Miyanaga, Y. Kawashima, T. Mikawa, K. Shimakawa, and K. Aono, “Demonstration of high-density ReRAM ensuring 10-year retention at 85 °C based on a newly developed reliability model,” in *Technical Digest - International Electron Devices Meeting (IEDM)*, pp. 31.4.1–31.4.4, IEDM, 2011.

[113] Z. Wei, T. Takagi, Y. Kanzawa, Y. Katoh, T. Ninomiya, K. Kawai, S. Muraoka, S. Mitani, K. Katayama, S. Fujii, R. Miyanaga, Y. Kawashima, T. Mikawa, K. Shimakawa, and K. Aono, “Retention model for high-density ReRAM,” in *4th IEEE International Memory Workshop (IMW)*, IEEE, 2012.

[114] B. Gao, J. Kang, H. Zhang, B. Sun, B. Chen, L. Liu, X. Liu, R. Han, Y. Wang, B. Yu, Z. Fang, H. Yu, and D. Kwong, “Oxide-based RRAM:

Physical based retention projection," in *Proceedings of the European Solid State Device Research Conference, ESSDERC*, pp. 392–395, ESSDERC, 2010.

[115] S. Menzel (PGI-7, Forschungszentrum Jülich), "private communication," 2016.

[116] Y. Chen, B. Govoreanu, L. Goux, R. Degraeve, A. Fantini, G. Kar, D. Wouters, G. Groeseneken, J. Kittl, M. Jurczak, and L. Altimime, "Balancing SET/RESET Pulse for $> 10^{10}$ Endurance in HfO_2 1T1R Bipolar RRAM," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3243–3249, 2012.

[117] N. Raghavan, R. Degraeve, A. Fantini, L. Goux, D. J. Wouters, G. Groeseneken, and M. Jurczak, "Modeling the Impact of Reset Depth on Vacancy-Induced Filament Perturbations in HfO_2 RRAM," *IEEE Electron Device Lett.*, vol. 34, no. 5, pp. 614–616, 2013.

[118] C. B. Lee, D. Lee, A. Benayad, S. R. Lee, M. Chang, M.-J. Lee, J.-H. Hur, Y.-B. Kim, C.-J. Kim, and U.-I. Chung, "Highly Uniform Switching of Tantalum Embedded Amorphous Oxide Using Self-Compliance Bipolar Resistive Switching," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 399 – 401, 2011.

[119] D. Kalaev, E. Yalon, and I. Riess, "On the direction of the conductive filament growth in valence change memory devices during electroforming," *Solid State Ionics*, vol. 276, pp. 9–17, 2015.

[120] S. B. Lee, H. K. Yoo, K. Kim, J. S. Lee, Y. S. Kim, S. Sinn, D. Lee, B. S. Kang, B. Kahng, and T. W. Noh, "Forming mechanism of the bipolar resistance switching in double-layer memristive nanodevices," *Nanotechnology*, vol. 23, no. 31, pp. 315202/1–9, 2012.

[121] C. Nauenheim, C. Kuegeler, A. Ruediger, and R. Waser, "Investigation of the electroforming process in resistively switching TiO_2 nanocrosspoint junctions," *Appl. Phys. Lett.*, vol. 96, no. 12, p. 122902, 2010.

[122] G.-S. Park, Y.-B. Kim, S. Y. Park, X. S. Li, S. Heo, M. J. Lee, M. Chang, J. H. Kwon, M. Kim, U.-I. Chung, R. Dittmann, R. Waser, and K. Kim,

"In situ observation of filamentary conducting channels in an asymmetric Ta_2O_{5-x}/TaO_{2-x} bilayer structure," *Nat. Commun.*, vol. 4, pp. 2382/1–9, 2013.

[123] R. Ramprasad, "First principles study of oxygen vacancy migration in tantalum pentoxide," *J. Appl. Phys.*, vol. 95, pp. 954–957, 2004.

[124] B. Govoreanu, G. S. Kar, Y.-Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D. J. Wouters, J. A. Kittl, and M. Jurczak, "$10 \times 10\,\mathrm{nm}^2$ Hf/HfO_x Crossbar Resistive RAM with Excellent Performance, Reliability and Low-Energy Operation," in *IEEE International Electron Devices Meeting - IEDM '11*, pp. 31.6.1–31.6.4, IEDM Tech. Dig., 2011.

[125] T. Diokh, E. Le-Roux, S. Jeannot, C. Cagli, V. Jousseaume, J. F. Nodin, M. Gros-Jean, C. Gaumer, M. Mellier, J. Cluzel, C. Carabasse, P. Candelier, and B. D. Salvo, "Study of resistive random access memory based on $TiN/TaO_x/TiN$ integrated into a 65 nm advanced complementary metal oxide semiconductor technology," *Thin Solid Films*, vol. 533, pp. 24–28, 2013.

[126] E. Linn, S. Menzel, S. Ferch, and R. Waser, "Compact modeling of CRS devices based on ECM cells for memory, logic and neuromorphic applications," *Nanotechnology*, vol. 24, no. 38, p. 384008, 2013.

[127] T. Tamura, T. Hasegawa, K. Terabe, T. Nakayama, T. Sakamoto, H. Sunamura, H. Kawaura, S. Hosaka, and M. Aono, "Switching property of atomic switch controlled by solid electrochemical reaction," *Jpn. J. Appl. Phys.*, vol. 45, no. 12-16, pp. L364–6, 2006.

[128] S. Menzel, M. Waters, A. Marchewka, U. Böttger, R. Dittmann, and R. Waser, "Origin of the Ultra-nonlinear Switching Kinetics in Oxide-Based Resistive Switches," *Adv. Funct. Mater.*, vol. 21, no. 23, pp. 4487–4492, 2011.

[129] S. Menzel, M. Salinga, U. Böttger, and M. Wimmer, "Physics of the switching kinetics in resistive memories," *Adv. Funct. Mater.*, vol. 25, no. 40, pp. 6306–6325, 2015.

[130] P. E. Gaillardon, D. Sacchetto, S. Bobba, Y. Leblebici, and G. D. Micheli, "GMS: Generic memristive structure for non-volatile FPGAs," in *VLSI and System-on-Chip, 2012 (VLSI-SoC), IEEE/IFIP 20th International Conference on*, pp. 94–98, Oct 2012.

[131] R. Waser, V. Rana, S. Menzel, and E. Linn, "Energy-efficient redox-based non-volatile memory devices and logic circuits," in *Energy Efficient Electronic Systems (E3S), 3rd Berkeley Symposium on*, pp. 1–2, 2013.

[132] E. Linn (IWE II, RWTH Aachen University), "private communication," 2015.

[133] T. You, Y. Shuai, W. Luo, N. Du, D. Bürger, I. Skorupa, R. Hübner, S. Henker, C. Mayr, R. Schüffny, T. Mikolajick, O. G. Schmidt, and H. Schmidt, "Exploiting Memristive $BiFeO_3$ Bilayer Structures for Compact Sequential Logics," *Advanced Functional Materials*, vol. 24, no. 22, pp. 3357–3365, 2014.

[134] J. Mustafa, *Design and Analysis of Future Memories Based on Switchable Resistive Elements.* PhD thesis, RWTH Aachen University, 2006.

[135] E. Linn, *Complementary Resistive Switches.* PhD thesis, RWTH Aachen University, 2012.

[136] S. Tappertzhofen, E. Linn, L. Nielen, R. Rosezin, F. Lentz, R. Bruchhaus, I. Valov, U. Böttger, and R. Waser, "Capacity based Nondestructive Readout for Complementary Resistive Switches," *Nanotechnology*, vol. 22, no. 39, pp. 395203/1–7, 2011.

[137] J. van den Hurk, E. Linn, H. Zhang, R. Waser, and I. Valov, "Volatile resistance states in electrochemical metallization cells enabling non-destructive readout of complementary resistive switches," *Nanotechnology*, vol. 25, no. 42, p. 425202, 2014.

[138] A. Schönhals, R. Waser, S. Menzel, and V. Rana, “3-bit read scheme for single layer Ta_2O_5 ReRAM,” in *Non-Volatile Memory Technology Symposium (NVMTS), 2014 14th Annual*, pp. 1–4, Oct 2014.

[139] J. van den Hurk, V. Havel, E. Linn, R. Waser, and I. Valov, “Ag/GeS_x/Pt-based complementary resistive switches for hybrid CMOS/Nanoelectronic logic and memory architectures,” *Scientific Reports*, vol. 3, p. 2856, 2013.

[140] A. Marchewka, B. Roesgen, K. Skaja, H. Du, C.-L. Jia, J. Mayer, V. Rana, R. Waser, and S. Menzel, “Nanoionic Resistive Switching Memories: On the Physical Nature of the Dynamic Reset Process,” *Advanced Electronic Materials*, vol. 2, no. 1, 2016.

[141] A. Siemon, S. Menzel, A. Marchewka, Y. Nishi, R. Waser, and E. Linn, “Simulation of TaO_x-based Complementary Resistive Switches by a Physics-based Memristive Model,” *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1420 – 1423, 2014.

[142] A. Siemon (IWE II, RWTH Aachen University), “private communication,” 2015.

[143] P.-E. Gaillardon, L. Amarù, A. Siemon, E. Linn, A. Chattopadhyay, and G. D. Micheli, “Computing Secrets on a Resistive Memory Array,” in *Design Automation Conference (DAC)*, 2015.

[144] O. Kavehei, E. Linn, L. Nielen, S. Tappertzhofen, S. Skafidas, I. Valov, and R. Waser, “Associative Capacitive Network based on Nanoscale Complementary Resistive Switches for Memory-Intensive Computing,” *Nanoscale*, vol. 5, no. 11, pp. 5119 – 5128, 2013.

[145] L. Nielen, A. Siemon, S. Tappertzhofen, R. Waser, S. Menzel, and E. Linn, “Study of Memristive Associative Capacitive Networks for CAM Applications,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, pp. 153–161, June 2015.

Acknowledgement

This thesis would not have been possible without the support of many people. I would like to express my gratitude to all of them.

I thank Prof. Dr. Regina Dittmann for very spontaneous and willing substitution of Prof. Dr. Rainer Waser, for her excellent and unobstructed supervision of my PhD thesis and great support for organizational matter.

I would like to thank Prof. Dr. Rainer Waser for giving me the opportunity to work within his institute in the highly interesting field of non-volatile memory research. In this highly fascinating topic, he gave me the freedom to follow my interests and to enhance my personal and professional skills.
Furthermore, I want to express my gratitude to Prof. Dr. Tobias Noll for agreeing to act as second reviewer for this thesis. I appreciate his very helpful support for general and detailed questions and organizational needs.

I would like to thank my supervisor Dr. Vikas Rana to his scientific support. His inspiring ideas and discussions helped to guide this work into the right direction.
Special thanks go to Dr. Eike Linn for his great and valuable scientific support. He acquainted me with his CRS logic-in-memory concept, which resulted in a main topic of my thesis. Furthermore, he supported me in writing publications and by fruitful discussions and enabled successful cooperations with several colleagues from IWE II, RWTH Aachen University.
Thanks to Dr. Stephan Menzel for discussions about fundamentals and all valuable comments, suggestions and corrections to improve my publications.
I would like to thank Anne Siemon for wonderful cooperation and her support for publications. She presented her computation-in-memory concept for the two crossbar adder schemes to me. Without her, lots of experiments and great results would not have been possible.
Thanks to Lutz Nielen for cooperation and his support in experiments on MIN / MAX gates and ACN structures. Additionally, he gave me beneficial input for improving publications.
I would like to thank René Borowski and Alfred Steffen for their extensive dis-

cussions, guidance and support in device fabrication and clean room activities. To Dr. Stefan Trellenkamp I want to express my gratitude for his great job in e-beam writing and the countless discussions on this interesting topic. He assisted me in principle questions about designing new structures and solving problems in e-beam lithography process.
I am grateful to Marcel Gerst for the support in hardware and software issues and the measurement equipment. He was involved in designing the impedance converter, which was required to perform the pulsed MIN / MAX gate experiments.
I thank Bernd Roesgen for fruitful discussions about scientific fundamentals and support in measurement equipment. He was also involved in designing the impedance converter for proof-of-concept measurements. I appreciated all private discussions and the entertaining atmosphere.
Thanks to Ms. Astrid Besmehn for discussions about XPS fundamentals and for XPS measurements.
I would like to thank all the staffs from Ernst Ruska-Centre (FZ Jülich) and Central Facility for Electron Microscopy (RWTH Aachen University) for FIB cross-sections and TEM images.
I would like to thank Dr. Paul Meuffels for the support in interpretation of XRD / XRR measurements and fundamental and general discussions.
I am grateful to Jochen Friedrich for the support on SEM equipment and measurements.
Thanks to Hehe Zhang for support in XRR and XRD measurements.
Many thanks to Hailey Williamson for proofreading and spell check.
I would like to thank Maria Garcia, Martina Heins, Luise Snyders and Michaela Ott for their support in administrative questions during my time at PGI-7.

Furthermore, I thank my other office mates, Florian Lentz, Wonjoo Kim and Archana Dangwal as well as Michael Paßens and Nabeel Aslam and all other colleagues for providing an entertaining working atmosphere.

Last but not least, special thanks go to my family for supporting and encouraging me during my studies. I want to thank my daughter, Jessica, for bringing so much joy, laugh, variety and energy into my life.

Band / Volume 37
Resistive switching in ZrO_2 based metal-oxide-metal structures
I. Kärkkänen (2014), xviii, 125 pp
ISBN: 978-3-89336-971-3

Band / Volume 38
Resistive switching phenomena of extended defects in Nb-doped $SrTiO_3$ under influence of external gradients
C. Rodenbücher (2014), xiii, 200 pp
ISBN: 978-3-89336-980-5

Band / Volume 39
Micro-spectroscopic investigation of valence change processes in resistive switching $SrTiO_3$ thin films
A. Köhl (2014), viii, 166 pp
ISBN: 978-3-89336-988-1

Band / Volume 40
Strained Silicon and Silicon-Germanium Nanowire Tunnel FETs and Inverters
S. Richter (2014), iii, 117 pp
ISBN: 978-3-95806-002-9

Band / Volume 41
Integration of Redox-Based Resistive Switching Memory Devices
F. Lentz (2014), i, 166 pp
ISBN: 978-3-95806-019-7

Band / Volume 42
Ladungstransportuntersuchungen an nanofunktionalen Bauelementen mit Diodencharakteristik basierend auf funktionalisierten Nanopartikeln
N. Babajani (2015), iv, 138, XLVII
ISBN: 978-3-95806-026-5

Band / Volume 43
Transport and Noise Properties of Nanostructure Transistors for Biosensor Applications
J. Li (2015), vii, 175 pp
ISBN: 978-3-95806-034-0

Band / Volume 44
Quantitative scanning tunneling spectroscopy of non-polar III-V compound semiconductor surfaces
M. Schnedler (2015), 122 pp
ISBN: 978-3-95806-075-3

Schriften des Forschungszentrums Jülich
Reihe Information

Band / Volume 45
Model-based Algorithm Development with Focus on Biosignal Processing
Y. Yao (2015), x, 169 pp
ISBN: 978-3-95806-080-7

Band / Volume 46
Growth and characterization of crystalline rare-earth based thin oxide fims for the application as gate dielectric in nanotechnology
A. B. Schäfer (2015), xiii, 157 pp
ISBN: 978-3-95806-111-8

Band / Volume 47
TEM/STEM Investigations of Phase Change Materials for Non-volatile Memory Applications
M. Bornhöfft (2017), viii, 135 pp
ISBN: 978-3-95806-221-4

Band / Volume 48
Investigation of ternary nitride semiconductor alloys by scanning tunneling microscopy
V. Portz (2017), 140 pp
ISBN: 978-3-95806-232-0

Band / Volume 49
Redox processes and ionic transport in resistive switching binary metal oxides
K. Skaja (2017), VII, 203 pp
ISBN: 978-3-95806-236-8

Band / Volume 50
Investigation of switching mechanism in Ta_2O_5 -based ReRAM devices
W. Kim (2017), iii, 138 pp
ISBN: 978-3-95806-261-0

Band / Volume 51
Development of ReRAM-based Devices for Logic- and Computation-in-Memory Applications
T. Breuer (2017), x, 180 pp
ISBN: 978-3-95806-270-2

Weitere ***Schriften des Verlags im Forschungszentrum Jülich*** unter
http://wwwzb1.fz-juelich.de/verlagextern1/index.asp

Information
Band / Volume 51
ISBN 978-3-95806-270-2