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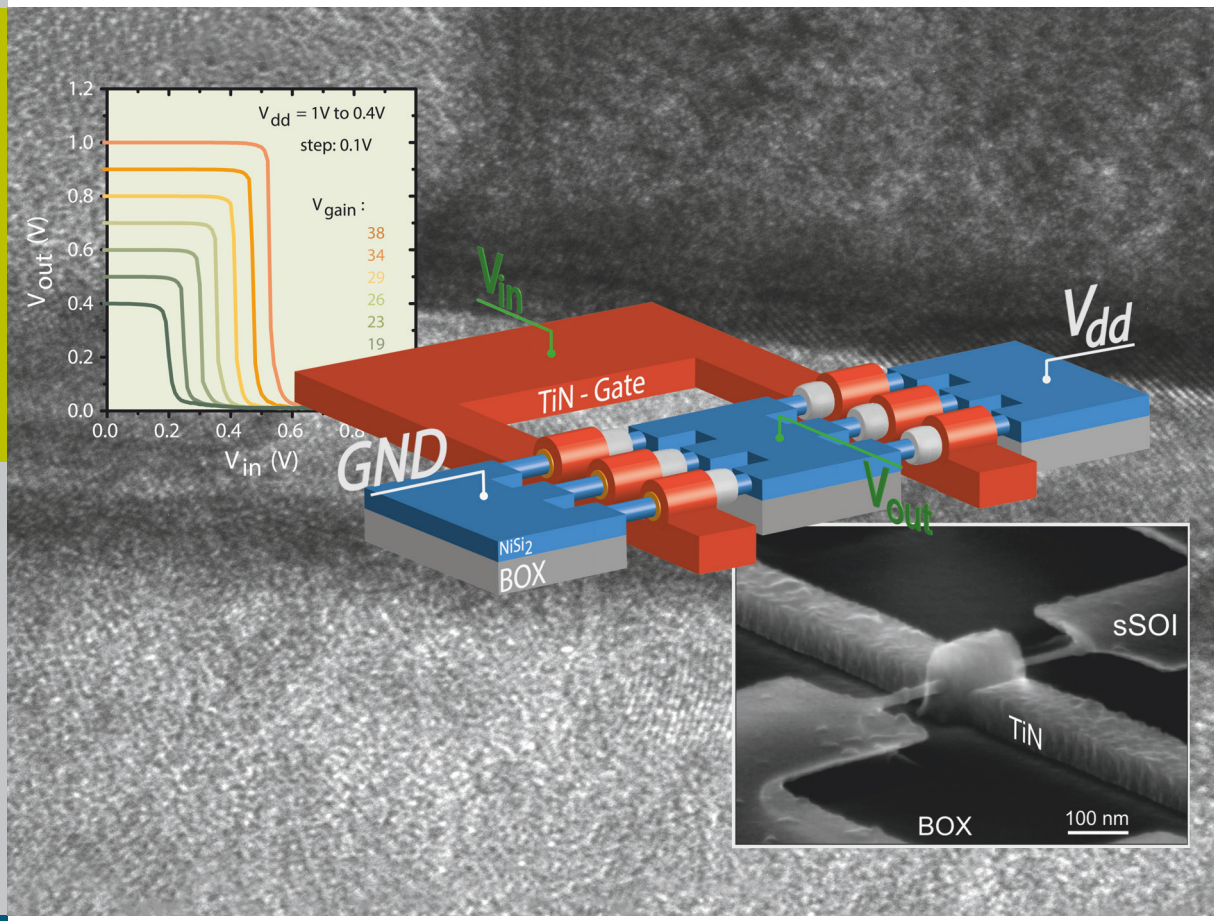

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Abstract

In the era of portable electronic devices energy efficient integrated circuits (ICs) are highly demanded where the power consumption needs to be minimized by the reduction of the supply voltage V_{dd}. Digital circuits based on the complementary metal-oxide-semiconductor field effect transistors (MOSFETs), however, owns a physical limit of the minimum inverse sub-threshold slope (SS) of 60 mV/dec at room temperature. As consequence, the reduction of V_{dd} either leads to low ON-current or increases the OFF-current exponentially which in turn results in high power loss during idle state. Tunnel field effect transistors (TFETs) are proposed as a novel device concept with the potential to replace MOSFETs in low power applications. In comparison, TFETs can offer steeper transition between the OFF and the ON-state (SS<60 mV/dec) since the current transport mechanism relies on band-to-band tunneling.

Within the framework of this thesis strained Si gate-all-around (GAA) nanowire TFETs are fabricated in order to achieve high tunneling currents and small SS. Very small nanowires, down to 5 nm in thickness and down to 15 nm in width, are surrounded by HfO_2/TiN as high-k dielectric and metal gate to obtain optimal gate electrostatics for the device. Tilted ion implantation into the preformed thin epitaxial $NiSi_2$ has been performed to benefit from dopant segregation that results in sharper doping profile for source and drain. Strained Si GAA nanowire p- and n-TFETs have been characterized indicating comparable current performance with 5 µA/µm at V_{dd}=0.5 V. SS below 60 mV/dec has been measured for the n-TFET for $I_d < 10^{-4}$ µA/µm at V_{ds}= 0.1 V at room temperate. However, most of the switching characteristics of the TFETs yield SS larger than the thermal limit. Trap-assisted tunneling is found to be the main root cause. High defect densities, especially in the source/channel interface, creates a parasitic current flow that obscure the SS < 60 mV/dec in the subthreshold region. Substantial characterization with pulsed I-V and temperature dependent DC measurements showed improved switching characteristics due to the reduction of the trap tunneling process.

Complementary TFET (CTFET) inverter with and without ambipolar behavior are fabricated to demonstrate the applicability of the sSi GAA NW TFETs in logic circuits. By comparing the voltage transfer characteristics, both circuits indicate the

basic inverter behavior but the ambipolar current conduction needs to be suppressed to obtain high static noise margins, larger voltage gain and – more importantly - to enable V_{dd} scaling. The suppression of the parasitic tunneling current has been achieved by using a gate-drain underlap with selective SiO_2 spacer at the drain side. Robust CTFET inverter are achieved for the first time with large static noise margins.

Based on the successful optimization of the inverter circuit, the world's first half SRAMs with strained Si nanowire CTFET have been fabricated to explore the capability of TFETs for 6T-SRAM cells. Electrical measurements on cells with outward faced n-TFET access transistors have been performed to determine the static behavior. SRAM butterfly curves are created that allow the assessment of cell functionality and stability. The forward p-i-n leakage at certain bias configuration of the access transistor may lead to malfunctioning storage operation. This effect holds true even without the contribution of the ambipolar behavior but is justified by the inherent unidirectional current transport property of TFETs. Lowering the bit-line bias of the SRAM is found to mitigate this effect resulting in functional hold, read and write operation of the 6T-SRAM cell.

Kurzfassung

Im Zeitalter der mobilen Elektronik steigt die Relevanz nach energieeffizienten integrierten Schaltungen (ICs), bei der die Versorgungsspannung (V_{dd}) reduziert wird, um den Stromverbrauch zu verringern. Digitale Schaltungen, die auf Metall-Oxid-Halbleiter Feldeffekttransistoren (MOSFETs) basieren, verfügen über eine physikalische Begrenzung der minimal erreichbaren inversen Unterschwellensteigung (SS) von 60 mV/dec bei Raumtemperatur. Infolgedessen führt eine Reduktion von V_{dd} entweder zum niedrigen Einschaltstrom oder erhöht den Ausgangsstrom exponentiell, was zu einem erhöhten Leistungsverlust im Leerlaufbetrieb führt. Der Einsatz von Tunnelfeldeffekt Transistoren (TFET) sollen hingegen die MOSFETs in den energiesparsamen Anwendungen ersetzen. Durch das Prinzip des Band-zu-Band Tunneln ist ein steileres Schaltverhalten zwischen AUS und AN Zustand (SS<60 mV/dec) im Vergleich zu MOSFETs möglich.

Im Rahmen dieser Arbeit werden verspannte Silizium Gate-All-Around (GAA) Nanodraht TFETs hergestellt mit dem Ziel, hohe Tunnelströme und kleine SS<60 mV/dec zu realisieren. Sehr kleine Nanodrahtabmessungen mit 5 nm Dicke und bis zu 15 nm in der Breite werden hierbei erreicht. Als high-k Dielektrikum und Gatemetall wurden HfO_2/TiN verwendet, welches die Nanodrähte vollständig umschließt für die optimale Gateelektrostatik. Stromkennlinienmessungen der verspannten Si GAA Nanodraht p-und n-TFETs zeigten vergleichbare Ströme mit 5 µA/µm bei $V_{dd} = 0.5$ V. Für den n-TFET wurden SS unter 60 mV/dec bei Raumtemperatur gemessen bei Strömen von $I_d < 10^{-4}$ µA/µm für V_{ds}= 0.1 V. Jedoch liegt das Maß des Schaltverhaltens für die meisten TFETs über diese thermische Limitierung. Der Grund dafür ist das sogenannte Trap-assisted Tunneling. Hohe Störstellendichte, speziell an den Source/Kanal Übergang, erzeugen einen parasitären Strombeitrag und verhindern das Auftreten von SS < 60 mV/dec im Unterschwellenbereich. Die Ergebnisse der Kennlinien durch kurze Pulsmessungen sowie Messungen in Abhängigkeit der Temperatur zeigten eine Verbesserung des Schaltverhaltens durch die Reduktion des Trap-Tunneling Prozesses.

Erste komplementäre TFET (CTFET) Inverter Schaltungen mit und ohne ambipolares Verhalten wurden hergestellt, um die Eignung der verspannten Si GAA Nanodraht TFETs im Logikschaltungen zu demonstrieren. Hierbei zeigte sich, dass das ambipolare Verhalten unterdrückt werden muss um hohe Rauschpegel (SNM), Spannungsverstärkungen und vor allem eine V_{dd} Skalierbarkeit zu gewährleisten. Die Unterdrückung der Ambipolarität wurde durch die Erzeugung eines Gate-Drain Underlap

mit selektivem SiO_2-Spacer an der Drainseite erreicht. Dadurch konnten erstmals robuste CTFET Inverter experimentell gezeigt werden, die einen hohen Rauschpegel aufweisen.

Mit der Optimierung der Inverterschaltung wurden Half-SRAMs mit verspannten Si Nanodraht CTFETs weltweit erstmalig experimentell hergestellt, um die Funktionalität der TFETs in 6T-SRAM Zellen zu untersuchen. Das statische Verhalten wird an den Half-SRAM Zellen mit einer Outward-faced n-TFET Konfiguration als Zugriffstransistoren gemessen. Mit der Erzeugung der Butterfly Kurven wurde die Funktionalität sowie die Stabilität der Speicherzellen bewertet. Die Ergebnisse zeigen, dass aufgrund der SRAM Operation (Lesen, Schreiben, Standby) bedingte Vorwärtsspannung an den TFETs als Zugriffstransistoren hohe Leckströme verursacht werden, was zum Fehlverhalten der SRAM Zelle führt. Dieses Verhalten tritt auch für TFETs ohne Ambipolarität auf und ist durch die unidirektionale Stromtransporteigenschaft der TFETs begründet. Eine Spanungsminderung an den Bit-Lines des SRAMs ist eine mögliche Maßnahme, um die SRAM Operationen in einer 6T-SRAM Zelle erfolgreich durchzuführen.

Content

1. Introduction

Astonishing technological development has changed the world over the past century. Thanks to fast information processing the IT industry has gained new possibilities that enabled great changes in commerce, communication and entertainment. Cloud based infrastructure provides the foundation for machine-to-machine communication. Terms like "internet of things" arise where sensors, e.g. in wearables, measure and gather data. The information is transferred to computing devices, which evaluate the data in real time giving feedback to the user. In 2014 the number of global mobile devices (7.6 billions) exceeded the world's population. For the same year, Cisco Visual Networking Index (VNI) estimated the worldwide mobile data traffic to amount up to 69% of the overall transferred data corresponding to 2.5 EB (exabytes = 1million terabyte) per month. Current prognostications assume an increase by a factor of 10 until the year 2019 surpassing 24.3 EB/month with 11.5 billion mobile devices [1].

The demanded computational speed for handling such large amount of data has grown exponentially during the last decades in order to enable the scenario above. The breakthrough has started in 1960 with the advent of integration of solid-state transistors on a common chip rather than wiring individual, discrete components by hand. Since then, devices were continuously scaled down to increase the performance of a single device on one hand and the packaging density on a chip on the other hand. More transistors on a chip permit more computing power in order to fulfill requirements given by the International Technology Roadmap for semiconductors (ITRS) [2]. Huge investments in research and development have been made to shrink the critical dimensions of devices down to the greatest extent possible. The technology advancement has been well predicted up to now by Moore's law back in 1965 [3] stating that the device density on an integrated circuit doubles every two years. When traditional scaling was facing its end, Intel Corporation, a leading company in the semiconductor industry, introduced several innovative concepts such as applying strain to the Si channel for the 90 nm node (2003-2005), to improve charge carrier mobility [4] or exchanging the SiO_2 with a high-κ dielectric for the 45 nm node (2007-2009) [5]. A more sophisticated concept was implemented in 2012 by moving away from planar to tri-gate FinFETs with a 3D device architecture to push the node down to 22 nm [6], once again confirming the continued validity of Moores Law.

Today, metal-oxide-semiconductor field-effect-transistors (MOSFETs) are still the core building blocks of digital integrated circuits. State of the art Central Processing Units (CPUs) with 14nm technology nodes were first fabricated by Intel containing several billions of transistors [7]. An alliance led by IBM Research recently demonstrated a test chip with working transistors based on 7 nm node utilizing extreme ultraviolet lithography (EUV) [8]. They postulate an area scaling improvement close to 50% over the present focused 10 nm node which Intel plans to move into by 2017 [9]. Further shrinking, however, becomes more and more difficult since physical scaling limits are reached that give rise to leakage currents. Instead, future nodes might be driven by new transistor designs to continue the performance improvements.

Having such immense transistor counts on a chip, power density becomes an important factor. In general, the total power consumption of a chip can be given by the following expression:

$$P_{total} = P_{dynamic} + P_{static} = C_{load} V_{dd}^2 f + I_{leak} V_{dd} \tag{1.1}$$

The dynamic part $P_{dynamic}$ describes the power dissipation during switching of the integrated circuit by charging and discharging the load capacitance C_{load} with frequency f and supply voltage V_{dd}. The second part represents the static power consumption P_{static} addressing the non-active devices on the chip which still provide a certain OFF-current. Even though the main contribution comes from $P_{dynamic}$, the static power consumption increases as more devices are added on the chip that would also increase the total leakage current I_{leak}. For mobile systems this means higher battery drain even when the device is in idle state. A more critical consequence is, that heat dissipation increases considerably. External cooling systems as in working stations preserve the functionality to a certain degree, but limiting the power dissipation is mandatory to continue Moore's law. As equation (1.1) implies, reduction of the supply voltage V_{dd} is a promising approach to decrease the total power consumption.

For conventional MOSFETs, a reduction of the supply voltage leads to lower ON-current at the cost of computational speed. Scaling V_{dd} in conjunction with the threshold voltage V_{th} to maintain high ON-current increases the OFF-current exponentially since the inverse subthreshold slope SS, a figure of merit for transistors to evaluate the switching behavior, is limited to 60 mV/dec at room temperature (Figure 1.1). For applications requiring sufficient current modulation from the OFF to the ON-state of 10^5, the supply voltage level cannot be reduced below 0.3 V with the SS restriction [10]. Therefore, a good tradeoff between power loss and performance can only be achieved with steep-slope devices which overcome the inherent limitation of MOSFETs.

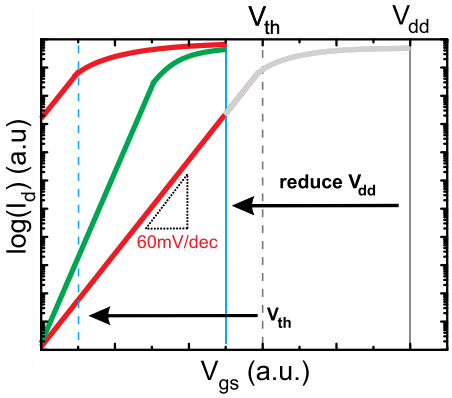

Figure 1.1: Schematic representation of MOSFET transfer characteristics (red-curve). Reducing the supply voltage V_{dd} either lowers ON-current or increasing OFF-current exponentially depending on V_{th} scaling. Transfer characteristics maintaining large I_{on}/I_{off} ratio at low V_{dd} can only be achieved with inverse subthreshold slope smaller than 60 mV/dec (green-curve).

One of the most promising concepts for steep-slope devices is the tunneling field-effect-transistor (TFET). The charge carrier transport is based on quantum mechanical band-to-band tunneling (BTBT) through a gate controlled potential barrier instead of overcoming the barrier by thermionic emission. This different working principle theoretically allows a more abrupt transition from the OFF to the ON-state. The BTBT mechanism had been experimentally discovered by Esaki in 1958 with Ge based p-n diodes, demonstrating negative differential resistance as proof for the tunneling current [11]. First attempt to apply BTBT into a transistor was proposed in the late 1980s [12][13]. TFETs gained much interest when in 2005 the first device capable of inverse subthreshold slopes below 60 mV/dec was reported utilizing carbon nanotubes [14] and two years later even for TFETs based on Si technology [15]. Up to the present, many research groups invest significant effort to dethrone MOSFETs gaining various insights on TFETs, especially, for clarifying fundamental performance boosters. However, even though a broad spectrum of TFETs with different materials and architectures exhibiting SS $<$ 60 mV/dec has been reported [16][17], the average switching slopes of all these devices are still larger than 60 mV/dec. Additionally, the experimentally demonstrated TFETs still suffer from low I_{on}-currents which makes it difficult to compete with the state of the art complementary MOS (CMOS) technology.

Detailed analysis of TFETs for circuit performance is quite rare since it requires accurate compact models in the best case for p- and n–devices. Instead, look-up table models based on simulation data are used to predict circuit performance. Latest TFET results shown in [17][18] are supporting the statement that TFETs are well suited for

low-power and moderate frequency based logic and analog circuits. So far experimental demonstration of TFETs has been only done for inverters with Si nanowires [19][20]. Deeper insight into more advanced circuits would be beneficial to evaluate the potential of TFETs with respect to CMOS integrated circuits.

The present work is structured in 7 chapters. After this introductory part chapter 2 provides the theoretical background with the focus on the different transport mechanisms of TFETs and MOSFETs. Furthermore, TFET related parasitic properties are presented to support the upcoming discussions. In chapter 3 the advantage of the Si platform for TFETs and potential design considerations are elaborated with the goal to improve the overall TFET performance. The combination of various technology boosters results in TFETs with strained Si gate-all-around nanowires, that offer optimal condition to meet the key design rules, sets the basic building block for the devices in this entire work. Detailed I-V characterization on the fabricated p- and n-TFETs will be presented and analyzed in Chapter 4. Complementary TFET inverters are demonstrated in Chapter 5 and, for the first time, the functionality of 6T-SRAM cell will be investigated by means of fabricated half-SRAMs given in Chapter 6.

2. Theoretical background

The following chapter provides the essential theoretical background in order to elucidate the TFET device concept and physical relations for the description of the experimental results in this work. Starting with an introduction, the working principle of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and the Tunnel Field Effect Transistor (TFET) will be explained in depth to emphasize the significant difference in charge transport mechanisms which are fundamental for the subthreshold characteristics of these two devices. Concepts from quantum mechanics have to be taken into account to support the explanations. In addition, critical parasitic and inherent properties of TFETs will be introduced which influence the TFET performance and applicability.

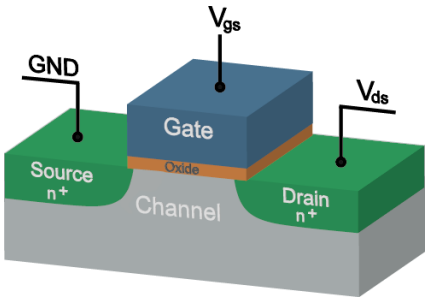

Figure 2.1: Schematic of a three terminal n-channel MOSFET with the isolated gate acting as a voltage driven current switch to enable charge transport from the source to the drain.

2.1 MOSFET operation

Metal-oxide-semiconductor field effect transistors (MOSFETs) are the elemental current switches of state-of-the-art integrated circuits. These three-terminal devices utilize the electric field effect in order to control the current through the channel. A

schematic illustration of an n-type MOSFET[1] is shown in Figure 2.1. Both current terminals are n^+-doped forming the source and drain regions. In general, the terminal denoted as source is connected to the ground while the drain is linked to supply voltage. This drain-source voltage V_{ds} determines charge carrier transport from the source to the drain terminal in the ON-state operation. The core of the device is the gate electrode where the main switching takes place. It is located between source and drain on top of the substrate, which is isolated by an oxide. This insulated metal gate electrode acts as a plate capacitor modulating the electrical resistance of the channel. In case no gate-source voltage V_{gs} is applied the channel resistance is very large and the entire device acts as an open switch. By applying a positive V_{gs}, the electrical field attracts electrons to accumulate below the gate forming a conductive n-channel which allows current flow from source to drain terminal.

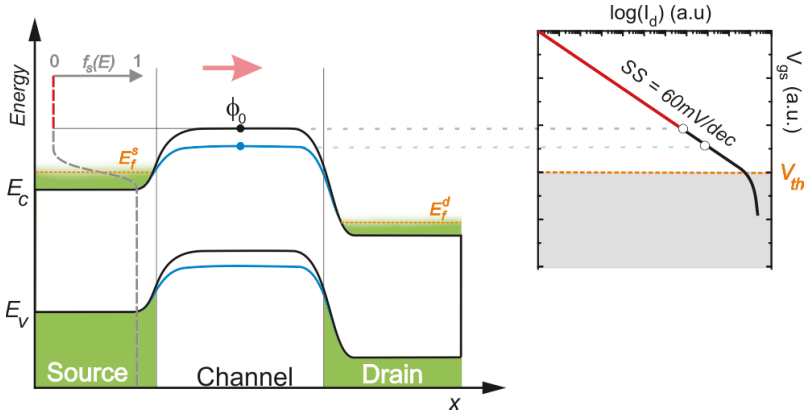

Figure 2.2: Band profile of an n-MOSFET describes the increase of current I_d by applying a positive gate voltage V_{gs}. This lowers the channel energy barrier and enables electron flow from source. The channel surface potential ϕ_0 scans along the thermally broadened tail of the Fermi function with increasing V_{gs} which increase I_d by a factor of 10 for every 60 mV. Note that the Fermi distribution function is similar at the drain side but left out for simplicity.

In order to get further insight to the switching principle of MOSFETs, the conduction and valence bands of the device along source, channel and drain are depicted in Figure 2.2. Between the high doped source/drain and intrinsic channel region, a potential barrier for electrons ϕ_0 is formed. When a positive gate-source

[1] For simplicity, consideration within the fundamental chapter focuses on n-type transistors. All findings can be applied to p-type devices by appropriate change of the signs and parameters.

voltage V_{gs} is applied, the bands in the channel move down allowing electron transport from source to the positive biased drain side. The drain current I_d raises exponentially with V_{gs} and depends on the injection of carriers from a thermally broadened Fermi distribution function of electrons at the source side. Once charge carriers enter the channel, they travel by drift and diffusion mechanism to the drain. Thus, the total current is limited by the channel resistance. This is the reason why manufactures in the past put the focus on scaling the channel length.

2.1.2 Subthreshold characteristics

Figure 2.2 illustrates the transfer characteristics $I_d(V_{gs})$ of an n-MOSFET below and above a threshold voltage V_{th}. In order to obtain the switching performance of MOSFETs we need to look at the drain current in the subthreshold regime $V_{gs} < V_{th}$. One approach is to utilize a simple one dimensional model to calculate the current flow in MOSFETs given by the Landauer formalism [21]:

$$I_d = \frac{2e}{h} \int_{-\infty}^{\infty} T(E)\,[f_s(E) - f_d(E)]\,dE \tag{2.1}$$

where e is the elementary charge, h the Plank constant, $T(E)$ is the transmission probability of charge carriers and $f_s(E)$, $f_d(E)$ are the Fermi distribution functions. The boundaries of the energy integral can be modified considering that only electrons contributes to the drain current with energy greater than the potential barrier height ϕ_0 for electrons. Hence, $T(E) = 1$ for $E > \phi_0$ and $T(E) = 0$ for all other energies and equation (2.1) becomes:

$$I_d = \frac{2e}{h} \int_{\phi_0}^{\infty} [f_s(E) - f_d(E)]\,dE \tag{2.2}$$

Since a positive drain voltage $V_{ds} > 0$ is applied for an n-MOSFET, the drain Fermi energy level is $E_f^d < E_f^s$ which means that charge injection from drain to channel can be neglected $f_d(E > \phi_0) \approx 0$. Due to the fact that the channel potential is larger than the source Fermi energy level ($\phi_0 \gg E_f^s$) in the subthreshold regime, only electrons from the high energy tail of the Fermi distribution function at the source $f_s(E > \phi_0)$ are injected into the channel. This allows the employment of the simpler Boltzmann distribution for $f_s(E)$ to approximate the exponential increase in current (see Figure 2.3):

$$I_d \approx \frac{2e}{h}\int_{\phi_0}^{\infty} f_s(E)\,dE \approx \frac{2e}{h}\int_{\phi_0}^{\infty} \exp\left(-\frac{E-E_f^s}{k_BT}\right)dE = \frac{2e}{h}k_BT\,exp\left(-\frac{\phi_0-E_f^s}{k_BT}\right) \tag{2.3}$$

An important figure of merit describing the rate of current increase of a transistor in dependence of V_{gs} is the inverse subthreshold slope SS with the following expression [22]:

$$SS = \left(\frac{\partial \log I_d}{\partial V_{gs}}\right)^{-1} = \ln(10)\left(\frac{1}{I_d}\frac{\partial I_d}{\partial V_{gs}}\right)^{-1} = \ln(10)\left(\frac{1}{I_d}\frac{\partial I_d}{\partial \phi_0}\frac{\partial \phi_0}{\partial V_{gs}}\right)^{-1} \tag{2.4}$$

The derivative $\partial I_d/\partial\phi_0$ and $1/I_d$ can be calculated from equation (2.3) resulting in:

$$SS = k_BT\ln(10)\left(\frac{\partial\phi_0}{\partial V_{gs}}\right)^{-1} \tag{2.5}$$

The relation between the surface potential and the gate voltage is described by the capacitances at the gate dielectric-substrate interface of the device:

$$\partial\phi_0 = eV_{gs}\left(\frac{C_{ox}}{C_{ox}+C_{depl}+C_{inv}}\right) \tag{2.6}$$

where C_{ox} is the oxide capacitance, C_{depl} the depletion capacitance and C_{inv} the inversion capacitance. Both, C_{depl} and C_{inv} stem from the charges at the Si surface below the gate oxide. In the subtreshold regime the gate voltage is too low to form an inversion layer, thus C_{inv} can be neglected. The inverse subthreshold slope in (2.5) combined with (2.6) leads to:

$$SS = \frac{k_BT}{e}\ln(10)\left(1+\frac{C_{depl}}{C_{ox}}\right) \tag{2.7}$$

For a well-designed MOSFET, C_{ox} has to be greater than C_{depl} as stated in [10] to allow one-to-one movement of the channel bands with the applied gate voltage. At room temperature $T \cong 300\text{K}$ the minimum value of the inverse subthreshold slope for MOSFETs yields to:

$$SS = \frac{k_BT}{e}\ln(10) \approx 60\text{mV/dec}\ . \tag{2.8}$$

This means that at least 60 mV gate voltage is required in order to increase the drain current of a MOSFET by one order of magnitude at room temperature. Equation (2.8) reveals that the thermal dependency of SS caused by the high energy tail of the Fermi distribution function at the source is responsible for the limited switching slope. Any

transistor structures whose switching relies on thermal emission over a potential barrier faces this inherent limitation independent of its scale or material. As a consequence, the obstacle of minimum 60 mV/dec restricts further scaling of the supply voltage on integrated circuits, since a certain minimum voltage window is needed to switch between $I_{\mathbf{on}}$ and $I_{\mathbf{off}}$.

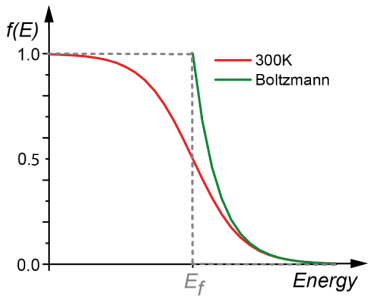

Figure 2.3: Plot of the Fermi distribution function with thermal broadening (red). The Boltzmann distribution function (green) approximate the Fermi function only at the high energy tail denoted as the Boltzmann tail.

2.2 Tunnel FETs

One of the most promising candidates for steep slope devices appropriate for low power electronics are Tunneling FETs (TFETs). The device structure of a TFET, as displayed in Figure 2.4, resemble that of the MOSFET with one significant difference. While in MOSFETs, source and drain are doped with the same dopant type, in a TFET, source and drain are oppositely doped. In equilibrium, this gated p-i-n diode forms a staircase-like band structure, as can be seen in Figure 2.5 for an n-type TFET. Similar to the

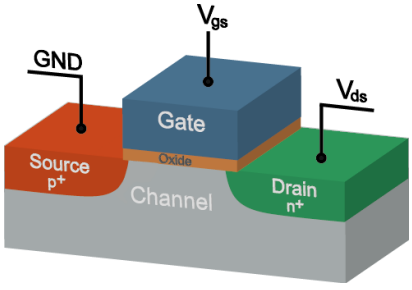

Figure 2.4: Device structure of an n-type TFET. Characteristic feature of such transistors is the opposite doping of source and drain.

n-type MOSFET, a positive V_{ds} is applied at the n-doped drain terminal to attract charge carriers from the source. When a positive V_{gs} is applied, an n-channel is formed below the gate moving the energy bands in the channel downwards. As soon as the conduction band of the channel moves below the valence band of the source an energetic overlap window is created allowing electron tunneling from the source to the empty states in the channel by band-to-band tunneling (BTBT). This energy overlap is denoted as the tunneling window $\Delta\Phi = E_V^{source}\text{-}E_C^{chan}$ with the narrow tunneling path resulting from the strong band bending. Since charge carriers within the tunneling window $\Delta\Phi$ can contribute to the total current only a distinct part of the Fermi distribution function is considered while the high and low energy tails are blocked by the source and channel bandgap. This band-pass like behavior is a distinct feature of TFETs and the reason why they can provide much steeper switching.

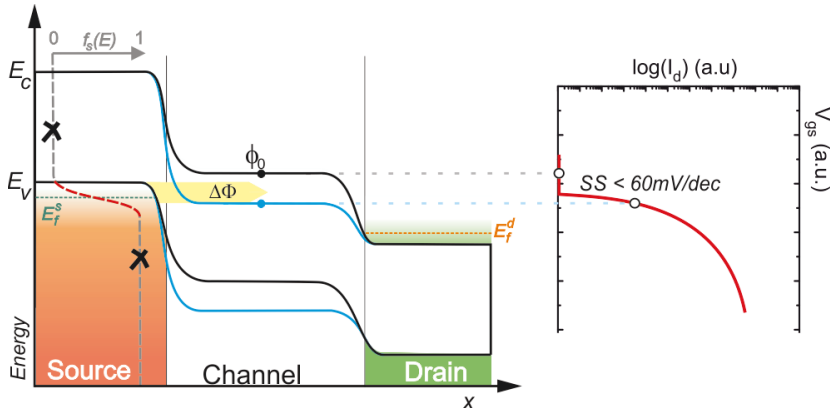

Figure 2.5: Illustration of the band profile of an n-type TFET. Increasing the gate voltage allows band overlap between source valence and channel conduction band edge. The bands in this overlap window is narrow enough to allow charge carrier tunneling. A steeper current increase is possible by this charge transport mechanism since the thermal tail of the Fermi distribution function is cut off.

2.2.1 Band-to-Band tunneling

The tunneling through a potential barrier is a quantum mechanical process. In classical mechanics, particles, such as electron, with energies lower than the potential barrier will not be able to reach the other side but instead are reflected back. However, in the domain of quantum mechanics, elementary particles can be treated as discrete plane

waves, a concept to fully describe quantum objects. This wave-particle duality allows the description of electrons as a wave function $\psi(x) = \psi_0 exp(ikx)$ which is able to penetrate and travel through the potential barrier. Here, ψ_0 is the amplitude of the wave, i the imaginary number and k stands for the wave number. For simplicity the tunneling process of a 1D plane wave is considered as depicted in Figure 2.6(a).

The time independent Schrödinger equation is applied, since it is assumed that the quantum mechanical system does not vary with time but only in spatial 1D direction:

$$\frac{-\hbar^2}{2m^*}\frac{d^2}{dx^2}\psi(x) + V(x)\psi(x) = E\psi(x) \tag{2.9}$$

with $\hbar = h/2\pi$ being the Planck constant, m^* the effective mass, $V(x)$ the function of the potential barrier and E the energy of the wave. Using the wave function in equation (2.9), an expression for k is obtained:

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}\big(E - V(x)\big)} \tag{2.10}$$

In case $E > V(x)$ we get a travelling wave with a constant amplitude and wavelength. Once the wave enters the potential barrier $E < V(x)$ the wave $\psi(x) = \psi_0 exp(-kx)$ decays exponentially. Note that the wavenumber k becomes imaginary within the potential barrier for $x\epsilon[0{:}\,d]$. The Wentzel-Kramers-Brillouin (WKB) approximation assumes that the spatial extent of $V(x)$ does not change rapidly in the x direction and must be larger than the incident particle wavelength. Thus the barrier can be approximated with infinitesimal wide rectangular potentials and a plane wave solution of the following form can be used:

$$\psi(x) = \psi(0)\exp\left(-\int_0^x \sqrt{\frac{2m^*}{\hbar^2}(V(x) - E)}\, dx\right) \tag{2.11}$$

The WKB tunneling probability $T_{WKB}(E)$ is defined by the ratio of the probability densities of the wave function $|\psi(x)|^2$ to the right and to the left of the potential barrier.

$$T_{WKB}(E) = \frac{|\psi(d)|^2}{|\psi(0)|^2} = \exp\left(-2\int_0^d \sqrt{\frac{2m^*}{\hbar^2}(V(x) - E)}\, dx\right) \tag{2.12}$$

For TFETs, the tunneling barrier between source and channel can be described by a triangular potential with a constant tunneling distance d which is independent of the energy E over the entire energy window $\Delta\Phi$, as shown in Figure 2.6(b). This leads to

a simple linear expression of $V(x) = x * \mathcal{E}e$ with $\mathcal{E}$ being the corresponding electric field and gradient of the potential barrier. From Figure 2.6(b) the tunneling distance can be expressed as $d = E_g/e\mathcal{E}$ and thus modifies equation (2.12) to [22]:

$$T_{WKB} = \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3\hbar\mathcal{E}e}\right) \tag{2.13}$$

In case a large V_{gs} is applied, the tunneling distance can be substituted by the screening length λ which describes the spatial extension of the depletion region within the n-i junction [23]. In general, λ is composed of λ_{dop}, considering the steepness of the doping profile at the source, and λ_{chan}, describing the length scale of the electrostatic potential which the gate bias can modulate. Hence, the electric field in equation (2.13) can be replaced with $\mathcal{E}e \approx (E_g + \Delta\Phi)/(\lambda_{dop} + \lambda_{chan})$ and the tunneling probability for TFET becomes:

$$T_{WKB} = \exp\left(-(\lambda_{dop} + \lambda_{chan})\frac{4\sqrt{2m^*}E_g^{3/2}}{3\hbar(E_g + \Delta\Phi)}\right) \tag{2.14}$$

This analytical expression shows that not only the gate voltage modulates the tunneling probability but also depends on the chosen device material and geometry. A reduction of the tunneling length implies an exponential increase of the BTBT transition probability and therefore of the BTBT current.

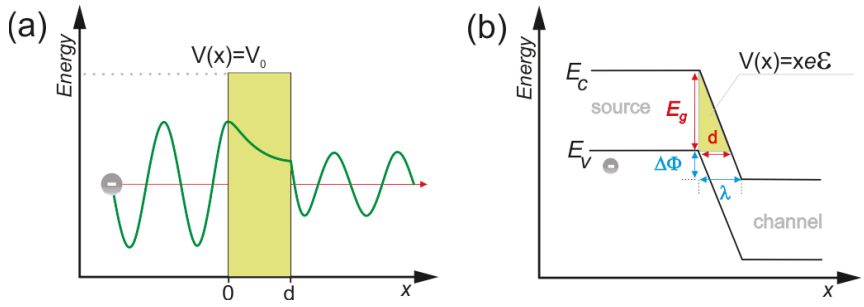

Figure 2.6: (a) Quantum mechanical tunneling of a plane wave through a potential barrier. The probability of penetration depends on the barrier thickness and height. (b) Approximation of the potential barrier in TFET with a triangular shaped barrier.

2.2.2 Subtrehsold characteristics of TFETs

In order to derive the inverse subthreshold slope for TFETs we can take the Landauer formalism in equation (2.1) with some modifications to calculate the tunneling current which is equivalent to the drain current I_d. For simplicity, we assume that a high drain voltage V_{ds} is applied so that the carrier injection from the drain side can be neglected. Charge transport can only happen within the energetic overlap window $\Delta\Phi = E_V^{source} - E_C^{chan}$ of the source valence and the channel conduction band (equal to the channel surface potential ϕ_0) with a transmission probability $T(E)$ given by T_{WKB} from equation (2.14):

$$I_d = \frac{2e}{h}\int_0^{\Delta\Phi} T_{WKB}\, f_s(E)\, dE \;=\; \frac{2e}{2} T_{WKB} F_s(\Delta\Phi)\,, \tag{2.15}$$

where $F_s(\Delta\Phi)$ is the primitive of the source Fermi distribution function [24]. Taking equation (2.4) into account, the subthreshold slope can be calculated as follow:

$$SS = \ln(10)\left(\frac{1}{I_d}\frac{\partial I_d}{\partial V_{gs}}\right)^{-1} = \ln(10)\left(\frac{1}{I_d}\frac{\partial I_d}{\partial \Delta\Phi}\mathrm{e}\right)^{-1}$$

$$= \frac{\ln(10)}{e}\left(\frac{1}{T_{WKB}}\frac{\partial T_{WKB}}{\partial \Delta\Phi} + \frac{1}{F_s(\Delta\Phi)}\frac{\partial F_s(\Delta\Phi)}{\partial \Delta\Phi}\right) \tag{2.16}$$

Note that ideal electrostatic coupling between gate and channel bands is assumed so that an one-to-one channel potential movement with the applied gate bias $\partial\Delta\Phi/(\partial V_{gs} e) = 1$ is enabled. The SS for TFETs in equation (2.16) depends on two terms where the first part stems from the variation of T_{WKB} with changing surface potential. A high tunneling probability for a small change in V_{gs}, ideally close to unity $T_{WKB} \approx 1$, is a necessary condition to enable high tunneling currents. The second part involving the primitive of the Fermi function at the source side $F_s(\Delta\Phi)$ with changing gate bias describes the amount of available electron charges at the transparent tunneling window $\Delta\Phi$. In order to achieve significant charge tunneling, the charge occupancy probability should be as large as possible. Thus, the Fermi distribution function has to be located relatively to the tunneling window so that the high Fermi energy tail is not exploited for tunneling (see Figure 2.5). Hence, an efficient tunneling barrier modulation alone is not sufficient for steep SS. In case the tunneling probability is close to unity, the first part of equation (2.16) can be neglected and a Taylor expansion of the integral function $F_s(\Delta\Phi)$ for small $\Delta\Phi$ to the first order leads to [25]:

$$SS \approx \frac{\ln(10)}{e} \Delta\Phi \ . \tag{2.17}$$

In contrast to MOSFETs, the inverse subthreshold slope for TFETs is insensitive to temperature in case the energy band pass filtering of the Fermi distribution function excludes the Boltzmann tail. Instead, the SS of TFETs has a linear dependency on the applied gate voltage since $\Delta\Phi \propto V_{gs}$. This is an interesting feature that should result in SS $<$ 60 mV/dec lower than the thermionic emission limit at low V_{gs}. Especially for small supply voltages V_{dd} the onset strength of TFETs is expected to outperform the slopes of MOSFETs [16]. However, SS indeed varies with V_{gs} resulting in a less steep slope for large biasing scheme. Thus, when extracting the non-constant slope, an averaged SS over several magnitudes in drain current can be helpful for comparison purposes.

From the derivation, the TFETs strength lies in the subthreshold regime. In the following, parasitic characteristics such as ambipolar behavior and additional current injection mechanisms are presented which degrade the subthreshold swing of TFETs in reality. These effects make it very challenging to obtain steep slopes in experimental TFETs. It is worth to mention that the following undesired effects which shadow off the steep BTBT transition are not necessarily independent of each other but rather occur simultaneously depending on the applied gate voltage.

2.3 Ambipolar switching behavior in TFETs

The term ambipolarity describes the current conduction for both positive and negative gate polarities which is an inherent property of symmetrical doped p-i-n structures as for TFETs. In Figure 2.7, the n-TFET becomes conductive for positive V_{gs}, V_{ds} (shown in blue) and reaches the OFF-state when the gate voltage is reduced. When a highly negative V_{gs} is applied, the bands in the channel move up and open a tunneling window at the channel and drain junction which induces a BTBT current (shown in red). Strictly speaking, due to ambipolar behavior, symmetrical doped TFETs can operate as both n-type and p-type device depending on the biasing scheme.

From the perspective of an n-type TFET, the current, denoted as p-branch, at negative V_{gs} in the I_d-V_{gs} characteristics represents the ambipolar current. The device reaches its minimum OFF-current within a voltage interval ΔV_{off} where BTBT occurs at neither of the junctions. According to the band structures in Figure 2.7, the gate voltage interval ΔV_{off} separating the n- and p-branches in the transfer characteristics can be estimated as follows:

$$\Delta V_{off} = \frac{1}{e}(\Delta B_s + \Delta B_d) - V_{ds}$$

$$\Leftrightarrow \quad e\Delta V_{off} = \left(E_C^{Chan} - E_V^S\right) + \left(E_C^D - E_V^{Chan}\right) - eV_{ds}$$

$$\Leftrightarrow \quad e\Delta V_{off} = E_g - (E_V^S - E_C^D) - eV_{ds} \tag{2.18}$$

with ΔB_s and ΔB_d being the energy needed to create a band overlap at the corresponding p-i or i-n junctions. Note that E_C^{Chan}-E_V^{Chan} equals the channel bandgap E_g. Equation (2.18) demonstrates that the voltage interval ΔV_{off} depends on the channel bandgap E_g, the applied V_{ds} as well as on the positions of the valence/conduction band of source and drain, respectively. In case the Fermi levels E_f at source and drain are located at the band edges the term $(E_V^{source} - E_C^{drain})$ becomes zero. However, ΔV_{off}

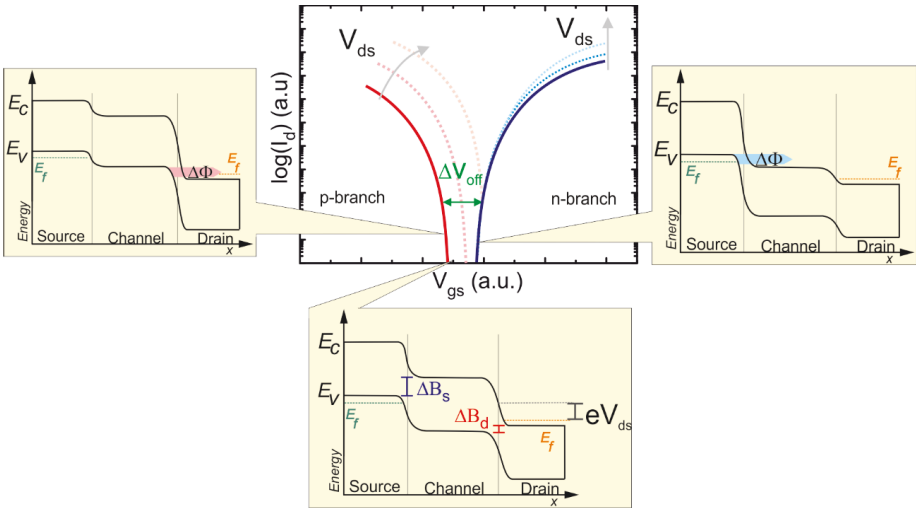

Figure 2.7: Schematic transfer characteristics of an n-TFET with symmetric dopant concentration at source and drain exhibiting current conduction not only for positive but also for negative V_{gs} denoted as ambipolar behavior. The corresponding band structure is depicted for both conducting cases and the OFF-state.

decreases for degenerately doped regions where E_f moves further into the bands. Especially for high V_{ds}, as depicted in Figure 2.7, ΔV_{off} reduces drastically since the bands at the drain are shifted down and allow an earlier set in of the ambipolar current for the same V_{gs}. Hence, n-and p-branches intersect with each other leading to increased leakage currents in the OFF-state. In general, ambipolar conduction is not desired as

a switching device for logic applications, instead a single and distinct threshold for ON/Off state is more adequate.

2.4 Trap assisted tunneling

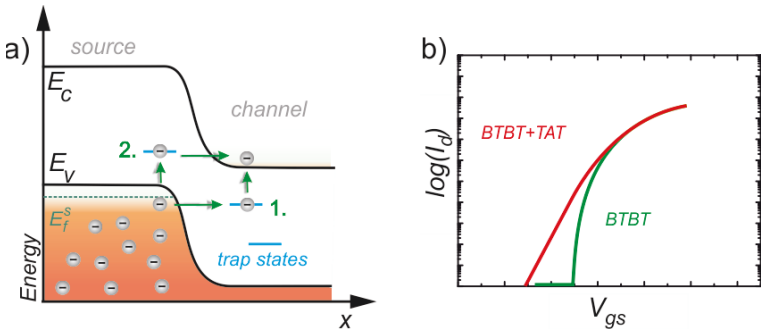

Figure 2.8: a) Trap states within the bandgap allow charge carriers to enter the channel even without tunneling window. Instead, charges tunnel to the trap states and reach the channel by thermal excitation. b) I_d-V_{gs} characteristics illustrating the subthreshold degradation when the undesired trap to conduction band tunneling masks the steep BTBT current.

The superior switching ability of TFETs only holds for the assumption when the band alignment blocks the charge carriers and permits large charge flow through the tunneling window. In reality, traps states are available within the bandgap reflecting the non-perfect crystal in the material. Usually in experimental TFETs additional lattice defects are introduced at the tunnel junction by ion implantation [26] or interface and border traps at the dielectric/semiconductor interface [27], [28] which increases the trap density. These traps allow charge carriers to enter the channel bands by the process of trap assisted tunneling (TAT), as illustrated in Figure 2.8(a). Charge carriers can occupy a trap state via tunneling followed by thermal excitation into the channel conduction band [29]. Note that the sequence may exchange so that both paths given in Figure 2.8 are possible. Since TAT is induced even before the tunneling window is established, the current in the transfer characteristics sets in at very small V_{gs} and obscures the subthreshold slope of the BTBT current, especially in the steepest current region (Figure 2.8(b)). Trap assisted tunneling for TFETs, as explained here, is very similar to the Poole-Frenkel mechanism, which is originally used to model field enhanced thermal excitation of carriers through traps in oxides [22]. The TAT current induced by Pool-Frenkel emission modified for TFETs is given as [22] [30]:

$$I_d^{TAT} \propto V_{gs} \exp\left[\frac{e}{k_B T}\left(2\sqrt{\frac{e(V_{gs}-V_{off})}{4\pi\varepsilon_0\varepsilon_{ox}d}}-\phi_B\right)\right] \tag{2.19}$$

where ε_0 stands for the vacuum permittivity, ε_{ox} the relative permittivity of the gate oxide, d the thickness of the gate oxide, V_{off} stands for the gate voltage where the current reaches the minimum and ϕ_B the potential barrier height which the charge carrier has to overcome to reach the channel. This parasitic current transport mechanism is temperature dependent since thermal excitation of charge carriers is involved [31]. Hence, for a high trap density at the tunnel junctions, the band pass behavior like switching diminishes. The high energetic Fermi tail of the distribution function, which is supposed to be blocked, increases the minimum SS of TFETs similar to MOSFETs.

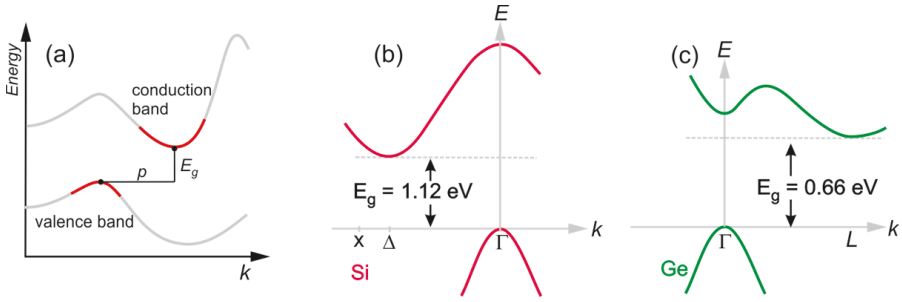

Figure 2.9: (a) Schematic valence band maximum and the conduction band minimum in indirect bandgap materials. In addition to the change in energy, inter band charge carrier transfer also requires the change in momentum by phonon-charge carrier interactions. (b) and (c) show the location of the band maxima/minima and their location in k-space for Si and Ge, respectively, adapted from [32].

2.5 Phonon assisted tunneling

Typical group IV semiconductors, such as Si or Ge, have an indirect band gap, where the valence band maximum and conduction band minimum are not located at the same crystal momentum in the reciprocal (or momentum) space (Figure 2.9). Thus, a BTBT process for these indirect semiconductors requires phonon interactions with tunneling charge carriers in order to satisfy the momentum conservation. Although the tunneling

probability is reduced because of this, the effect is disregarded at room temperature, where sufficient phonons are presumed to be present. However, electron-phonon scattering in general influences the TFET subthreshold performance since the energy of electrons might be increased. In case of Si, the main phonon assisted BTBT contribution stems from transverse acoustic phonons due to the highest occupation number where charge carriers can gain an energy of about 18.6 meV [33],[34]. At certain wave vectors close to the Δ-point, scattering with transversal optical phonons can lift the energy of charge carriers up to 63 meV [35],[36]. This has severe effect when traps are available in the bandgap enabling BTBT even before an energetic overlap window between source and channel is created. Simulation modules of Ref. [37] also show increased OFF-current even without the presence of traps due to possible inter band transition by phonon scattering alone. Additionally, phonon occupation increases with higher temperature which leads to temperature dependent subthreshold characteristics. Even though, the SS of TFETs degrades with phonon scattering involvement, SS below 60 mV/dec should be possible [37]. The slope is limited due to the high trap density which creates high charge carrier capture rates to an extent that the resulting leakage current may exceeds the BTBT current.

2.6 Shockley-Read-Hall recombination/generation

Recombination process of an electron in the conduction band with a hole in the valence band via a trap state is referred to as Shockley-Read-Hall recombination [38], [39]. These trap states are located within the bandgap. For indirect semiconductors this non-radiative transition process is more likely than direct recombination since the energy difference to a trap state is smaller. The energy release of the charge carriers after this process is transferred in form of lattice vibrations. The electron-hole pair recombination/generation rate R_{SRH} is described by [39], [22]:

$$R_{SRH} = \frac{np - n_i^2}{\tau_p \cdot (n + n_1) + \tau_n (p + p_1)} \tag{2.20}$$

with the auxiliary variables n_1 and p_1 defined by:

$$n_1 = n_i \, exp\left(\frac{E_T - E_F}{k_B T}\right), \qquad p_1 = n_i \, exp\left(\frac{E_F - E_T}{k_B T}\right) \tag{2.21}$$

where n and p stands for the carrier density, τ_n and τ_p are carrier lifetimes of electrons and holes, respectively. The intrinsic carrier density n_i can be expressed as:

$$n_i = \sqrt{N_C N_V}\, exp\left(-\frac{E_g}{2k_B T}\right) \tag{2.22}$$

where N_C and N_V are the density of states in conduction and valence bands, respectively. Note that the sign in equation (2.20) determines either a net recombination or generation rate. R_{SRH} reaches its maximum, when the energy of the traps states $E_T = E_F$ are equal to the Fermi level of the intrinsic semiconductor. This indicates that traps with energies near the mid-gap region are effective recombination centers.

For TFETs, SRH occurs mainly in the channel of the device which is usually intrinsic. However, for positive drain voltages, electrons and holes tend to flow to the n-doped drain and p-doped source as shown in Figure 2.10(a). The R_{SRH} recombination/generation rate is no longer in equilibrium. A net generation rate of charge carriers is dominating, since n and p are reduced in the channel changing the sign of equation (2.20). This parasitic current limits the minimum achievable current leakage current of TFETs in the OFF-state. Figure 2.10(b) depicts schematically the increase of I_{off} which further deteriorates with increasing V_{ds}. Considering equation (2.22), the generation rate also depends on the bandgap E_g so that the leakage current based on SRH is even more pronounced for small band gap materials.

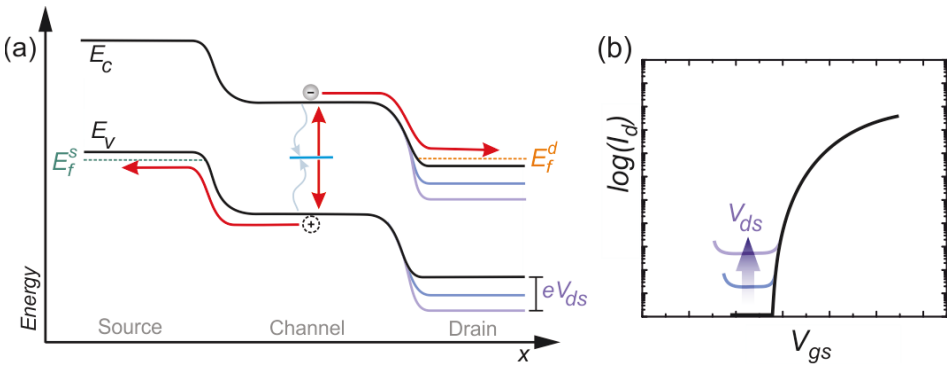

Figure 2.10: (a) Schockley-Read-Hall charge carrier generation dominates in the channel of the n-TFET in reverse bias condition of the p-i-n band structure. (b) This resulting leakage current degrades the I_d-V_{gs} characteristics in the OFF-state due to increased leakage current floor, which is more pronounced for higher V_{ds}.

2.7 Output characteristics

2.7.1 MOSFETs

In MOSFETs the output characteristics I_d-V_{ds} are typically characterized by two regimes: the linear and saturation regime of the drain current I_d. For a high gate voltage, which surpass the threshold voltage $V_{gs} > V_{th}$, inversion charges accumulate below the gate terminal. This lowers the channel barrier to the point where the conduction band edge is below the Fermi levels of source and drain. From both terminals, charge carriers are emitted thermally over the remaining barrier to the channel. As can be seen in Figure 2.11, a net current starts to flow linearly with increasing V_{ds} pushing the bands of the drain down. As long as $0 < V_{ds} < V_{gs} - V_{th}$ is fulfilled, I_d is in the linear regime, where the drain Fermi level is larger than the channel conduction band. The current flow is proportional to the difference of the source and drain Fermi level $I_d \propto E_F^S - E_F^d$. Further increase of $V_{ds} > V_{gs} - V_{th}$ shifts the drain Fermi potential below the channel conduction band and creates a pinch-off region near the drain. Charge carriers stemming from the drain become negligible since occupation of the high energy states of the drain Fermi function decreases exponentially. As a consequence, the current flow reaches its maximum for a fixed V_{gs} and does not increase with V_{ds} but keeps constant. Larger saturation currents can be achieved for increasing the gate voltage giving rise to a larger fraction of the source Fermi function contributing to the current.

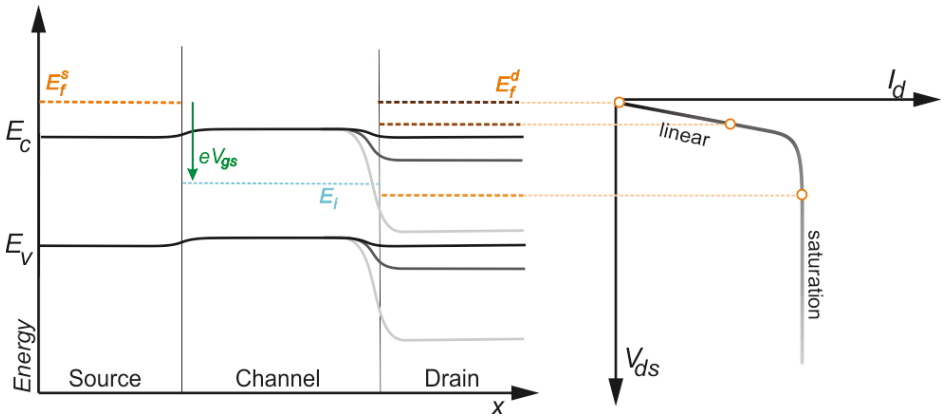

Figure 2.11: Band profile along the direction of current transport illustrates the I_d-V_{ds} characteristics of an n-MOSFET. At a high constant gate voltage the channel barrier is greatly reduced so that current in the output characteristics increase linearly and saturates with increasing V_{ds}.

2.7.2 TFETs

The main difference of the output characteristics for TFETs is that it may exhibit an exponential onset at low drain voltage instead of the linear onset as for MOSFETs [23][40]. This non-linear behavior is not desired since the set in of the saturation regime is shifted to larger V_{ds} which degrade circuit applications, e.g. inverters. The reason for the exponential onset is depicted in Figure 2.12. Driving the device into the ON-state with a larger V_{gs} leads to charge inversion in the channel where most charges stem from thermal injection rather from the drain than from the small tunneling current originating from the source. When the drain bias increases, charge flows back to the drain and reduces the inversion charges in the channel. Consequently, the screening of the gate potential relaxes and the channel bands move down. As a result the channel potential changes and so does the tunneling window for small V_{ds} causing an exponential current increase [41][42]. This is an intrinsic property of the p-i-n structure of TFETs and is referred as drain-induced-barrier-thinning (DIBT) which is not related to short channel effects. The current begins to saturate for a drain bias $V_{ds,sat}$ which sets the drain Fermi potential below the channel conduction band so that the energetic tunneling window reaches its maximum value defined by $E_f^s - E_c^{chan}$ instead of $E_f^s - E_f^d$.

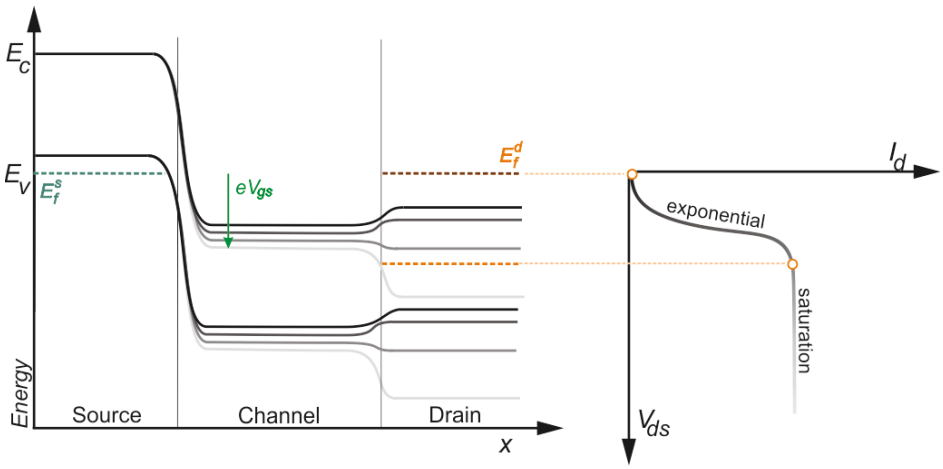

Figure 2.12: The output characteristics of TFETs is characterized by an exponential onset at low V_{ds}. At high V_{gs} the inversion charge mainly comes from the drain terminal which decreases with increasing drain voltage. As result, the drain bias has an impact on the channel bands and thus influences the tunneling window at the source/channel interface.

One possible way to suppress the exponential onset is to scale down the device towards the quantum capacitance limit (QCL), where the inversion charge concentration is reduced due to limited density of states (DOS) in 1D structures, e.g. carbon nanotube TFETs [43][44]. This weakens the screening effect created by the charges from the drain and allows the channel bands to follow the applied gate bias. A more practical way to attain the linear onset for TFETs is to increase the source doping. Strong degenerately doped source provide a narrow depletion region at the source-channel transition which is less sensitive to small changes in the channel band position and thus reduces DIBT [41][45][46]. However, too high source doping shifts the Fermi distribution function further into the valence band. Consequently, the source-channel tunnel window lies within the exponential tail of the Fermi function (decrease the charge carrier occupancy probability, see Equation (2.16)). In this case the minimum SS of TFET devices is constrained to 60 mV/dec as for MOSFETs [47]. Thus, there is a trade-off for choosing the right source doping concentration to enable a linear onset and without sacrificing steep slopes.

A further typical feature inherent to output characteristics of TFETs, is the unidirectional conduction depending on the applied drain voltage. In contrast, the source and drain of a MOSFET are exchangeable due to the fact that they have the same doping type. The same drain bias can be applied in either terminal while the other is grounded resulting in the same output characteristics. TFETs, however, only operate as desired in the reverse bias condition[2]. Swapping the bias condition by applying ground to drain and high potential at source results in forward biasing the p-i-n diode. In this operation, the gate has basically no impact on the current in the output characteristics and it behaves essentially as a forward biased diode [48]. This remarkable characteristic of TFETs needs to be considered and requires additional effort in respect respect of CMOS like circuit design.

[2] Terminology originate from p-n diodes, i.e. n-doped drain at a higher potential than p-doped source.

3 Design aspects to improve Si-TFET peformance

In the previous chapters the theoretical switching mechanism of TFETs has been discussed, especially in the subthreshold regime. With the potential to break the 60 mV/dec limitation, TFETs gain a lot of interest as a promising concept for reduced power consumption in analog and digital CMOS circuits. Lead by this ambition, many groups succeeded in the past decade to fabricate TFETs with different device structures showing evidence of sub-60 mV/dec switching operation. Some of them are summarized in Table 3.1.

Table 3.1: Experimental TFET characteristics with different structures featuring minimum point SS < 60mV/dec measured at the listed V_{ds} and I_d from the literature.

Device structure	SS_{min} [mV/dec] @ (V_{ds}, I_d)	Reference
SOI p-TFET	42 (-0.1V, 0.1pA/µm)	*Mayer 2008* [49]
Silicided-source p-TFET	46 (-1V, 0.1pA/µm)	*Jeon 2010* [50]
Mulit-gate SOI p-TFET	46 (-0.1V, 0.1pA/µm)	*Leonelli 2010* [51]
Vertical Si-NW p-TFET	30 (-0.1V, 0.1pA)	*Gandhi 2011* [52]
Strained SiGe/SOI p-TFET	33 (-0.1V, 0.1pA/µm)	*Villalon 2012* [53]
SOI n-TFET	53 (0.1V, 1nA/µm)	*Choi 2007* [15]
Double-gate strained Ge heteroj. n-TFET	50 (0.5V, 1pA/µm)	*Krishnamohan 2008* [54]
Ge-source/Si heteroj. n-TFET	40 (0.5V, 1pA/µm)	*Kim 2009* [55]
III-V heteroj. n-TFET	57 (0.05V, 1nA/µm)	*Dewey 2011* [56]
III-V/Si heteroj. n-TFET	21 (0.1V, 1pA/µm)	*Tomioka 2012* [57]
Strained Si Trigate NW n-TFET	30 (0.1V, 0.2pA/µm)	*Knoll 2013* [19]

The transfer characteristics of the corresponding TFETs are shown in Figure 3.1. This overview reflects the common trend of today's experimental TFETs exhibiting rather poor ON-current performance compared to MOSFETs. Although, extracted SS values have been experimentally demonstrated down to 21 mV/dec [57] at room temperature, the related current levels are very low, some of them even well below the minimum operating current of 10 pA/µm indicated by ITRS for low standby power applications [2]. As discussed in [58] ,TFETs should provide SS with sub-60 mV/dec up to a current of 1 to 10 µA/µm at $V_{ds} \leq 0.5$ V to be considered as attractive and competitive with MOSFETs.

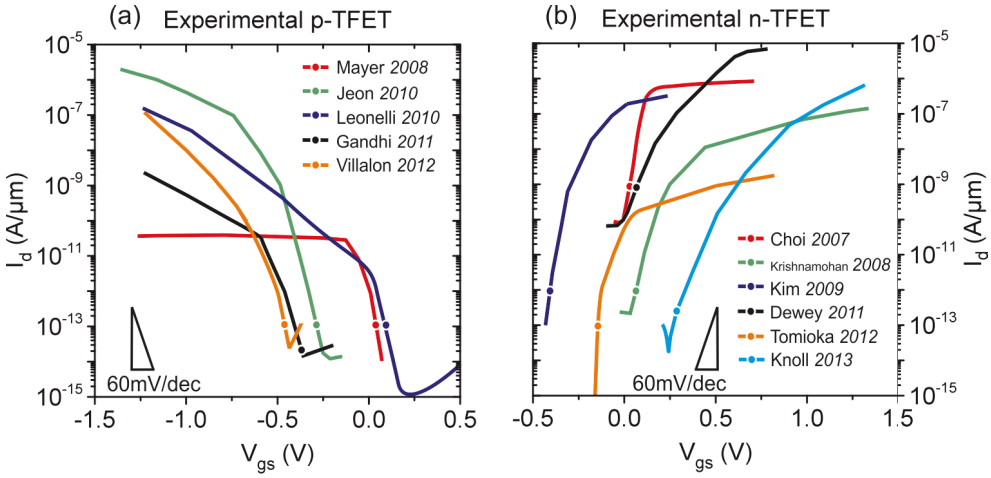

Figure 3.1: Transfer characteristics of published TFETs listed in Table 2.1 separated in (a) p-TFETs and (b) n-TFETs. The circle indicates the measured minimum point SS.

A smart design strategy should be implemented in order to achieve the full performance of experimental TFETs which should exhibit an inverse subthreshold slope smaller than 60mV/dec over many orders of magnitudes and high I_{on}. Both of these desired properties are directly linked to the transmission probability described by the WKB approximation given in equation (2.14) where the key parameters can be deduced. Considering that the tunneling probability $T_{WKB} \rightarrow 1$ is targeted, the band gap E_g, effective mass m^* and screening length λ need to be scaled. The first two parameters are semiconductor material specific while the last parameter is defined by the gate electrostatics and the dopant concentration gradient at the source. Low and direct band gap materials as III-V are favorable, e.g. InAs, InGaAs, that result in TFETs with high tunneling currents [56]. In addition, III-V heterostructure can provide different band alignments, e.g. staggered, or even broken band offsets to allow tunneling

currents at much smaller V_{gs}. However, so far many experimental results based on these materials show rather poor I_{on}/I_{off} ratio which is mainly due to the increased OFF-current caused by the small bandgap [59]. Furthermore, non-optimized gate stacks result in high trap densities at the oxide interface of III-V TFETs. This leads to high gate leakage currents [60] and also degrades SS due to trap induced tunneling [56]. In long term, improvements can be expected in terms of better electrostatics [61] and eventually fully integration of p-and n-devices in the CMOS-technology [60][62].

In contrast, TFETs based on the most well-known group IV semiconductor, Si, generally show lower ON-currents [49]. This is consistent with the theoretical predictions, since Si has larger indirect bandgap with higher effective masses than III-V materials. Although Si seems less attractive for TFETs, many experimental results have been successfully conducted on Si TFETs (see Table 3.1). In several benchmarks such as I_d vs. SS [60][63], or the comparison of I_{on}/I_{off} ratio [59], Si based TFETs are still listed among the best. The most relevant advantage of Si TFETs is the access to the most mature technology already developed for MOSFETs. The exploitation of several technology boosters such as thin fully depleted Si on insulator (FDSOI) [15], strain engineering [64] or the application of SiGe compounds [65] are some possibilities to improve electrostatics, E_g and m^*. Also hetero structure designs with Si(Ge)/Ge are considered to narrow the bandgap in the tunneling region [55]. Especially with the development of GeSn [66] and SiGeSn [67], direct bandgaps can be established in distinct locations of the device. Thus, bandgap engineering has grown in variety for group IV semiconductors. A further advantage of Si TFETs is the easier processing of p- and n-type devices on the same chip which allows faster adaption to CMOS circuit applications with TFETs. In the next chapters, essential building blocks and several technology boosters applied in this work will be presented in detail to emphasize their relevance for TFET improvement. In addition, experimental results of the corresponding device modules are presented and analyzed with respect to the TFET device applicability.

3.1 Strained Si

Although research in strain technology started in the 1950s [68], the first commercial application of strain as booster along with scaling of MOSFETs began with the 90 nm node technology mainly to increase carrier mobility in the channel [4]. For the improvement of all-Si TFETs tunneling current, strain engineering is an effective approach to reduce $m^*$and especially E_g, making Si more competitive compared to low band gap materials. These parameters are tuned by altering the Si crystal symmetry by applying

strain which in result manipulates the band structure. In general, strain can be applied locally via stressors directly on transistors or applying global stress techniques, which produce a uniform strain throughout the layer before device fabrication. A very common way to apply global strain to the Si layer is to utilize strain-induced substrates with hetero epitaxy. For instance, when a thin Si layer is grown pseudomorphically on a thick strain-relaxed SiGe virtual substrate, the in-plane lattice constant of Si will adapt the lattice to the underlying SiGe layer. As consequence, the Si layer becomes in-plane biaxial tensely strained. Depending on the Ge content x of the $Si_{1-x}Ge_x$ layer, the tensile strain value can be increased with higher Ge content. Hence, the percentage of strain within the Si layer is determined by the resulting lattice mismatch:

$$\varepsilon_{biax,strain} = \frac{a_{SiGe} - a_{Si}}{a_{Si}} \tag{3.1}$$

where the lattice constant a_{SiGe} of the SiGe alloy is linear interpolated by Vegard's law:

$$a_{SiGe} = a_{Si}(1 - x) + a_{Ge}x \tag{3.2}$$

However, the strain can only be preserved up to a certain layer thickness which is determined by the lattice mismatch [69]. Going beyond this critical thickness it is more favorable for the system to form misfit dislocations at the Si/SiGe interface [70]. This, in turn, leads to strain relaxation of the Si layer.

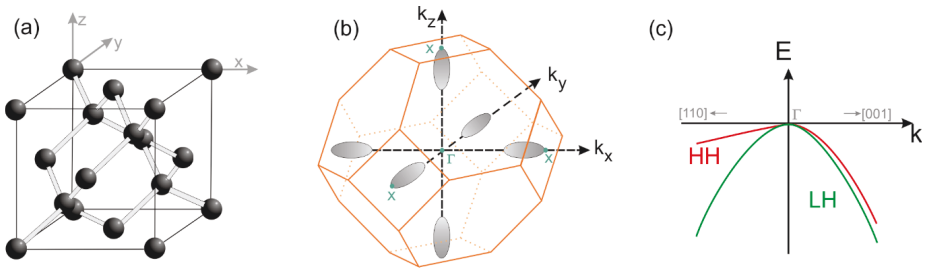

Figure 3.2: (a) depicts the primitive diamond cubic cell of unstrained Si. The primitive cell in the reciprocal space is shown in (b), including the Δ6 ellipsoids of constant energy of the conduction band minimum at all axis directions. (c) The two-fold degenerated valence band is composed of the heavy hole band (HH) with a weak curvature and the light hole band showing a more pronounced curvature.

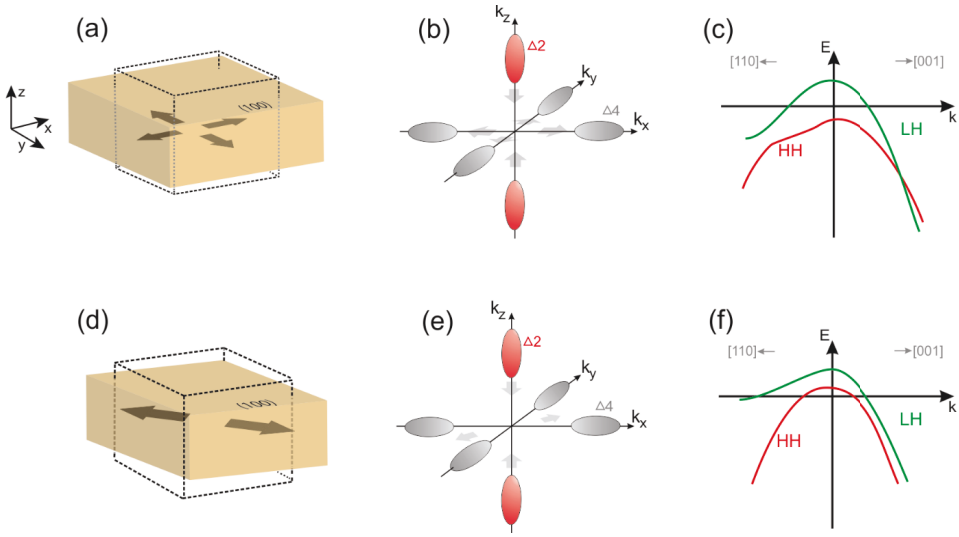

Figure 3.3: (a) Biaxial tensile and (d) uniaxial tensile strain along [110] direction on a cubic crystal leading to sub-band splitting of the conduction band (b), (e), from Δ6 valleys into Δ4 and Δ2 valleys, respectively. (c), (f) the LH band lifts accordingly. (c) and (f) is based on [71] and [72].

In order to obtain strained Si on insulator (sSOI), the commercially most relevant process is the SMART Cut technique [73]. Here, the strained Si grown on a SiGe/Si donor wafer is bonded on a new wafer which has a SiO_2 passivated surface. Subsequently the SiGe buffer layer is removed such that only the sSOI remains.

The crystal structure of unstrained Si is composed of periodic arrangement of diamond cubic cells, the so called primitive cell of Si (Figure 3.2(a)). By using the tight binding model [74] the crystal lattice can be translated in the reciprocal space k resulting in a band constellation as shown in Figure 2.9(b) for Si. Considering all three crystal directions, the reciprocal space of the Si diamond lattice is depicted in Figure 3.2(b). This primitive cell in the reciprocal space is denoted as the 1. Brillouin zone (1.BZ), which contains all relevant energy bands to describe charge transport in FETs [22]. The conduction band minimum is located at the Δ-symmetry line close to the x- point. Since symmetry of the direct cubic lattice[3] is also reflected in the 1.BZ, the conduction band minimum is present in all six directions of the reciprocal space. This leads to a six-fold (Δ6) degeneracy of the conduction band minimum simplified as constant energy ellipsoids, named as valleys (Figure 3.2(b)). The Γ-point, where the maximum valence band for Si is located, lies in the center of the 1.BZ ($k_x = k_y = k_z = 0$). At this point two bands, the light hole (LH) and the heavy hole (HH) bands overlap

[3] The Si cubic cell has 6 equal surfaces. Electron travelling in any of them experience the same electrical property (isotropic electron transport).

for the same energy, thus the valence band is two-fold degenerated (Figure 3.2(c)). The name of the bands corresponds to their effective mass m^*. Note that the physics of strain induced valence band modification is rather complex due to the anisotropic property. Because of that, Figure 3.2(c) only consider the LH and HH bands in [001], the crystal axis direction, and the [110], the x-y in-plane direction. For holes or electrons, the effective mass is obtained using a parabolic band model to approximate the dispersion relation $E(k)$ along different directions around the conduction band minimum or valence band maximum. The resulting parabolic curvature is inverse proportional to the effective mass m^*:

$$m^* = \frac{h^2}{(2\pi)^2}\left(\frac{d^2E}{dk^2}\right)^{-1} \tag{3.3}$$

Since (100) Si wafers are exclusively used in this work for device fabrication, the following discussion will only cover the biaxial and uniaxial tensile strain along [110]-direction which corresponds to the channel direction. The effect of strain on the symmetry properties of the Si crystal can be illustrated by its effect on a cube which reflects the same symmetry as the Si crystal unit cell. For biaxial tensile strain, as shown in Figure 3.3(a), symmetric tension is only applied in-plane (x-y) increasing the area but shorten the lattice in z-direction due to volume conservation. This breaks the lattice symmetry between x-y plane and z-axis resulting in a splitting of the six-fold degenerated Δ6 valleys into Δ4 and Δ2 valleys [75] [71]. The separation in energy of these levels allows a repopulation of electrons of the lower energy Δ2 valleys which

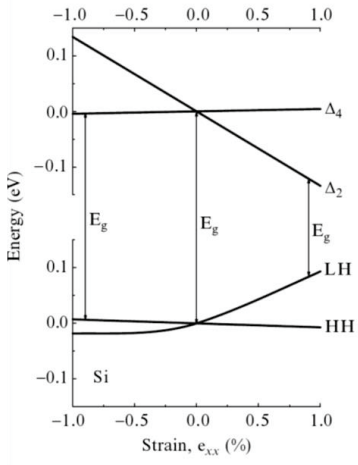

Figure 3.4: Calculation of band gap narrowing based on the applied biaxial strain on Si. Negative strain values imply compressive while positive tensile strain. Taken from [76].

provide smaller m^*[4]. For the valence band biaxial tensile strain also lifts up the band degeneracy. In addition, band warping is greatly pronounced for the valence band changing $m^*$of the HH and LH bands. According to the calculation in [71], the stronger warped LH band is lifted up in energy compared to the HH band yielding a smaller hole effective mass. In case of uniaxial strain along the [110]-direction the result is similar to the biaxial case in terms of band splitting for the conduction [64] as well as in the valence band [72]. The main difference between these two strain types is that the x-y plane is no longer a square instead it has a shape of a rhombus. It is assumed that the crystal symmetry of diamond structures is more distorted for uniaxial strain applied at such diagonal axis, hence, results in greater band warping [71]. This has been experimentally verified by measuring the mobility enhancement at high uniaxial stress [77].

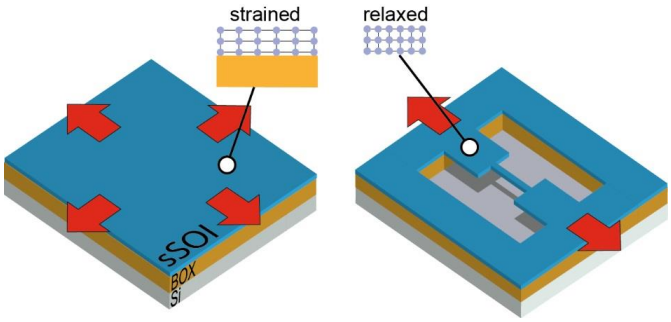

Figure 3.5: Concept with large pulling pads realized on a pre-strained SOI layer to introduce high uniaxial strain along NWs. The inset schematically shows the relaxation of the Si lattice when the buried oxide is removed.

An overview of the relative shift of the conduction and valence bands is given in Figure 3.4 showing band gap narrowing for increased biaxial tensile strain in Si. The resulting bandgap is determined by the difference of the $\Delta 2$ conduction band valleys and the LH valence band. This also holds for uniaxial tensile strain where increased stress showed a reduction of the threshold voltage in MOSFETs [78]. Based on the present findings the biaxial tensile strain creates larger band shifts as compared to the uniaxial tensile strain for the same strain values [79]. In terms of TFETs, high biaxial tensely strained Si would be a better choice. However, as presented above for global strain techniques, a trade-off between high strain values and defect concentration limits the continuous strain extension. Instead, uniaxial strain techniques are more appropriate in applications aiming for higher strain values beyond 1% [80]. All in all, both

[4] Assuming that current transport is in parallel to the x-y plane. The $\Delta 2$ valleys provides the strongest curvature and hence smaller effective mass for charge transport.

strain types presented here are boosting the TFET performance due to band splitting induced bandgap reduction. In addition, the effective mass is reduced compared to unstrained Si as long as the sub-band splitting in the corresponding valence and conduction band is large enough, such that most charge carriers occupy the first sub-band ($\Delta 2$ for electrons and LH for holes). It has been verified that strain enhances currents on devices that relies on tunneling through a barrier [81].

3.1.1 Introducing high uniaxial strain in NW-array structures

One way to introduce large strain in devices with nanowire (NW) architecture is the employment of the so called dumbbell shaped bridge concept on biaxial pre-strained SOI substrates [82]. The narrow NW is located in between two larger pads, as depicted in Figure 3.5. Releasing the underlying buried oxide (BOX) of the entire bridge (NW and the pads) structure by HF wet-etch is the key to enhance the strain along the NW. As a result the tensile strained atomic lattice tends to relax such that the larger strain pad generates a great pulling force at both sides of the narrower NW. In addition, the initial biaxial tensile strain in the centered NW converts into uniaxial strain uniformly along the wire due to anisotropic relaxation of the perpendicular strain component [83]. Depending on the geometrical dimensions of the bridge structure, the resulting longitudinal strain in the NW can be adjusted. Successful integration of uniaxial tensile strain up to 4.5 % (7.6 GPa) on Si NWs [82] and 3 % on Ge NWs [84] have been demonstrated with this approach. Moreover, this concept allows the optimization of NW TFETs. Therefore, we adapt the concept and investigate its feasibility in our fabrication process. A scanning electron microscope (SEM) image of the suspended NW bridge including the large pulling pads is depicted in Figure 3.6. Different NW and pad dimensions have been considered to gain a better understanding of the strain adjustment in this structure. A simplified calculation of the expected strain is given in [82] based on the dimensions of the bridge but neglect the material properties.

Raman spectroscopy has been performed on the entire NW bridge to characterize the resulting elastic strain. This non-destructive investigation approach relies on the interaction of incident photons, usually from a laser source, with matter giving information about the potential excitement states like oscillation- and rotation states of the molecules in the considered material system. Due to the induced strain enhancement, the lattice constant is altered and thus also the excitement states. This leads to a frequency shift of the backscattered photons. A specific Raman spectrum where only the Raman scattering intensities are plotted against the wavenumber (inverse of the wavelength) of the NW bridge with two distinct peaks is shown in Figure 3.7(a). The

high intensity peak in green belongs to the large pads indicating almost complete relaxation since the wavenumbers are located close to the value of unstrained Si bulk with 520 cm^{-1} [85]. In contrast, the Raman line of the 20 nm wide NW shifts down to smaller wavenumbers of about 508 cm^{-1}. Based on the Raman shift $\Delta\omega$ (wavenumber difference between strained and unstrained Si), the strain ε_{uni} along the NW is calculated with the following semi-empiric equation from [82]:

$$\varepsilon_{uni} = \frac{\Delta\omega}{3.27\ \mathrm{cm}^{-1}} \tag{3.4}$$

The larger the shift toward smaller wavenumbers the greater is the uniaxial strain. On each bridge structure multiple measurements at various power down to 2 mW were done in order to cancel out local heating effects caused by the laser which might alter the strain. Figure 3.7(b) shows an overview of different bridge configurations at constant NW (500 nm) and pad length (600 nm). All measured NWs independent of the dimensions exhibit a larger tensile strain than the initial strain of 0.8 % in the biaxial strained SOI layer. While a clear trend can be seen with smaller NW width, a more significant impact on the strain enhancement stems from the pulling pad width variation. This is because of the larger cross section ratio between the pads and the NW generating more force per area. According to deformation potential theory calculations in [79], the bandgap reduction in Si induced by uniaxial strain along [110] direction is described with ΔE_g = -6.19* ε_{uni}. The largest strain value of about 3.5 % has been achieved which corresponds to a bandgap reduction of the Si NW of ΔE_g= -0.22 eV. Hence, a successful introduction of such high strain in Si TFET process would greatly benefit the tunneling current performance.

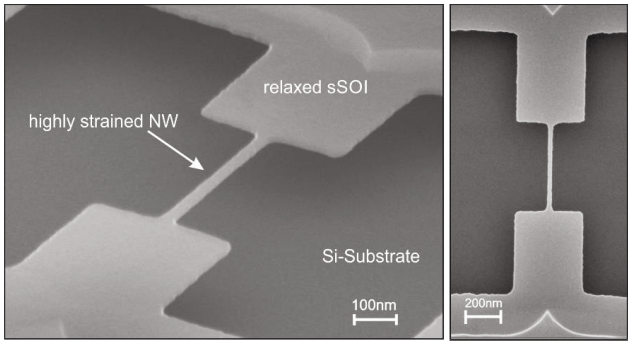

Figure 3.6: SEM image of a free-standing NW bridge structure with a constant sSOI thickness of 10nm. The narrow, highly strained NW has a width of 20nm and a length of 500nm, whereas the relaxed pads has a width of 400nm and length of 500nm.

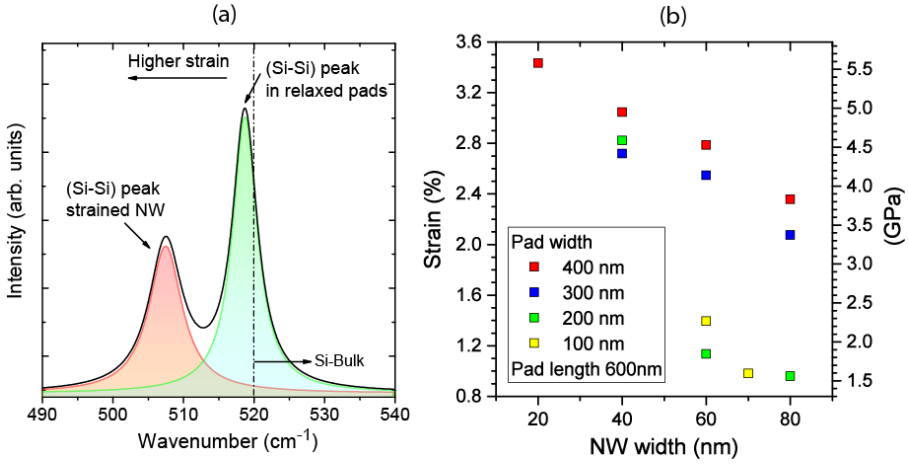

Figure 3.7: (a) Raman spectrum of a strained NW with 20nm width and 500nm length in between relaxed pulling pads with the area of 400x600 nm² each. (b) Overview of the extracted strain results depending on the NW width and applied relaxed pulling pad width.

3.2 High-*k* and metal gate stack

The gate switching capacity is the core component of TFETs since it shifts the energy bands at the oxide-channel interface in order to control charge carrier tunneling. How well the band movements are efficiently transferred for a given change in gate voltage depends on the characteristics of the metal-oxide-semiconductor (MOS) system. Considering that TFETs should operate at small supply voltage swings, an efficient coupling between gate and channel is crucial to obtain sub-60 mV/dec slopes. For long decades the MOS technology used thermal oxidization to create native SiO_2 as gate oxide. This is justified by a perfect atomic structure between these material types enabling low trap concentrations between the SiO_2/Si interface. Otherwise, the resulting dangling bonds raise the decay time of the switching and thus enhance additional parasitic capacitance to the system admittance. Furthermore, high density of interfacial traps is detrimental for TFETs since they promote trap assisted tunneling [29]. A key requirement is that the gate voltage should mainly drop over the oxide such that a high oxide capacitance C_{ox} is achieved. For a classical planar device the capacitance resembles a plate capacitor which is defined:

$$C_{ox} = \varepsilon_0 \varepsilon_{ox} \frac{A}{d} \tag{3.5}$$

where ε_0 is the vacuum permittivity, ε_{ox} the relative permittivity of the oxide, d its thickness and A the area of the capacitor. Increasing the area to reach the goal is out of question because of switching speed degradation[5], hence, a large capacitance per area is needed. Therefore, scaling down the oxide thickness was the main attempt in the past to achieve this. However, when the SiO_2 thicknesses had approached 1.5 nm the insulator properties were no longer reliable [86]. Instead, gate leakage current increased exponentially with decreasing oxide thickness mainly caused by charge tunneling through the thin oxide layer.

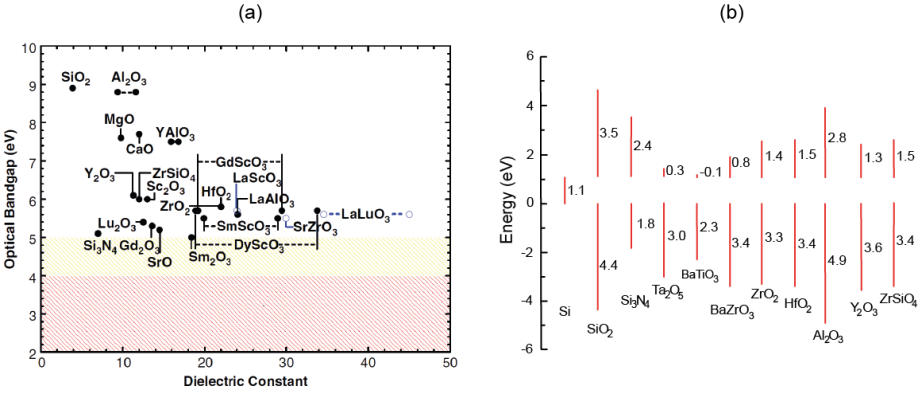

Figure 3.8: Overview of various high-k dielectrics showing (a) the optical bandgap in dependence of dielectric constant, taken from [87], and (b) the conduction- /valence band offsets compared to Si, extracted from [88].

High-k dielectrics as alternative oxide replacements provide a relative permittivity ε_{high-k} greater than SiO_2 (ε_{SiO_2}=3.9). This relaxes the constraint for extremely thin gate oxides since a higher permittivity allows larger physical thicknesses without lowering the specific capacitance. The concept of equivalent oxide thickness (EOT) is a convenient measure for comparing the thicknesses of oxides with different dielectrics:

$$EOT = d_{SiO_2}^{eff} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} d_{high-k} \tag{3.6}$$

It simply translates a certain high-k oxide thickness into a thickness that a layer of SiO_2 would have to achieve the same C_{ox}. Therefore, in order to pursue EOT scaling, switching to high-k dielectrics is mandatory. It has been shown that thin oxides with

[5] The time for charging up a capacitance is proportional to the area of the capacitor.

large k values improves SS and the overall tunneling current for TFETs [89]. However, only considering the relative permittivity value is not sufficient since many high-k materials also reveal low energy offsets between the energy bands [90]. Typically, bandgaps larger than 5 eV and band offsets with at least 1 eV with respect to the conduction and valence band are necessary to suppress electron/hole leakage. An overview of the high-k dielectrics emerged from research is shown in Figure 3.8. One of the most prominent and most applied among them is Hf oxide providing k~20 [91]. The combination with metal gates such as TiN or TaN is favorable over polycrystalline-Si as it avoids further parasitic capacitances caused by depletion formation within the poly-Si gate itself.

3.2.1 Gate stack characterization based on TiN and HfO_2

HfO_2 in combination with TiN is the main gate stack for the device fabrication in this work. In the following, MOS capacitor structures are measured to evaluate the gate performance in terms of capacitance, leakage current and density of interfacial traps D_{it}. In this regard, 3 nm HfO_2 was deposited by atomic layer deposition (ALD) on RCA[6] cleaned p-type Si(100) samples followed by 60 nm TiN from atomic vapor deposition (AVD) on top of the dielectric. After patterning and dry-etch, the structures were annealed at 400 °C for 10 min in N_2 (96%) and H_2 (4%) atmosphere. The results of the C-V measurements are shown in Figure 3.9(a). Normalized accumulation capacitance of about 2.15 µF/cm² has been obtained at f=100 kHz taken from gate voltage $V = V_{flat} - 1$ V, where V_{flat} is the flat band voltage determined by the maximum of the second derivative of $1/C(V)^2$ [92]. Based on the measured accumulation capacitance C_{acc}/A averaged over several samples an EOT of 1.2 to 1.6 nm is roughly estimated by calculating the capacitance equivalent thickness (CET) and subtracting the quantum mechanical correction in Si [91][93]:

$$EOT \approx \frac{\varepsilon_0 \kappa_{SiO_2} A}{C_{acc}} - 0.4\,\text{nm} = CET - 0.4\,\text{nm} \tag{3.7}$$

The HfO_2 used here offers a relative permittivity $k \approx 18$ [94][93]. This results in an EOT of 0.6 nm for 3 nm HfO_2 according to equation 3.6. The other part adding up to the EOT stems from the interfacial layer formed in between the high-k and Si with about 1 nm SiO_x. It is well known that, during HfO_2 deposition, the oxygen creates SiO_2 at the Si surface and thus hinders EOT scaling [95]. However, direct contact HfO_2/Si

[6] Named after the company Radio Corporation of America

interface is not suitable as well, since Hf-Si bonds may cause electric states in the Si bandgap [96]. Instead, for an optimum interface structure, the Si surface should be terminated at least by one monolayer of oxygen. Nevertheless, with this gate stack configuration gate leakage current densities in the range between 10^{-5} to 10^{-4} A/cm^2 have been measured.

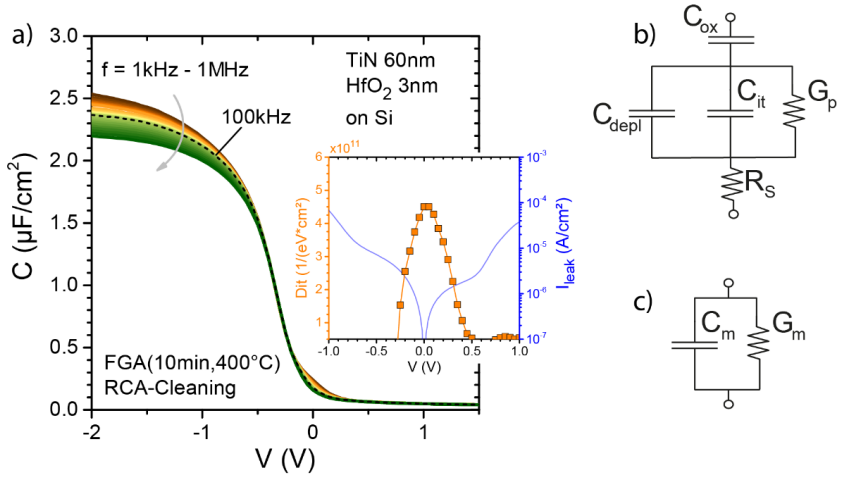

Figure 3.9: (a) C-V characteristics of the TiN/HfO_2 gate stack on Si measured at f = 1 kHz to 1 MHz. The inset depicts the D_{it} and the gate leakage current at the corresponding gate voltages. (b) Small signal equivalent circuit of the MOSCAP in depletion, showing the oxide capacitance C_{ox}, the series resistance R_S, the depletion capacitance C_{depl}, the interface trap capacitance C_{it} and conductance G_p. (c) Equivalent circuit from the analyzer with measured capacitance C_m and conductance G_m

One relevant parameter extractable from MOS structures is the density of interface traps located between high-k oxide and Si which introduce energy levels within the bandgap. This usually originates from unsatisfied termination of the dangling bonds at the interface or due to surface contamination prior the gate stack deposition. Pronounced D_{it} may hold enough charge carriers which effectively pin the Fermi level. Consequently, the semiconductor is not fully depleted and the minimum capacitance is not reached. Further, they degrade the channel mobility due to scattering. The measurement of the CV curves with various AC signal frequencies f in the range of 1 kHz to 1 MHz as displayed in Figure 3.9(a) indicates frequency dispersion in strong accumulation ($V \ll 0$) and in the depletion region. While the first might be caused from series resistance, the latter is characteristic for the presence of interfacial trap states. For DC gate bias around 0 V, the Fermi level is positioned close to mid gap.

The superimposed AC signal with small amplitude (~25 mV) induces an oscillation around the energy level. Traps in proximity can change their occupancy to certain frequencies which result in an additional trap capacitance C_{it} and in parallel to a trap conductance G_p (Figure 3.9(b)). Obviously, D_{it} hump vanishes for higher frequency due to the fact that time constants of interfacial traps are relatively long. The conductance method, proposed by Nicollian and Goetzberger [97], determines the D_{it} by analyzing the loss caused by the capture and emission of carriers in the trap level charge state. Therefore, based on measured capacitance C_m and conductance G_m (Figure 3.9(c)), the parallel conductance G_p can be obtained:

$$\frac{G_p}{\omega} = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{3.8}$$

where ω=2πf. The D_{it} is estimated by the following equation:

$$D_{it} = \frac{2.5}{e}\left[\frac{G_p}{\omega}\right]_{max} \tag{3.9}$$

For the fabricated MOSCAP with HfO_2 a D_{it} of $4.5 \cdot 10^{11}$ $eV^{-1}cm^{-2}$ has been extracted.

3.3 Multi Gate structure

In TFETs, improved gate electrostatic control at the tunnel junctions is of great importance to enable high tunneling currents for considerably low gate voltage. This corresponds with the reduction of the screening length λ_{chan}, as depicted in Figure 2.6(b) in chapter 2.2.1. When λ_{chan} is scaled, the spatial extension of the depletion region between source/channel interface decreases resulting in a higher barrier transparency. In general, the length scale λ_{chan} is strongly influenced by the device geometry which can be calculated by Poisson's equation shown in [98]. For a planar single-gate FET the screening length has the following expression [99]:

$$\lambda_{chan} = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}} \tag{3.10}$$

where ε_{si}, ε_{ox} are the dielectric constant and t_{si}, t_{ox} the thickness of Si and the applied gate oxide, respectively. Further decrease of λ_{chan} can be achieved by using multiple gate architectures as illustrated in Figure 3.10. According to analytical and numerical calculations [100], the screening length of the multi-gate architecture with square shaped channel cross-sections is reduced by a factor of $\sqrt{1/N}$ for each effective gate number N surrounding the channel leading to a generalized relationship for λ [101][98]:

$$\lambda_{chan} = \sqrt{\frac{\varepsilon_{si}}{N\varepsilon_{ox}} t_{si} t_{ox}} \tag{3.11}$$

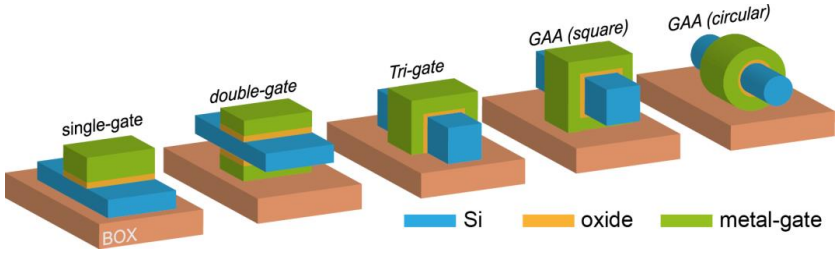

Figure 3.10: Schematic of FETs with different gate architecture from simple single-gate to gate-all-around structure featuring the best electrostatic control.

As for circular shaped nanowires λ_{chan} is given [102][103]:

$$\lambda_{chan} = \sqrt{\varepsilon_{si} t_{si}^2 \ln\left(1 + \frac{2t_{ox}}{t_{si}}\right) \frac{1}{8\varepsilon_{ox}}} \tag{3.12}$$

Figure 3.11 shows the calculation of the screening lengths for the different gate architectures shown in Figure 3.10, where HfO_2 is used as gate oxide with a thickness $t_{ox} =$ 3 nm and a dielectric constant $\varepsilon_{ox} = 18$ [94]. As the Si becomes thinner the depletion width exceeds the channel thickness turning it into a fully depleted body. This improves the gate control furthermore, due to close vicinity of the gates resulting in a deeper impact in the entire channel. Gate-all-around (GAA) architecture in conjunction with small scaled nanowires and thin high-permittivity (high-κ) gate dielectric provides the ultimate architecture for the need of TFETs allowing efficient channel modulation by the gate.

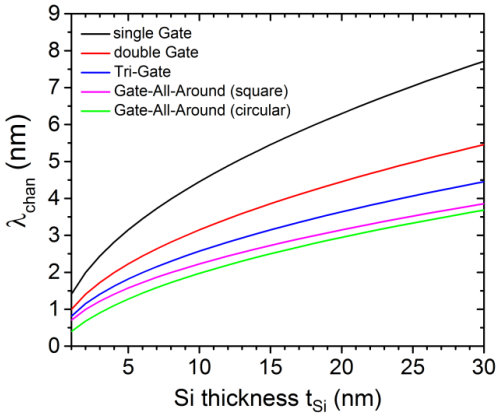

Figure 3.11: Screening length for different gate configurations as a function of the Si thickness assuming HfO_2 as gate dielectric with thickness $t_{ox} = 3$ nm and a dielectric constant $\varepsilon_{ox} = 18$ [94].

3.4 Steep tunneling junction with implantation into silicide

As already discussed in the previous chapter 2.2.1, the overall depletion length λ is not only influenced by λ_{chan} the device geometry but also depends on the source doping λ_{dop}. A decrease of λ_{dop} requires a high doping level and steep doping gradient to enable sharper transition of the energy bands at the tunnel junction. The creation of doped S/D regions with conventional ion implantation and thermal annealing usually lead to fairly broad dopant profiles. In addition, ion implantation induced crystal defects need to be healed which depends on the applied temperature. Otherwise, available trap states promote the contribution of TAT as discussed in chapter 2.4. One way to create sharp dopant pockets is the employment of implantation into silicide (IIS) which will be presented in the following section.

3.4.1 Formation of thin epitaxial $NiSi_2$

Ni silicide is the most applied metal-Si alloy especially in the nano-scaled CMOS technology in order to reduce the total resistance of devices. This is due to the fact that

silicides based on Ni require less thermal budget to establish low resistivity and more important consume less Si as compared to Ti or Co silicides which is beneficial for very thin Si layer configurations [104]. Different Ni silicide phases exist below $< 1000°C$ [105], but only nickel mono-silicide NiSi and nickel di-silicide $NiSi_2$ are interesting for processing. While poly crystalline NiSi shows the lowest resistivity of about 20 µΩcm [104], $NiSi_2$ with 35 µΩcm [106] provides similar cubic structure as Si indicating a lattice mismatch of only 0.4 % [105]. This results in atomically sharp interfaces to Si, significantly improved line/edge roughness and low contact resistance to p- and n-type Si. Based on this advantages, $NiSi_2$ is more suited for ultra-shallow S/D junction formation in highly scaled structures, e.g. Si NWs, than NiSi.

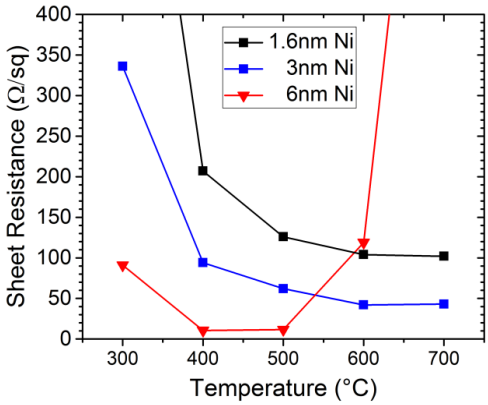

Figure 3.12: Sheet resistance measurements of Ni silicide formed on 60 nm SOI at different temperatures. Thin Ni film of 1.6 nm, 3 nm and 6 nm are investigated. Only the latter one (red) reveals small sheet resistances originating from NiSi.

Since Ni silicidation is a self-aligned process, silicide is only formed in direct contact with Si, whereas no reaction on other materials as oxides is performed saving additional lithography steps. The formation of the different Ni silicide phase follows a certain sequence depending on the applied temperature. Usually, at low temperature up to 300 °C the first nickel rich phase Ni_2Si is formed. Thermal treatment within a large thermal window between 300 °C to 600 °C leads to the creation of the NiSi phase whereas nucleation of the desired $NiSi_2$ only starts beyond that. However, the Ni silicide phase is also influenced by the available amount of Ni which has significant impact on very thin Ni film silicidation. In Figure 3.12 the 6 nm Ni film yields the smallest sheet resistance in the thermal window where the small resistivity NiSi phase is expected. Degradation of the sheet resistance at higher temperature is due to simultaneous phase change into $NiSi_2$ and especially agglomeration of NiSi [107]. In comparison, the sheet

resistance for 3 nm and 1.6 nm is larger but stays stable towards high temperatures. *Rutherford backscattering spectrometry* (RBS) measurements are done to investigate the stoichiometry, thickness and crystallinity of the Ni silicide formed at 500 °C on the sample surface (see Figure 3.13). The principle of RBS is based on elastic back the incident high energetic He^+-ions with the target atoms. The resulting energy of back

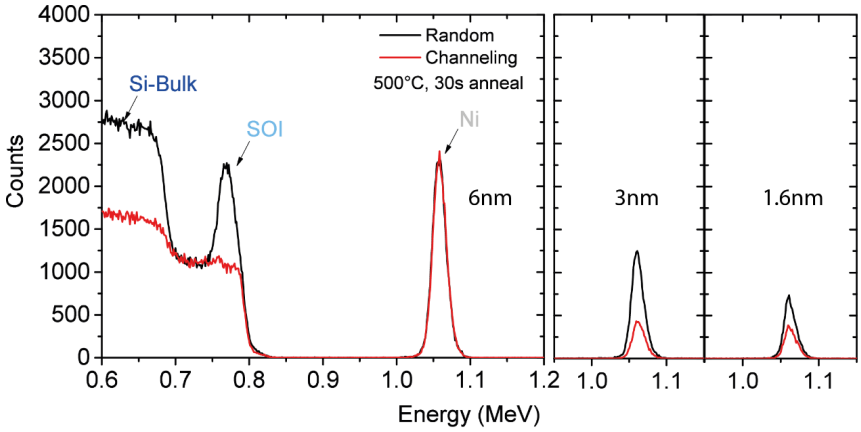

Figure 3.13: RBS measurements of the Ni silicides from Figure 3.12. Based on the random measurements the corresponding Ni silicide thickness can be derived, given in Table 2. Channeling measurements reveal that the 6 nm Ni form a non aligned NiSi phase, whereas 3 nm and 1.6 nm directly transforms into a partially aligned $NiSi_2$ phase.

scattered He^+-ions can be used to determine the composition and distribution of the analyzed material [108]. The peak at an energy ~1.1 MeV corresponds to Ni. In channeling mode the ion beam is aligned to the <110> crystal axis of Si to evaluate the crystal quality of the silicide. Less backscattering indicates partial crystal alignments of the silicide grains. No channeling is detected for the 6 nm Ni case confirming the polycrystalline NiSi phase which can be simulated from the RBS spectrum. In contrast, channeling is observed for Ni thicknesses below 3 nm indicating the direct transition into cubic crystalline $NiSi_2$ phase as the only phase for all temperatures T > 400°C. The explanation for this is the extremely thin Ni which limits the supply via diffusion to form Ni-rich phases during the thermal anneal. Furthermore, considerable stress in the thin Ni silicide layer promotes $NiSi_2$ formation which has a smaller lattice mismatch than other phases [109]. The summary of the resulting silicide phase, resistivity and thickness is listed in Table 3.2.

Table 3.2: Overview of the silicide phase, thickness and resistivity after Ni silicidation of different thicknesses.

Deposit Ni thickness [nm]	Silicide phase @ 500°C	Silicide thickness [nm]	Resistivity [μΩcm]
6	NiSi	12.5	19
3	$NiSi_2$	10	45
1.6	$NiSi_2$	5.5	55

One important parameter which also relies on the amount of Ni is the resulting silicide thickness. For thin Si body full $NiSi_2$ silicidation by preventing significant lateral diffusion is controlled by choosing the exact thickness of Ni [106][110]. The ratio of estimated silicide thickness t_{sil} to both deposited metal t_{Ni} and consumed Si t_{Si} to form $NiSi_2$ is given [105]:

$$\frac{t_{sil}}{t_{Ni}} = 3.59 \quad , \quad \frac{t_{sil}}{t_{Si}} = 0.98 \tag{3.13}$$

The calculated $NiSi_2$ thickness is in agreement with the values extracted from the RBS random measurements for 3 nm and 1.6 nm Ni. Based on equation (3.13), the needed initial Ni film can be calculated according to the Si thickness in order to control lateral $NiSi_2$ encroachment.

$$t_{Ni} = t_{si} \cdot 2.72 \tag{3.14}$$

Even though $NiSi_2$ is obtainable at low temperatures, the option for higher silicidation temperature is preferred to lower the density of (111)-facets at the interface and thus improve the silicide quality as can be seen in the decreased sheet resistance in Figure 3.12 [109][111].

3.4.2 Implantation into $NiSi_2$

The idea of dopant segregation based on the employment of $NiSi_2$ is a well-known approach to minimize contact resistances in Schottky-barrier MOSFETs [112]. We choose thin $NiSi_2$ because of its higher thermal stability and perfect alignment with the gate. The resulting doping pocket with high concentration piled up at the $NiSi_2$/Si interface and rapid fall off is also beneficial for reducing the energy barrier at the tunneling junction of TFETs. There are two ways to pursuit steep pockets through dopant segregation. One way is to perform the implantation into Si first and subsequent silicidation transports and accumulates the dopants by the moving silicide/Si

interface, denoted as *snow plough effect*. However, remaining implantation defects with

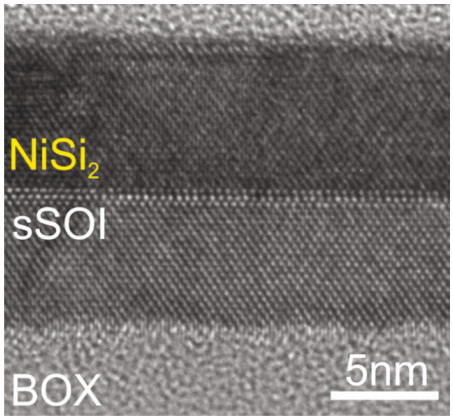

Figure 3.14: TEM cross section of epitaxial $NiSi_2$ indicating an atomic sharp interface. In this case 2.7 nm Ni is applied on 15 nm strained SOI to establish 10 nm $NiSi_2$ at 700 °C for 30 s with rapid thermal anneal (RTA).

this approach may enhance dopant diffusion during silicidation and also hinders $NiSi_2$ formation. Instead, performing silicidation prior ion implantation on defect free Si leads to high quality epitaxial $NiSi_2$ with atomic sharp interfaces, as can be seen in the *transmission electron microscopy* (TEM) image shown in Figure 3.14. Thus, implantation into silicide (IIS) is the main approach to create steep doping pockets in this work. In this concept silicide is formed beforehand and subsequent ion implantation parameters are adjusted in a way such that most ions are confined within the thin silicide layer [113]. The advantage hereby is that the main implantation damage is located in the Si metal alloy decreasing the demand for high temperature anneal. Instead, a low temperature anneal is expected to be sufficient for dopant diffusion out of the silicide film and pile up at the $NiSi_2$/silicon interface. This is because the solid solubility of dopants is rather small within the silicide and leads dopants to diffuse to the Si interface while dopant diffusion in Si is neglected due to low the temperature [114].This dopant accumulation at the interface should form the desired highly doped pocket with a sharp decay.

Experiments have been done in order to roughly determine the implantation parameters for the IIS process. In this case rather thick SOI of 60 nm is used to simplify the investigation. On top of that 8.5 nm $NiSi_2$ is formed with 2 nm Ni annealed at 700 °C for 30 s in a Helios Matson® RTA-system in forming gas ambient with 4 % H_2 and 96% N_2. Subsequently ion implantation has been performed with P^+ as n-dopant and B^+ as p-dopant to observe dopant segregation at the $NiSi_2$/sSi interface. We also

consider BF_2^+ as alternative p-dopants which is found to produce less transient enhanced diffusion during the activation anneal in Si [115]. Low implantation energies in conjunction with a large tilt of 45° to the surface normal estimated by TRIM simulation [116] should enable a shallow implantation where most of the dopant resides in the $NiSi_2$. An overview of the implantation parameters for each dopant type is given

Table 3.3 Dopant implantation parameters into 8.5 nm $NiSi_2$/SOI

Dopant species	Implant energy	Dose	Tilt angle
B^+	0.7 keV	$1{\cdot}10^{15}\,cm^{-2}$	45°
BF_2^+	3.5 keV	$1{\cdot}10^{15}\,cm^{-2}$	45°
P^+	3 keV	$1{\cdot}10^{15}\,cm^{-2}$	45°

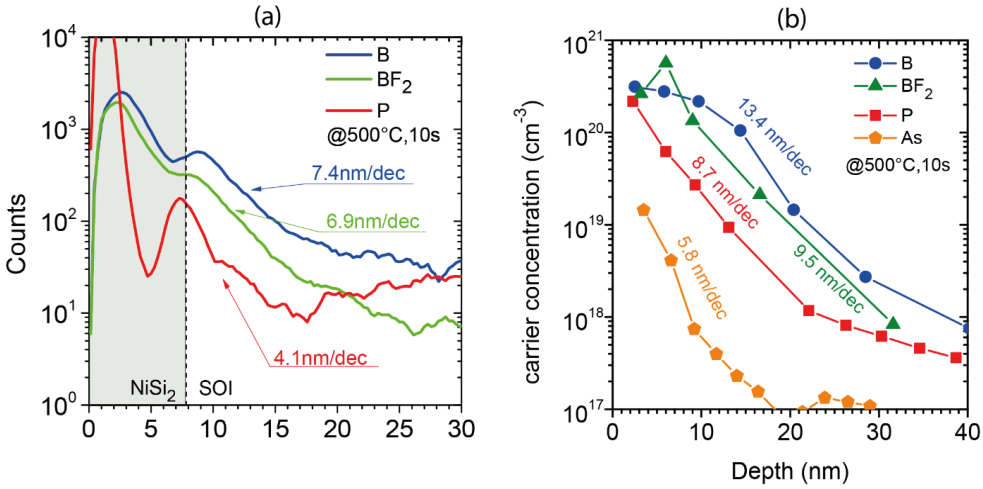

Figure 3.15: (a) SIMS dopant profile after 500 °C for 10 s drive out anneal. All dopants pile up at the $NiSi_2$/SOI interface. (b) Comparison to conventional dopant activation at the same temperature and time without $NiSi_2$ measured by ECV. Dopant profile is broader in this case.

in Table 3.3. All samples are tempered at 500 °C for 10 s to drive the dopants out of the silicide. Figure 3.15(a) demonstrates the dopant distribution in dependency of depth determined by *secondary ion mass spectrometry* (SIMS) [117]. This thin film analyze technique sputters the target surface with an ion beam while secondary ions from the target are collected and analyzed by its mass and charge to determine the elemental composition. A maximum peak for all dopants is observed at the $NiSi_2$/SOI interface confirming the successful segregation effect. The P peak is more significant compared to the B and BF_2 dopants which can be explained by the larger diffusion

constant of B in Si. Moreover, the dopant profile of B and BF_2 are comparable. Apparently the effect of dopant diffusion retardation by the fluorine during annealing is negligible in the $NiSi_2$/Si configuration and only has a noticeable contribution in pure Si.

Due to the two material system ($NiSi_2$/SOI) confined in a shallow junction, it is rather difficult to extract the total dopant concentration with SIMS. Furthermore, SIMS can only provide the atomic distribution rather than the electrically active dopant distribution. Therefore, the experiment has been repeated on samples without $NiSi_2$ with the goal to determine the electrically active dopant concentration at 500 °C in Si utilizing electrochemical CV (ECV) measurements. This technique is based on an electrolyte-semiconductor forming a Schottky contact at the interface [118][119]. In reverse bias, a depletion region is formed. Since the depletion region behaves like a capacitor between the electrolyte and the non-depleted region below, measuring the capacitance provides the carrier concentration and thereby the electrically active dopant density. The advantage of the electrolyte instead of a metal for the Schottky contact is the possibility of vertical etching of the semiconductor enabling a depth resolution of the carrier concentration. When p-Si is investigated dissolution process happens at forward bias. In this case hole charges are created at the electrolyte-semiconductor junction necessary to electrolytically dissolve the semiconductor. However, for n-doped Si, the semiconductor needs to be illuminated to promote hole generation and the attraction to the interface, which only happens at reverse bias [120]. By alternating between CV measurements and etching, a doping level profile of any arbitrary depth can be obtained as shown in Figure 3.15(b). Note that the ECV measurement especially close to the interface must be treated cautiously because of the still remaining defects at such low temperature and high implantation dose of $1{\cdot}10^{15}\,cm^{-2}$ giving the potential for larger errors.

At 500 °C annealing temperature fairly high dopant activation has been measured for B reaching a concentration of about $1{\cdot}10^{20}\,cm^{-3}$ even 10 nm below the surface region. Again, the broader B depth profile stems from the larger diffusion in Si. BF_2 only provides a slight improvement with respect to the diffusion depth. Probably significant diffusion retardation of the fluorine is only noticeable at high annealing temperatures aiming for large dopant regions as reported in [115]. Figure 3.15(a) indicates steep dopant profile for Arsenic implantation, however, the active dopant concentration is much lower for $T = 500$ °C compared to P. From comparing the dopant profile distribution in Figure 3.14 it becomes evident that the segregation process with $NiSi_2$ has the potential to provide steeper dopant pockets. The challenge is the parameter setup for the ion implantation such that most of the implanted dopants reside in the silicide.

3.5 Summary

In this chapter diversity of technology boosters are elaborated in detail with the goal to enhance the TFET performance for the Si homo junction platform. The target is to obtain high ON-currents with SS below 60mV/dec by reducing the parameters band gap E_g, effective mass m^* and the screening length λ.

The nanowire architecture with small diameter allows the ultimate gate-all-around design that provides excellent gate electrostatics due to the reduction of λ. Further optimization can be achieved by including HfO_2 as high-k gate oxide and TiN as metal gate to improve the gate control. EOT of about 1.8 nm are obtained where the largest contribution is caused by the SiO_2 interfacial layer during the high-k deposition. Furthermore, the nanowire design allows the application of uniaxial tensile strain to reduce m^* and E_g on biaxial pre-strained Si wafers. Suspending the thin wire preserves the strain along the preferred [110] direction which can be enhanced by forming relaxed pads that pulls the wire at each side. Notably high strain values up to 3.5% tensile strain has been achieved. Although this approach offers a simple way to modify the strain in nanowires, these large pads limits the applicability when it comes to package density. In addition, highly strained nanowires become more fragile, e.g. reduced thermal budget compared to unstrained Si, and needs to be considered in the fabrication process. Tilted ion implantation into the silicide in combination with low temperature anneal should enable sharp dopant pockets which are crucial for steep tunneling junctions in TFETs. Silicidation with Ni to obtain the crystalline $NiSi_2$ phase is well suited for this attempt as it provides sharp atomic interfaces between the S/D and channel especially viable in small Si dimensions. Tests on SOI samples successfully demonstrate the dopants (P, B, BF_2) piling up at the $NiSi_2$/Si interface after 500°C anneal. The dopant gradient is small since dopant diffusion is lowered at this temperature.

4. Strained Si nanowire TFETs

In this chapter TFETs based on strained Si nanowires with high-k/metal gate-all-around (GAA) approach will be presented. The employment of this device architecture should improve the overall TFET performance mainly based on the reduction of the bandgap E_g and the screening length λ as discussed in chapter 3. Besides performance related aspects, the goal is to establish a process for p- as well as n-TFETs with comparable performance that lay the fundamental for CMOS applications in the upcoming chapters. The challenge is to realize an appropriate steep source doping for both device types. In the beginning of this chapter the fabrication process of the strained sSi NW TFETs will be introduced. Subsequently, the I-V characteristics will be demonstrated to evaluate the device performance. Further analysis such as pulsed I-V, temperature dependent I-V and charge pumping are performed in order to gain more insight into the switching characteristics of the sSi GAA NW TFET platform.

4.1 Device Fabrication

The process flow of strained Si NW TFETs is illustrated in Figure 4.1, where the entire fabrication process can be grouped into four sub processes. Strained silicon on insulator (sSOI) substrates with a (100)-surface and a background p-doping level of about $1{\times}10^{15}$ cm^{-3} from the semiconductor manufacturer SOITEC® with an sSOI thickness of 15 nm on 145nm buried oxide (BOX) are used. These substrates are fabricated by pseudomorphic growth of Si on relaxed $Si_{1-x}Ge_x$ with a Ge content of $x = 20$ %. The strained Si is then transferred to an oxidized handle wafer via wafer bonding techniques. The resulting biaxial tensile strain in the sSOI layout is about $\varepsilon_{biax} = 0.8$ % which corresponds to a stress of 1.3 GPa [73]. Before the main fabrication steps, $19.5{\times}19.5$ mm^2 pieces are cut from a 300 mm wafer. Photoresist AZ5214 is spun on the wafer beforehand in order to protect the surface.

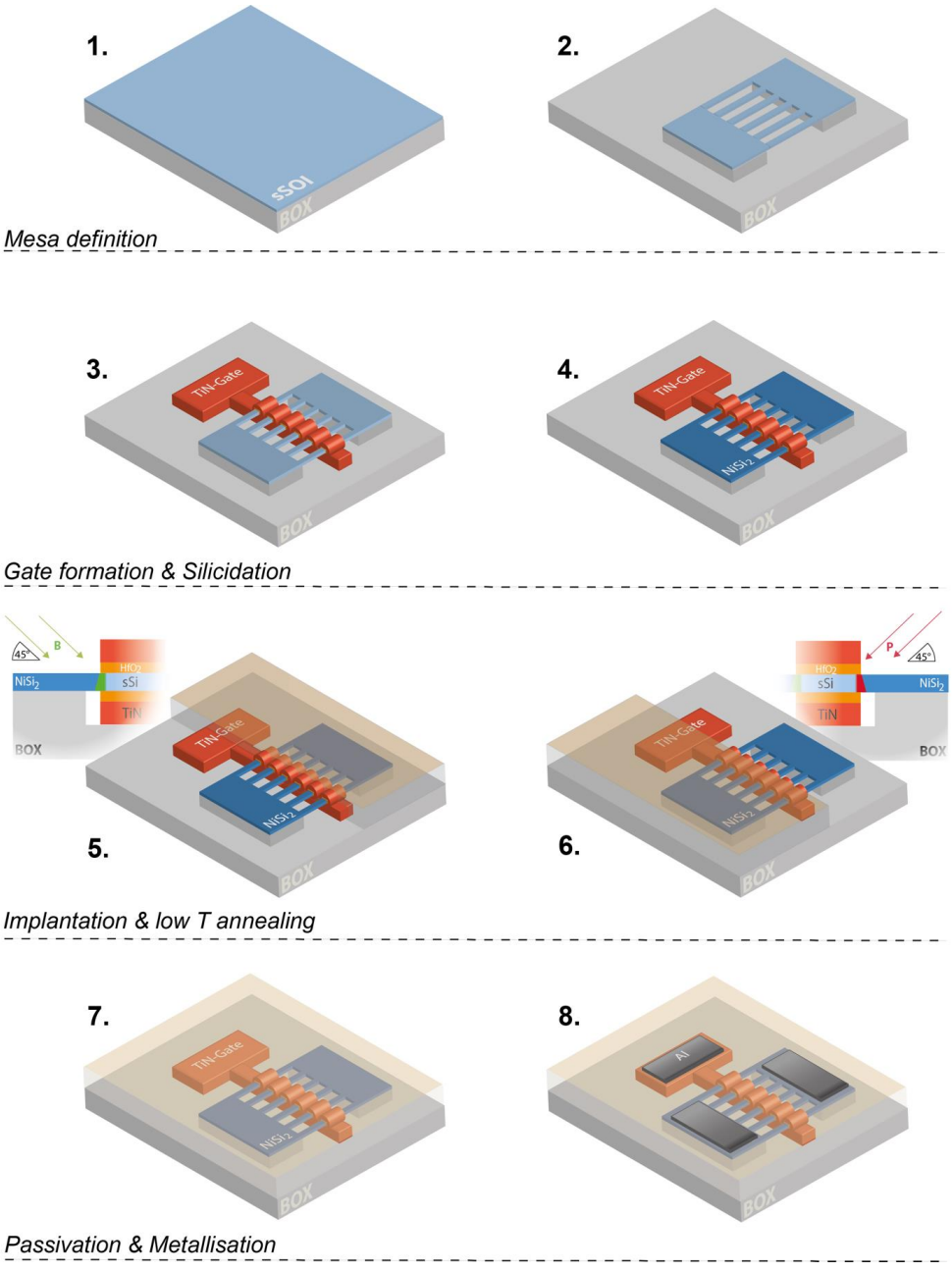

Figure 4.1: Process flow of the strained Si NW TFET with HfO_2/ TiN as gate stack.

1. *Sample preparation and electron-beam marker definition*
   The first step is a short dip in de-ionized water to pre-clean the sample pieces to remove rough particles after sawing followed by acetone and propanol bath to remove the resist. For the realization of NW structures of several tens of nm, electron beam lithography (EBL) is indispensable to enable high resolution as well as high alignment accuracy. EBL relies on marker structures for orientation and alignment. Therefore, an optical lithography step is performed first with positive deep ultraviolet (DUV) photoresist UV6.06 and subsequent reactive ion etching process (RIE) to transfer the 20×20 µm^2 square marker pattern to the samples. The RIE etch begins with an SF_6/O_2 plasma to etch the top sSOI layer, the BOX with CHF_3 and finally SF_6/Ar to achieve a deep etch of about 600 nm into the Si-Bulk. The UV6.06 mask is removed with acetone and propanol. Additional cleaning was performed in H_2SO_4 : H_2O_2 solution at (2:1) ratio, also known as piranha etch.

2. *Definition of mesa and NW array*
   To achieve better resolution, the NW array is patterned with EBL after coating the samples with negative electron beam resist hydrogen silsesquioxane (HSQ XR-1541) diluted (1:1) with methyl isobutyl ketone (MIBK). Subsequent RIE etch with Cl_2/Ar created by an inductively coupled plasma (ICP) enables highly anisotropic etching of the uncovered sSOI layer. Afterwards, HF-1 % wet etch removes both the HSQ mask and the SiO_2 below the NW which finally leads to mesa structure with suspended NWs. The NW patterning converts the initial biaxial tensile strain into uniaxial strain uniformly along the wire due to anisotropic strain relaxation [121]. An optional thermal oxidation can be used to thin down the NW diameter and smooth out the sidewalls and edges after RIE process . Figure 4.2 shows scanning electron microscopy (SEM) images of the NW array after this process step. This way to fabricate NWs utilizing EBL and RIE etch is denoted as the top-down approach.

3. *Gate stack formation*
   The sSi samples are cleaned with the standard RCA cleaning[7] [122]. Subsequently, a 3 nm thick HfO_2 layer is deposited by atomic layer deposition (ALD) forming the high-k dielectric layer. Directly on top, a 60 nm thick TiN layer as metal gate is deposited by atomic vapor deposition (AVD). Both tools provide highly conformal growth rates ensuring a high-k/metal gate wrapping around the NW (Figure 4.3). Afterwards, a second EBL step is performed for

[7] Note that after RCA about 3nm of Si is consumed.

the gate patterning. In this step non-diluted HSQ is used which is more durable to relatively long etching times. The pattern is transferred into the TiN by RIE etching with $Cl_2/SF_6/Ar$ plasma using ICP source to increase the selectivity to HfO_2. Thereafter, a wet etch solution is used to remove TiN residuals which usually remain at the Si sidewalls. A further HF1%-dip takes off the HfO_2 and the HSQ resist.

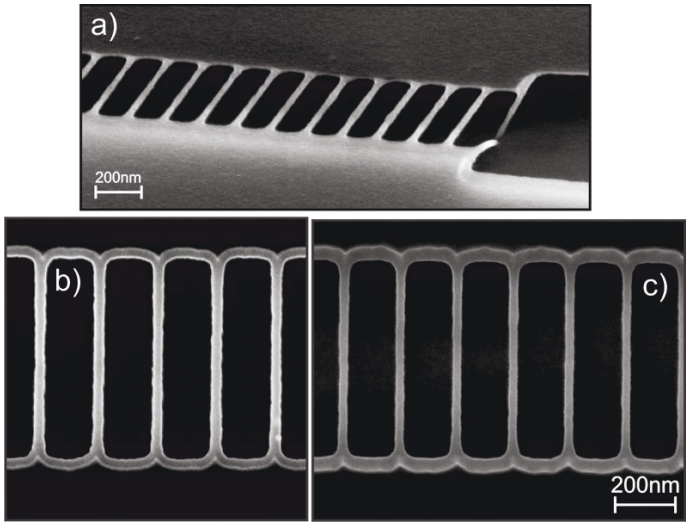

Figure 4.2: (a) SEM images of the suspended sSi NW array with 20 nm width after mesa definition. (b) Rough edges of the NWs can be smoothed out with a short thermal oxidation treatment and subsequent HF1%-dip (c). Less contrast at the NW contour is a sign for smoother edges.

4. *Source/Drain silicidation*

Once the gate process is completed, a thin Ni film of 3 nm is sputtered on the entire sample. The Si thickness before deposition needs to be measured by ellipsometry to determine an accurate Ni thickness according to equation (3.2). This self-limiting process allows fully silicidation of the NW decreasing the S/D resistance but inhibiting lateral Ni encroachment into the channel. The annealing temperature for silicidation is performed in forming gas ambient (N_2/H_2) with 10% H_2 at 700 °C for 30 s. Only the Ni in contact with the exposed sSi reacts and forms $NiSi_2$. Unreacted Ni residuals are etched in diluted sulphuric acid H_2O : H_2SO_4 (1:3) to avoid shortcuts between S/D and gate.

5./6. Implantation into silicide (IIS –process)

In order to prevent intermixing of the different dopant types during ion implantation, electron beam resist is used as implantation mask to cover either source or drain. A tilt ion implantation approach of 45 ° into the silicide was developed to enable high dopant accumulation close to the gate. In case nothing else is mentioned, boron ions (B^+) as p-dopants are implanted at an energy of 1.5 keV. After the PMMA removal and covering of the corresponding regions, phosphorus ion (P^+) implantation is performed as n-dopants at 3 keV. The implantation energy has been carefully chosen according to TRIM simulations [116] with the intention that the concentration peak is located close to the NW surface. Different dose for both dopant types are considered ranging from $1{\times}10^{14}$ to $5{\times}10^{15}$ cm^{-2}. A low temperature anneal at 500 °C is performed to drive the dopants out of the silicide and create dopant pockets at the $NiSi_2$ /channel interface by dopant segregation.

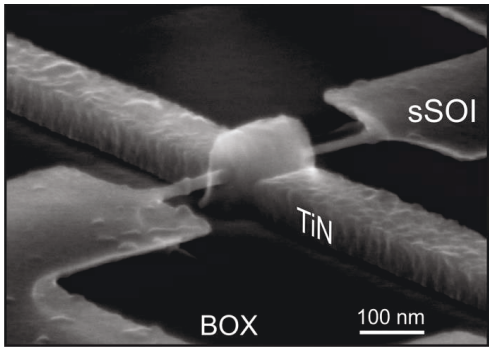

Figure 4.3: SEM image after the gate process. In this case only the narrow NW is suspended which is completely wrapped around by the gate.

7. Passivation

The sample surface is passivated with 100 nm SiO_2 by plasma-enhanced-chemical vapor-deposition (PECVD) at 350 °C. Contact windows are defined with optical lithography using negative AZ nLOF 2020 resist followed by an RIE etch based on CHF_3 to open the windows.

8. Contact metallization

HF-dip is performed to ensure an oxide free surface within the contact windows. Pt/Cr are employed as final metal contacts deposited by electron beam evaporation. 5 nm Cr

is applied here to improve the adhesion of the 150nm Pt. Excessive metal on the photoresist is removed by lift-off process using acetone bath. In the final step, the samples are heated in forming gas for 10 min at 400 °C. This treatment should improve the metal contacts and also the high-k/metal gate stack by saturating the dangling bonds with hydrogen atoms [123][124].

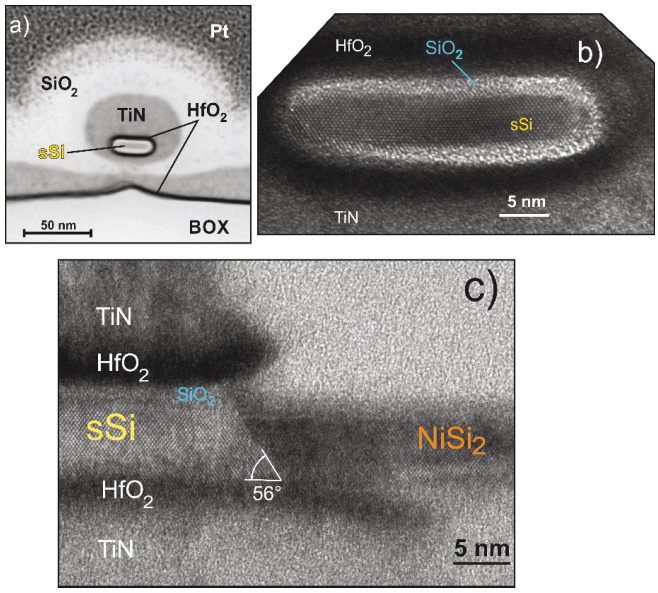

Figure 4.4: (a) Overview of the cross section of a single NW is shown after fabrication process. (b) TEM image revealing the maintained single crystalline sSi NW wrapped around by HfO_2 and TiN. (c) A further TEM image along the NW indicate the $NiSi_2$ formation of the entire Si NW up to the gate interface.

The processed TFETs are cut via Focused ion beam (FIB) to observe and determine the outcome of the critical process steps. An overview of a single NW cross section is illustrated in Figure 4.4(a) where the sSi NW in the center is surrounded by the HfO_2 and TiN. A close-up and more detailed image of the NW is provided by the TEM image in Figure 4.4(b). After processing the sSi NW inside the channel region remains single crystalline. The NW has a final thickness of 5 nm and the width of this particular NW is about 40 nm. More relevant is the thickness of the gate dielectric. The HfO_2 is about 2.8 nm thick and the SiO_2 interfacial layer amounts to 1.2 nm. Using equation (3.6) the effective oxide thickness (EOT) is about 1.8 nm of the corresponding TFETs. In addition, a cut along the NW direction (current flow direction) has been performed as shown in Figure 4.4(c) to observe the S/D to channel transition. The estimated Ni

thickness for silicidation turns out to be sufficient to silicide the non-gated NW completely throughout the entire thickness. Apparently no significant Ni encroachment happened in the self-aligned process so that the sSi inside the gate is left untouched. The TEM also reveals a clear NiSi/sSi interface with an atomically flat (111) facet which is likely to be formed with $NiSi_2$ and confirms its presence [114].

4.2 Electrical characterization of sSi GAA NW TFETs

In this section the *I-V* characteristics of the strained Si NW array TFETs with wrap gate are presented. Both n- and p-TFET devices are measured with a Keithley SCS4200 analyzer. Figure 4.5 presents the I_d-V_{gs} transfer characteristics of the fabricated sSi GAA NW n- and p-TFETs according to chapter 4.1. The fundamental

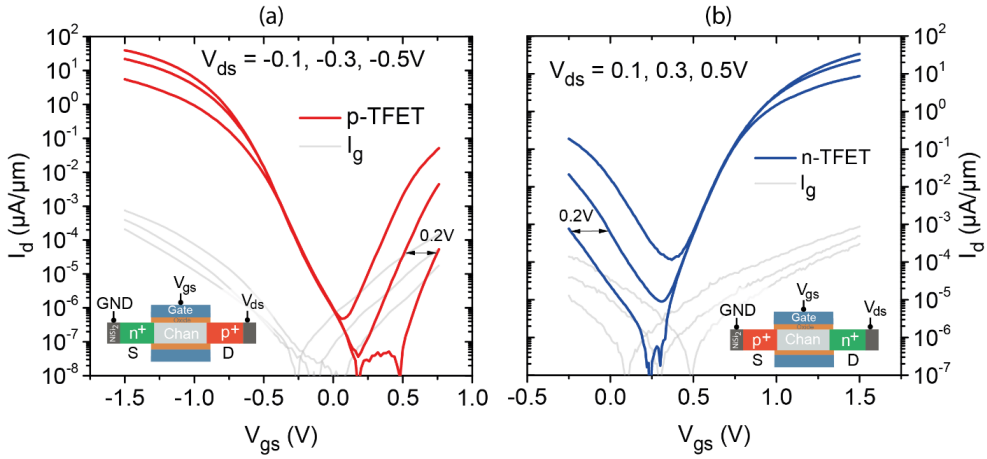

Figure 4.5: I_d-V_{gs} transfer characteristics of (a) p- and (b) n-TFET with strained Si GAA NWs of 40×5 nm^2 cross section and 200 nm gate length. Both devices show comparable performance in the ON-state but due to ambipolar behavior also conduct current in the OFF-state. The inset show the source/drain doping and voltage bias constellation

difference between these two devices are the dopant species at source and drain. As for the p-TFET, phosphorus (P) ion implantations at a dose of $5{\times}10^{15}$ cm^{-2} has been applied in the source and $1{\times}10^{15}$ cm^{-2} of boron (B) ion implantation at the drain side.

In case of the n-TFET, BF_2^+ is implanted at the source with $5{\times}10^{14}$ cm^{-2} while the drain is doped with $1{\times}10^{15}$ cm^{-2} of P^+. Both TFETs feature NWs with a dimension of 5 nm in thickness and 40 nm in width (40×5 nm^2 cross section). The gate length amounts to about 200 nm. To ensure a fair I_d performance comparison between the p-TFET with an array of 60 NWs and the n-TFET with 40 NWs, the measured drain current is normalized by the gate width. Low drain voltages at $|V_{ds}| = 0.1$, 0.3, 0.5 V are considered here. Both transfer characteristics of the devices in the ON-state indicate similar current performance with a minimum I_{off} of ~10^{-6} µA/µm and I_{on} of several µA/µm (see output characteristics in Figure 4.7) leading to I_{on}/I_{off} ratios of about 10^6 at $V_{ds} =$ 0.1 V. However, the devices show an undesired current conduction in the OFF-state when positive V_{gs} is applied to the p-TFET and vice versa for the n-TFET. In this case inter band to band tunneling is no longer established between source and channel. Instead, this ambipolar tunneling current stems from the band overlap between channel and drain. The subthreshold swing SS for the ambipolar current is comparable to the actual ON-current branch simply because the drain side is

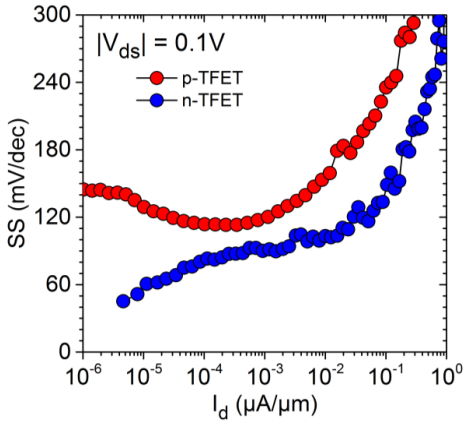

Figure 4.6: Extracted inverse subthreshold slope SS in dependence of I_d for the corresponding TFETs depicted in Figure 3.5.

also realized by the IIS process as depicted in Figure 4.1 resulting in a steep and highly doped pocket. As V_{ds} is set to larger voltages the parasitic tunneling current sets in earlier resulting in an increase of the current for the same gate voltage. This effect explains the shift of the ambipolar current branch towards the ON-state which corresponds to V_{ds} steps of 0.2 V. Consequently, the pronounced ambipolar currents with larger V_{ds} degrades the I_{on}/I_{off} ratio. As the minimum OFF-current is limited by large

ambipolarity, the steepest part of the transfer characteristics is cut off which is indicated by the n- and p-TFET in Figure 4.5. Therefore, only the transfer characteristics at small V_{ds} reveal the full tunneling current information at the source/channel junction without being obscured by the ambipolar current. Hence, the inverse subthreshold slope SS vs. I_d shown in Figure 4.6 has been extracted at $|V_{ds}| = 0.1$ V to record the entire subthreshold regime but neglecting the current data points where I_d is below the gate leakage I_g. In detail the p-TFET indicates a minimum point slope of SS = 113 mV/dec in current regions of 10^{-4} to 10^{-3} µA/µm. However, a slight SS increase is observed when going towards I_{off} so that the smallest average slope amounts to SS_{avg}= 124 mV/dec over three orders of magnitude in current. In turn, the n-TFET provides a steeper switching over the current region with SS_{avg} of 70 mV/dec. A striking result is the minimum point slope below 60 mV/dec extracted at currents smaller than 10^{-5} µA/µm. Since the gate architecture is the same for both devices the better performance of the n- over the p-TFET might be explained by the higher B activation at 500°C in comparison to P realized by the IIS-process.

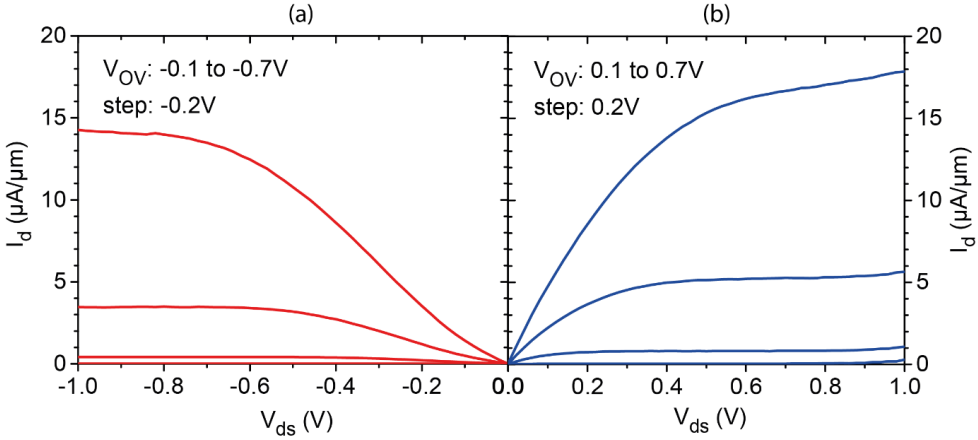

Figure 4.7: Output characteristics I_d-V_{ds} of (a) p- and (b) n-TFET with strained Si GAA NWs of 40x5 nm² cross section and 200 nm gate length for the same gate overdrive voltage $|V_{OV}|=|V_{gs}-V_{off}|$ from 0.1 to 0.7 V.

The output characteristics I_d-V_{ds} of the corresponding sSi NW GAA TFETs show good saturation behavior (Figure 4.7) for both n-and p-type. A slight "S"-shape is observed for the p-TFET at low V_{ds} which can be explained by drain induced barrier thinning [23]. As described in chapter 2.7.2, the direct influence of the drain potential to the tunneling junction accounts for the exponential current increase. According to *De Michielis et al.*, also the variation of the charge occupancy function with respect to

the tunneling energy window needs to be considered [45]. They have shown by simulation that for higher doping levels at the source the change of the charge occupancy becomes insignificant and restores the linear onset. Indeed, the n-TFET provides such linear characteristic at low V_{ds} which in turn substantiates high B activation at the source. In terms of current performance both devices are fairly similar with 3.2 µA/µm for the p-TFET and 5.5 µA/µm for the n-TFET at supply voltages $|V_{dd}|=|V_{ds}|=|V_{OV}|=0.5$ V. Here $V_{OV} = V_{gs}-V_{off}$ denotes the gate overdrive voltage where V_{off} corresponds to the gate voltage determined at OFF-currents I_{off} =1 nA/µm (V_{off} for p-TFET: -0.3 V and n-TFET: 0.5 V). The measured current levels of the presented p-and n-type sSi GAA NW TFETs are in good agreement with state of the art Si NW homo junction tri-gate TFETs [125].

Moreover, basic analog performance of the sSi NW GAA TFETs is analyzed to extend the dataset and also to evaluate their capability in this area. The most basic analog application realized by a single FET is the common source amplifier where the voltage gain $A_V = g_m/g_d$ is the most interesting figure of merit. It can be calculated by the transconductance $g_m = \partial I_d/\partial V_{gs}$ over the conductance $g_d = \partial I_d/\partial V_{ds}$ ratio. The following analysis through the analog parameter is restrained on the n-TFET since the p-type counterpart yields comparable results as reported in [126].

The transconductance g_m normalized to the gate width is presented in Figure 4.8 in dependence of the gate overdrive voltage V_{OV}. For TFETs I_d is mainly determined by the tunneling resistance and thus leads to an exponential trend of g_m. In this regard, sSi GAA NW TFETs should show an improved electrostatics resulting in much higher transconductance due to the better coupling between gate and the tunneling junction. The corresponding NW n-TFET achieves transconductance up to g_m = 95 µS/µm at V_{ds}= 0.5 V and V_{OV} = 1 V which is about a factor of two larger than the reported p-type 10 nm NW TFETs results [126] at the same bias configuration. However, the extracted values are inferior compared to g_m of MOSFETs because of the still lower currents of the TFETs [127][128]. In the focus of low power analog circuits where transistors need to operate in small current regions an appropriate transconductance is desired. The so called transconductance efficiency is $g_m/I_d = (\partial I_d/\partial V_{gs})/(1/I_d) = \ln(10)/\mathrm{SS}$ is a measure indicating the transconductance per current unit, i.e. to determine the power consumption of the amplifier [129]. The devices offer a nearly constant g_m/I_d about 23 V^{-1} over a wide current range. The maximum g_m/I_d ratio is located at the subthreshold regime due to its SS^{-1} proportionality (see Figure 4.9). Thus, the n-TFET achieves values with g_m/I_d = 82 V^{-1} at V_{ds} = 0.1 V where SS goes below 60 mV/dec demonstrating that well optimized TFETs bear the potential to provide larger gain than MOSFETs for the same current dissipation [130].

In contrast, the conductance g_d is derived from the output characteristics and is displayed in Figure 4.10. Highest value of g_d reaches up to 25 µS/µm when going to

gate overdrive voltages of $V_{OV} = 0.5$ V and rapidly drops down below 1 µS/µm towards large drain voltages V_{ds} once entering the saturation region of the output characteristics. The slight increase of g_d for very large drain voltages can be attributed to the impact of ambipolar conduction as also slightly implied in the output characteristics in Figure 4.7.

Considering both g_m and g_d the intrinsic voltage gain A_V can be derived as a function of V_{OV} for different values of V_{ds} as presented in the inset of Figure 4.10. The voltage gain increases with increasing drain voltage due to large g_m in combination with the small g_d so that a maximum value A_V over 260 is obtained. Compared to our GAA NW MOSFETs, the TFETs exhibit clearly higher gain for V_{ds} set to 0.5 V. The resulting voltage gain of the GAA NW TFETs are even higher than the numbers reported for 20 nm FinFETs [126] for specific bias configurations. The reason for this is the significantly small g_d of TFETs stemming from the good output saturation behavior as the main predominant factor even though g_m is smaller compared to the FinFETs [131] or in GAA MOSFETs [132]. In contrast to the MOSFET counterpart, TFETs can even maintain a small output conductance for small gate lengths since they are more robust against short channel effects offering better scalability for analog applications. Therefore, sSi GAA NW TFETs might be an attractive option, e.g. serving as low power amplifier, for analog circuits at moderate frequency. Further benchmarking of these sSi GAA NW TFETs on basic analog functions can be found in [133].

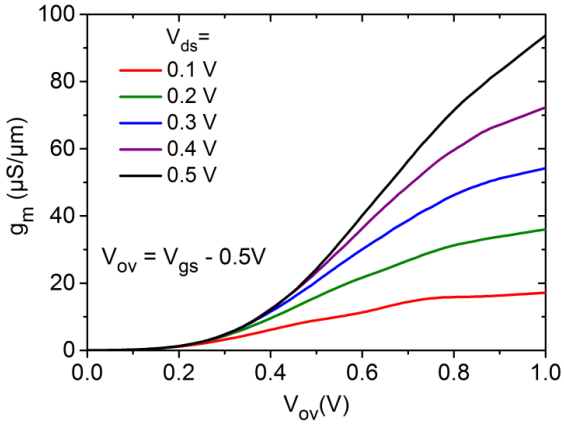

Figure 4.8: Transconductance g_m of the sSi GAA NW n-TFET shown in Figure 4.5(b) normalized to the gate width as a function of the gate overdrive voltage V_{OV} for different V_{ds} ranging from 0.1 V to 0.5 V.

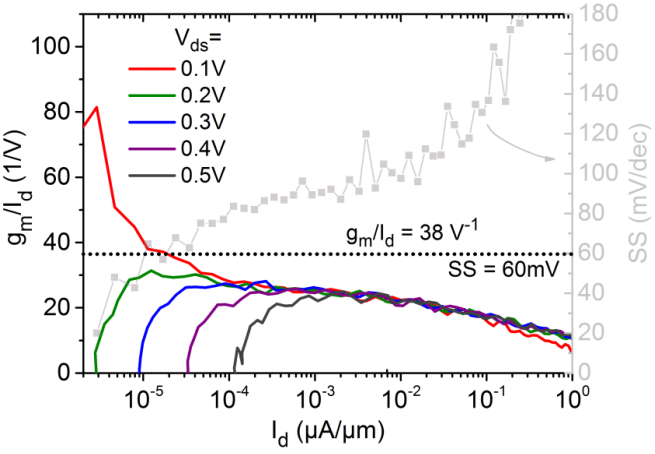

Figure 4.9: Transconductance efficiency g_m/I_d of the sSi NW GAA n-TFET. The SS data measured at V_{ds}=0.1 V are included to highlight the increase of g_m/I_d above 38 V^{-1} at SS<60 V/dec.

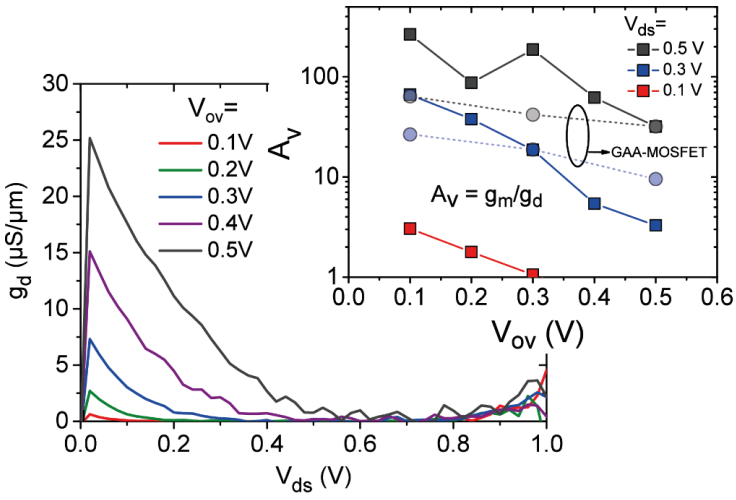

Figure 4.10: Low output conductance g_d of the sSi NW GAA n-TFET corresponds to the good saturation behavior in the output characteristics. The inset demonstrates the intrinsic gain of the n-TFET for different V_{ds}. The gain of GAA-MOSFETs are included for comparison.

4.3 Pulsed *I-V* measurements

The DC transfer characteristics at room temperature indicate that none of the fabricated sSi NW GAA TFETs feature SS significantly below 60 mV/dec for many orders of magnitude of I_d as theoretically predicted. So far, only the n-TFET has indicated such desired characteristics however only at very low currents. Such steep switching is practically difficult to achieve even when the essential building block are utilized, as discussed in chapter 3. Substantial leakage currents, e.g. from the gate, ambipolar behavior as well as trap assisted tunneling (TAT) are always present in the OFF-current region and may obscure the sharp onset of the BTBT current near the threshold voltage. Especially TAT is a serious issue for experimental TFETs particularly when ion implantation is employed. Defects generate energy states in the bandgap which are gradually filled with charge carriers when the gate voltage is increased. Due to thermal excitation these trapped carriers are likely to overcome the energy barrier allowing charge transport before the band overlap between source and channel is established for BTBT, thus degrades the achievable SS.

In general, the TAT process involving charge capture and thermal emission occurs within a characteristic time constant. A quantitative estimation of trap time constant τ_{trap} for a trap at a distance x from the interface capturing a charge via elastic tunneling process is given by [134][135][136]:

$$\tau_{trap}^{-1} = v_t N_c \sigma \exp(-2kx) \exp\left(\frac{\Delta E}{k_B T}\right) \tag{4.1}$$

where v_t is the thermal velocity, N_c the carrier concentration, σ the trap cross-section, k is the attenuation coefficient for electron wave function, ΔE the difference between the trap level energy and the majority carrier band edge and k_B the Boltzmann constant for the semiconductor temperature T. First demonstrations on MOSFETs with pulsed *I-V* (PIV) measurements at different time regimes allows the characterization of trap charge and discharge contribution from the SiO_2/HfO_2 gate oxide [137]. The main idea of sweeping V_{gs} faster than the response time of the oxide traps which is found to be in the range of microseconds should suppress charge trapping that leads to improved I_d-V_{gs} characteristics expressed in less threshold voltage shifts [138]. However, the situation is more complicated for TFETs with TAT generation not only from the semiconductor/oxide interface but also traps within the semiconductor body at the source/channel junction where the main charge transport takes place. Only few experimental reports analyzing TFETs with the PIV technique have been published so far. Mohata *et al.* first demonstrated the potential of this technique on III-V devices [139], decreasing the minimum SS_{min} from 180 mV/dec to 100 mV/dec. Similar results were

obtained later by Rajamohanan *et. al.* [140] still based on III-V devices and for the first time in Si NW TFETs by Knoll *et al.* [125]. They all achieved improved SS behavior at short pulses down to 1 µs which they attribute to suppressed trap assisted tunneling. Therefore, PIV measurements are performed on the sSi NW GAA n-TFETs to investigate the transfer characteristics by trying to eliminate the TAT influence and thus to reveal the 'intrinsic' TFET performance possible with this method.

The equivalent circuit of the PIV setup is depicted in Figure 4.11(a). Short rectangular pulses for the gate terminal are provided by *Tektronix AWG7122C Waveform Generator* while V_{ds} is supplied from a DC port of the generator holding a constant voltage for the entire measurement. For visualizing the applied gate voltage pulse *vg* and more important the pulse response of the device under test, a *Tektronix DPO70604C Digital & Mixed Signal Oscilloscope* [8] (6 GHz bandwidth) is used in our setup. In order to track the pulse response at the oscilloscope, the source probe is connected to a *Femto DHCPA-100* current-to-voltage amplifier that converts the actual source current I_s to a voltage signal *vis*. This operational amplifier provides a gain G which is variable from 10^3 to 10^8 V/A. High G values are necessary especially for recording small current regions of TFETs, but because of the gain-bandwidth limitation of the amplifier there is a trade-off between gain and available bandwidth. In this regard, the circuit is impedance matched to our best knowledge to ensure largest bandwidth in order to enable small rise and fall times $t_r = t_f = 5$ ns with less distortion.

The multiple pulse approach [138] is used here to reconstruct the entire I_d-V_{gs} curve, where each input pulse represents one distinct V_{gs} point starting from amplitude $V_{gs,max} = 1$ V. Figure 4.11(b) depicts a recorded pulse and the pulse response of the Si GAA NW n-TFET as an example for a gate voltage at 1 V. A low duty cycle is implemented setting the high pulse duration to 30 µs which repeats every 2 ms. This allows the device under test to reset the charge trapping condition for most of the time ($t_{low} = 66 \cdot t_{high}$) while being switched on for extremely short times. In this way a pulse train of the same pulse can be applied for averaging purposes. The data point (vg_{meas},vis_{meas}) is extracted from the top of the pulse at a certain time after the pulse rising edge (e.g. $t_{meas} = 10$ µs). In this manner, further gate voltage pulses with decreasing amplitude are applied to complete the data set for the region of interest in the transfer characteristic. Note that before extracting the data point of each pulse, an averaging of about 1000 waveforms is performed to reduce noise.

The result of the PIV measurements on the sSi GAA NW n-TFET at V_{ds}= 0.1 V is shown in Figure 4.12 including the pulse response of the device at $vg = 0.88$ V, 0.68 V and 0.58 V. We choose the extraction time for the single data point at $t_{meas} =$ 10 µs and 5 µs to examine the TAT influence at shorter pulse duration. If t_{meas} is

[8] Note that the gate voltage and the output voltage signal (corresponds to the device current) extracted from the oscilloscope is labeled as *vg* and *vis*.

chosen too small a region will be considered where the pulse is not yet constant. As shown Figure 4.9(a-c), we observe a strong peak at the rising pulse edge followed by an RC-delay. The strong overshoot at the beginning of the pulse is reported as displacement current which originates from charging and discharging of the gate-source

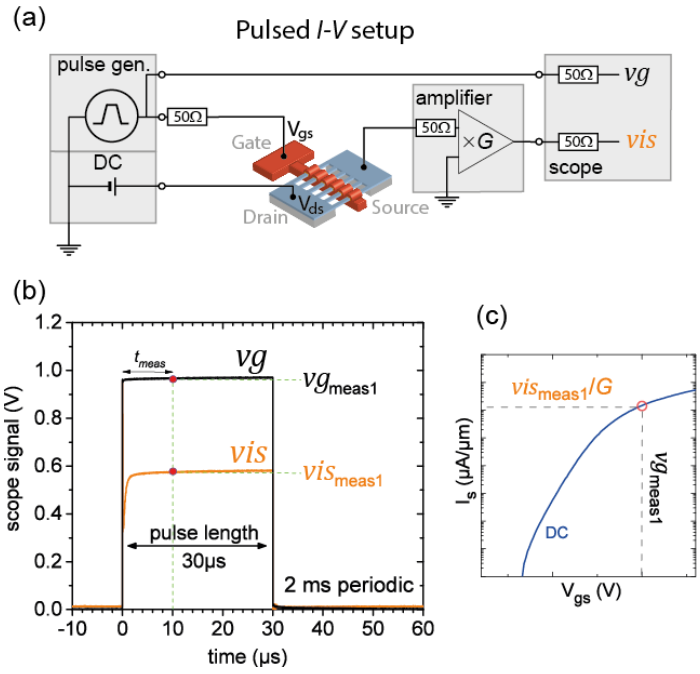

Figure 4.11: (a) Circuit configuration of the pulsed *I-V* setup to measure the sSi NW GAA n-TFET. (b) The oscilloscope waveforms of the incident gate pulse *vg* = 1 V with a length of 30 µs and the resulting output voltage pulse *vis*. The pulse is repeated every 2 ms. In this example the data point is taken after t_{meas} = 10 µs on the top part of the pulse. (c) Plot of the data point extracted from the pulse to the DC the transfer curve for comparison. More pulses at different *vg* are necessary to investigate the region of interest.

(C_{gs}) and gate-drain (C_{gd}) capacitance during the rise and fall time [141]. The RC-delay describes a characteristic time constant needed for charging the gate. Its value is a combination of the parasitic capacitances of the measurement setup and the gate capacitance of the device itself. Hence, steeper behavior is wrongly interpreted at such small t_{meas} because the TFET is not fully charged to the targeted gate voltage when

the current is sampled leading to false conclusion of trap suppression. It is worth mentioning that we prefer the approach of applying a pulse with a fixed time duration of 30 µs and extract the data at the desired time t_{meas} rather than using several pulses with different time durations (e.g. 5 µs and 10 µs). In fact, there is no difference, except that the duty cycle is changed without having any impact on the results. We average the data points at the extraction time over a certain time window of 500 ns indicated as boxes in the pulse response shown in Figure 4.12(a-c). A small DC offset is commonly introduced by the amplifier and becomes more obvious for smaller gate voltage pulses since the overall pulse is smaller in this case (low level vis_{low} is not exactly at 0 V). To avoid measurement errors we need to subtract vis_{low} from vis_{high} to obtain the corrected vis_{meas} value. By dividing vis_{meas} with the applied gain G leads to I_s.

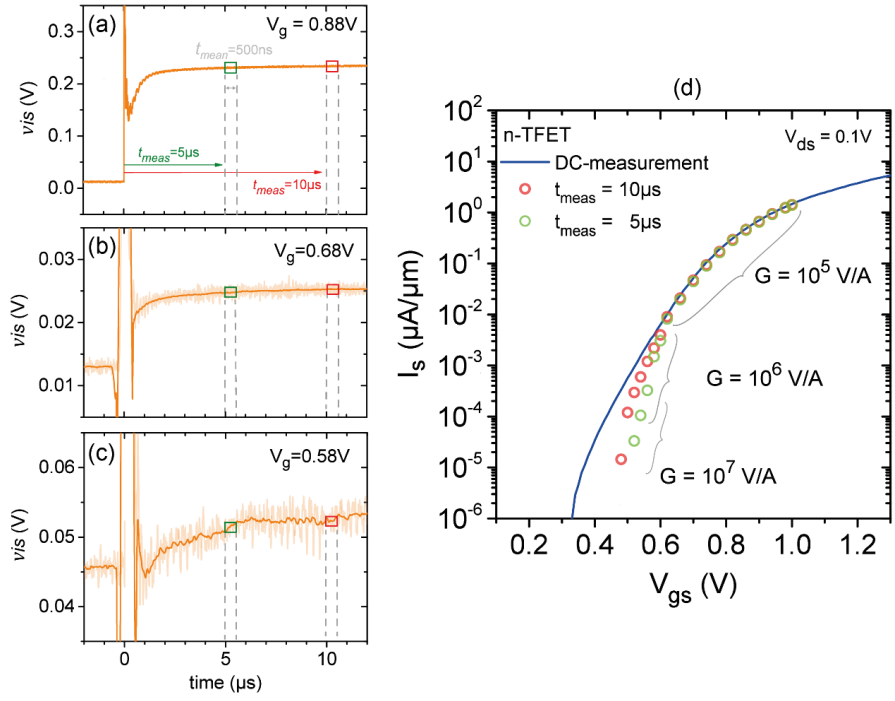

Figure 4.12: (a-c) Various output pulses for different gate voltage configurations while keeping V_{ds} at 0.1 V. *is* current has been extracted at t_{meas} of 5 (green) and 10µs (red) averaging the data points within a window of 500 ns. (d) The extracted data are plotted against the DC sSi GAA NW n-TFET transfer characteristics. Note that the extracted data *vis* has to be divided by the corresponding amplification value G to obtain the current value I_s.

It has been verified that I_d and I_s are similar with the difference that I_s takes the gate current into account and therefore limits the achievable current minimum floor ($I_s > 10^{-6}$ µA/µm). However, data points at this low current range are discarded due to the oscilloscope resolution limitations. Post processing of the measured pulse response was performed to reduce the large peak to peak noise for larger gain G, especially for low gate voltages as depicted in Figure 4.12(c).

The extracted pulsed I-V points for distinct V_{gs} are plotted in Figure 4.12(d) along with the DC measurement at $V_{ds} = 0.1$ V. The red data points represent the measurement at $t_{meas} = 10$ µs of the pulse showing perfect agreement with the DC transfer characteristic at high gate voltages but deviations occur at gate voltages below 0.6 V. The pulsed I-V points fall off steeper in this region. The trend is more striking for smaller t_{meas} as shown for the data points $t_{meas} = 5$ µs. Figure 4.13 illustrates the SS of the PIV curves in dependency of the normalized I_d. The steeper switching behavior is highlighted here by the improved I_{sub60}-current transition from $1 \cdot 10^{-5}$ µA/µm to $3 \cdot 10^{-2}$ µA/µm.

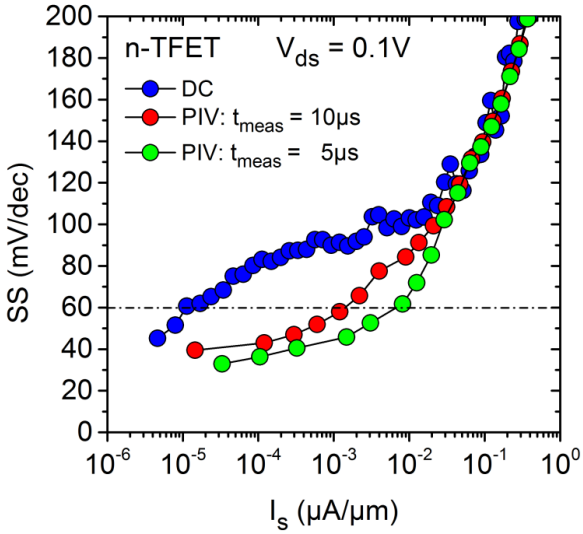

Figure 4.13: Extraction of SS vs. I_d of the corresponding transfer characteristic shown in Figure 4.12. The PIV measurement results indicate SS improvement over the DC measurement due to decreased influence of TAT.

At high gate voltages the TFET is obviously in the ON-state where BTBT is confirmed to be the dominant mechanism. Whereas at lower gate voltages the BTBT

contribution is reduced since the tunneling window shrinks and TAT governs the overall device current. We suspect that the decrease in current in the subthreshold regime with PIV is linked to the suppression of partial traps states with trap life times t_r longer than t_{meas}. According to Tyagi *et al.* the trap life time inside doped Si is influenced by the impurity concentration which can be in the range of several micro seconds [142]. While Young *et al.* observed oxide related de-trapping enhancement up to 5 µs with pulse measurements, they conclude that oxide trapping-free characteristics are obtained when going for faster PIV measurements [138]. These reports might explain the improvements in our considered pulsed time range assuming that our devices mainly suffer from traps at the oxide interface and within the semiconductor material.

Independent from our group, Smets *et al.* used a similar PIV setup to analyze trap degradation in different III-V TFETs [141]. They could observe an improved ON-current performance by suppressing large concentration of oxide/interface traps. These charged traps screen off the gate electric field causing a V_{gs} stretch-out during DC measurements. The results became more significant when the device was cooled down to $T = 4$ K when performing PIV. They assume that the trap lifetime t_r increases with decreasing temperature, as also predicted by Tyagi *et al.* [142] and Vais *et al.* [136], enabling a stronger trap suppression. However, Smets *et al.* did not see any difference between DC and PIV measurements when it comes to the subthreshold regime for time scales down to $t_{meas} = 0.5$ µs.

One possible reason for TAT being influenced even at longer pulses in our Si GAA TFETs might be explained by the different semiconductor body material with different energy trap levels in the channel as compared to the III-IV materials. According to Equation (4.1) and estimations in the literature [134], charge interaction with mid-gap traps happens at rather large time constants $1\,\mu s < t_r < 1$ ms. Whereas, charge trapping close to the band edge dissolves at much shorter time constants ($t_r <$ 1 ns) [136]. Therefore, we conclude that the Si GAA TFETs have negligible trap concentration within the oxide, since we do not observe any change in the ON-current during PIV. Instead, based on the improvement in the subthreshold regime, we assume that large mid-gap trap concentrations are present in the body material and at the Si/HfO_2 interface.

In general, the PIV method which has been developed to analyze oxide traps in gate stacks, may provide evidence for the presence of traps in TFETs. However, since the region of interest in TFETs lies in the OFF-state current it is quite challenging to obtain fully suppressed trap characteristics for extremely short PIV ($<$ 500 ns) which is highly susceptible to measurement errors.

4.4 Temperature dependent I-V measurements

In this chapter the subtreshold analysis of the fabricated TFETs has been extended to gain more physical insights by performing DC measurements at various temperatures T. The samples were mounted on a probe station which has the option to heat up (~500K) or to cool down with liquid nitrogen (~77 K). Temperature dependent measurements of an n-MOSFET will be shown in the following to indicate the difference to the n-TFET. The transfer characteristics I_d-V_{gs} of an n-MOSFET are presented in Figure 4.14 fabricated with the same process as the sSi GAA NW TFETs with the only difference that both source and drain are doped with P. Sweeping the temperature from 400 K down to 80 K indicates a large temperature dispersion in the subthreshold regime because current conduction in MOSFETs relies on thermal excitation over the channel potential barrier. At lower temperatures the Boltzmann tail vanishes and the carrier distribution at the source is mainly determined by the Fermi energy level so that the channel barrier has to be reduced by further increase of the gate potential in order to achieve the same current level as compared to room temperature. This results in a steeper slope since SS is proportional to T (see equation (2.8)) and shifts the threshold voltage V_T to larger voltage values. Beyond the subthreshold regime the ON-current increases with low T due to the fact that the carrier mobility improves within the channel [143].

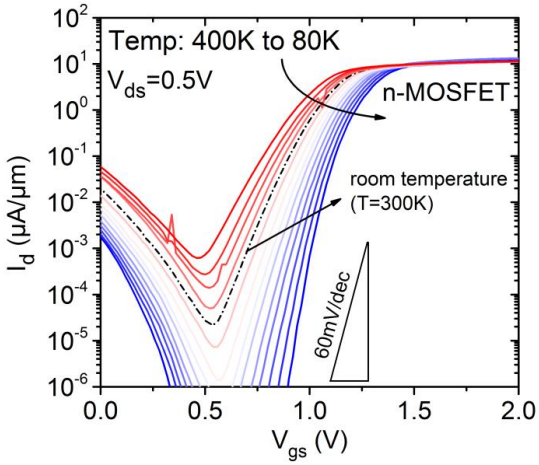

Figure 4.14: Measured transfer characteristics of an n-MOSFET with sSi GAA NW array at different temperatures. The gate has a length of 250nm and the NW width and thickness amount to 50 nm and 5 nm, respectively.

In contrast, the achievable TFET currents at low temperatures are not limited by the mobility but rather by the bandgap which primarily determines the tunneling distance. Less temperature sensitivity in comparison to MOSFETs is expected for ideal TFETs due to energy filtering that blocks the Boltzmann tail of the Fermi distribution function. The measured temperature dependent transfer characteristics of a sSi GAA NW n-TFET with NW width of 50 nm and thickness of 5 nm in thickness is depicted in Figure 4.15 for (a) V_{ds} = 0.1 V and (b) 0.5 V. The ON-state is less temperature sensitive down for $V_{gs} \geq 1$ V while the current below the threshold is reduced by about four orders of magnitude for T in the range of 400K to 80 K. Thus, we observe that the transfer curve gets much steeper and the onset shifts to larger V_{gs} at smaller temperatures T independent of V_{ds}. Similar behavior of the current can be seen in the ambipolar current branch marked in yellow. For low temperatures (T < 250 K) the OFF-current is extremely small falling below the resolution limit of the measuring setup which explains the flattening of the OFF-current. Because of that a larger separation of the actual ON-current and the ambipolar current branch is observed for lower T. Note that the slight OFF-current hump observed in Figure 4.12(a) at V_{ds} = 0.1 V is caused by the parasitic current stemming from the gate. Apparently the continuous stressing of the gate during the measurements led to an increased gate leakage current.

Because of the energy filtering principle, the current of TFETs is supposed to be less temperature dependent but instead is sensitive to changes of the tunneling probability T_{WKB}. Indeed, for gate voltages larger than 1 V BTBT is apparently the dominant charge transport mechanism confirmed by the small temperature dispersion. The slight current change proportional to T can be attributed to the change of the Si bandgap energy E_g with changing temperature [22]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{4.2}$$

where $\alpha \approx 4.73 \times 10^{-4}$ eV/K and $\beta \approx 636$ K are material dependent constants well known for Si [144]. $E_g(0)$ denotes the Si bandgap at 0 K which has a value of 1.17 eV for unstrained Si. Thus, the bandgap is reduced by about 70 meV from 80 K to 400 K. Due to the T_{WKB} equation (2.14) this reduction has an exponential dependency on I_d as a consequence, hence, a small increase is observed in the logarithmic scale in Figure 4.15. In addition, temperature dependent phonon distribution may also affect the transfer characteristics since BTBT in indirect bandgap materials such as Si relies on the assistance of phonons.

In the subthreshold region, however, the presence of trap states in the tunnel junction give raise to parasitic TAT and SRH currents. Their contribution to the total current strongly depends on temperature and is the main reason why SS remains above the thermal limit of $\ln(10) \cdot k_B$ over the whole temperature range. The extracted SS vs.

T for V_{ds}=0.1 V in Figure 4.16 demonstrates the SS degradation for both n-and p-TFETs for elevated temperatures. A drastic increase of SS is observed for T>300 K where strong charge carrier trapping is more likely. When the temperature is reduced, the SS decreases to 40 mV/dec at 80 K. In this case, parasitic charge transport by thermal excitation of carriers originate from trap states are reduced. The band pass filtering configuration of the TFET is lost due to the presence of traps. Instead, the high energetic Boltzman tail re-appears which explains why the SS follows the thermal limit at best. Only by suppressing TAT suggests a pure BTBT performance of the TFET that is only limited by its physical constraints which are dependent on material specific parameters such as bandgap, effective mass, doping profile and geometry. SRH contribution is fairly low in the sSi GAA NW TFETs and only noticeable at low V_{ds}=0.1 V and T above 300 K where the ambipolarity branch and ON-current branch are greatly separated from each other as depicted in Figure 4.12(a). Therefore, we conclude that the OFF-current is mainly limited by TAT.

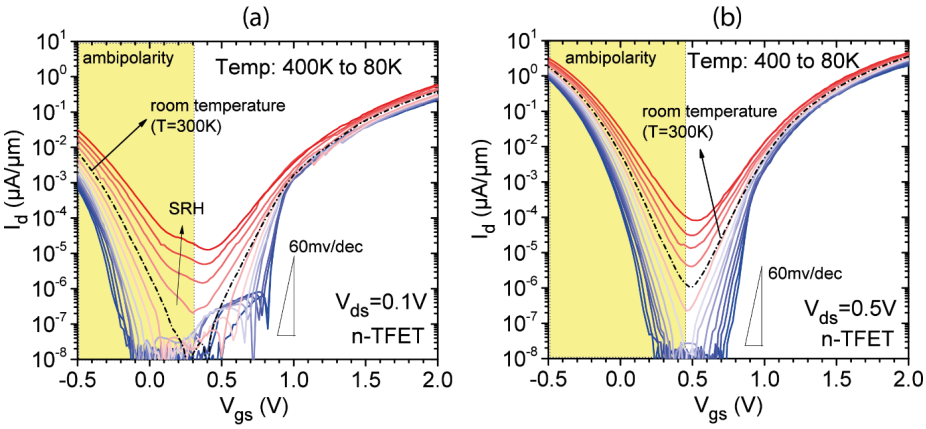

Figure 4.15: Transfer characteristics of an sSi GAA NW n-TFET measured at temperatures ranging from 400 K to 80 K at (a) V_{ds} =0.1V and (b) V_{ds} =0.5 V. Each NW has a cross-section of 50×5 nm^2 and a gate length of about 250 nm.

For further analysis of the trap induced charge transport mechanism in the transfer characteristics the activation energy E_a has been extracted from the temperature dependent I-V measurements of the sSi GAA n-TFETs. Depending on the E_a value additional conduction mechanism relying on thermal excitation can be identified. Calculating the activation energy E_a requires an Arrhenius analysis of the measured data [28][145][146]. The I-V data obtained in Figure 4.15 is presumed to have an exponential dependence to the thermal energy k_BT:

$$I_d \propto \exp\left(-\frac{E_a}{k_B T}\right) \tag{4.3}$$

Taking the natural logarithm yields a linear function of the form $y = mx + b$ with E_a being the slope and $1/k_B T$ the dependent variable. The Arrhenius plot is shown in Figure 4.17(a) for the sSi GAA NW n-TFET at $V_{ds} = 0.5$ V covering the whole range from the OFF to the ON-state ranging from V_{gs}=0.5 V to 1.5 V. Noticeable change in current occurs at 220 K upwards, whereas below that temperature dependence is fairly weak as obvious from the horizontal line. Note that for gate voltages close to the OFF-state, corresponding to $V_{gs} \leq 0.7$ V, the curve flattens rapidly for low temperatures due to the limited current resolution of the measurement setup. Therefore, E_a extraction is only performed in the temperature range from 220K to 400K.

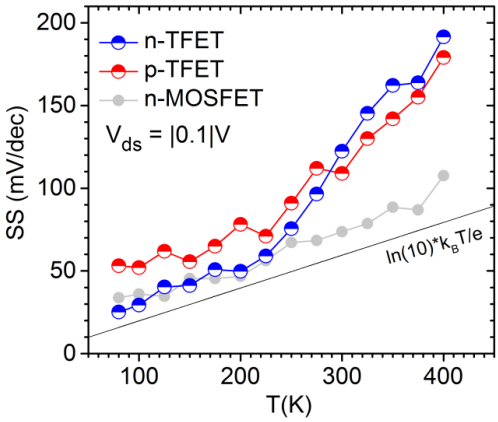

Figure 4.16: Inverse subthreshold slope SS vs. temperature T for the n- and p-TFET including the n-MOSFET for comparison. All devices feature gate-all-around NWs with 50 nm width and 5 nm thickness.

Fitting the slope for each V_{gs} curve results in an energy value which is plotted in Figure 4.17(b). The voltage region with high activation energies indicates where SRH and TAT is likely to take place due to the fact that E_a reflects an energy barrier height that requires such thermally assisted conduction mechanics. The largest peak for the activation energy is located in the OFF-state corresponding to $V_{gs} \leq 0.5$ V with a value of 0.45 eV, which is evidently smaller than half of the Si bandgap. Therefore, the minimum OFF-current cannot be just explained by SRH carrier generation whose main contribution arises from the intrinsic carrier concentration n_i which is proportional to $\exp(-E_g/2k_B T)$ according to equation (2.22). In addition, other thermionic based

mechanisms such as TAT are likely to retain the lower device current limit. This agrees with the findings in the transfer characteristics where SRH is only observed for low V_{ds} (Figure 4.15). In fact, TAT from the ON- and ambipolar current branch intercept, obscure SRH which explains the much smaller width of the energy peak for $V_{ds} = 0.5$ V in the OFF-state (Figure4.17(b)). In contrast, BTBT is assumed to be present for energies E_a below 0.1 V [147]. This is the case for $V_{gs} = 0.9$ V and fits to the assumption presented in Figure 4.15 where the temperature dependence of the transfer characteristics becomes much weaker due to BTBT dominance in the total ON-current. The transition from the OFF to ON-state namely at activation energies of 0.45 eV to 0.1 eV happens in a small gate voltage range of about ΔV_{gs}=0.4 V. An abrupt transition is desired to avoid the intermediate region dominated by TAT and thus improves the TFET switching characteristic.

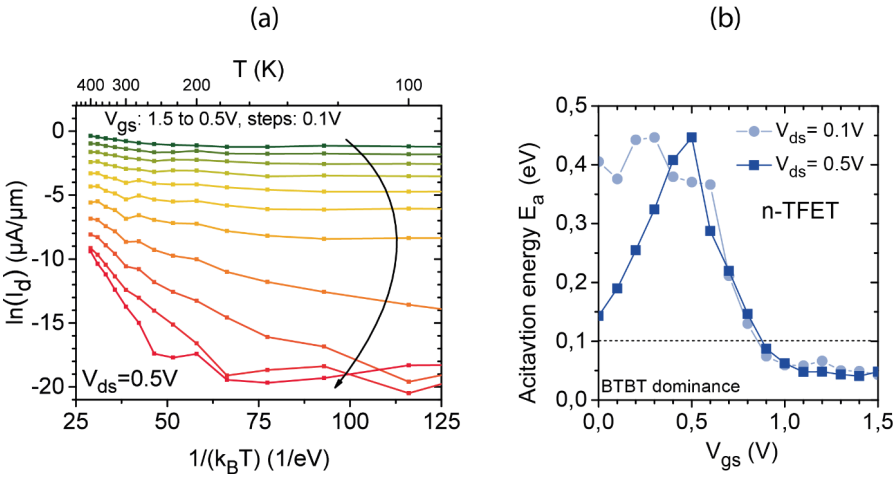

Figure 4.17: (a) Arrhenius plot of sSi GAA NW n-TFET at $V_{ds} = 0.5$V and for various gate voltages. The activation energy E_a is extracted from the slope of each curve. (b) E_a is plotted against V_{gs} indicating the dominance of TAT and BTBT.

4.4.1 Bandgap estimation from SRH current

The bandgap of the sSi NW GAA n-TFET can be approximated by utilizing the SRH generation- recombination current from the temperature *I-V* measurements. According to Figure 4.15 this characteristic current only appears in the OFF-state at $V_{gs} = 0.2$ V for low $V_{ds} = 0.1$ V so that SRH is not obscured by the TAT contribution. Thus we

can assume that the total current I_d is set up by SRH which is proportional to the intrinsic carriers and defined as [28]:

$$I_d = n_i \propto T^{1.5} \exp\left(-\frac{E_g}{2k_B T}\right) \tag{4.4}$$

Transformation of equation (3.16) for the Arrhenius plot allows the determination of E_g from the slope of the following linear equation:

$$\ln\left(\frac{I_d}{T^{1.5}}\right) = -\frac{1}{2k_B T} E_g \tag{4.5}$$

The Arrhenius plot in Figure 4.18 presents the SRH peak currents measured at temperatures above 225 K. However, the current trend below 275 K saturates due to the resolution limit of the setup. Hence, we only consider the data points from $T = 275$ K to 400 K to extract the bandgap. A linear fit of these results in $E_g = 1.01$. Compared to the band gap of conventional Si ($E_g = 1.12$) this value is about 0.11 eV smaller. The initial strain along the NW is supposed to be 0.8 % which causes a bandgap reduction of 50 meV (see chapter 3.1.1). Probably the estimated band gap is too optimistic since we did not consider the temperature dependence of the bandgap in this extraction approach. However, previous work reported that TiN metal gate deposit from the AVD creates great compressive stress with more than 1% at a thickness of 60 nm to Si layers [93]. Therefore, we assume that the additional band gap decrease stems from the tensile strain enhancement on the sSi NWs of the TiN metal in the gate stack.

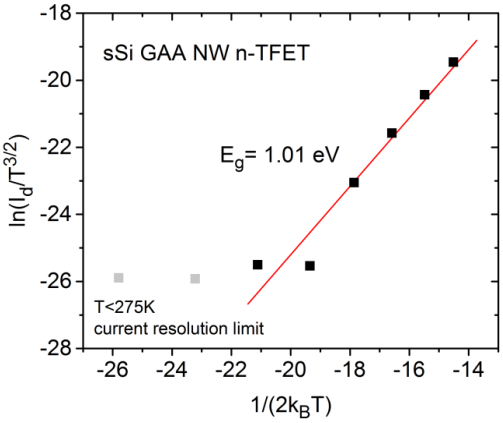

Figure 4.18: (a) Arrhenius plot of the SRH current measured from a sSi GAA NW n-TFET to extract the band gap. Only SRH current from 275 K to 400 K were considered here because for lower temperature the current is limited by the measurement setup.

4.4.2 Trap level estimation

Trap assisted tunneling is the most detrimental mechanism in the subthreshold regime of the transfer characteristics indicated in Figure 4.15 causing an SS dependence on the temperature. The reason is the thermally assisted transport in the TAT process once the charge carriers enter a trap state. By modeling TAT in TFETs as the Poole-Frenkel mechanism (see chapter 2.4) a relation between temperature dependent *I-V* data and the barrier height ϕ_B can be created [28][30]. A schematic of the Poole Frenkel emission process is illustrated in Figure 4.19(a) highlighting the thermal excitation of carriers from a trap state described as a notch in the conduction band with the height ϕ_B. Calculating ϕ_B by using the Arrhenius analysis simply reflects the trap level within the band gap from point of view of the conduction band edge. The equation (2.19) of the Poole Frenkel emission current is modified for the Arrhenius plot as follow:

$$\ln\left(\frac{I_d}{V_{gs}}\right) = \frac{1}{k_B T}\left(2\sqrt{\frac{e(V_{gs}-V_{off})}{4\pi\varepsilon_0\varepsilon_{ox}d}} - \phi_B\right) \tag{4.6}$$

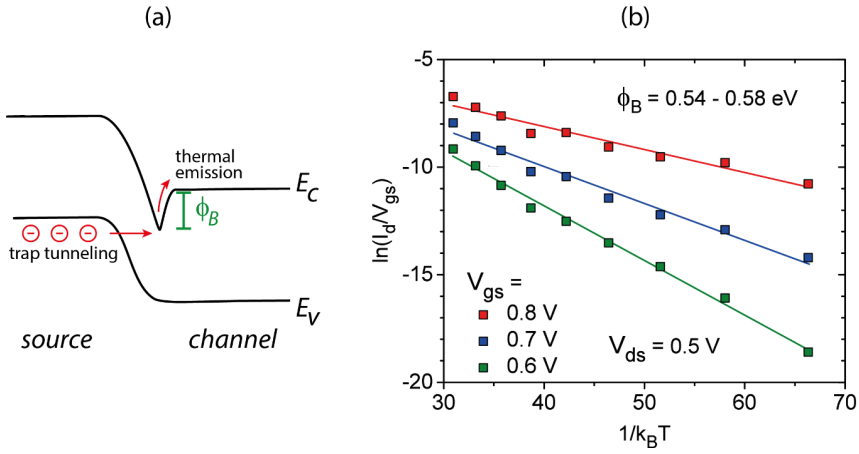

Figure 4.19: (a) Schematic of the Poole-Frenkel mechanism in an n-TFET where the band gap is effectively reduced due to trap states. A trap with an energy below the conduction band can be described as a potential barrier with the height ϕ_B. (b) Extraction of ϕ_B by applying the Arrhenius analysis on the Poole-Frenkel mechanism for different gate voltages.

From the best line fit of the current data points, a slope m can be extracted for calculating the energetic barrier height of trapped carriers:

$$\phi_B = 2\sqrt{\frac{e(V_{gs} - V_{off})}{4\pi\varepsilon_0\varepsilon_{ox}d}} - m \tag{4.7}$$

The result is shown in Figure 4.19(b) for the temperature dependent *I-V* data of the sSi NW GAA n-TFET measured at $V_{ds} = 0.5$ V. According to the transfer characteristics in Figure 4.15(b) and the activation energy plot in Figure 4.17(b) the gate voltage has to be around 0.5 V to 0.9 V to address the subthreshold regime where TAT is dominating. Thus, three distinct gate voltages at $V_{gs} = 0.6$, 0.7 and 0.8V are considered for the extraction to improve the statistics. The oxide thickness d corresponds to the equivalent oxide thickness (EOT). According to the TEM image of Figure 4.4 the thicknesses of HfO_2 is 2.8 nm and the SiO_2 interfacial layer about 1.3 nm resulting in an overall EOT of 1.81 nm. A barrier height of $\phi_B = 0.54$ -0.58 eV has been extracted, which is roughly in the range of $E_g/2$ of the sSi band gap. This suggests that the corresponding n-TFETs suffer from mid-gap traps which cause a degradation of the slope and prevent sub-60 mV/dec switching. Only at low temperature the traps "freeze out" enabling TFET switching without TAT contribution.

4.5 Density of interface states

Apart from traps in the semiconductor material, defects located at the gate oxide and sSi channel interface are also a source for TAT contribution. Moreover, charged interface states can screen the applied gate voltage and degrade the control of the channel potential. Therefore, it is important to characterize the quality of the HfO_2/sSi interface of the processed sSi NW GAA TFETs. In chapter 3.2.1 the conductance method was introduced as indirect method to extract the density of interface states D_{it} , which is commonly used for MOS capacitors. However, due to the scaled NWs in this device architecture the true capacitance of the device is very small and is usually disguised by parasitic capacitances. This limits the accuracy of this method making it inappropriated for GAA NW TFETs.

A more reliable and precise method allowing an in-depth analysis of the interface is provided by the Charge Pumping (CP) measurement [148]. The conventional CP approach was first designed for Si-Bulk MOSFETs where the charge pumping current I_{cp} is measured between the electrically short S/D and the bulk material. In order to extend this approach to SOI based devices, a gated p-i-n junction is needed [149]. Since the proposed structure simply corresponds to the design of TFETs, we adapt the approach and set up the measurement as shown schematically in Figure 4.20 using the *Keithley SCS4200 analyzer*. A small reverse bias is applied on the p-i-n junction by

grounding the source and setting a positive voltage to the drain terminal[9]. The gate is pulsed where the choice of the pulse voltage configuration should enable an alternation between accumulation and inversion conditions.

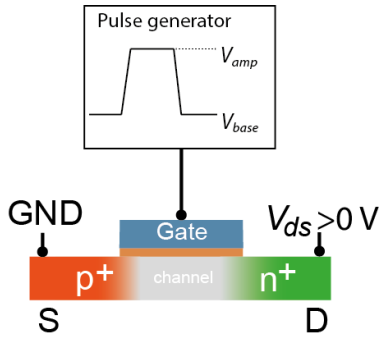

Figure 4.20: Charge pumping setup for Si NW TFET. The p-i-n structure is reverse biased while the gate is pulsed to electrically 'pump' the device from accumulation into strong inversion.

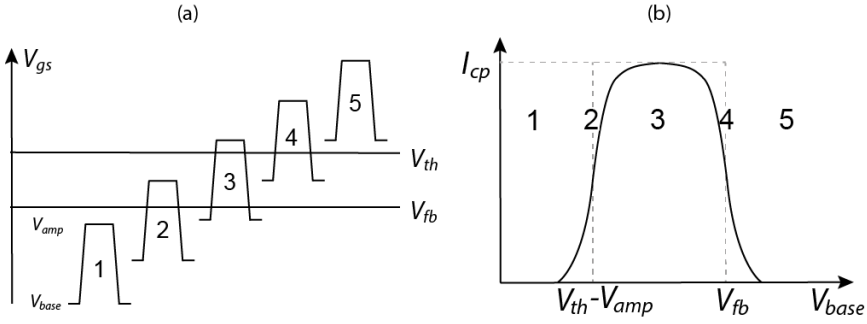

Figure 4.21: (a) Schematic illustrating the basic principle of the charge pumping technique with base voltage sweep V_{base} and constant pulse amplitude V_{ampl}. (b) The CP current I_{cp} for the corresponding gate pulse configuration (after [150]).

For an incident gate pulse, the transistor is switched from accumulation to inversion where the channel strongly depletes and electrons accumulate below the gate filling the traps at the interface. After a short pulse duration which is shorter than the trap

[9] Assuming that the corresponding device is a n-TFET

lifetime, the channel is pumped back into accumulation attracting holes as majority carriers from the drain side. These carriers recombine with the electrons trapped at the interface giving rise to a recombination current. This net current flow is designated as the charge pumping current I_{cp} measured at the drain. A common measurement routine of charge pumping is the application of a pulse sequence with constant amplitude V_{ampl} and variation of the voltage base level V_{base}, called base-level charge pumping. The schematic of the working principle is illustrated in Figure 4.21 showing a base voltage V_{base} sweep of the pulse and the resulting charge pumping currents. The maximum I_{cp} is reached in the third case depicted in Fig. 4.21 where the base voltage of the pulse is below the flat band voltage ($V_{base} < V_{fb} - V_{ampl}$) and the pulse amplitude exceeds the threshold voltage ($V_{ampl} > V_{th} - V_{fb}$). In this case the pulse scans the entire band gap energy and provides I_{cp} that corresponds to the maximum amount of traps.

However, under realistic conditions parasitic currents such as gate leakage through the thin oxide and the contribution of BTBT current from the highly doped source and drain may add up to the measured I_{cp}. According to *Masson et al.* [151], the parasitic part can be compensated by measuring the I_{cp} at low frequencies (f=1 kHz) and subtracting it from the initial CP results at higher frequencies. The CP current I_{cp} is proportional to both the pulse frequency f and the amount of interface traps per area N_{it}:

$$I_{cp} = N_{it} A f e \tag{4.8}$$

with A ($= W \cdot L_g$) describing the gate area and e being the elementary charge. The density of traps per energy can be obtained when $D_{it} = N_{it}/\Delta E$ is normalized over the energy interval given by $V_{th} - V_{fb}$. *Toledano et al.* reported that the CP current is a sum of both interface and oxide traps within the high-k material [152]. In this case individual trap levels can be accessed by changing the discharge time. This enables a spatial trap profiling with respect to the interface due to the spatial lifetime dependence of traps.

CP measurements have been performed on sSi GAA NW p-TFETs to determine the oxide interface quality after fabrication. Based on the information of the device transfer characteristics, shown in Figure 4.22(a), the V_{base} sweep starts from 0.8 V to -0.5 V to ensure the gate pulsing between accumulation and inversion. The pulse amplitude is set to V_{ampl} = -1.3 V and the frequency to f = 1 MHz. In addition, the CP measurements have been measured at a pulse frequency f = 1 kHz to determine the parasitic currents. The corrected I_{cp} curve is (blue) presented in Figure 4.19(b) as a function of V_{base}. A maximum current is observed at V_{base}= -0.1 V with I_{cp} = 24.8 nA for a device with an array 60 NWs with cross section of 45×5 nm^2 and a gate length

of 350 nm. By applying equation (4.8) the density of interface states N_{it} can be calculated which amounts to $7.3\times10^{12}\,cm^{-2}$. In comparison with the fabricated MOSCAPs utilizing the same gate stack process (presented in chapter 3.2.1) this value is about one order of magnitude higher. One of the greatest concerns for the increased interface states is the tilted ion implantation which cause damage in the thin high-k gate oxide at the gate edges. A high density of interfacial states is detrimental for TFETs due to their sensitivity to TAT. As reported by Sajjad et al. [29], D_{it} of the presented devices needs to be reduced to roughly $1\times10^{11}\,cm^{-2}$ (factor 70) to mitigate the TAT current significantly so that the BTBT current dominates in the subthreshold regime. MOSFETs with similar gate stacks were fabricated under tight industrial condition to prove that such small D_{it} are in practice achievable [153].

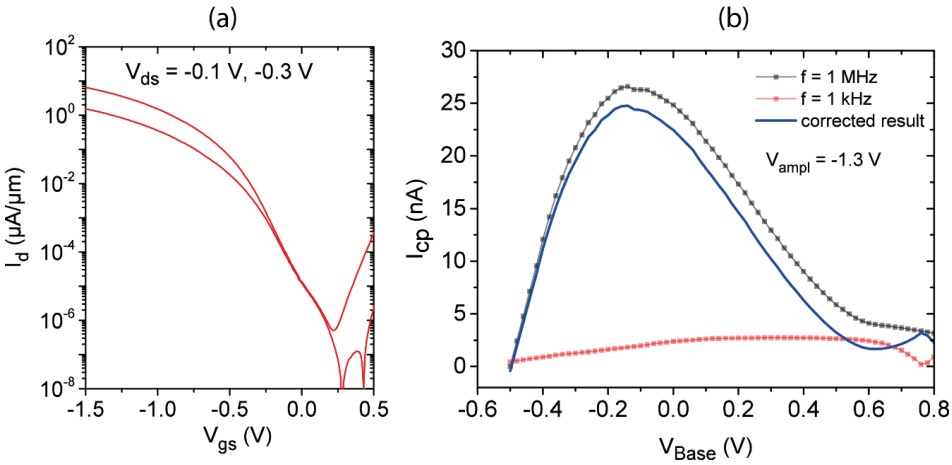

Figure 4.22: (a) Transfer characteristic of the considered sSi GAA NW p-TFET used for the charge pumping measurement with 60 NWs (45×5 nm^2 cross section per NW) and 350 nm gate length. (b) Charge pumping current I_{cp} vs. V_{base} after the parasitic current correction (blue curve).

4.6 Conclusion

TFETs based on strained Si NW-arrays with TiN/HfO_2 wrap gate have been demonstrated and electrically characterized. P- and n-type TFETs with comparable performance were realized providing I_d of 3 to 5 µA/µm at V_{DD}=0.5 V. In terms of the inverse subthreshold slope SS the n-TFET shows slightly better results than its p-type counterpart with 70 mV/dec for three orders of magnitude in I_d. At very low currents

several points of SS below 60 mV/dec are measured but degrades rapidly with increasing I_d. This striking result is more likely for sSi GAA NW n-TFETs. This is because of the application of boron at the source in combination with the IIS process results in higher activation than phosphorous which is also confirmed by the suppressed exponential onset in the output characteristics. All in all, the n- and p-TFETs performance presented here are similar to the state-of-the-art Si NW p-TFETs reported in [154] through the wrap gate architecture and small NW dimensions leading to improved gate electrostatics. Moreover, these Si devices indicate smaller bandgaps due to enhanced tensile strain that is induced by the TiN gate stack. However, many TFETs, especially the n-type, reveal strong performance fluctuations. One reason for this might be the difficulty to control the p-dopant profile at the source for such small scaled NWs since the diffusion coefficient is large for B in Si. Nevertheless, the results presented here demonstrate the potential of sSi GAA NW TFET to achieve SS $<$ 60 mV/dec under further optimized conditions.

Basic analog parameters are extracted with focus on the voltage gain A_V. As a result, remarkable high A_V has been measured for TFETs, in the same order as the state-of-the art NW p-TFETs. This is achieved by the improved gate electrostatic of the GAA NW architecture leading to higher currents and consequently larger transconducatnce g_m as well as small conductance g_d that implies good output saturation. Especially because of the latter parameter these scaled NW TFETs even exhibit voltage gain performances which surpasses equally scaled MOSFETs. Hence, the sSi GAA NW TFETs might be an interesting choice for specific analog applications, e.g. sensors, that operate at moderate frequencies.

Pulsed I-V measurements at room temperature reveal steeper switching in the subthreshold regime for pulses of several microseconds. Additional temperature dependent analysis shows strong temperature dependence of SS which is a sign for additional conduction mechanism relying on thermionic emission. For gate voltages exceeding a certain threshold the temperature dependence drops due to the dominance of BTBT between source and channel. Hence, both investigations provide evidence that trap assisted tunneling through mid-gap trap states is the major hindrance preventing SS$<$60 mV/dec of the sSi GAA NW TFETs. Apparently the employed IIS-process is not sufficient to eliminate all traps. We conclude that due to the tilted ion implantation the sSi close to the S/D channel interface is likely to be damaged so that the low temperature anneal is not sufficient to remove these defects. This also holds for the gate oxide which shows higher D_{it} values compared to fabricated non-implanted MOSCAPs. A solution to reduce the trap density may be achieved by sophisticated annealing strategy with the goal to remove crystal and high-k defects created by ion implantations but sustain a sharp doping profile. However, at low temperature measurements (T $\leq$ 80 K) the potential of the sSi GAA NW TFETs without the presence of TAT

current is demonstrated. The SS stays below 60 mV/dec for almost 4 order of magnitude in I_d due to the freeze-out of the traps states.

5. Inverters with complementary TFETs

A desired future scenario is the substitution of MOSFETs with TFETs to establish integrated circuits especially for low power applications. The key question hereby is the CMOS compatibility of the TFETs to adapt the established logic gate layouts as well as the interaction between several devices in a network. In this regard, complementary TFET (CTFET) inverters are taken as the first step to investigate and evaluate the feasibility of TFETs in circuit applications. So far, only few reports can be found on experimental CTFET based on Si since the implementation of n- and p-TFETs on the same chip is still challenging [19][155][20]. Recently *Mori et al.* managed to fabricate a 23-stage ring oscillator with Si CTFET [156] although the ambipolar behavior degrades the oscillator performance. Based on the study of the previous chapter we adapt the process of the sSi GAA NW TFET platform for both n- and p-type transistors and apply them on a single chip in order to fabricate complementary TFET inverters. Static inverter characteristics will be presented setting the focus on the inherent properties of TFETs to determine their impact on the inverter characteristics.

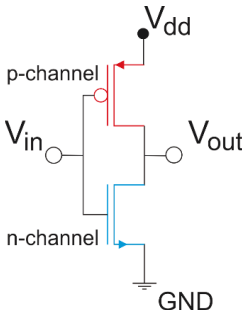

Figure 5.1: Circuit layout of a CMOS inverter composed of a p- and n-type MOSFETs. It is driven by the supply voltage V_{dd} which determines the maximum voltage swing between the high and low level.

5.1 Working principle of CMOS inverters

The inverter is the basic logic element in digital electronics. As the name suggests, this logical NOT-gate provides a negation of the input voltage V_{in} to the output $V_{out} = \overline{V_{in}}$. Hence, a logical "high" ($= V_{dd}$) input level is converted to a logical "low" (= 0 V) output level and vice versa. The CMOS inverter[10] as illustrated in Figure 5.1 utilizes complementary n- and p-type transistors. Both of them are electrically connected in series at the drain terminal where the output voltage V_{out} can be measured. The source terminal of the n-device is connected to the ground, while the source contact of the p-device is connected to the supply voltage V_{dd}. The input voltage V_{in} is applied to a common gate contact for both transistors. Based on this specific back-to-back configuration in combination with a shared gate, complementary switching is enabled meaning that only one of the two devices is turned ON depending on the applied V_{in}. For a high input voltage the n-device activates and pulls the output voltage of the inverter towards the ground potential acting as a pull-down transistor. Since the source terminal of the n-MOSFET is attached to ground the gate voltage corresponds to the inverter input voltage $V_{gs}^{n} = V_{in}$. In contrary, the source terminal of the p-type transistor is attached to the supply voltage which leads to the following effective gate voltage relation for the p-MOSFET $V_{gs}^{p} = V_{in} - V_{dd}$. Hence the p-MOSFET only switches ON for low V_{in} where the supply voltages are forwarded to V_{out} and thus function as a pull-up transistor.

The voltage transfer characteristic (VTC) $V_{out}(V_{in})$ of the inverter can be fully deduced by superimposing the current from the output characteristics I_{ds}-V_{ds} of the n- and p-devices. This so called load-line plot approach requires a common coordinate set. Such plot is depicted in Figure 5.2(a) where the coordinates and variables are the choice of the n-channel device. Hence, the current characteristics of the p-device has to be modified according to the relations (note that V_{gs}^{p} and V_{ds}^{p} are always negative):

$$\begin{aligned} V_{in} &= V_{gs}^{n} = V_{gs}^{p} + V_{dd} \\ V_{out} &= V_{ds}^{n} = V_{ds}^{p} + V_{dd} \\ I_{ds}^{n} &= -I_{ds}^{p} \end{aligned} \tag{5.1}$$

[10] Alternatively, the inverter can be implemented just by n-MOS or p-MOS logic which simplifiers the realization but sacrifices performance speed and especially suffers from higher power dissipation compared to the CMOS technique.

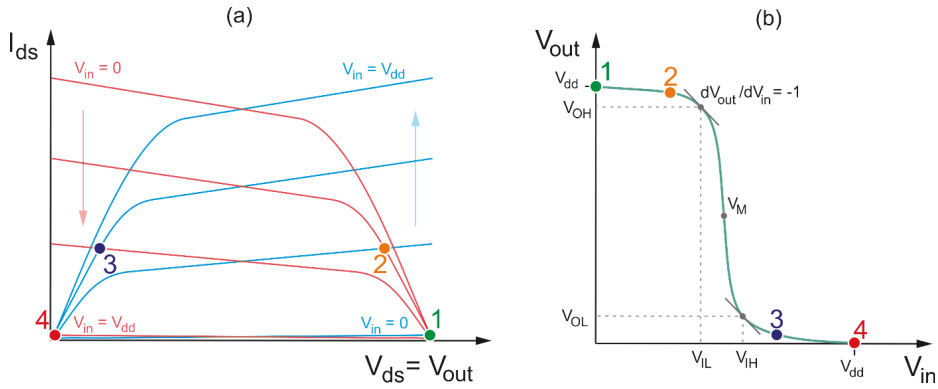

Figure 5.2: (a) Load-line plot of the n- (blue) and p-device (red) of the CMOS inverter. Each crossing point represents the current through both devices for a certain V_{in} and determines the resulting V_{out}. The arrows and numbers indicate the increase of V_{in} from 0 V to V_{dd}. (b) Corresponding voltage transfer characteristic of the inverter including the assigned V_{out} operating points.

where p and n subscripts in the current and voltage variables denote the corresponding device type. For each V_{in} a specific configuration of the load-line is established. Since the p- and n-transistors are connected on the same path, the current I_d flowing through both devices is supposed to be equal (Kirchhoff's 1. law). This means that the intersection of the load lines for a specific V_{in} determines the corresponding output voltage V_{out} point. The current read from the intersection point can be treated as the static leakage current of the inverter. Figure 5.2(a) highlights the different cases with numbers starting from $V_{in} = 0$ V to V_{dd}. It clearly shows that the device operating in the saturation regime dominates and sets the logic state of the inverter. The operation points V_{out} are assigned to the resulting VTC plot given in Figure 5.2(b) creating the characteristic shape of an inverter with its two logical states. V_M describes the switching threshold of the inverter VTC and is defined at $V_{in} = V_{out}$. At this point the inverter resides in an ambiguous state since both devices operate in the current saturation regime where a change of the input voltage leads to large output variation. By definition, this ambiguous transition region of the VTC extends to the point where the slope of the VTC curve, which corresponds to the voltage gain, is $dV_{out}/dV_{in} = -1$. In addition, this also sets the boundary points for the high and low input voltage (V_{IH}, V_{IL}) as well as high and low output voltage (V_{OH}, V_{OL}) as marked in Figure 5.2(b). A V_{in} signal larger than V_{IH} is considered as high level input while below V_{IL} as low level input and thus can be mapped to a valid logical state. A measure for the robustness of the inverter is the noise margin (NM) which defines a maximum tolerated voltage variation so that the logical state is not flipped. The noise margin for the high state is defined as:

$$NM_H = V_{OH}\text{-}V_{IH} \tag{5.2}$$

which can be easily understood when having two inverters connected in series. The high output voltage V_{OH} of the first inverter has to be as large as possible (maximum V_{dd}) so that V_{in} for the second inverter is well above V_{IH}. The same approach can be applied to the noise margin for the low state leading to:

$$NM_L = V_{IL}\text{-}V_{OL} \tag{5.3}$$

Based on these definitions the VTC should provide a very narrow transition region between the two logical states. Thus the gain at the threshold switching point V_M should be as large as possible. It is also desirable for having V_M located at $V_{dd}/2$ to allow symmetric values for NM_L and NM_H[11]. An ideal inverter VTC is a step function which would provide a maximum NM = $0.5\times V_{dd}$ for each high and low state, thus covers the complete voltage swing. Devices with output characteristics I_d-V_{ds} showing good output saturation and large current increase in the linear region are important requirements to approach the ideal inverter.

The total power consumption of the inverter is composed of two components a static P_{stat} and a dynamic P_{dyn} part. P_{stat} describes the consumption of the inverter during the hold case when one of the logical level is established and is given by:

$$P_{stat} = I_{dd} \cdot V_{dd} \tag{5.4}$$

with I_{dd} being the current flowing through both p- and n-device in the static case. This current depends on the inverter input voltage V_{in} and can be determined by using the load-line plot. P_{dyn} calculates the consumption when the inverter switches the logic states. Since in this case both transistors will turn on for a short duration (passing the transition region) a high short-circuit current is generated and hence for high switching frequency P_{dyn} generally has a significant higher contribution than P_{stat}. The dynamic power consumption is expressed:

$$P_{dyn} = C_{out} \cdot V_{dd}^2 \cdot f \tag{5.5}$$

where f is the switching frequency. C_{out} consider the charges in the load capacitances attached at the output of the inverter, e.g. gate of the next logical element and capacitances of interconnects. It also includes the internal parasitic capacitances from the n- and p-transistors. The resulting overall power consumption of the inverter is defined:

[11] Some applications, e.g. using inverters for signal level restoring, may need asymmetric VTCs.

$$P = C_{out} \cdot V_{dd}^2 \cdot f + I_{dd} \cdot V_{dd} \tag{5.6}$$

In terms of low power digital electronics the goal is to scale down the supply voltage. For inverters the limitation of scaling is given by the threshold voltage of the transistors. Once V_{dd} is at or even below this value the transistors operate in the subthreshold region. For the load-line plot this means that the saturation behavior is basically non existing leading to a VTC which is strongly degraded. Technically, the inverter still operates when the gain at V_M still exhibits a gain of -1. However, in this case $V_{OH}, V_{OL}, V_{IH}, V_{IL}$ coincide in the same V_M point so that any kind of noise level results into logic state flipping. In that sense, TFETs provides the opportunity to maintain the inverter performance at lower supply voltages due to the potential of superior subthreshold slope at smaller voltage swings.

5.2 Inverter based on sSi NW GAA CTFETs

The implementation of complementary TFETs in the inverter layout is shown in Figure 5.3 (left). It should be mentioned that there is no standard circuit symbol for TFETs. Thus, we employed the most common symbol with the bracket[12] indicating the source region [157][158]. The arrows denote the technical current flow from high to low potential. Similar to the CMOS design both p- and n-TFETs are connected back-to-back forming a common drain terminal which corresponds to the output of the inverter. The main difference is the configuration of the dopant types to establish the appropriate source and drain regions to allow the devices to operate in the reverse bias regime. In this case the n-doped source of the p-TFET is attached to the supply voltage V_{dd} while the p-doped source of the n-TFET is grounded.

The fabrication process of the CTFET inverter with sSi GAA NW TFETs depicted in Figure 5.3 (right) employs the top-down approach on the same strained SOI samples as explained in chapter 4.1. Some minor changes have been made for the CTFET inverter which will be briefly outlined. The mesa has been extended such that it includes two parallel NW arrays with 60 NWs each. Therefore, both devices are designed directly without the need of additional lithography steps for interconnects. A gate pad with two gate finger structure is applied to the NWs to enable a common voltage input terminal V_{in}. The gate stack consist of 3 nm HfO_2 as gate dielectric and

[12] The bracket has been adapted from the tunnel diode.

60 nm TiN as gate metal. $NiSi_2$ silicidation to the exposed sSi has been carried out to lower the resistance of the thin sSOI layer especially between the devices in the drain contacts. Prior to the tilted ion implantation into silicide (IIS) process, implantation windows are formed by electron beam lithography using PMMA resist as shadow mask. We created narrow stripe shaped windows according to the dopant species, e.g. for the n-dopant implantation, the source side of the NW p-TFET as well as the drain side of the NW

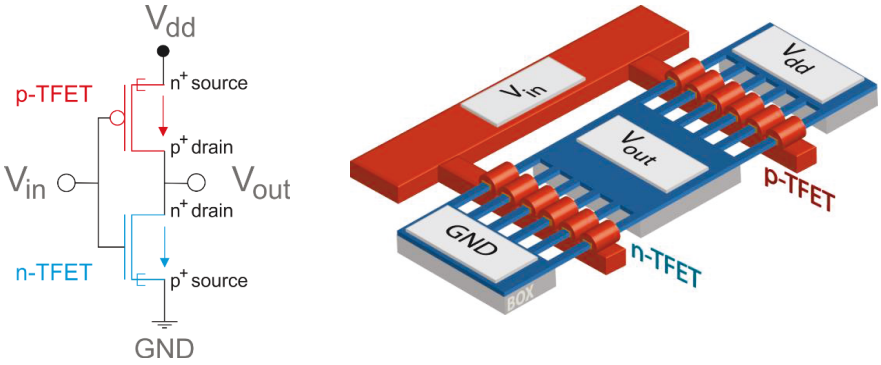

Figure 5.3: Circuit layout of a complementary TFET inverter highlighting the dopant configuration in source and drain as the main difference to the MOSFET design. The schematic on the right shows the implementation of the CTFET inverter based on sSi GAA NW p- and n-TFETs.

n-TFET are opened and vice versa for the p-dopants. Phosphorous and boron are employed as n- and p-dopants, respectively. If not particularly mentioned the implantation dose is set to $1{\times}10^{15}$ cm^{-2}. All details to the process steps are given in chapter 4.1.

5.2.1 CTFET inverter characterization

The normalized transfer characteristics I_d-V_{gs} of the sSi GAA NW p- and n-TFETs forming the CTFET inverter are plotted in Figure 5.4 (a), giving the information for which gate voltage the device is turned ON or OFF. The presented devices feature NWs with cross-sections of $40{\times}5$ nm^2 and a gate length of about 350 nm. Both transfer curves are very similar in terms of ON-current, a necessary condition to enable symmetric switching for the inverter. This also applies to the inverse subthreshold slope shown in Figure 5.4(b) where both transistors indicate an SS of 125 mV/dec in the

current region from 10^{-5} to 10^{-3} µA/µm. Compared to the single TFET in chapter 4, the n-TFET exhibits a higher inverse subthreshold slope, while the value of the p-TFET is well reproduced. When switching the device in the OFF state a significant ambipolar current is clearly visible caused by channel to drain tunneling. Furthermore, the transfer curves are shifted towards positive V_{gs} and are also separated by about 0.75 V with respect to their current minimum. Thus, a high absolute gate voltage is needed to turn on the n-TFET.

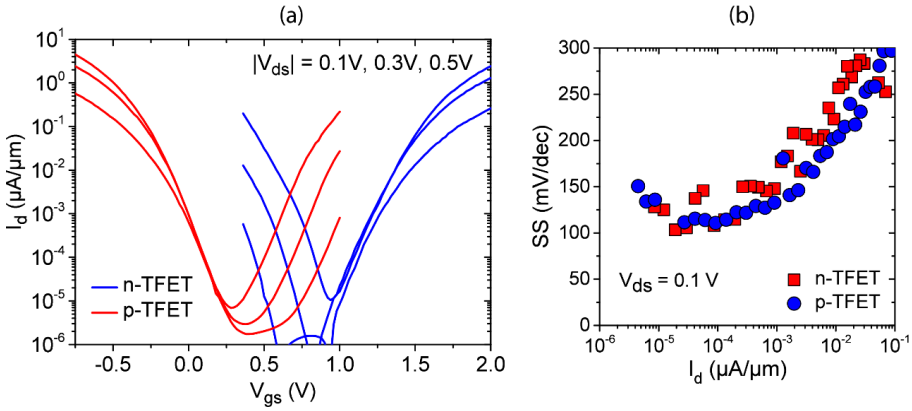

Figure 5.4: (a) Transfer characteristics I_d-V_{gs} of the sSi GAA NW p-and n-TFET on the same inverter layout for different V_{ds} with the presence of ambipolar behavior. (b) The corresponding inverse subthreshold slope SS at V_{ds}=0.1 V.

The output characteristics I_d-V_{ds} at different gate voltage configurations are measured for the p- and n-TFET. In Figure 5.5 (a-b) the output current is recorded for gate voltages corresponding to the device's ON-current branch from Figure 5.4(a). For comparison, the same gate overdrive voltage from $V_{OV}(=V_{gs}- V_{off}) = 0.1$ to 0.5 V is taken for both devices where V_{off} is extracted at currents of 1nA/µA. At supply voltages $V_{dd}(=V_{OV}=V_{ds}) = 0.5$ V the current amounts to 0.85 µA/µm for the p- and 0.35 µA/µm for the n-device, both with good current saturation. A super-linear increase ("S"-shape) for small V_{ds} is observed at the output curves for both TFET types. Apparently the dopant activation for this specific devices is not high enough to screen off the drain voltage dependence on the source-channel tunneling window [45]. In case the gate voltage is driven to the OFF state of the respective devices the ambipolar behavior is triggered. The impact of ambipolarity on the output characteristics is shown in Figure 5.5(c-d). Instead of the desired saturation behavior (grey) the current increases exponentially for rising V_{ds} as emphasized in log-scale.

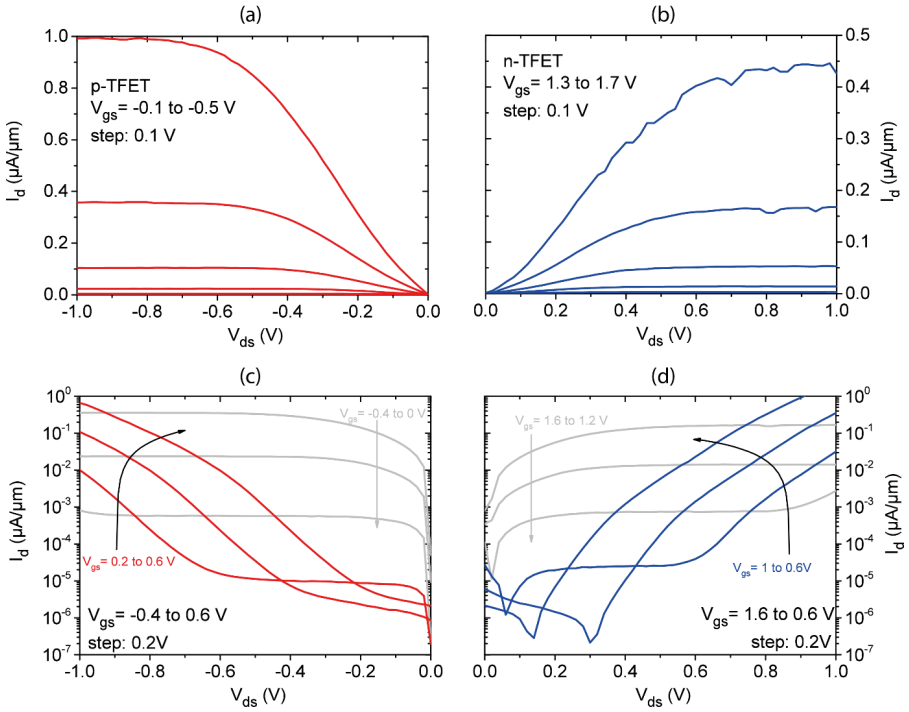

Figure 5.5: (a-b) Output characteristics I_d-V_{ds} of the p-and n-TFET extracted up to gate over drive voltages of 0.5 V. (c-d) The change in output behavior when V_{gs} is driven in the tranistor's OFF-state where ambipolar effects set in.

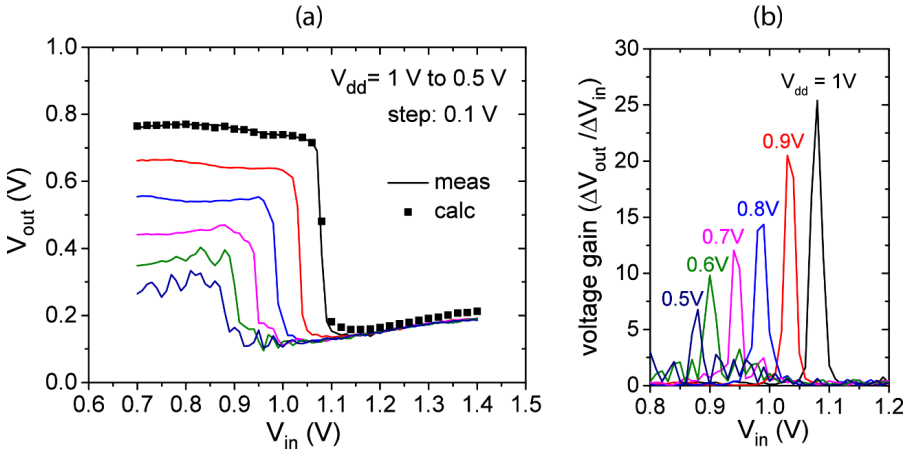

Figure 5.6: (a) Measured voltage transfer characteristics of the sSi GAA NW CTFET inverter. (b) Voltage gain extraction with the highest gain located at the threshold switching point V_M for each V_{dd}.

The voltage transfer characteristics (VTC) for the GAA NW CTFET inverter are recorded for V_{dd}= 1 to 0.5 V according to the setup in Figure 5.3. Because of the voltage shift and separation of the transfer characteristics the definition of the input voltage V_{in} has to be adjusted to allow both TFETs to switch on complementarily. Setting the V_{in} sweep from 0.7 to 1.4 V presents the result of the VTC in Figure 5.6(a). The inverter VTC provides two distinct and fairly constant logical states with a sharp transitions. The corresponding voltage gain $\Delta V_{out}/\Delta V_{in}$ in the transition region indicates a proportional dependence on the applied supply voltage, thus the highest (smallest) value is obtained for V_{dd}=1 V (0.5V) with a gain of 25 (6). However, the VTC shows a significant degradation: neither the maximum logical level (V_{dd}) nor the lowest logical level (GND) are reached. This is caused by the presence of ambipolar behavior.

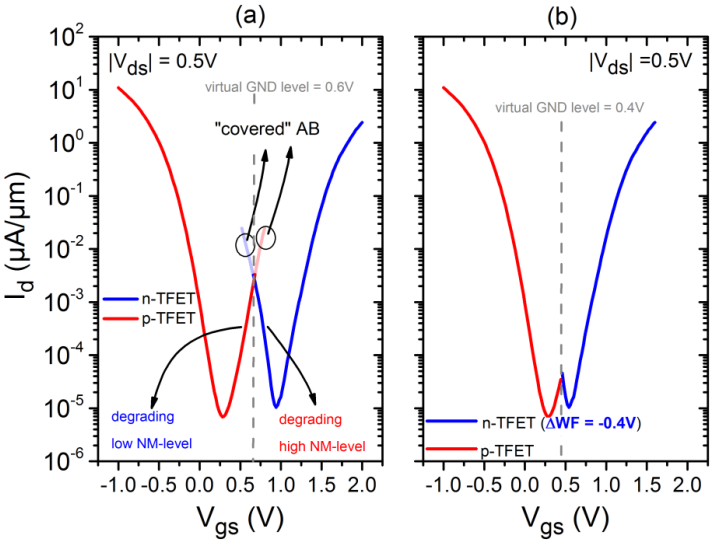

Figure 5.7: (a) Transfer curves of the CTFET at V_{ds}=0.5 V emphasizing the ambipolar current branch which degrades the inverter VTC. (b) Shifting the gate work function of the n-TFET by ΔWF = -0.4 V decreases the ambipolar effect. The "covered" current branches are effectively eliminated and are not considered in the inverter operation.

For instance, at low input voltage V_{in}=0.7 V and V_{dd}=1 V the p-TFET with $V_{gs}^{p} = V_{in}$-V_{dd} = -0.3 V turns on (see Figure 5.5(c)) and tries to pull V_{out} to V_{dd} but at the same time the n-TFET with $V_{gs}^{n} = V_{in}$ becomes conductive as it accesses the ambipolar region preventing the output voltage to reach V_{dd}. The same effect holds true when a high input voltage is applied. As a result the two logical levels is not separated by the full voltage swing given by V_{dd} which in turn affects the achievable noise margins. In case V_{dd}= 1 V the noise margin NM_H=0.2 V and NM_L=0.33 V for the logical high and

low level, respectively. Consequently, the noise margin is even smaller for scaled V_{dd} operation making this CTFET inverter with ambipolar effect extremely vulnerable to external noise interference in low power circuit perspective.

By taking a closer look at the transfer characteristics of the p- and n-device as depicted in Figure 5.7(a) the inverter only takes into account the part of the ambipolar branch that has a lower (higher) V_{gs} than the virtual GND level for p (n) devices respectively. This virtual GND defines the logical low voltage level of the inverter input and can be defined arbitrarily. In this case the V_{gs} at the crossing point of the p- and n-TFET transfer curves is chosen to be the virtual GND. Since the voltage beyond the virtual GND will not be applied to the device, the current information beyond this level is not relevant for the inverter

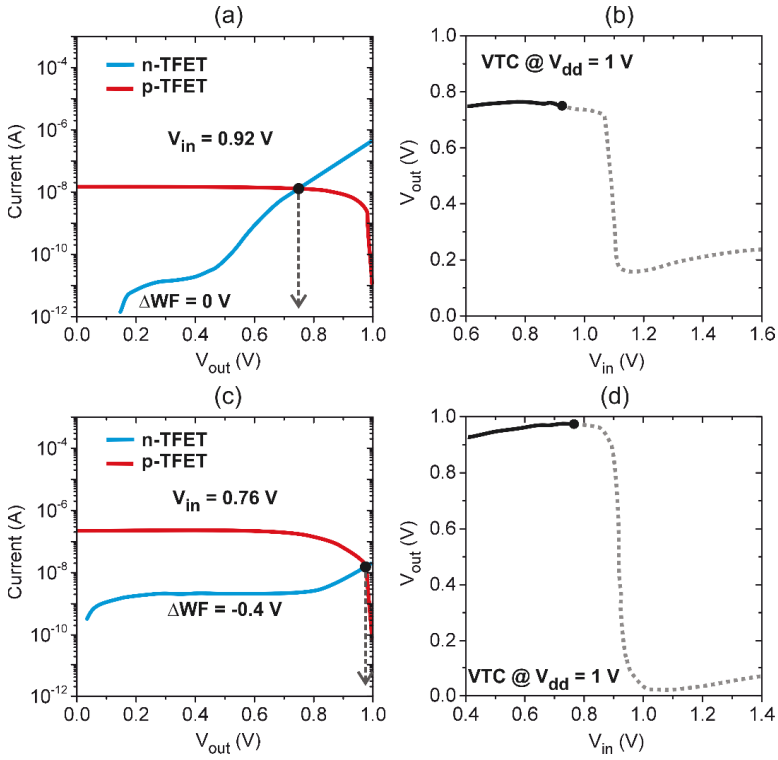

Figure 5.8: (a) The load line plot and VTC of the inverter for V_{dd}=1 V for a specific V_{in} demonstrates the effect of reduced ambipolarity through gate work function shift of the n-TFET by (a-b) ΔWF= 0 and (c-d) ΔWF= -0.4.

and does not degrade its operation. For studying purpose we calculated the VTC in *MATLAB* based on detailed *I-V* dataset measured from the p- and n-device (Figure

5.4(a)) instead of measuring the VTC directly. The script for the VTC calculation has been validated where the points match quite well with the measured VTC of the CTFET (Figure 5.6(a)). Since both devices are fairly symmetric around V_{gs} = 0.6 V we define this value as the reference logical low level for the input voltage V_{in}^{low}= 0.6 V of the inverter. The logical high input level depends on the applied supply voltage, hence V_{in}^{high}= V_{in}^{low}+V_{dd}. Consequently the switching threshold voltage is calculated as follow V_M = V_{in}^{low}+V_{dd} × 0.5. Keeping the scenario of V_{dd} = 1 V the calculated VTC demonstrates the degraded low and high logical level in Figure 5.8 (a-b). As the load-line plot indicates for V_{in}= 0.92 V, the ambipolar effect causes a parasitic current flow in the n-TFET which is supposed to be OFF due to the fact that V_{in} is smaller than V_M = 1.1 V. As a consequence of the higher n-TFET current, the load-lines intercept already at lower $V_{out} < V_{dd}$ = 1 V.

Since currents on the left (right) side of the virtual GND are not relevant for the n-TFET (p-TFET) in the inverter circuit, it is appropriate to modify the gate work function of the devices such that the transfer curves move closer together. This approach shifts the undesired ambipolar current branch into the regime beyond the virtual GND level which effectively suppresses the influence of ambipolarity on the inverter switching behavior. This is demonstrated in Figure 5.7(b) where the gate work function of the n-TFET is artificially reduced by 0.4 V. Keep in mind that the reference virtual ground needs to be reduced by half of the work function shift to keep the symmetry between the transfer characteristics. The computed VTC of this change is shown in Figure 5.8(c-d). Again for a low input voltage V_{in}= 0.76 V ($< V_M$ = 0.9 V) the n-TFET exhibits well output saturation where a slight increase is observed for large drain voltages[13] (V_{out}=V_{ds}^{n}). The resulting VTC of the modified CTFET inverter indeed shows an improved behavior by nearly reaching the nominal low V_{out}^{low} ≈ GND and high level V_{out}^{high} ≈ V_{dd}. Since a small degree of ambipolarity is still existing (Figure 5.8(d)) a slight degradation is apparent for very high and low V_{in} signals. It is worth mentioning that metal gate work function engineering of this GAA NW CTFET inverter could enable proper operation with V_{dd} down to 0.3V (not shown) which was not possible without the modification due to the large separation of the transfer curves of the p- and n-device. This is quite important as steep slopes of TFETs are usually exploited at fairly low currents, i.e. SS < 60 mV/dec for $I_{ds} < 10^{-6}$ µA/µm as presented in chapter 4.2. Although the gate work function adaption can be realized by using an appropriate metal gate this method only works for the simple inverter circuits based on pull-up and pull down transistors. In case of a pass-transistor, i.e. in SRAM-cells, the ambipolarity has to be eliminated at device level.

[13] For large V_{ds} the ambipolar current sets in earlier and becomes larger in the OFF-state of the transfer characteristics. This explains the sudden increase in the output current for increasing V_{ds}.

5.3 Suppression of the ambipolar behavior in NW GAA CTFETs

In the previous chapter the ambipolar behavior has been identified as one of the major problems that limit proper inverter functionality. The present GAA NW CTFET fabrication approach employs symmetric implantation dose with the focus to establish steep source junctions for both device types. However, the corresponding drain junctions are created by the same manner resulting in a narrow tunneling barrier width at the drain-channel interface. Therefore, in order to minimize the ambipolar conduction of the TFETs OFF-state special care needs to be taken for the drain junction during the device fabrication and thus requires an asymmetric TFET approach regarding S/D implementation. In general, all assumptions for improving the tunneling probability as discussed in chapter 3.1 have to be reversed on the drain junction to prevent the parasitic tunneling current.

Different approaches have been reported to achieve the goal such as TFETs with hetero high-k materials to reduce the electrostatic control on the drain side [159][160]. A less challenging implementation is the reduction of the doping concentration to create a less abrupt p-n junction at the channel-drain side [161]. In that sense, we reduced the ion implantation dose while the annealing process is maintained. The measured devices did not show a clear trend as a function of the implantation dose so that we come to the conclusion that reducing the dopant concentration by ion implantation is not appropriate and rather difficult to handle for thin and suspended NW platforms. Furthermore, the presence of $NiSi_2$ at the drain side promotes dopant segregation at the channel interface and thus increase the difficulty to establish the desired low dopant concentration for the respective side.

A more reliable way to prohibit the ambipolar conduction is the employment of a gate-drain underlap which was first mentioned by *Verhulst et al.* for TFETs [162]. This simply allows a spatial shift of the steep drain junction away from the gate voltage influence which reverse bias (with respect to the drain potential) triggers the parasitic tunneling current. The suppression of the ambipolar current depends on the underlap distance between gate and drain junction [163][164].

5.3.1 Fabrication CTFETs with gate-drain underlap

The schematic of a NW cross section of the CTFET inverter in Figure 5.9(a-b) depicts the concept of the gate-drain underlap utilizing a SiO_2 drain spacer to create the underlap distance. The fabrication follows the inverter process introduced in chapter 5.2

with the exception that several process steps are added after the gate formation. These steps include the deposition of SiO_2 by plasma-enhanced-chemical vapor-deposition (PECVD) at 350°C on the entire surface with a thickness of 70 nm. Patterning the drain spacer has been done by electron beam lithography with negative e-beam resist (HSQ) and RIE etching with CHF_3 plasma. It is important to mention that the last few 10 to 5 nm of SiO_2 is removed by HF-1% wet etching since the following silicidation step requires a complete oxide-free and smooth Si surface. The resulting sSi GAA NW CTFET inverter with gate-drain underlap is illustrated in Figure 5.9(c) indicating a SiO_2 spacer with a length of 40 to 50 nm.

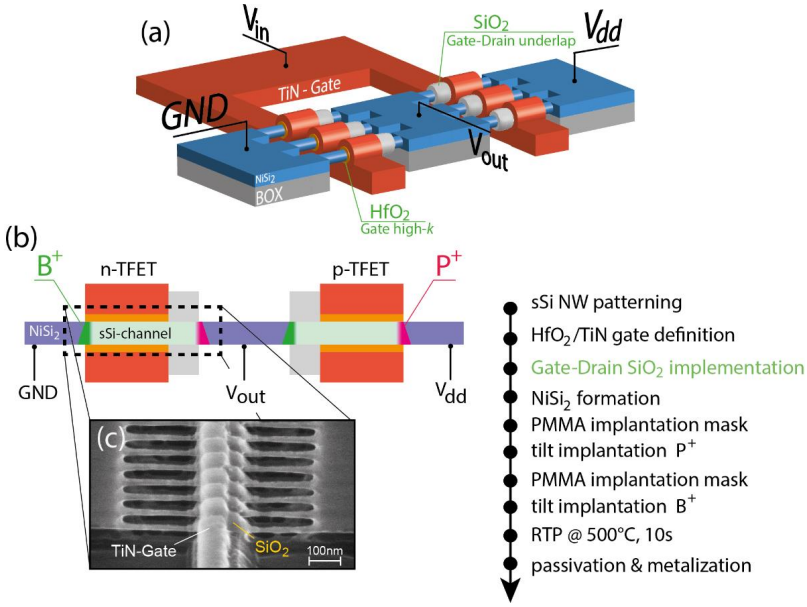

Figure 5.9: (a) Schematic of sSi GAA NW CTFET inverter with gate-drain underlap. (b) Cross section along a single NW through n- and p-TFET including the doped junctions at the $NiSi_2$ and the sSi interface. (c) SEM image of a single TFET after the gate-drain underlap process with SiO_2. An overview of the key process steps is given for the modified CTFET inverter fabrication.

5.3.2 I-V characteristics of TFETs with gate-drain underlap

The I_d-V_{gs} transfer characteristics of the sSi GAA NW p- and n-TFETs are presented in Figure 5.10. In this case the TFETs feature 50 NWs per device where each NW has 45 nm in width and 5 nm in thickness. The gate length amounts to 350 nm. In order

to emphasize the relevance of the gate-drain underlap approach, also TFETs without ambipolarity suppressing spacers were fabricated in parallel (dashed lines). When the gate voltage is biased in the OFF-state, both p- and n-devices with gate-drain underlap (solid lines) indicate a strong reduction of the parasitic tunneling at the drain. The remaining I_{off} current is mainly caused by the gate leakage I_g, as depicted in Figure 5.10. Obviously, the increased tunneling distance set by the SiO_2 spacer is sufficient to lower the charge carrier tunneling probability significantly between channel and drain. However, the same distance, in turn, causes a slight decrease of the I_{on} current as evident for the n-TFET (p-TFET) at large (small) gate voltages. The gate-drain underlap adds an intrinsic Si region between the channel and the silicide at the drain (Figure 5.9(b)), which leads to an increase of the total resistance. Due to the lower out diffusion coefficient of phosphorous as compared to boron, the resistance is more pronounced for the n-TFET than for the p-TFET and thus explains the large I_{on} difference. Similar behavior has been reported by *Wan et al.* [163], where a larger underlap

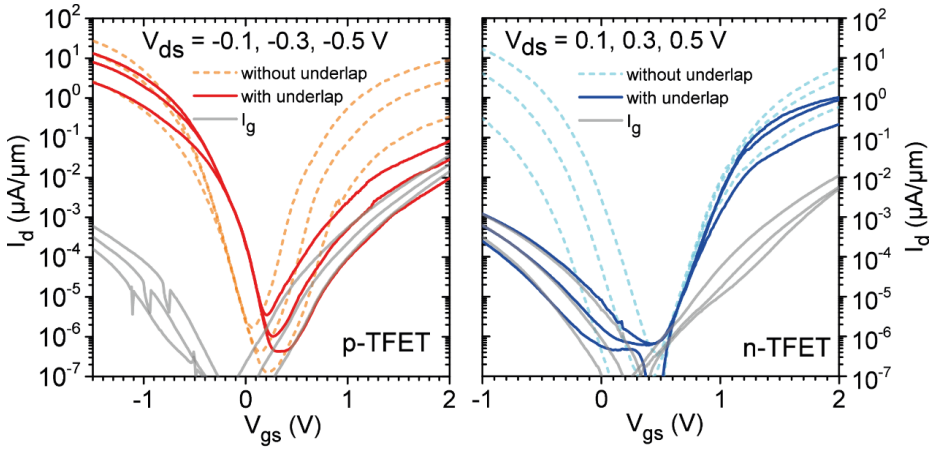

Figure 5.10: Transfer characteristics of the sSi GA NW n- and p-TFET with gate underlap in comparison to the corresponding TFET device fabricated in parallel without ambipolar suppressing SiO_2 spacers.

region was needed in this case for the n-TFET because of the higher boron diffusion. The inverse subthreshold slope plotted as a function of I_d is extracted for $|V_{ds}| = 0.1$ V for both devices in Figure 5.11. An average SS of 110 mV/dec has been measured for the p-TFET while the n-TFET yields SS of 139 mV/dec in the I_d range from 10^{-6} to 10^{-3} µA/µm. The slightly degraded SS for the n-TFET utilizing boron as source can be attributed to the afore mentioned larger diffusion resulting in less steep doping profiles.

The I_d-V_{ds} output characteristics of the TFETs are displayed in Figure 5.12 again revealing good current saturation for large V_{ds}. The typical exponential onset in the

linear region is more pronounced for the n-TFET which supports the assumption of a broader and less concentrated dopant pocket at the source-channel interface. At a supply voltage of V_{dd}=V_{OV}=V_{ds}=0.5 V, we measured a drain current of 0.14 µA/µm for the p-TFET and 0.1 µA/µm for the n-TFET while at V_{dd} = 1 V, I_d amounts to 4.5 µA/µm and 2.3 µA/µm for the p- and n-TFET respectively, providing fairly symmetric conditions for the inverter.

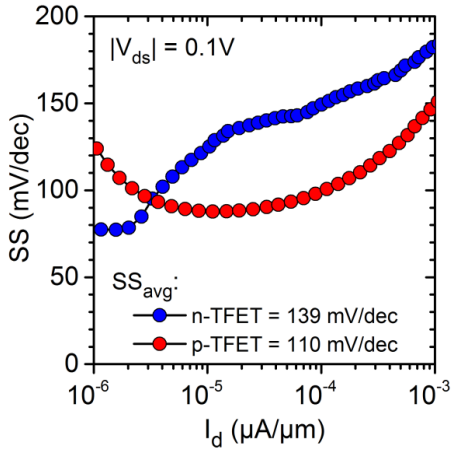

Figure 5.11: SS vs. I_d of the corresponding n- and p-TFET measured for a supply voltage of 0.1 V

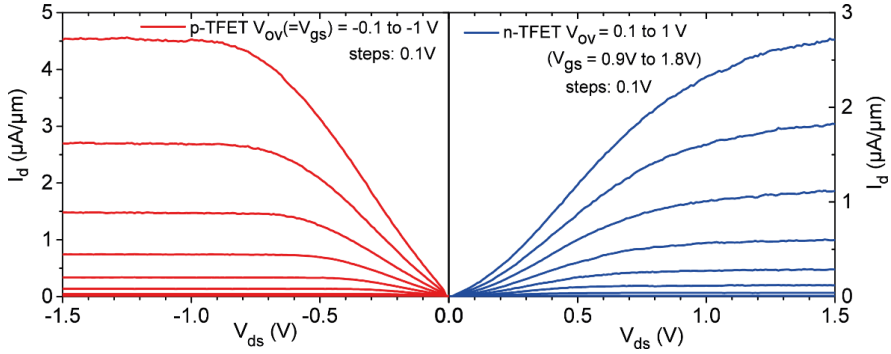

Figure 5.12: Output characteristics of the sSi GAA NW CTFET taken for gate overdrive voltages V_{ov}=V_{gs}-V_{off} up to 1 V. Note that V_{off} for the n-TFET is set to 0.8 V whereas V_{off} = 0 V is taken for the p-TFET.

5.3.3 CTFET inverter characteristics with suppressed ambipolar behavior

Complementary sSi GAA NW TFET inverters with gate-drain underlap are measured according to the schematic of Figure 5.9(a). A pair of electrically matched n- and p-TFETs were chosen similar to the devices shown in Figure 5.10. The resulting inverter VTC is presented in Figure 5.13 for V_{dd}=1 V down to 0.2 V. In contrast to the CTFET inverter shown in chapter 5.2.1, the present inverter VTC is very symmetric indicating a transition point between the two logic levels close to $V_{dd}/2$. This is because both n- and p-device transfer characteristics have a smaller offset to the 0 V gate voltage origin. However, a minimal shift of the VTC to the right is still remaining which can be attributed to the slight displaced transfer characteristics towards positive V_{gs}. A more significant difference which comes with the suppression of the ambipolarity is the constant output voltage level V_{out}. The high output level approaches the supply voltage V_{dd} (maximum possible voltage value) even for very low input voltage V_{in} which proves that the n-TFET is not conductive at this state. This also holds for the low output level of the inverter being pulled to the GND entirely due to the successful ambipolarity suppression of the p-TFET. Thus, both logical levels (high/low) are separated by the maximum voltage swing of V_{dd}.

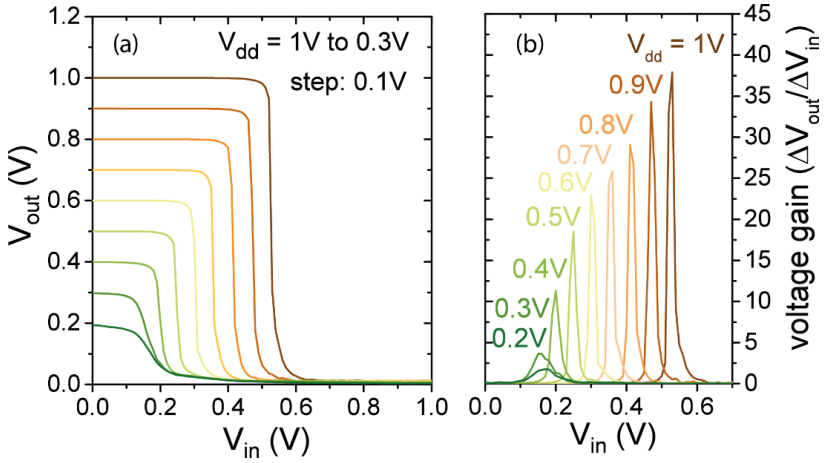

Figure 5.13: (a) VTC of the CTFET inverter with suppressed ambipolar behavior measured at supply voltages V_{dd} from 1V down to 0.2 V. (b) The voltage gain of the inverter indicating the highest value in the transition region at the corresponding V_{dd}.

The transition zone between these two levels is very narrow resulting in a high voltage gain. This is in particular interesting for analog circuits where the inverter

exclusively operates in this transition region as a signal amplifier. At V_{dd}=1 V the gain amounts to 38 and a gain value of more than 10 is still obtained for smaller V_{dd}=0.4 V outperforming the CTFET inverters shown in Figure 5.6. The limitation of the CTFET inverter is reached once V_{dd} is set to 0.3 V and below, where the gain starts to drop drastically. In addition, also the two distinct output levels start to degrade. At smaller V_{dd} the currents of the n- and p-TFETs in the load-line plot are shifted closer to each other up to a point where the saturation region is no longer considered. In this case the impact of the exponential onset becomes more severe in the load-line plot leading to a further increase of the ambiguous transition region of the VTC. Although a general improvement of the inverter gain is expected for TFETs without "S"–shape in the output characteristics, the main limiting factor for the minimum V_{dd} operation, however, is caused by the relative offset between the n- and p- transfer curves (Figure 5.10). It has the same magnitude as the critical V_{dd} meaning that both devices operate close to the current minimum. A practical solution for this would be to apply different metal gates with matched work functions to shift the transfer curves of the complementary devices to the point of origin.

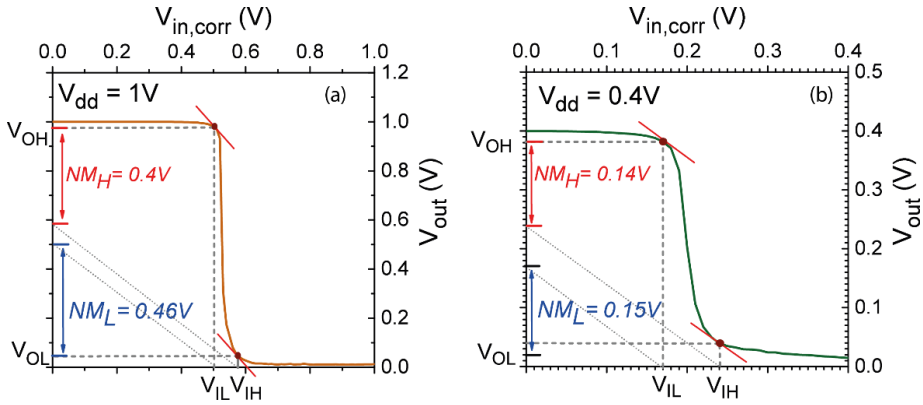

Figure 5.14: Linear approximation of the VTC to estimate the static noise margins for the high NM_H and low NM_L level at (a) V_{dd}=1 V and (b) V_{dd}=0.4 V. The VTCs have been shifted to move the transition point to V_{in}= $V_{dd}/2$ to allow correct NM estimation.

In order to estimate the noise margins, a piecewise approximation of the VTC is needed to determine the boundary points of the transition zone. As explained in chapter 5.1, these are the points of the VTC where the voltage gain $\Delta V_{out}/\Delta V_{in}$=-1. The output voltage and input voltage for high (V_{OH},V_{IH}) as well as for low (V_{OL},V_{IL}) is defined by the position of these boundary points as marked in Figure 5.14. Large noise margins for the high level NM_H= V_{OH}-V_{IH}= 0.4 V and low level margin NM_L= V_{IL}-V_{IL}=

0.46 V can be achieved. For smaller V_{dd} =0.4 V the noise margin for both, high and low $NM_{H/L}$ = 0.15 V which is still about 40% of the applied supply voltage[14]. Note, that for the noise margin extraction procedure the inverter VTC has to be shifted so that the transition point is placed at V_{in}=V_{dd}/2 to allow a correct NM estimation.

Static current leakage during the logical "high" and "low" states in the order of 10^{-10} A has been measured for the present CTFET inverter which is two orders of magnitude lower than the former CTFET inverter generation as shown in Figure 5.8. Hence, TFETs with suppressed ambipolar behavior also strongly benefit in terms of lower static power consumption according to equation (5.3)

5.4 Conclusion

Complementary TFET inverters with tensely strained NW GAA have been fabricated on the same chip. Individual *I-V* measurements of the p- and n-TFET show symmetric performance. The inverter VTC measurements reveal functional inverter operation providing two distinct logical output states but also a strong degradation of the noise margins. The most crucial issue is the ambipolar behavior which is present on both p- and n-TFETs limiting the usability of the inverter. Because of the inverter working principle gate work function shifting can be a short-term solution to suppress the ambipolar behavior and allow proper functionality of the inverter exploiting the small SS especially at low supply voltages. However, for more complex circuits where CTFET needs to be employed as pass-transistors the ambipolar current has to be eliminated.

This motivates the improvement of the sSi GAA TFET inverter by employing a gate-drain underlap realized by a SiO_2 spacer with the intention to reduce the parasitic tunneling at the channel-drain interface. The underlap simply mitigate the gate bias influence to the drain tunneling junction which leads to an improved OFF-state for both n- and p-TFETs. The measured CTFET inverter with suppressed ambipolar behavior shows significant improvements in terms of noise margins and intrinsic voltage gain as compared to the first fabricated device generation. However, the gate-drain underlap approach induces a trade-off between ambipolar suppression and reduction of I_{on} current depending on the underlap distance. An extended channel part is created which cannot be modulated by the gate and, hence, results in an additional resistance to the entire device. One way to circumvent this is to implant the drain first for both device types and apply a longer anneal time to enable a dopant pocket with broader profile throughout the high resistive region. Typically n-dopants such as phosphorous

[14] Ideal inverter with a step-function leads to $NM_{H/L}$ of 0.5 V_{dd} and span the complete voltage swing.

or arsenic dopant types have low diffusion constants and should be performed first in the process schedule [163]. Consequently, source and drain of each device type needs to be processed individually.

A very similar approach but using a gate drain overlap has been proposed by *Abdi et al.* [160]. Here the drain dopant extends into the channel region. One issue of this approach is the questionable larger C_{gd} and the impact on the switching threshold of the TFETs. Also the ambipolar conduction reappears once the drain dopant concentration is larger than 10^{19} cm^{-3}. Our attempt to simulate this approach to the sSi GAA NW platform with TCAD (technology computer aided design) simulations only shows negligible impact on the ambipolar branch.

Even though the current is decreased, the presented CTFETs with gate-drain underlap still provide large currents compared to different Group-IV CTFET platforms [20] attributed to the gate-all-around NW design and additional boosters such as tensile strain. In fact, the static behavior is so far the best among the reported experimental CTFETs inverter [154] due to the removal of the ambipolar conduction. This achievement does not only result in CTFET inverter which is more robust against noise and lower in power consumption but also open doors for the employment of CTFET in more advanced circuit environment.

6 CTFET half-SRAM

The static random access memory (SRAM) cell is the most prevalent digital building block for cache memories in microprocessors for fast data access. In comparison to the much slower dynamic RAM (DRAM), the SRAM may occupy up to 70% of the processors area due to its larger size and requires a permanent supply voltage to retain the stored information [165]. With respect to the growth in mobile applications the use of TFETs might solve the stability challenges that SRAMs are facing due to aggressive voltage scaling. The most common design is the symmetric six transistor SRAM cell (6T-RAM) based on the CMOS technology, as displayed in Figure 6.1(a), with two cross-coupled inverters (to store the logical state) and two access transistors (AT) allowing read and write operations. So far, assessment of TFETs on the SRAM performance has been analyzed by means of mixed-mode device/circuit TCAD simulations [157][166][158][167][168] and with look-up tables utilizing Verilog-A models for the TFET [169][170]. Such early analyses relied mainly on the idealized TFET models where fundamental aspects of experimental devices such as parasitic phenomena caused by ambipolarity and the forward p-i-n leakage are neglected. As already seen for the inverter circuit, the ambipolar behavior needs to be suppressed to increase SRAM stability. The unidirectional conduction property caused by the asymmetric source and drain regions of TFETs, however, is identified to be the main obstacle for advanced circuits that make use of pass-transistors as in SRAMs. This limits the functionality of the 6T-SRAM cell since the access transistor is required to conduct current from source to drain and vice versa. Several modified SRAM cell topologies are proposed to circumvent this issue using outward or inward faced access transistor configurations and/or by adding more transistors at cost of area to enhance the operation stability: 6T-cell with one inward and one outward AT [157], 7T cell with outward ATs plus an extra transistor mainly for performing the read operation [169], 6T cell with p-type inward AT in combination with read-assist techniques [166], 10T Schmitt-Trigger cells [171] and a 8T hybrid TFET/CMOS cell [168]. Recent simulation results with ideal and calibrated TFET templates emphasize acceptable performances with the employment of 6T-SRAM with outward faced access transistors [167]. However, to our best knowledge, no experimental SRAM cell based on TFETs has been reported to verify the predicted performance. One of the main reasons is the limited capability for many

researchers to fabricate the required numbers of TFETs for one SRAM cell. Furthermore, complementary devices are not well established in many TFET platforms preventing them from adapting the proposed SRAM designs.

Therefore, in order to experimentally verify the functionality of TFETs in the 6T-SRAM design we investigate the static behavior of a half SRAM (HSRAM) cell with our sSi GAA NW TFETs. The choice of the half-cell is sufficient for measuring the inverter voltage transfer characteristics (VTCs) in dependency of the AT influence. Depending on the SRAM operation, different bias configurations are applied which make it possible to reconstruct the butterfly curves based on the resulting VTCs. From the butterfly curves the static noise margins (SNM) can be extracted and used to prove the full 6T cell stability.

6.1 6T-SRAM principle

The following subchapter will briefly explain the SRAM operations in the state-of-the-art CMOS 6T-cell to facilitate the understanding in the upcoming chapters. The core of the SRAM is a pair of inverters, composed of the transistors (M4, M5) and (M2, M1) in Figure 6.1(a), forming the storage element for a single binary digital bit. Both

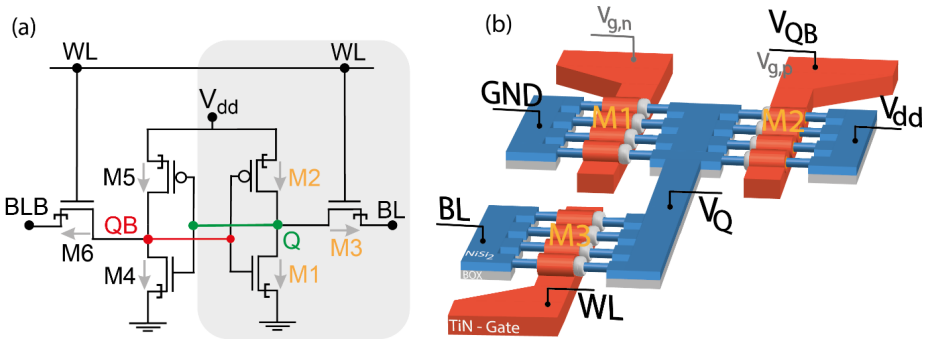

Figure 6.1: (a) Circuit of the symmetric 6T-SRAM cell with complementary TFETs. The grey marked area defines the half SRAM cell composed of an inverter and an outward n-type TFET as access transistor. (b) Schematic of the fabricated HSRAM cell with sSi GAA NW CTFET including the gate-drain underlap approach to suppress the ambipolar behavior.

are cross-coupled such that the output of one inverter is connected to the input of the other and vice versa. Because of that the voltages levels at the storage node Q and QB

defined at the output/input of each inverter are always complementary to each other. This enables exactly two stable states which are used to allocate each single digital bit: Q=0 V and QB=V_{dd} for logical '0' and Q=V_{dd} and QB=0 V for logical '1'. The access of the storage node Q/QB and hence the stored bit during the read or write operation is performed over the two n-type (M6, M3) access transistors (AT) by addressing the write-line (WL) and the differential bit lines (BL and BLB). It is important that the fabricated SRAM cell is symmetric to minimize the variability between the mirrored parts of the cell.

In order to evaluate the static behavior of the SRAM cell the static noise margin (SNM) is considered. The SNM gives the maximum amount of noise voltage that the cell can tolerate at both inverter inputs while maintaining the bi-stable operation points. Hence, it quantifies the magnitude of voltage required to flip the cell data. The SNM of the SRAM can be extracted by means of the voltage transfer characteristics (VTCs) of each inverter in the cell to create the so called butterfly curve for proving the stability for each SRAM operation: hold, read and write [165].

For the hold-operation, the n-type ATs is switched OFF by setting a low voltage at WL, while any voltage combination of 0 V or V_{dd} is applied on the bit-lines BL/BLB to mimic a read or write operation of neigbhouring SRAM cells in the same column. In this case the ATs decouple the voltage disturbance from BLB/BL such that the cross-coupled inverter can reinforce each other to retain the data. As a result, the butterfly curve for the hold-operation shown in Figure 6.2(a) is formed by the VTC of one inverter (blue) and the inversed VTC represented by the mirrored but cross-coupled inverter (orange). The hold SNM (HSNM) is determined by the length of the largest square that fits in the smallest wing and can be calculated according to [172].

The read-operation starts by pre-charging of both bit-lines BL/BLB to the high voltage level V_{dd} followed by turning-ON the ATs by applying a high voltage at WL. The main interaction happens at the bit-line which is connected to the 0 V storage node where the bit-line discharges through the AT and pull-down transistor in series. Hence, the VTC of the inverter with the corresponding storage node as output cannot reach the low voltage level (GND) during the current discharge. This leads to a deformation of the butterfly curve resulting in a smaller read SNM (RSNM), as can be seen in Figure 6.2(b). However, as long as the three crossing points are presented in the butterfly curve the SRAM is able to preserve the stored information. For robust read-operation this means that the pull-down transistor (M1) should offer a higher drivability compared to the AT to avoid voltage increase of the storage node from which in the worst case leads to data flipping. The critical point for data flipping is given by the inverter noise margin.

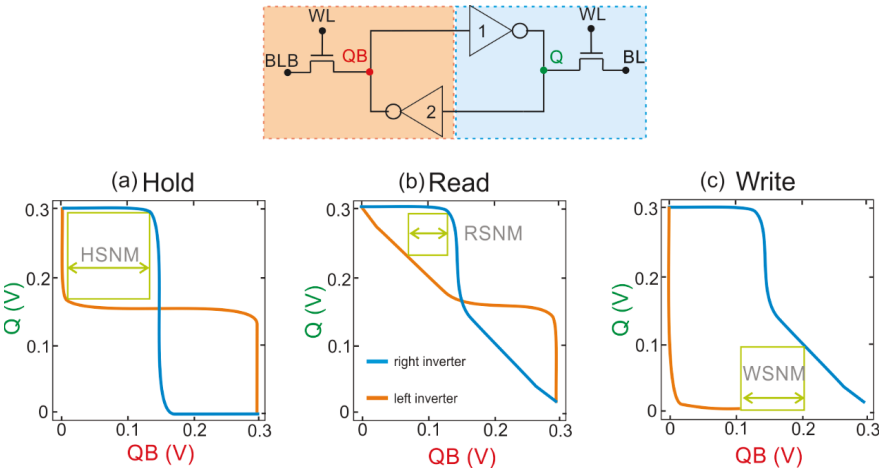

Figure 6.2: Butterfly curve for the SRAM operation (a) hold, (b) read and (c) write composed of the VTC of the respective inverter. The definition of the corresponding SNM is shown by the largest square between the VTCs. The different line color of the butterfly curve corresponds to the VTC of the half SRAM cell as indicated at the top.

In order to perform the write-operation the bit-line pair is forced to differential voltage levels, e.g. BL= V_{dd} and BLB=0 V, while the ATs are turned ON[15]. The impact of the bit-lines through bidirectional ATs, as realized by n-MOSFETs, would lead to deformation of both inverter VTCs. However, the strongest deformation happens for the inverter which AT is connected to the bit-line driven to 0 V. This is based on the fact that the n-type AT, as pull-down transistor, offers a better drivability to forward low voltage potentials[16]. Consequently, the bit-line with the low voltage level dominates the write operation process forcing the storage node to 0 V as reflected in the VTC behavior (orange-curve) in Figure 6.2(c). The mirrored inverter side has a supporting function for changing the bit in the SRAM cell (blue-curve). In contrast to the other operation, the write butterfly curve depicted in Figure 6.2(c) features only one crossing point between the VTCs that coincide with the logical value intended to be written. Hence, the more deformed the butterfly curve is the more robust is the write operation indicated by write SNM (WSNM) that separates the VTC.

[15] In this case we assume that the storage nodes have the inverted voltage levels with respect to the bit-lines, hence Q = 0 V and QB = V_{dd} which corresponds to logical 0.

[16] Typically n-MOSFET is considered to be switched ON for $V_{ds} > V_{gs} - V_{th}$ and $V_{gs} > V_{th}$, hence working in the saturation regime. In circuits this is only possible when one of the S/D terminal is permanently forced to 0 V.

6.2 HSRAM design with CTFETs

Based on the symmetry of the 6T-SRAM cell the static behavior can be evaluated by the butterfly curves which their construction requires the half-cell voltage transfer characteristics to be taken for various BL and WL. In this regard, we fabricated half-SRAM (HSRAM) cells implemented with the sSi GAA NW CTFETs to investigate their functionality. A schematic of the CTFET HSRAM design and the contacts is depicted in Figure 6.1(b). The process is the same as presented in chapter 5.3.1 but with a total of 3 TFETs connected during the mesa definition (Figure 6.1(b)): the pull-down n-TFET (M1), pull-up p-TFET (M2) forming the inverter and an additional n-TFET (M3) as access transistor. Instead of a single gate contact for the pull-up and pull-down TFETs, we have chosen to design independent gates for each device to encounter the work function shift which leads to a fairly large separation of the n- and p transfer characteristics. This workaround allows us to electrically adjust the threshold voltage of each device, by adding an offset to the applied gate voltages.

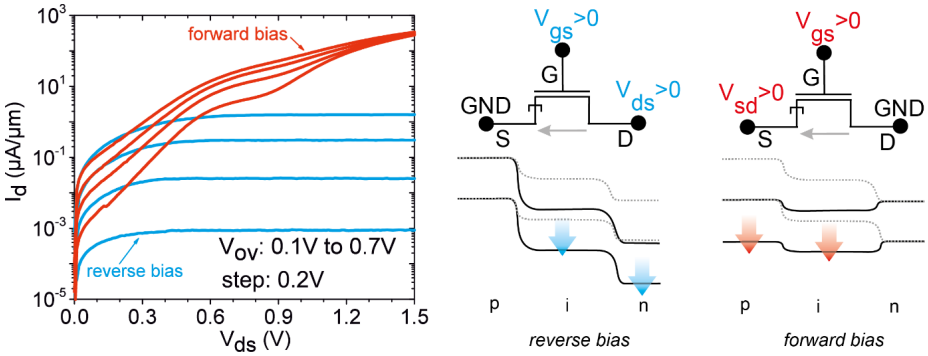

Figure 6.3: Output characteristics of an experimental n-TFET for different source/drain biasing scheme. The blue curves show the standard reverse bias operation. In contrast, positive bias (red curve) at the source leads to forward biased p-i-n diode operation resulting in undesired high S/D current leakage almost independent of the applied gate bias.

One of the main concerns is the unidirectional current conduction of TFETs because of the asymmetric S/D doping. This inherent TFET property has been addressed by other groups as the main limiting factor preventing a proper operation of the 6T-SRAM design [157][171][167]. In detail, depending on the TFET connection as O-AT or I-AT either the RSNM or WSNM is significantly degraded due to the fact that the device can only forward the logical level in one direction. Figure 6.3 illustrates

the I_d-V_{ds} output characteristics of an experimental n-TFET emphasizing the non-symmetric current transport in TFETs. A positive voltage leads to reverse biasing (positive voltage at the n-region) of the p-i-n band structure resulting in the desired output behavior with current saturation (blue curves). In contrast, when a high potential is applied at the source terminal (i.e. V_{sd}>0.5 V), the n-TFET exhibits large current flow due to the forward biased p-i-n structure (red curves). In comparison to the standard operation this forward p-i-n current leakage is barely controlled by the gate. Instead, the current converges for V_{sd}>1.2 V meaning that the gate loses control of the drain current and only scales with V_{sd}. In particular this large uncontrolled parasitic current leads to improper operation of the SRAM and, hence, the forward biasing scheme should to be avoided.

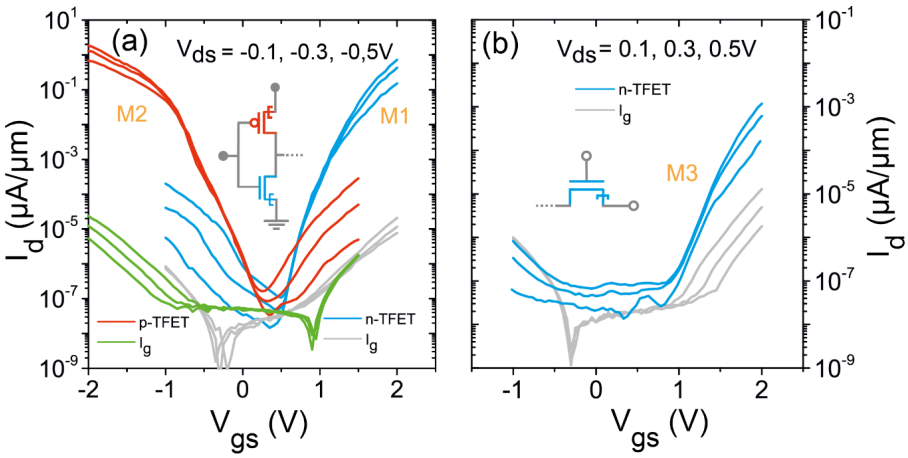

Figure 6.4: Transfer characteristics of the (a) p- and n-TFET of the inverter and (b) the n-TFET used as O-AT.

Due to unidirectional property, the n-TFET as AT can be connected in two different configurations: inward facing AT (I-AT), where the source is connected to the storage node or outward facing AT (O-AT) having the source at the bit-line. We decide to fabricate HSRAM cells with O-AT n-TFETs, as indicated in Figure 6.1(b), since simulations with calibrated TFETs yield promising results in comparison to the employment of I-ATs [167]. The introduction of the gate-drain underlap in the TFETs should mitigate the ambipolar behavior to improve the inverter VTC stability. The suppression of this parasitic behavior is also important for the ATs as reported by *Strangio et. al* where existing ambipolar conduction in either I-AT or O-AT prevents data retention in the SRAM cell [158].

6.3 Single device characterization

In the following, the transfer characteristics of the TFETs (M1, M2, M3) forming the HSRAM as depicted in Figure 6.1(b) are presented. Each device consists of an array of 60 NWs with dimensions of 30 nm in width and 10 nm in thickness. The gate length is 100 nm for all three TFETs. The device characteristics in Figure 6.4 indicate reduced ambipolar current in the OFF-state as a result of the selective SiO_2 spacer at the drain side forming a gate-drain underlap. Due to process variation, the n-TFET (M3) employed as O-AT shown in Figure 6.4(b) seems to have larger spacer length resulting in

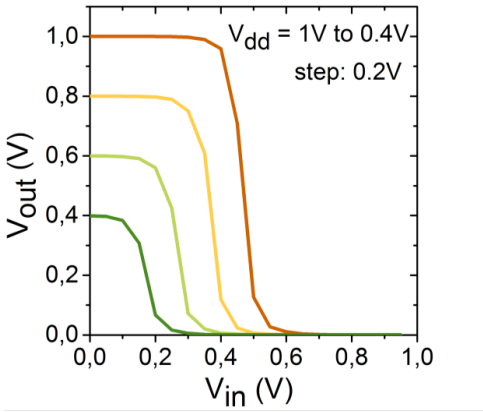

Figure 6.5: The VTC of the inverter shown in Figure 6.5(a) for different V_{dd} after threshold voltage adjustment of the n-TFET.

full suppression of the ambipolarity. However, in turn, the ON-current is also decreased since the enlarged intrinsic Si region below the spacer increases the total resistance of the device. The present devices feature ON-currents $I_d(V_{gs,min}+1\ \mathrm{V})$ that corresponds to 0.06 µA/µm, 0.01µA/µm, 1.1 nA/µm at $|V_{ds}|$=0.5 V, OFF-currents amount to 0.11 pA/µm, 0.2 pA/µm, 0.15pA/µm and the minimum SS of 100 ,160 ,220 mV/dec for the devices M1, M2 and M3, respectively. Even though the ON-current is relatively small, it is not a critical issue in our analysis since the main focus of the investigation lies in the static behavior of the cell. In that sense, the relative threshold voltage shift of the devices shown in Figure 6.4(a) and (b) is of great importance in the SRAM static behavior. Because the gate is separated for the pull-up and -down TFETs, we are able to modify the gate work function electrically by setting a threshold offset for the n-TFET M1 by 0.5 V to shift the transfer curves to the left and thus closer to the p-TFET M2, which does not need any correction. The inverter VTC of the electrically matched p- and n-TFETs after the work function correction is depicted in Figure 6.5

for V_{dd} in the range of 1 V down to 0.4 V providing constant high and low voltage levels with a transition of the two level at $V_{dd}/2$. Apparently the small degree of ambipolar conduction for the TFET inverter (Figure. 2(a)) does not degrade the inverter VTC.

6.4 Static performance of CTFET HSRAM

The measurement of the HSRAM follows the contact configuration depicted in Figure 6.1(b). For the investigation of the HSRAM static behavior, distinct gate voltage windows need to be defined for each individual device to compensate the threshold voltage shift. An overview of the low and high gate voltage definition for all three devices used in the HSRAM are summarized in Table 6.1.

The static performance of the HSRAM is measured for various bit- (BL) and write-line (WL) voltage level configurations in order to observe the potential behavior in the storage node Q in dependence of the voltage potential QB under different SRAM operations. All measurements have been performed at a supply voltage of V_{dd}=0.8 V.

Table 6.1 Low/high gate voltage definition
for each devices forming the HSRAM at V_{dd} = 0.8 V.

TFET devices		V_{low}	V_{high}
(M1) n-TFET, pull-down	$V_{g,n}$ =	0.5 V	1.3 V
(M2) p-TFET, pull-up	$V_{in} = V_{g,p}$ =	0 V	0.8 V
(M3) n-TFET, access transistor	WL =	1 V	1.8 V

The hold ability is investigated with WL=V_{low} for the AT while keeping the BL(B)=V_{dd} (see Figure 6.6(a)) to mimic a read operation of a neighboring cell within the same column. In this case, the AT should be ideally OFF, screening the cell from the influence of the BL(B), so that the HSRAM maintains a VTC at node Q equal to the characteristic shown in Figure 6.5 at V_{dd}=0.8 V. Instead, the resulting HSRAM VTC is strongly distorted as illustrated by the orange curve in Figure 6.6(b), while the green curve is just the mirrored version of the orange curve to account for the other half of the full 6T cell. The distortion in the hold case is caused by the forward biased p-i-n leakage in the O-AT, as discussed in chapter 6.2, since the high potential BL is

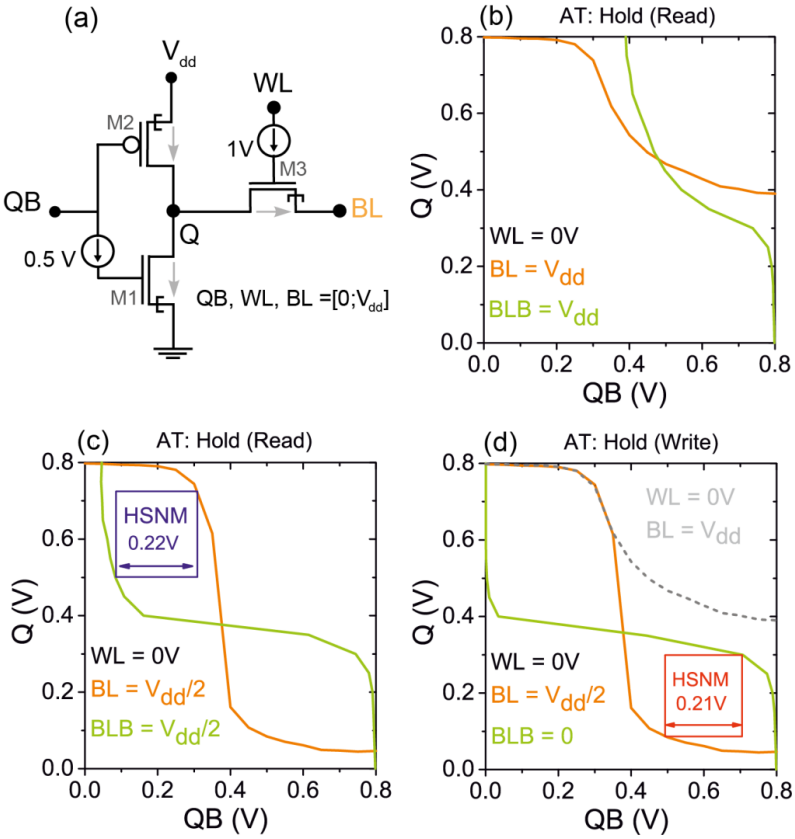

Figure 6.6: (a) Circuit of the HSRAM including the voltage generator to drive the TFETs to the desired voltage range. (b)-(d) depicts the butterfly curves generated from the measured VTCs of the HSRAM in hold for various BLB/BL combinations with V_{dd} and $V_{dd}/2$. Only the butterfly curves with three crossing points confirms hold stability.

applied at its source terminal. A significant current flow is established pulling up the potential in Q and hence lift up the low level of the VTC. This leads to a deformation of the butterfly with only one crossing point, a sign that data retention is not possible in the SRAM. Only reducing the BL(B) to $V_{dd}/2$ mitigates the parasitic current and maintains the VTC behavior (orange curve in Figure 6.6(c)). By considering both VTCs from each half cells the resulting butterfly plot is generated that proves a successful hold operation with BL(B)=$V_{dd}/2$ retaining the VTC voltage levels of the HSRAM (Figure 6.6(c)), in opposite to the case with full V_{dd}.

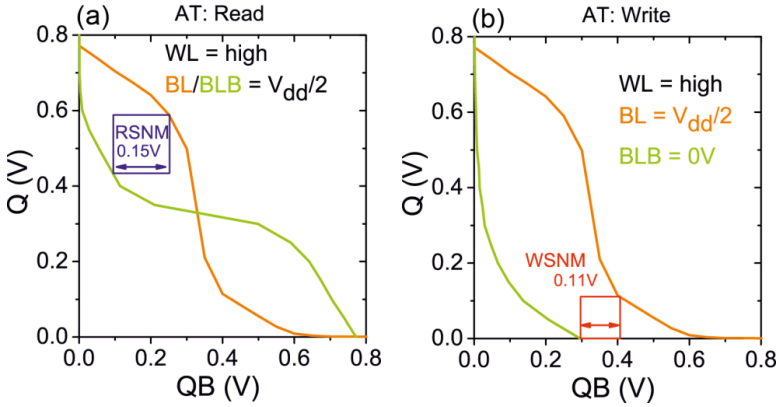

Figure 6.7: (a) The butterfly curves for read operation forming a butterfly curve from which we extract the RSNM as the maximum square that can fit inside the two VTCs. (b) In comparison, a successful write operation requires a large deformation of the VTCs with only one crossing point between the VTC curves. The WSNM is then extracted as the minimum square in between the two VTCs.

To test the hold condition under write of neighboring SRAM cells, we force the BL/BLB pair to differential voltage levels. The results in Figure 6.6(d)) demonstrate cell stability for $V_{dd}/2$ as high voltage potential for BL. However, when driving BL to V_{dd} the butterfly curve (dashed-grey and green curve) leads to only one crossing-point resulting in an unintended write operation of the cell. The hold static noise margin (HSNM) is extracted by the length of the quadratic square fitting in the smallest wing of the butterfly curve [172]. For the both hold(read/write) operation cases with BL= $V_{dd}/2$ as high voltage level the HSNM is slightly above 0.2 V. As we found that the cell in hold can only preserve the logic state operating with voltages lower than $V_{dd}/2$=0.4 V for BL(B), we continue the analysis by assuming the use $V_{dd}/2$ as high logic voltage level at the bit-lines.

Reading the cell is performed by applying high potential at both BL(B)=$V_{dd}/2$, as proposed in [167], and activating the AT with WL=V_{high}. Compared to the hold state in Figure 6.6(c) where the AT is switched OFF, the wings of the butterfly curve in Figure 6.7(a) is compressed but still preserve the three crossing points. In this case, the extracted noise margin for read (RSNM) is about 0.15 V.

With regard to the write operation, the butterfly curves shift apart due to the HSRAM VTC whose bit-line is connected to the low voltage potential with active AT (green curve in Figure 6.7(b)). Such strong deformation of the corresponding HSRAM VTC results from the pull-down n-TFET as AT, forcing the storage node to follow the BLB=0 V potential. Consequently, the write butterfly curve indicates only one crossing point between the VTCs which corresponds to the logical value intended to be written.

The write operation becomes more robust the larger the VTCs are separated [167]. In our case the extracted write static noise margin (WSNM) amounts to 0.11V.

6.5 Conclusion

Half SRAM cells composed of three transistors have been successfully fabricated based on the sSi NW GAA complementary TFETs with suppressed ambipolar behavior. With this half-cell approach the functionality of TFETs for the state-of the-art 6T-SRAM design was, for the first time, experimentally demonstrated by measuring the static behavior of the HSRAM voltage transfer characteristics at the storage node. Based on the butterfly curves we can confirm that the TFETs employed as ATs limit the operation stability of the SRAM cell due to the inherent asymmetric p-i-n structure. In our case when the source-drain polarity forces the p-i-n structure in forward bias, we observe large drain currents independent of the gate voltage as predicted by simulations [167][157][166]. Hence, the forward bias condition needs to be avoided since the device does not behave like a transistor. However, due to the working principle of a 6T-SRAM, the source drain polarity of an AT may switch. The higher the forward bias the higher is the chance for cell malfunction since the voltage levels cannot be retained in the storage nodes even with the ATs being switched OFF (hold-case). Based on this fact, we have to limit the highest possible voltage at the bit-line BL/B down to $V_{dd}/2$ to enable stable SRAM function for hold, read and write operations with outward faced n-TFET as AT. This requirement mitigates the impact of the forward biased parasitic p-i-n diode current which reduces the distortion of the resulting butterfly curves giving acceptable static noise margins. In other words, to solve the unidirectional limitation, design measures at circuit level are necessary such as the modification in the SRAM layout for TFETs or, as these results revealed, reducing the allowed voltages at the bit-lines in order to keep the 6T cell topology. In terms of dynamic performance evaluation of the SRAM with TFETs the entire cell with all six transistors are required. We assume that the 6T SRAM based on our sSi GAA CTFETs is slower than equally fabricated CMOS implementation since the cell operation is mainly driven by the side which bit-line is set on the low voltage potential (unidirectional n-TFETs as O-ATs). In contrast, MOSFET are bidirectional conducting meaning that the cell can initiate the operations at both ATs. Only SRAMs with ideal TFETs which provide larger currents at very small V_{dd} than MOSFETs may overcome this disadvantage and even has the potential to outperform MOSFET based 6T-SRAMs as reported in [167].

7 Summary and Outlook

Within the framework of this thesis TFETs based on strained Si nanowires have been investigated targeting low power circuit applications. For this purpose various technology boosters were employed to meet the design rules deduced from the band-to-band tunneling probability aiming for high tunneling currents and small SS $<$ 60 mV/dec for both n- and p-type TFETs. The fabrication of gate-all-around nanowire structures with TiN/HfO_2 improves gate electrostatics, whereas the tensile strain component reduces the band gap of Si. The creation of single crystalline $NiSi_2$ at the source/drain area of the free standing nanowires with thicknesses as small as 5 nm reduces the overall resistance of the device. For the formation of steep doping profiles at the source-channel and drain-channel junctions, tilted ion implantation into the preformed silicide is performed to benefit from dopant segregation at low temperatures.

I-V measurements show comparable performance of the sSi GAA NW n- and p-type TFETs with currents up to 5 µA/µm at V_{dd}=0.5 V. Minimum SS below 60 mV/dec at room temperature has been demonstrated for the n-TFET though at low currents of about 10^{-6} µA/µm. For higher gate voltages the slope of the TFETs increases so that the average SS is larger than 60 mV/dec. Substantial analysis with pulsed *I-V* and low temperature measurements identify TAT as the dominant process in the subthreshold region hindering SS to overcome the thermal limit. Residual defects introduced by the tilted ion implantation at the source-channel tunnel junction as well as the large density of interface states D_{it}, as determined by charge pumping, give rise to significant TAT contribution. A reduction of the trap density by a high temperature anneal is not an option since this would lead to enhanced dopant diffusion and thus to less sharp dopant profiles. Nevertheless, the performance of sSi GAA NW p- and n-TFETs of this work are comparable to the reported state-of-the-art Si NW p-TFETs which still indicate better characteristics (SS, I_{on}, I_{off}) compared to most Group-IV [154] and III-V TFETs [59].

Basic analog parameters such as g_m, g_d and g_m/I_d of the sSi GAA NW TFETs were extracted. Based on the first two parameters the intrinsic voltage gain has been calculated showing high voltage gain of 260 at V_{dd} of 0.5 V. This high value which even outperforms the number of correspondingly scaled MOSFETs is explained by the

very small conductance g_d that implies good output saturation in TFETs. As a result, these TFETs might be serving as low power common source amplifier.

With the possibility to fabricate n- and p-TFETs on the same chip, CTFET inverters have been studied in order to evaluate the feasibility of the sSi GAA NW TFETs for logic circuits. The first set of fabricated inverters indicated basic core functionality providing the two distinct logical output states in the voltage transfer characteristics. However, because the TFETs suffer from ambipolar conduction the inverter noise margin was strongly degraded. A short-term solution has been proposed by work function shift of the p- and n-TFET to reduce the contribution of the parasitic current. For a full suppression of the ambipolar behavior at device level, a selective SiO_2 spacer at the drain side of the TFETs has been applied to create a drain underlap. The fabricated inverters with this suppression approach demonstrated improved voltage transfer characteristics and larger inverter gain in comparison to CTFET inverter with ambipolar behavior. Consequently, the noise margins are also improved from 20% to 40% of the applied V_{dd} (max. 50% of V_{dd}) leading to a more robust CTFET inverter. Furthermore, without the presence of ambipolar behavior the current flow in the static case is lowered by about two orders of magnitude and hence offers a substantial reduction of the static power consumption.

With these optimized CTFET inverters, the logic circuit investigation has been extended to the 6T-SRAM cell by evaluating the static functionality of half-SRAMs for the first time. In this regard, three sSi GAA NW TFETs have been integrated on one chip. Measurements of the butterfly curves indicated that the unidirectional property of TFETs limits the SRAM operation in the 6T-cell. The critical component is the outward facing access transistor in the circuit topology which forces the p-i-n diode structure of the TFETs in forward bias for certain cell operations. This leads to severe current leakage and therefore malfunctioning of the storage operation, even without the contribution of ambipolar behavior. It has been demonstrated that lowering the voltage bias at the bit-lines mitigate the p-i-n leakage resulting in functional hold, read and write operation for the 6T cell design.

The experimental demonstration of sSi GAA NW TFETs in simple logic circuits is a step forward regarding the question whether TFETs can replace the MOSFETs. The effect of ambipolarity and the unidirectional current transport are identified as the two major obstacles for TFETs in CMOS integrated circuits. While the ambipolar behavior can be suppressed at device level, the unidirectional current transport needs to be circumvented on circuit level by modifying the circuit layouts or changing the voltage bias configuration to enable circuit functionality with TFETs. This mainly relates to circuit topologies relying on pass-transistors where voltage levels have to be transferred back and forth. Alternatively, new circuit specifically designed for CTFET might be helpful.

The presented sSi GAA NW TFETs still require improvements in ON-current as well as in SS in order to be considered as an option for the semiconductor industry for low power applications. Further optimization is expected for scaling down the EOT below 1 nm which has been successfully demonstrated for Ge/GeSn heterojunction TFETs [173]. More important, however, is the formation of a highly doped source region with small trap densities in the oxide-channel and source-channel interface ($< 10^{10}$ /cm^{-2}-eV [29]) to achieve a larger current range with SS $<$ 60 mV/dec. In this regard ion implantation should be avoided. Instead other approaches such as in-situ doping by selective epitaxial growth produce a box like doping profile with low defects in order to enhance the BTBT current and to minimize TAT. Most recently, remarkable results have been achieved by *Memisevic et al.* demonstrating vertically grown III-V nanowire TFETs with SS $<$ 60 mV/dec for currents up to 0.31µA/µm with the largest I_{60} current reported for TFETs to date [174]. This exemplifies that there is still room for further improvements in TFETs to meet the performance of theoretical simulations. Under those conditions, TFETs would outperform MOSFETs in terms of switching speed and power consumption at supply voltages $V_{dd} \leq 0.5$ V [175],[176].

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List of Publications

Journal papers

- A. Biswas, G. V. Luong, M. F. Chowdhury, C. Alper, Q. Zhao, F. Udrea, S. Mantl, and A. M. Ionescu, "Benchmarking of Homojunction Strained-Si NW Tunnel FETs for Basic Analog Functions," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1441–1448, Apr. 2017.

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