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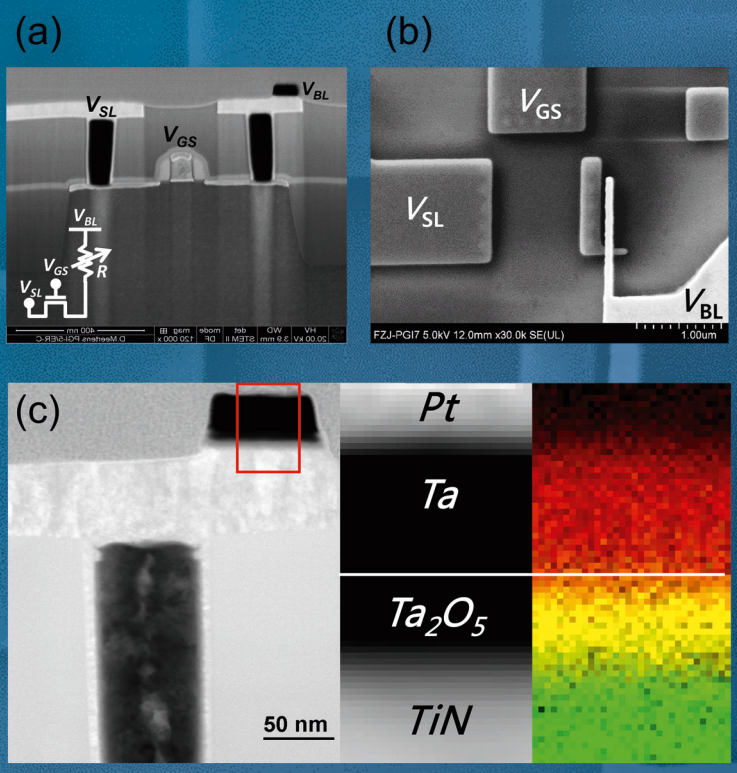

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Kurzfassung

Redox-basierte Speicherzellen (Redox-based Resistive Random Access Memory, ReRAM) sind von aktuellem Interesse für hochintegrierbare, kostengünstige, und energieeffiziente nicht-flüchtige Speicher (Non-Volatile Memory, NVM). Im Rahmen dieser Arbeit wurden Ta_2O_5-basierte Speicherzellen entwickelt, hinsichtlich verschiedener Gesichtspunkte untersucht und optimiert: (i) Untersuchung der schaltenden Ta_2O_5-Schicht, (ii) Einfluss der ohmschen Elektrode, (iii) Entwicklung formierfreier ReRAM-Zellen, (iv) Integration von ReRAM-Zellen und Halbleitertransistoren (MOSFET) und (v) die Implementierung einer modularen arithmetischen Funktion aus ReRAM-Blöcken.

Unterschiedliche Ansätze wurden verfolgt, um die Schalteigenschaften durch Modifikation der Ta_2O_5 Schicht zu verbessern. Bei der Abscheidung wurde der Effekt verschiedener Leistungen beim Hochfrequenzsputtern untersucht. Ebenso wurden unterschiedliche Materialdicken und Ta_2O_5/TaO_x - Doppelschichten getestet. Das optimierte Bauteil mit einer 7 nm dicken Ta_2O_5 - Schicht zeigt eine niedrige Formierspannung (1.8 V), eine akzeptable Schreibspannung (0.8 V) und ein gutes Widerstandsverhältnis ($R_{OFF}/R_{ON} > 300$) bei einer hohen Ausdauer von 10^6 Zyklen ($V_{RESET-STOP}$ = -2.0 V) und einer hohen Lebensdauer eines Zustandes von 10^4s bei 125°C. Die Schalteigenschaften des Oxids konnten durch die Modulation der Defektdichte im Oxid, welche durch eine Variation der Depositionsrate erfolgte, weiter verbessert werden, wobei die Depositionsraten über die Leistung beim Hochfrequenzsputtern einstellbar sind. Die besten Ergebnisse für eine 7 nm dicke Ta_2O_5 - Schicht wurden bei einer Leistung von 236 W gemessen, bei der insgesamt stabiles Schalten ($R_{OFF}/R_{ON} > 800$ bei $V_{RESET-STOP}$ = -2.2 V) mit hoher Ausdauer und Stabilität der Zustände vorliegt. Wird als schaltendes Oxid eine Ta_2O_5 (7 nm)/TaO_x (20 nm)-Bilayer-Schicht verwendet, kann der hochohmige Schaltzustand bei niedriger Strombegrenzung (50 μA) durch eine bessere Kontrolle über Defekte in der Ta_2O_5 - Schicht weiter optimiert werden. Allerdings erhöht sich durch die zugefügte TaO_x - Schicht - trotz ihrer hohen Leitfähigkeit - die Formierspannung von 1.8 V auf 3.8 V.

In bipolar schaltenden Speicherzellen hängen die Schalteigenschaften nicht nur von den Oxideigenschaften, sondern auch vom Material der ohmschen Elektrode ab. Zu diesem Zweck wurden vier verschiedene Elektrodenmaterialien (W, Ta, Ti und Hf) in eine Ta_2O_5 - Speicherzelle integriert und untersucht. Für Hf- und Ti-Elektroden ergaben sich Fehler beim Reset, wo hingegen Zellen mit W- und Ta-Elektroden ein stabiles Schalten zeigen. Dabei läuft der Resetprozess mit der W- Elektrode schneller ab, wo hingegen der Schaltprozess mit der Ta-Elektrode schneller abläuft. Diese Ergebnisse können auf der Basis von Defektformationsenergien (E_{VO}) in der Ta_2O_5 - Schicht erklärt werden: Die E_{VO} zur Erzeugung einer Sauerstoffleerstelle in der Ta_2O_5 - Schicht hängt vom Material der angrenzenden Elektrode ab und beträgt -1.5 eV für die Hf-Elektrode, -0.6 eV für die Ti-Elektrode, 0.1 eV bei einer Ta-Elektrode und 1.4 eV für eine W- Elektrode. Positive E_{VO} sind die Grundvoraussetzung für stabiles Schalten, da sich bei negativen E_{VO} die Anzahl der Sauerstoffleerstellen kontinuierlich erhöhen und somit eine nicht - schaltbare

leitende Schicht bilden würde. Höhere positive E_{VO} begünstigen den Einbau von Sauerstoffionen in die Oxidschicht. Dies erklärt den beobachteten schnelleren Ausschaltvorgang in Speicherzellen mit Wolframelektrode gegenüber dem schnelleren Einschalten in Zellen mit Tantalelektrode.

Parasitäre Kapazitäten in den Speicherelementen führen zu unerwünschten, hohen Entladeströmen, die besonders während des Formierprozesses die Speicherzelle dauerhaft beschädigen können. Daher ist die Reduzierung der Formierspannung auf 0 V sehr wichtig. Solche Speicherzellen werden als formierfreie Speicher bezeichnet. Formierfreie Speicher konnten in dieser Arbeit für unterschiedlich schaltende Oxidmaterialien (HfO_2, Ta_2O_5) und verschiedene Depositionsmethoden (PVD, ALD) durch Ionenimplantation von Sauerstoff (Dosis: $5.0 \times 10^{15}/\mathrm{cm}^2$ bei 30 keV) und Stickstoff (Dosis: $1 \times 10^{15}/\mathrm{cm}^2$ bei 30 keV) realisiert werden. Dadurch konnten die Formierspannungen in HfO_2 - Zellen von 3.8 V (ALD - HfO_2) und 1.8 V (PVD - Tao) auf jeweils 0 V gesenkt werden. Dabei bleiben die Schalteigenschaften der Speicherzellen (das $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ - Verhältnis, die Lebensdauer sowie die Stabilität der eingeschriebenen Zustände) vergleichbar zu den Zellen ohne Ionenimplantation. Um hohe Entladeströme durch die Formierungs- und Einschaltprozesse zu vermeiden, wurden die Speicherzellen in MOSFET-Strukturen integriert. Dies schafft die Möglichkeit, das inhärente Schalten der Zellen zu betrachten, indem das intrinsische nicht-lineare (NL) Verhalten der Ta_2O_5 - Schichten in einer 1T-1R-Konfiguration mit kontrollierten Strombegrenzungswerten (I_{CC}) analysiert wird. Die Nicht-Linearität wächst bei sinkendem Begrenzungsstrom. Die höchste Nicht-Linearität hat einen Wert von 12 und wurde bei einer Strombegrenzung von 3 μA gemessen. Dabei ist sie unabhängig von der Oxiddicke (7 nm, 13 nm) oder der Zellgröße (85 nm, 105 nm, 135 nm).

Abschließend wird ein neuer Ternärer-Modulo-Addierer Algorithmus, der auf einem ternären Zahlensystem basiert und Modulo-Operationen nutzt, für ReRAM Zellen mit mehreren Zuständen (Multilevel) gezeigt. Zur Überprüfung konnte die Addition von zwei 2-stelligen ternären Zahlen $\mathbf{p} = \mathrm{p}_1\mathrm{p}_0 = 21$ und $\mathbf{q} = \mathrm{q}_1\mathrm{q}_0 = 22$ mit drei Multilevelzellen ausgeführt werden. Die hierfür genutzten Zellen besitzen eine W-ohmsche Elektrode und sieben Speicherzuständen in einem Bereich von 1.1 $k\Omega$ bis 4.0 $M\Omega$. Basierend auf dem vorgestellten Algorithmus werden für die Übertrags- und Summenberechnung die Operanden p und q stellenweise an die Elektroden angelegt und das Ergebnis als Zustand der Zelle gespeichert. Damit eine gleichmäßige Schrittweite der Eingangsoperanden vorliegt, werden die Eingangsspannungen unter Zuhilfenahme von einer Offsetspannung berechnet.

Abstract

Redox-based Restive Random Access Memory (ReRAM) has recently received strong attention due to its potential payout toward high density, low-cost, low-energy NVMs. Development and understanding of Ta_2O_5 based ReRAM devices in this research work have been made under following experiments, (i) Ta_2O_5 switching layer, (ii) ohmic electrode, (iii) Forming-free ReRAM devices, (iv) ReRAM and MOSFET integration, and (v) implementation of modular arithmetic function.

In order to optimize the Ta_2O_5 switching layer, various approaches such as the effects of RF sputtering power in Ta_2O_5 deposition, the thickness effect of Ta_2O_5 switching layer, and the Bi-layer (Ta_2O_5 / TaO_x) structure have been made. The optimized 7 nm-thick Ta_2O_5 ReRAM device shows lower V_{FORM} (1.8 V), reasonable V_{SET} (0.8 V) with large memory window (R_{OFF} / $R_{ON} > 300$ at $V_{RESET-STOP}$ = -2.0 V), stable endurance up to 10^6 cycles (@1.0 μs) and good retention at 125 °C for 10^4 seconds. Further, defect density in the switching oxide can also affect the switching properties of ReRAM devices and a modulation of defect density is possible by deposition rate variation. The layer deposition rate changes depending on RF sputtering power of Ta_2O_5 layer. The best RF power condition (236 W) at given layer thickness (7 nm) was found in terms of memory window (R_{OFF} / $R_{ON} > 800$ at $V_{RESET-STOP}$ = -2.2 V) with high reliability (retention and endurance) performance. By introducing optimal Bi-layer (Ta_2O_5 / TaO_x) stack in Ta_2O_5 ReRAM device, the R_{OFF} performance further improves with 7.0 nm-thick Ta_2O_5/ 20 nm-thick TaO_x at low I_{CC} level (50 μA) due to a better control of defects in the Ta_2O_5 switching layer. However, the V_{FORM} of the Bi-layer increases from 1.8 V to 3.8 V in spite of highly conductive nature of TaO_x layer.

In bipolar resistive switching device, the performance is not only the function of oxide layer but also the ohmic electrode. Thus, the effect of ohmic electrode (OE) materials (W, Ta, Ti and Hf) in the Ta_2O_5 ReRAM device is analyzed. Early RESET failure has been observed from Hf-electrode and Ti-electrode while stable switching (RESET-SET) is shown from W-electrode and Ta-electrode. The faster RESET speed is observed with W-electrode compared with Ta-electrode in order to achieve similar R_{OFF} state. On the contrary, the SET speed is faster with Ta-electrode compared with W-electrode. The results can be explained with defect formation energy (E_{VO}) in Ta_2O_5 layer. The E_{VO} for the Ta_2O_5 layer is estimated to be -1.5 eV for Hf-electrode, -0.6 eV for Ti-electrode, 0.1 eV for Ta-electrode and 1.4 eV for W-electrode. A positive E_{VO} is required for stable switching, as the negative E_{VO} would result in a continuous increase of oxygen vacancy defect,V_O in the switching film, resulting in a non-switchable, conducting film. For the positive E_{VO}, the higher E_{VO} with W-electrode favors incorporation of the oxygen ions into the switching oxide layer decreasing the total amount of the V_O inside the switching oxide , therefore the RESET speed becomes faster with W-electrode. On the contrary, the lower E_{VO} with Ta-electrode can increase the amount of the V_O

inside the Ta_2O_5 layer, thus the SET speed becomes faster with Ta-electrode.

Since the high V_{FORM} can damage ReRAM devices especially in passive array configuration due to high overshoot current from its corresponding high parasitic discharge, it is highly required to reduce the V_{FORM} to 0 V i.e. forming-free. True forming-free devices are realized regardless of switching oxide material (Ta_2O_5, HfO_2) and its deposition methods (PVD, ALD) by optimized O_2 IIP ($5.0 \times 10^{15}/cm^2$ at 30 *k*eV) and N_2 IIP ($1.0 \times 10^{15}/cm^2$ at 30 *k*eV). The V_{FORM} has been reduced from 3.8 V (ALD-HfO_2), 1.8 V (PVD-Ta_2O_5) to 0 V. And the forming-free ReRAM devices with the O_2 IIP show comparable electrical performances in R_{OFF}/R_{ON} ratio, data retention and endurance. Next, ReRAM device is integrated with MOSFET in order to study the inherent switching property of device by inhibiting the unwanted overshoot current from the forming and SET process. Therefore, intrinsic non-linearity (NL) property of Ta_2O_5 ReRAM is analyzed in 1T-1R configuration with controlled I_{CC} levels. As the I_{CC} level decreases, the corresponding NL increases. The highest NL value of 12 is achieved from the $I_{CC} = 3.0\,\mu$A. The switching layer thickness (7.0 nm, 13 nm) and device size (85 nm, 105 nm, 135 nm) of the ReRAM devices do not show an impact on the NL value.

In the end, a new generic application of ReRAM devices is demonstrated. The resistor logic of ternary arithmetic is successfully proven with sum of two Trit modular addition with the ternary numbers, $\mathbf{p} = p_1p_0 = 21$ and $\mathbf{q} = q_1q_0 = 22$. Because the sum output $z = z_2z_1z_0$ needs three Trit digits, three ReRAM devices are required for this operation. Therefore, W-OE based Ta_2O_5 ReRAM array (1×3) with multi-state (7-states) realization from each device is used to implement the modular arithmetic. The used resistances for the 7-states range from 1.1 $k\Omega$ to 4.0 $M\Omega$. Based on the proposed schemes for the calculation of carry and sum, the logic operands p and q are applied to top electrode (TE) and bottom electrode (BE), respectively. An OFFSET voltage (V_{OFFSET}) is used to enable an equal stepping of operand voltages.

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Contents

Chapter 1

Introduction

Cost reduction is the main driving force for steadily increasing integration densities in the non-volatile memory business. Non-volatile memory (NVM) can retrieve the stored information even after power of system is turned off.

For the last decade, NAND Flash memory has been a dominant player in NVM markets due to its smaller feature size ($4F^2$) with simple memory cell structure. The method of choice to decrease cost of NAND Flash memory is to integrate more and more devices on the same area. However, NAND Flash memory is approaching its physical limits for multi-level capability, data retention, and etc..

Thus, new NVM concepts, which do not rely on charge storage like NAND Flash, are in the focus of nowadays research. Recently, Redox-based Resistive Random Access Memory (ReRAM) has been considered as a strong candidate for next generation memory application due to its simple device structure with excellent performance in terms of high memory window, good retention and excellent endurance with fast switching. The concept of ReRAM relies on the resistive switching effect where simple Metal-Insulator-Metal (MIM) devices can switch their resistance over several orders of magnitude. This change in resistance is non-volatile but reversible and can be triggered by appropriate voltage application.

Studies have shown that the region responsible for the change in resistance is very small, offering a tremendous potential in further down-scaling to the limit where NAND Flash cannot reach. Additionally, the device structure of these elements is a much simpler two terminal structure while Flash memory

needs three terminals. Especially, Ta_2O_5 -based ReRAMs draw a significant attention since they have demonstrated an excellent performance in term of higher endurance ($>10^{12}$), long retention at low current operation and fast switching [1–3]. The easiest and most area efficient structure is the passive crossbar array without a select transistor at each storage node, contrary to current charge based memory devices (NAND/NOR Flash memories).
In addition, the ReRAM has gained strong attention in new pioneering research areas to realize logic functionality [4, 5], intrinsic modular arithmetic using a ternary number system [6–10] and the functionality of neurons in the human brain [11, 12].

1.1 Scope of this work

The main focus of this work is to find out how each device parameter such as Ta_2O_5 thickness, Bi-layers (Ta_2O_5 -TaO_x), Ta_2O_5 sputtering power, Ta-OE thickness, and OE-materials can impact the performance of ReRAM devices in terms of switching cycles, memory window, non-linearity and reliability (retention and endurance). And also a capability for ternary arithmetic is shown with Ta_2O_5 ReRAM.
In the following chapter, an overview on the redox-based resistive switching and the corresponding materials is given. The development of switching oxide stack is analyzed in in Chapter 3 with following three sections. Sputtering parameters of the Ta_2O_5 and thickness of switching oxide layer will be discussed more in detail. After the optimization of switching oxide layer and the device properties, new type of switching stack with Bi-layer (Ta_2O_5 - TaO_x) will be introduced and impact of TaO_x layer on the ReRAM device performance will be shown.

- Effects of RF sputtering power in Ta_2O_5 switching oxide
- Ta_2O_5 switching layer thickness effect
- Bi-layer (TaO_x/Ta_2O_5) ReRAM Device

In chapter 4, effects of ohmic electrode (Ta, W, Hf, Ti) and thickness variation of Ta-ohmic electrode in Ta_2O_5 ReRAM will be discussed in two

sections.

- Role of ohmic electrodes (Ta, W, Hf, Ti)
- Thickness effect of Ta-OE

Defect formation energy for each ohmic electrode and thickness of Ta-ohmic electrode in Ta_2O_5 will be discussed. Difference of defect formation energy can affect the switching parameters such V_{FORM}, V_{SET}, V_{RESET} and the switching speed of RESET and SET process. Various device fabrication parameters of Ta_2O_5 ReRAM devices to reduce the forming voltage such as switching layer thickness and OE thickness, rapid thermal annealing (RTA) at different temperature in oxygen ambient and a new method to achieve a forming-free ReRAM devices will be discussed in Chapter 5 with three sections.

- Stack engineering of Ta_2O_5 ReRAM
- Lowering forming voltage with RTA process
- Forming-free ReRAM devices

In chapter 6, the ReRAM device is integrated with MOSFET device and the different characteristics of Ta_2O_5 based ReRAM in 1T-1R configuration are studied. The device parameters such as forming voltage, Non-Linearity and resistance ratio are analyzed at various current compliance levels for different device sizes and switching layer thicknesses.
The realization of an intrinsic modular arithmetic using a ternary number system has been made based on 7-states resistance levels of Ta_2O_5 ReRAM device in chapter 7.
Finally, the conclusion of the performed work and suggestion of future work are given in chapter 8.

Chapter 2

Principles of Resistive Random Access Memory (ReRAM)

A resistive switching (RS) memory is a two-terminal resistor device where the resistance state can be changed electrically between low-resistance state (LRS) and high-resistance state (HRS) based on how the resistor device is programmed as shown in Fig. 2.1. There are a couple of different RS memory types such as phase change memory, redox-based resistive memory, magnetoresistive memory and etc.. In this study, a focus will be made on the redox-based resistive memory.

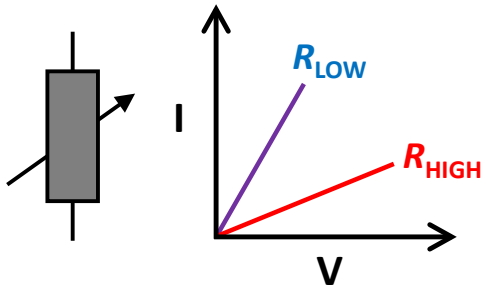


Figure 2.1: Schematic of a two-terminal RS memory element that can be switched between LRS and HRS.

2.1 Redox-based resistive memory

There are three major RS memory types in the redox-based resistive random access memory (ReRAM) memories, valence change memory (VCM), electrochemical memory (ECM) and thermochemical memory (TCM). A simple difference between ECM and VCM/TCM is that the conductive filament is induced by a metal ions (cation) migration in ECM while by an oxygen migration in VCM/TCM [13, 14].

2.1.1 Valence change memory: VCM

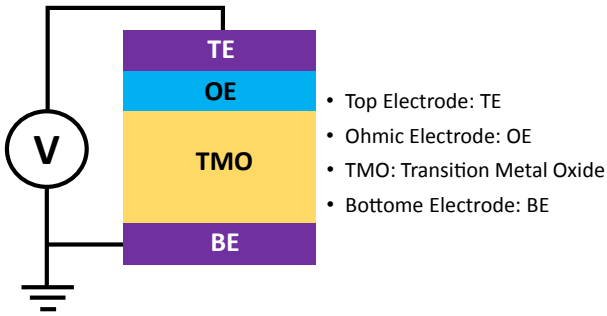


Figure 2.2: Cross-sectional structure of VCM cell, a OE is introduced to the TE side to induce an oxygen exchange reaction and generate an initial concentration of defects (i.e., oxygen vacancies) serving as a reservoir for the SET and RESET processes.

Fig. 2.2 shows a schematic of VCM cell and transition metals for TMO are Hf [15, 16], Ta [1, 2], Ti [17], or many others. The ohmic electrode (OE) also consists of the same transition metal used for TMO or different transition metals, e.g., a Ti/HfO_2 stack [18], or the same, e.g., a Hf/HfO_2 stack [19]. The use of the OE has been shown to improve switching since it allows the forming voltage (V_{FORM}) to be controlled. The OE acts as oxygen getter introducing oxygen vacancies and other types of defects in the TMO layer. The enhanced defect concentration causes a higher leakage current in the initial condition before forming, which can produce lower V_{FORM}. The valence change memory

(VCM) operates based on the internal changes of the transition metal oxide in between two electrodes and the changes are related to intrinsic defects of transition metal oxide. The mobile defects are oxygen vacancies or cation interstitials. The local motion of these defects induces a local valence change of the cations triggering a resistance switching [13, 20].

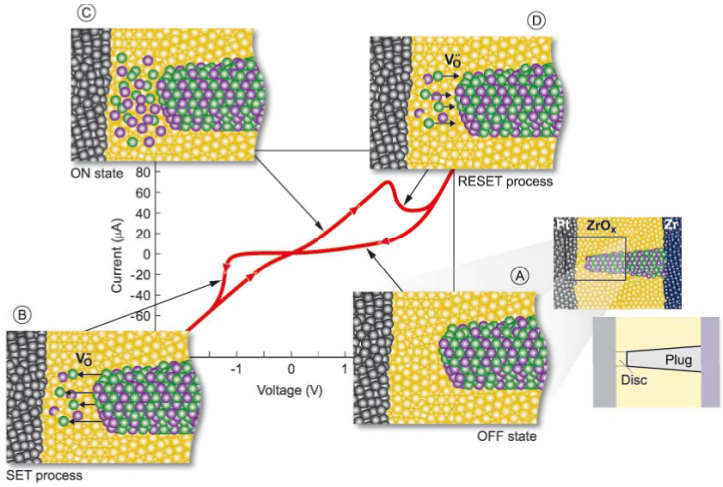


Figure 2.3: Illustration of VCM cell change during SET (B) and RESET (D) processes. Reprinted with permission of the authors [21].

Due to the large variety of defects present in dielectrics and their capability to alter the electrical properties in response of their motion, the resistive swtiching is observed in various oxides, including large bandgap dielectrics, most of the existing transition metal oxides (HfO_2 , WO_3, TiO_2, Ta_2O_5, ZnO_2), and perovskites ($SrTiO_3$) [14, 20].

The switching mechanism in VCM is based on the generation and migration of oxygen vacancies [22] through a field-assisted thermally activated hopping. VCM cells switch in a filamentary mode under bipolar operation conditions, with set and reset controlled by opposed drift of the ionic defects, in combination with redox reactions at electrode interfaces as shown in Fig. 2.3. Typically, VCM requires an forming step as an initialization of cell since it remains highly resistive at the initial state. Therefore, the V_{FORM} is higher

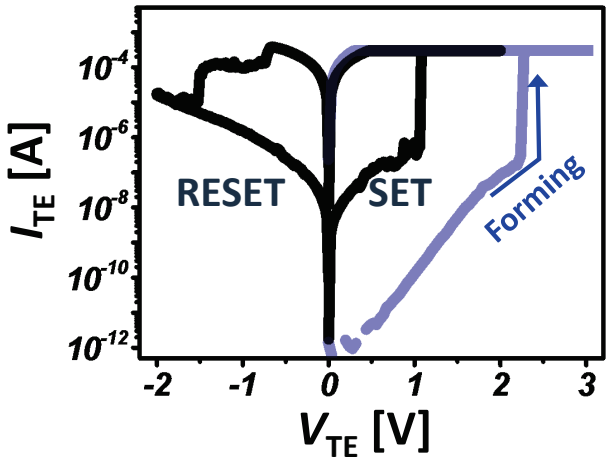


Figure 2.4: Typical *I-V* curves of Forming, RESET and SET in VCM based Ta_2O_5 ReRAM device.

than the voltages required for SET and RESET. Typical IV curves of bipolar filamentary switching (Forming, RESET and SET) for VCM cell is shown in Fig. 2.4.

2.1.2 Electrochemical metallization memory: ECM

In electrochemical metallization memory (ECM), the insulator material is an oxide or solid electrolyte such as chalcogenide thin film [21, 23] and one of the cell electrodes is made of an electrochemically active metal (such as Cu or Ag) while the other electrode is consisted of inert auxiliary electrode e.g. Pt, Ir, W. As shown in Fig. 2.6. During SET process, a positive voltage is applied to the active electrode leading to an oxidation (dissolution) of the electrode material while a deposition of metal (Ag or Cu) at the auxiliary electrode. Due to the high electric field, the deposited metal propagates in a filamentary form and it creates a short circuit in the cell, defining the low resistive ON state [24–26]. During RESET process, the filament can be dissolved by applying a voltage of an opposite polarity to turn the cell back in the high resistive OFF state [27].

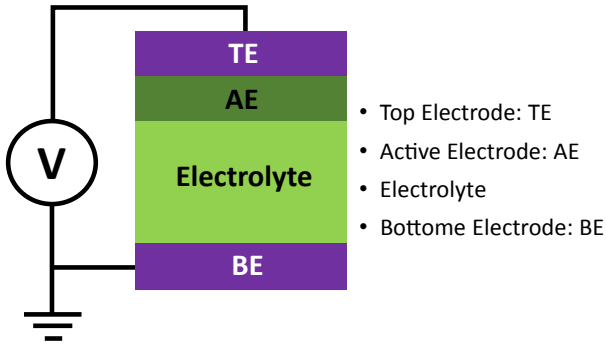


Figure 2.5: Cross-sectional structure of ECM cell, the metallic AE on the TE side consists of Ag, Cu, or alloys containing high-mobility metals to enable migration of those metallic ions and conductive filament (CF) (dis)connection in the solid electrolyte.

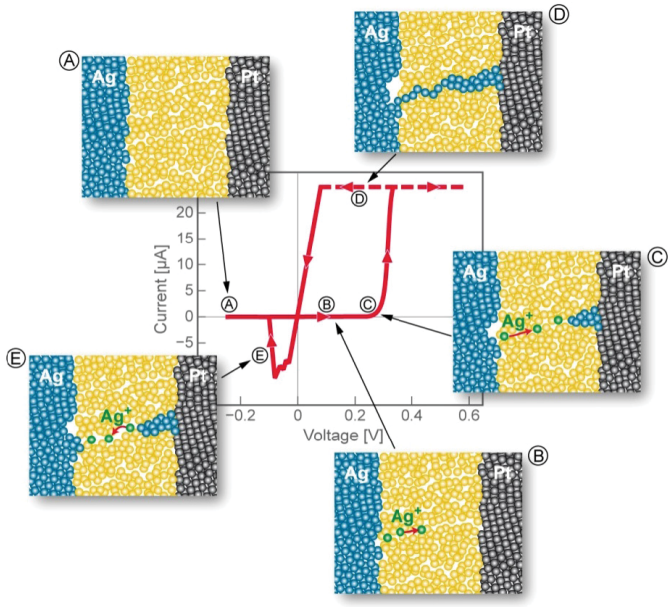


Figure 2.6: Illustration of ECM cell change during SET ((A)-(D)) and RESET (E) processes. Reprinted with permission of the authors [21].

2.1.3 Thermochemical Memory: TCM

Thermochemical switching relies on the material change within the functional layer without involvement of any electrode. As the switching is based on thermal effects, it is unipolar, i.e., the transitions between the resistive states can be induced by the same bias voltage polarity [28, 29]. Conductive filaments are formed during the electroforming process needed prior to memory switching. The forming process is initiated by the dielectric breakdown of the oxide and subsequent Joule's heating creating a filamentary conducting path between the two metallic electrode. The reason for the change in the resistance of CF during Forming and SET is reduction of the oxide within the filament creating better conducting suboxide phases or if the oxygen deficiency is high enough, metallic phase. The RESET transition can be described as a thermally activated solid-state process resulting in a local decrease of the metallic species. In order to stabilize the switching, a current limiter is used to prevent thermal breakdown of the conduction path.
NiO has been a typical material for resistive switching based on the TCM effect [28]. In NiO based metal insulator metal (MIM) structures, the stoichiometric oxide is thermochemically reduced to impure metallic Ni during the Forming and SET processes. The RESET process is carried out with lower voltage compared to the SET process.

Chapter 3

Development of Ta_2O_5 switching oxide

In this chapter, sputtering parameters of the Ta_2O_5 and thickness of switching oxide layer will be discussed in detail. After the material and the device properties optimization, new type of switching stack with Bi-layer (Ta_2O_5 - TaO_x) will be introduced and impact of TaO_x layer on the ReRAM device performance will be shown.

3.1 Effects of RF sputtering power in Ta_2O_5 switching oxide

In order to activate the resistive switching in the Ta_2O_5 ReRAM device, an electroforming step is required in which a conductive filament (CF) containing a high concentration of oxygen vacancies is formed [30, 31]. The forming voltage (V_{FORM}) is generally proportional to initial resistance state (R_{initial}) of the device [32] and is much higher than the switching voltage [33]. The high V_{FORM} can cause unstable resistance switching or degraded reliability [34]. Stable switching performance depends on controlled CF formation [35, 36]. Uncontrolled size of the CF can be caused by the high V_{FORM} due to increased parasitic capacitance discharge especially in passive array of ReRAM devices. Therefore, it is highly important to investigate, which process parameter in the Ta_2O_5 ReRAM can control the R_{initial} and V_{FORM} along with high switching performance such as off-state resistance

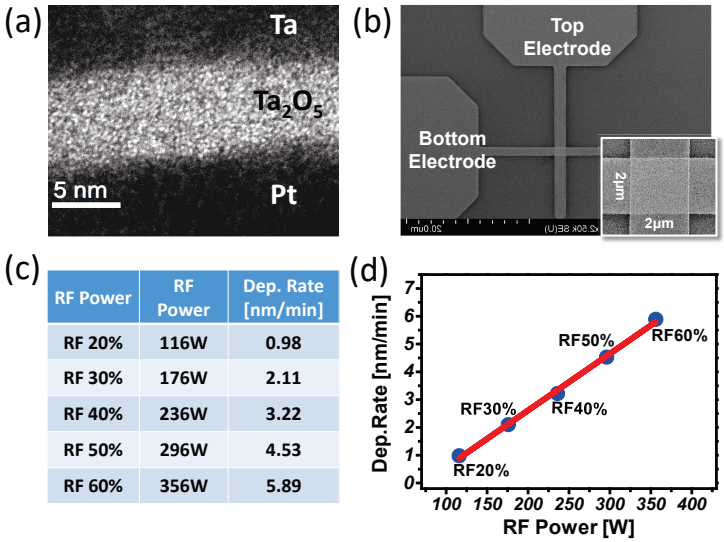
(R_{OFF}) and on-state resistance (R_{ON}) ratio, endurance and retention. Thickness reduction of switching oxide is one of the options to lower the V_{FORM} [19]. However, the approach causes higher leakage in the device and degrades the resistance window (R_{OFF} / R_{ON}), reliability and retention properties. Optimizing switching oxide by relative oxygen flow amount during reactive sputtering has been reported [37, 38]. However, it is difficult control the oxygen partial pressure during film deposition with flow control [39–41] and the uncontrolled film deposition can lead to hard forming process,resulting in an unstable switching, or sometimes, the devices become too conductive to realize the stable switching due to reset failures [39], [42]. Here, we report an alternative way to optimize the Ta_2O_5 thin-film for the reduction of the V_{FORM} and stable ReRAM performance by tailoring the reactive sputtering power (RF) during Ta_2O_5 film deposition at fixed oxygen flow. The thin-film growth rate is controlled by the sputtering RF power.

3.1.1 Device Fabrication

A bottom electrode (BE) with 30 nm-thick Pt is patterned on top of 430 nm-thick thermally grown SiO_2 layer from silicon wafer and 7 nm-thick Ta_2O_5 is deposited by reactive sputtering under process gas mixture of Ar (77%) and oxygen (23%) with 5 different conditions of RF power (116W, 176W, 236W, 296W, 356W) at the chamber pressure of $2.3\times\ 10^{-2}$ mbar. Regardless of RF power, a constant 7 nm-thick Ta_2O_5 has been deposited based on pre-calculated deposition rate for each RF condition. Without breaking the vacuum, 7 nm-thick Ta ohmic electrode and 25 nm-thick Pt are deposited by RF and DC sputtering, respectively. All depositions are performed at room temperature. Next, the top electrode (TE) is etched down with Reactive Ion Beam Etching (RIBE).

A TEM image of device stack from RF40% condition is shown in Fig. 3.1(a) confirming the amorphous nature of the Ta_2O_5 layer and its thickness to be 7 nm. Fig. 3.1(b) shows the SEM images of the Ta_2O_5 based ReRAM device with $2\times2\ \mu m^2$ size. 5 different RF power conditions for the Ta_2O_5 sputtering with corresponding deposition rate are shown in Fig. 3.1(c) and the deposition rate is linearly dependent on the RF sputtering power in Fig. 3.1(d).

The Ta_2O_5 film thickness has been verified by X-ray reflectometry (XRR).



RF Power	RF Power	Dep. Rate [nm/min]
RF 20%	116W	0.98
RF 30%	176W	2.11
RF 40%	236W	3.22
RF 50%	296W	4.53
RF 60%	356W	5.89

Figure 3.1: (a)TEM images of the Pt/Ta_2O_5/Ta/Pt ReRAM devices confirming target thickness of the corresponding layers. (b) Scanning electron microscopy image of the ReRAM device in crossbar configuration with inset image showing the device $2\times2\mu m^2$ device. (c) deposition rate for each RF power. (d) linear correlation between Ta_2O_5 deposition rate and the corresponding RF powers

The device electrical characterization has been performed with Agilent B1500A parameter analyzer for DC measurement and Keithley 4200SCS for AC measurement.

3.1.2 R_{initial}, V_{FORM} and 1st reset current

The box plots of initial resistance (R_{initial}) and forming voltage (V_{FORM}) for all RF power conditions are shown in Fig. 3.2(a) based on 50 devices for each RF power. The highest R_{initial} is observed from the RF20% (116W, $80\,G\Omega$) and then the R_{initial} starts decreasing rapidly up to $300\,k\Omega$ with RF30% (176W). The RF40% (236W) shows the lowest $R_{\text{initial}} = 50\,k\Omega$ and then, the resistance starts increasing again from RF50% (296W). The RF60% (356W) has the 2nd highest R_{initial} ($4\,M\Omega$) with wider distribution range. A similar trend is observed from the V_{FORM} in dark gray. The RF20% (116W) shows the highest $V_{\text{FORM}} = 3.8\,\text{V}$ and the forming voltage decreases abruptly with

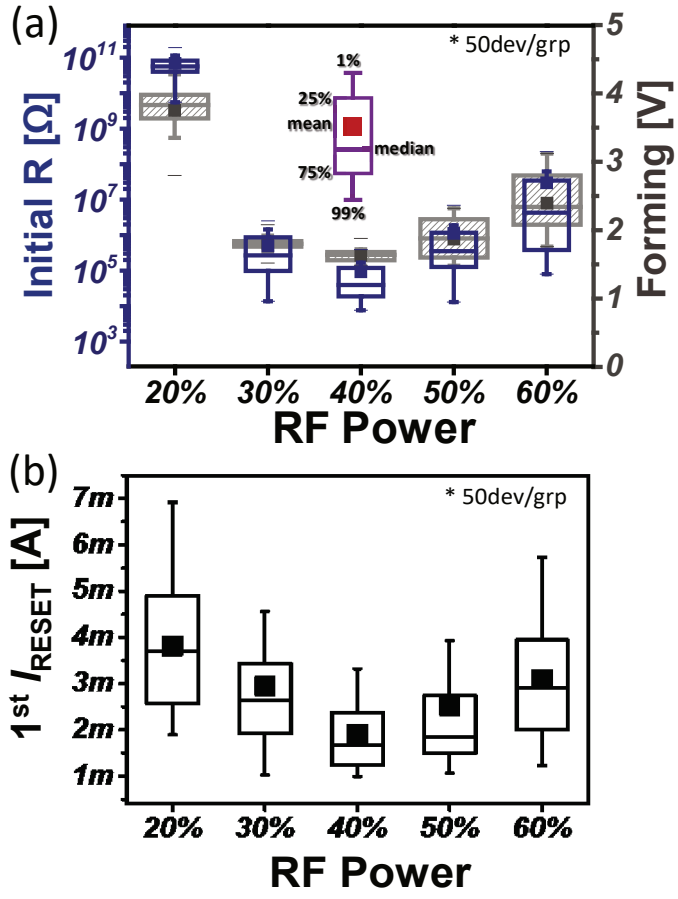


Figure 3.2: (a) Dependence of R_{initial} and V_{FORM} on the RF sputtering power for the TaO_x thin-film deposition. (b) Dependence of 1st reset current (I_{RESET}) on the RF sputtering power for the Pt/TaO_x/Ta/Pt ReRAM devices.

RF30% (176W, V_{FORM} = 1.8 V). The RF40% (236W) has the lowest V_{FORM} = 1.6 V and after that, the forming voltage starts increasing with RF50% (296W, V_{FORM} = 1.9 V). The RF60% (356W) has the 2nd highest V_{FORM} = ∼2.3 V with wider distribution range. In overall, the RF20% (116W) and RF60% (356W) show distinctively higher R_{initial} and V_{FORM} than the other conditions.

The 1st reset current (I_{RESET}) after the forming is compared for different RF

power condition since it shows a strong correlation with the V_{FORM}, shown in Fig. 3.2(b). Increased 1st I_{RESET} for higher V_{FORM} is expected due to the parasitic discharges during the forming process. The devices having RF20% condition show the highest 1st I_{RESET} (3.8mA),while the lowest I_{RESET} is observed from the RF40% (1.7mA). The non-monotonic behaviors of R_{initial} and V_{FORM} over sputtering power change are assumed to originate from the conflicting relationship between structural defect and oxygen content in oxide. Upsurge of the deposition rate leads to higher structural defect density in the thin-film, while the oxygen content on the contrary decreases. Lower oxygen content corresponds to a decrease of R_{initial}, whereas more structural defects in film will increase the R_{initial} [43].

3.1.3 $V_{\mathrm{RESET-STOP}}$ Effects on Device Performance

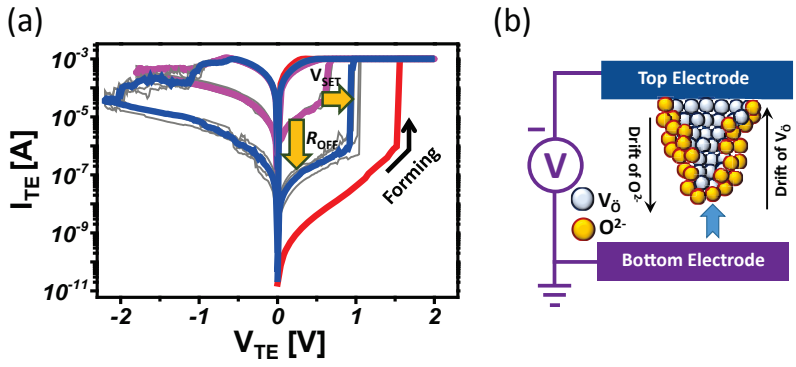


Figure 3.3: (a) Typical FORMING-SET-RESET *I-V* characteristics of the $Pt/Ta_2O_5/Ta/Pt$ ReRAM device. (b) A schematic diagram of the RESET process including the drift of oxygen vacancies towards the TE and an additional oxygen exchange reaction occurring at the TE/switching layer interface.

Typical *I-V* switching curves with RF40% (236W) are shown at two different reset stop voltage ($V_{\mathrm{RESET-STOP}}$) conditions (-1.8 V, -2.2 V) in Fig. 3.3(a). The $V_{\mathrm{RESET-STOP}}$ is defined as the maximum voltage applied during reset sweep. The thin gray lines correspond to multiple switching cycles for each $V_{\mathrm{RESET-STOP}}$ and the bold lines represent the average switching curve. The

off resistance state (R_{OFF}) and set voltage (V_{SET}) increase together with higher $V_{RESET-STOP}$. The $V_{RESET-STOP}$ = -2.2 V shows ~20 times higher R_{OFF} than $V_{RESET-STOP}$ = -1.8 V, while the R_{ON} remains same for both conditions. At the same time, the V_{SET} increases from 0.7 V to 1.0 V with higher $V_{RESET-STOP}$ = -2.2 V. A sketch of the reset mechanism including the movement of oxygen vacancy and oxygen ions is shown in Fig. 3.3(b). During the reset process, oxygen vacancies are depleted at the Pt-BE increasing the Schottky barrier height and hence the resistance increases. A higher voltage leads to a stronger depletion of oxygen vacancies close to the BE, i.e. the effective gap between filament and BE is increased, and thus the resistance is further increased. Therefore, depending on the sub-stoichiometry and the density of oxygen vacancy in the Ta_2O_5 thin-film, the characteristics of R_{OFF} are expected to change, which means each different RF power for the Ta_2O_5 sputtering can generate its modulated R_{OFF} value at the given $V_{RESET-STOP}$.

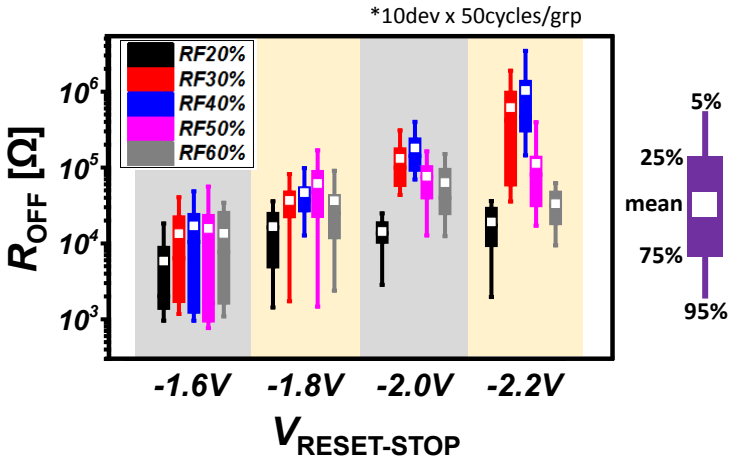


Figure 3.4: R_{OFF} change depending on $V_{RESET-STOP}$ for five different RF powers (20%, 30%, 40%, 50% and 60%) of the Ta_2O_5 ReRAM device.

The R_{OFF} changes with different $V_{RESET-STOP}$ conditions from -1.6 V to -2.2 V have been investigated in DC mode depending on the 5 different RF sputtering powers in Fig. 3.4. Each RF power has statistically been analysed

in bar plot based on 50 switching cycles of 10 devices. As we expected, the increased R_{OFF} is observed with higher $V_{RESET-STOP}$ for all RF sputtering powers. However, RF20% (116W), RF50% (296W) and RF60% (356W) start showing the saturated R_{OFF} values even though the $V_{RESET-STOP}$ keeps increasing. Especially, an earlier R_{OFF} saturation has been observed from the RF20% (116W) starting at $V_{RESET-STOP}$ = -1.8 V and the saturated R_{OFF} ($< 20\,k\Omega$) is the lowest value among the ones from all RF conditions. The R_{OFF} values from RF20% (116W), RF50% (296W) and RF60% (356W) become flat starting at $V_{RESET-STOP}$ as low as -1.8 V. Continuous R_{OFF} increase is observed only from the RF30% (176W) and RF40% (236W) as the $V_{RESET-STOP}$ becomes higher. At the $V_{RESET-STOP}$ = -2.2 V, the RF40% (236W) shows the highest R_{OFF} ($> 1M\Omega$), while the lowest R_{OFF} ($<20\,k\Omega$) is observed from the RF20% (116W). The RF40% (236W) increases the R_{OFF} faster than the RF30% (176W) meaning a higher R_{OFF} can be achieved with RF40% (236W) at the given $V_{RESET-STOP}$. The R_{OFF} is mainly modulated by Schottky barrier height between switching oxide, Ta_2O_5 and high WF metal, Pt electrode [44–47]. It seems that the Schottky barrier height is influenced by RF power conditions due to the different sub-stoichiometry and vacancy density in the pristine state of the switching layer, which determines the construction of conductive filaments during the forming process. Therefore, the modulation of R_{OFF} has been observed by the change of RF power.

The R_{ON} of RF30% (176W), RF40% (236W) and RF50% (296W) shows similar values ($\sim$600Ω) over all $V_{RESET-STOP}$ ranges, while the RF20% (116W) and RF60% (356W) have slightly higher R_{ON} with wider distribution in Fig. 3.5. Since the RF30% (176W) and RF40% (236W) can keep the R_{ON} values lower over all $V_{RESET-STOP}$ ranges with highly increased R_{OFF}, the both RF conditions show a good R_{OFF}/R_{ON} ratio unlike the other conditions as shown in Fig. 3.6. The RF40% (236W) shows a memory window (R_{OFF}/R_{ON}) higher than 10 even at low $V_{RESET-STOP}$ = -1.6 V and higher than 800 at $V_{RESET-STOP}$ = -2.2 V. The RF20% (116W) and RF60% (356W) show the R_{OFF}/R_{ON} ratio less than 50 even at the $V_{RESET-STOP}$ = -2.2 V with early saturated ratio and the RF50% (296W) has the similar saturation with a bit higher R_{OFF}/R_{ON} ratio. Therefore, it can be concluded that the RF40% (236W) is more suitable sputtering power to realize multi-level cell

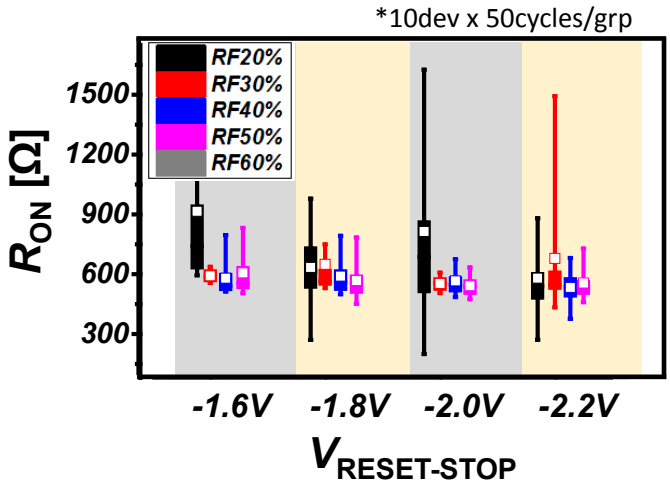


Figure 3.5: R_{ON} change depending on $V_{RESET-STOP}$ for five different RF powers (20%, 30%, 40%, 50% and 60%) of the Ta_2O_5 ReRAM device.

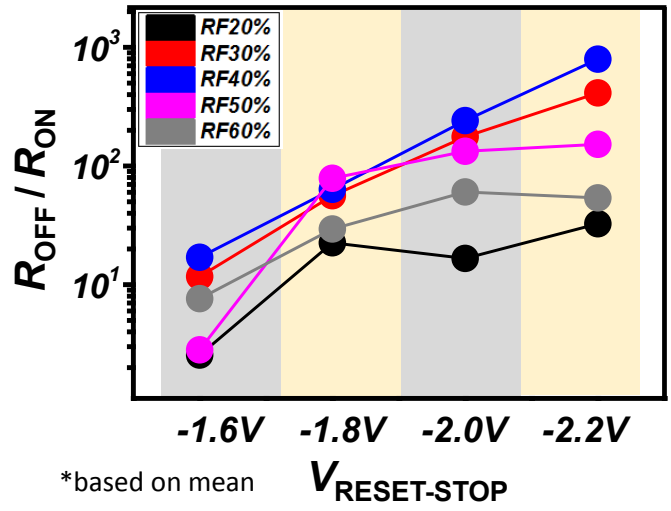


Figure 3.6: R_{OFF}/R_{ON} ratio change depending on $V_{RESET-STOP}$ for five different RF powers (20%, 30%, 40%, 50% and 60%) of the Ta_2O_5 ReRAM device.

(MLC) operation in the Ta_2O_5 ReRAM since the condition can offer improved memory window.

The correlation between the R_{OFF} and the V_{SET} for 3 different RF powers (20%, 40%, 60%) has been analyzed in Fig. 3.7.
The R_{OFF} and the V_{SET} have been extracted based on DC I-V switching cycles with 10 devices from each RF power condition by varying the $V_{RESET-STOP}$ from -1.6 V to -2.2 V with the increment of -0.2 V under the set current compliance (I_{CC}) of 1.0 mA and single device has 50 switching cycles for each $V_{RESET-STOP}$ condition.

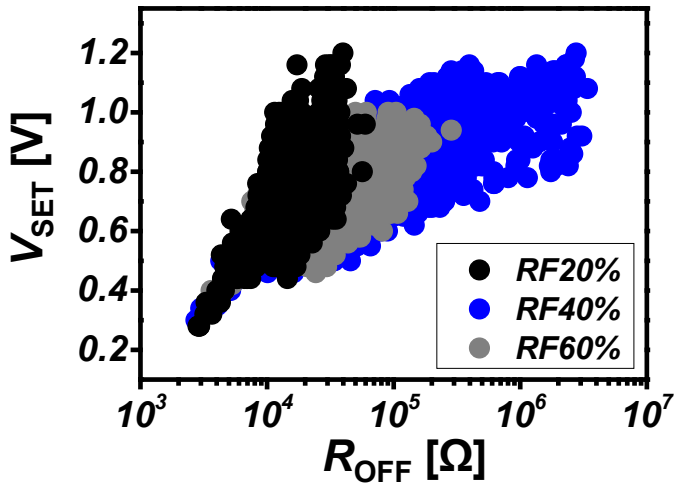


Figure 3.7: A fitting between the R_{OFF} and its corresponding V_{SET} depending on RF powers (20%, 40%, 60%) for the Ta_2O_5 ReRAM device.

As the R_{OFF} increases, the corresponding V_{SET} also becomes higher as observed from Fig. 3.3(a). The RF20% (116W) seems to have steeper correlation between the R_{OFF} and the V_{SET} compared with the RF40% (236W) and the RF60% (356W) under similar R_{OFF} ranges (3 $k\Omega$ ~40 $k\Omega$). The RF40% (236W) and RF60% (356W) show similar trends up to R_{OFF} ~200 $k\Omega$ range. However, the RF40% (236W) starts slightly deviating from this trend above 200 $k\Omega$ range.

3.1.4 I_{CC} Effects on Device Performance

The resistance of conductive filament becomes higher with lower current compliance [36]. Therefore, when the I_{CC} varies, its corresponding R_{ON} also

changes together. The R_{ON} variation with different I_{CC} conditions ranging from 400 μA to 1.0 mA at fixed $V_{RESET-STOP}$ = -1.8 V has been analyzed in DC mode in Fig. 3.8. The R_{ON} becomes lower as the I_{CC} increases regardless of the RF sputtering conditions.

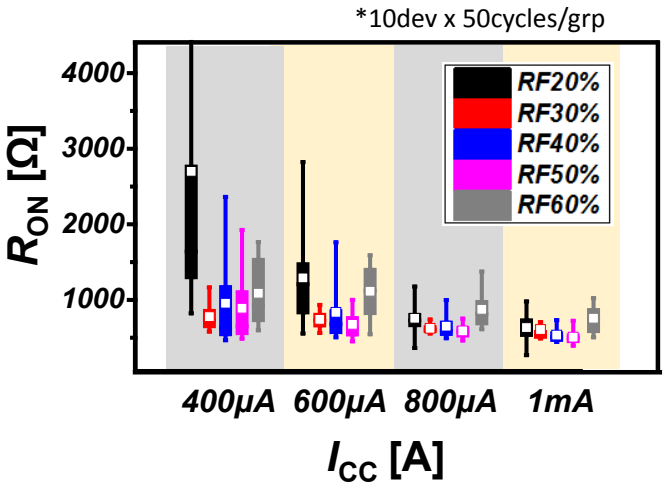


Figure 3.8: The R_{ON} comparison depending on I_{CC} levels with five different RF powers (20%, 30%, 40%, 50% and 60%) for the Ta_2O_5 ReRAM device.

The highest R_{ON} ($\sim 2.5\,k\Omega$) is observed from the RF20% (116W) with wider distribution among split conditions at I_{CC} = 400 μA. However, the R_{ON} difference between the RF20% (116W) and the rest of RF power conditions becomes smaller as the I_{CC} increases. The RF60% (356W) has slightly increased R_{ON} over all I_{CC} conditions while the rest of RF conditions (RF30%, 40% and 50%) show similar R_{ON} states over all I_{CC} ranges. The minimum I_{CC} required for stable switching from our Ta_2O_5 ReRAM is about 200 μA. When it is considered, the R_{ON} decrease from 1.0 mA to 400 μA is fairly small, only $\sim 2\times$ reduction for RF40% (236W) and $\sim 5\times$ reduction for RF20% (116W).

3.1.5 Multi-Level-Cell (MLC) Realization

For neuromorphic applications, the ReRAM needs to implement multilevel cell (MLC) capability which can store more than one bit (2 levels) in single

cell. The MLC capability of ReRAM can be realized by two approaches. The 1st approach is limiting I_{CC} during set operation [48] and the 2nd one is controlling the reset stop voltage ($V_{RESET-STOP}$) during reset process [49]. The 2nd approach to control the $V_{RESET-STOP}$ is favoured for MLC application since it can handle various high resistance states (HRS) by simply changing the $V_{RESET-STOP}$ [50][51][52]. A high resistance window between off-state resistance (R_{OFF}) and on-state resistance (R_{ON}) at reasonable voltage is desirable. The MLC capability of the Ta_2O_5 ReRAM device with different RF sputtering power have also been analysed in this experiment.
The narrow R_{ON} variation with I_{CC} change implies that limiting current during set operation is not a good option to implement the MLC operation in our Ta_2O_5 ReRAM. Since the RF40% (236W) shows the most desirable increase of R_{OFF} over $V_{RESET-STOP}$, more detailed R_{OFF} response from RF40% (236W) with wider $V_{RESET-STOP}$ ranges from -1.2 V to -2.4 V has been shown in Fig. 3.9.

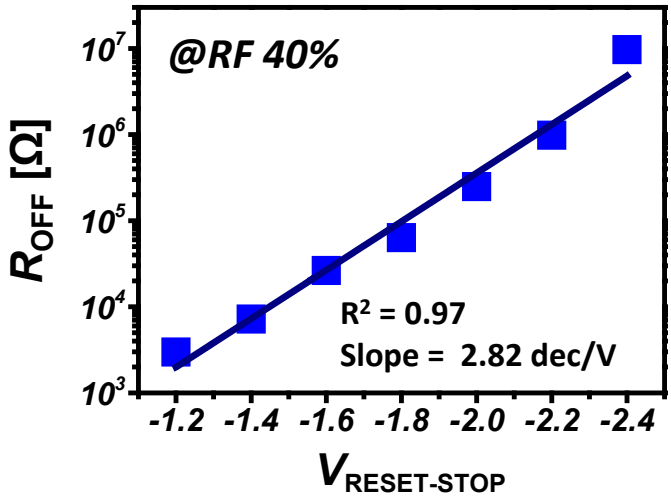


Figure 3.9: Relationship between the $V_{RESET-STOP}$ and its corresponding R_{OFF} for the RF40% condition. A linear regression and slope are calculated.

A well-fitted linear regression ($R^2 = 0.97$) between the $V_{RESET-STOP}$ and the R_{OFF} is observed with slope of 2.82 dec/V. Based on the calculated fitting-slope, we can expect $\sim \times 600$ higher R_{OFF} with only 1.0 V increase of

the $V_{\mathrm{RESET-STOP}}$. Based on the measurement results, it can be speculated that each RF power for reactive sputtering produces different electrical characteristics in the Ta_2O_5 ReRAM and the difference in electrical performance can be originated from the altered sub- stoichiometry and defect density of the Ta_2O_5 switching layer. And the largest $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio can be obtained from the RF40% (236W) and the RF condition can produce fairly high R_{OFF} ($\sim 10 M\Omega$) at reasonable $V_{\mathrm{RESET-STOP}}$(@-2.4 V), while maintaining low R_{ON}.

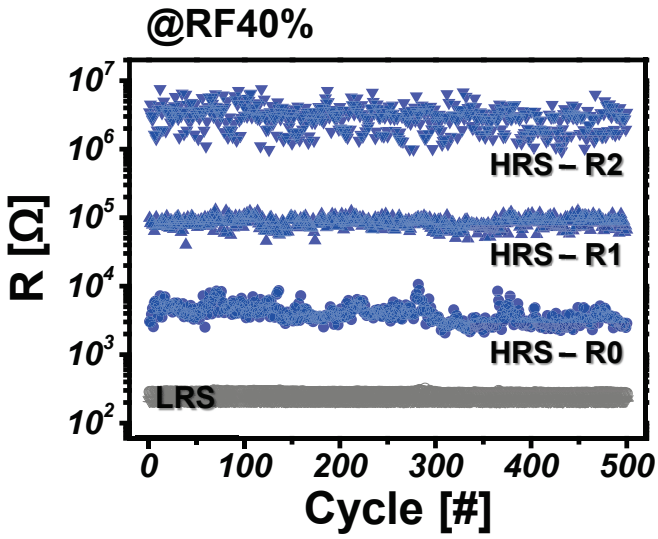


Figure 3.10: 2-bit MLC performance up to 500 cycling with 1.0 μs pulse width for both set and reset from RF40% condition

Therefore, further analysis on the RF40% (236W) condition has been carried out with short pulses in AC mode. Fig. 3.10 shows the AC operation of 2-bit multi-level-cell (MLC) with 1.0 μs single pulse up to 500 cycles with the RF40% (236W) condition. Prior to the reset pulse, the starting resistance level always maintains at the low resistance state (R_{ON}) $\sim 300\,\Omega$ for all R_{OFF} states. Each R_{OFF} state is achieved with 1.0 μs reset pulse and then the R_{OFF} state returns to the R_{ON} state with corresponding set pulse of 1.0 μs pulse width. The next higher resistance state is achieved with the increased amplitude of the reset pulse with fixed 1.0 μs pulse width. The state read in the AC mode has been

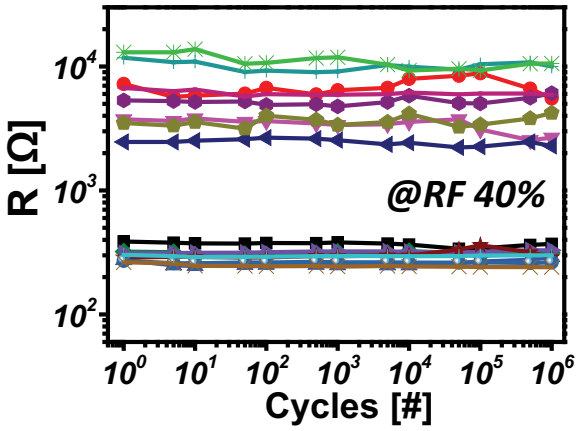


Figure 3.11: Endurance of the Ta_2O_5 ReRAM sputtered at RF40% (236W) condition up to 10^6 cycles based on pulse width of 1.0 μs for both reset and set.

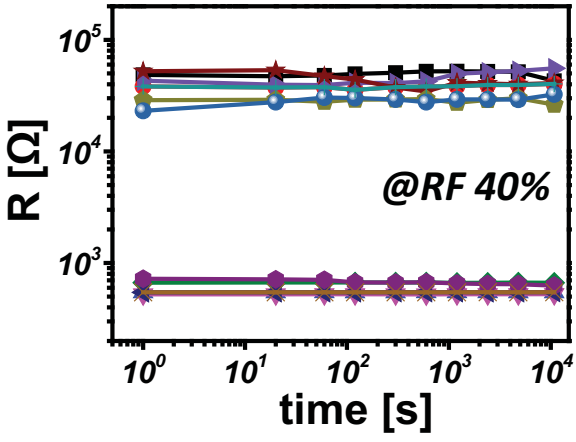


Figure 3.12: The retention of the 7 nm-thick Ta_2O_5 ReRAM sputtered RF40% (236W) condition. Both states are highly stable at 125°C up to 10^4 seconds.

performed with 1.0 μs at 0.2 V pulse amplitude. The multi-resistance states are made based on single pulse operation and the distribution of each HRS can be improved further by resistance state-correction algorithms.

3.1.6 Endurance and Retention of RF40% sputtered ReRAM Device

Successful endurance of 8 devices up to 10^6 cycles has been achieved for the 40% RF (236W) condition, shown in Fig. 3.11 and the applied reset conditions are -1.4 V $\sim$ -1.6 V with 1.0 μs pulse width. The resistance states in Fig. 3.11 are verified with the AC read pulse of 0.2 V with 1.0 μs pulse-width. The retention performance from the RF40% (236W) condition has been measured at 125°C up to 10^4 seconds with 7 devices and an excellent retention up to 10^4 seconds has been achieved as shown in Fig. 3.12.

3.1.7 Summary of this section

In this section, the impact of the RF sputtering power (116W, 176W, 236W, 296W, 356W) on the Ta_2O_5 ReRAM devices has been analyzed. The XPS results confirm that the relative amount of oxygen in the Ta_2O_5 thin-film decreases with higher deposition rate of film. The R_{initial} is a parabolic function of the RF sputtering power. From the RF20% (116W, 80 $G\Omega$) to the RF40% (236W, 50 $k\Omega$) power condition, the R_{initial} decreases, whereas it starts increasing again for the RF50% (296W, 200 $k\Omega$) and RF60% (356W, 2 $M\Omega$). The R_{OFF} has a close match with corresponding V_{FORM}, showing lowered R_{OFF} with higher V_{FORM}. The RF40% (236W) power condition shows the highest R_{OFF} with stable R_{ON} over all $V_{\text{RESET-STOP}}$ ranges and the highest memory window ($R_{\text{OFF}} / R_{\text{ON}} >$ 1,000 at $V_{\text{RESET-STOP}} =$ -2.2 V). The 2-bit MLC performance up to 500 cycling with 1.0 μs pulse width is achieved with RF40% (236W) sputtering power condition. These ReRAM devices show an excellent endurance up to 10^6 cycles with 1.0 μs pulse width and good retention at 125 °C for 10^4 seconds. This analysis could pave the way to optimize the switching material in order to obtain the high performing ReRAM device and will be highly beneficial for ReRAM device communities.

3.2 Ta_2O_5 Switching Layer Thickness Effect

As previously mentioned, ReRAM device structure is composed of a metal-oxide layer located between an oxidizable electrode and an inert electrode serving as an ohmic contact and a Schottky barrier respectively during the switching process. In general, it is considered that resistive switching is sustained by the formation and breakage of the conductive filament (CF) such as a metallic filament [53] and/or an oxygen vacancy filament formed in the oxide layer [54],[55]. The metallic filament is considered to be formed by metal ions migration from the oxidizable electrode toward the inert electrode during application of positive bias to the oxidizable electrode. The oxygen vacancy filament is caused by the migration of oxygen ions during application of negative or positive bias to the oxidizable electrode in the oxide layer. However, to activate the resistive switching in the Ta_2O_5 ReRAM device, an electroforming step is required by which a conducting filament containing a high concentration of oxygen vacancies is formed. The V_{FORM} is much higher than the switching voltage, and causes an important incompatibility with low-voltage scaled CMOS technology. Therefore, it is important to reduce the V_{FORM} as low as the SET voltage or to have the forming-free ReRAM devices. The forming-free ReRAM devices will be discussed in chapter 5. The V_{FORM} in ReRAM generally depends on the switching-oxide thickness and can be reduced for thinner oxide. However, effect of oxide thickness on the switching property has not been intensively investigated yet, while this issue is very important for device scaling. In this section, we studied thickness dependence of switching oxide Ta_2O_5 based on DC switching characteristics and respective retention properties.

3.2.1 Device Fabrication

30 nm-thick Pt as the BE is patterned on top of 430nm-thick thermally grown SiO_2 layer from silicon wafer and Ta_2O_5 with four different thickness (3 nm, 5 nm, 7 nm, 13 nm) is deposited by reactive sputtering under process gas mixture of Ar (77%) and oxygen (23%) with RF power 236W at the chamber pressure of 2.3 $\times$ 10^{-2} mbar. And then, without breaking the

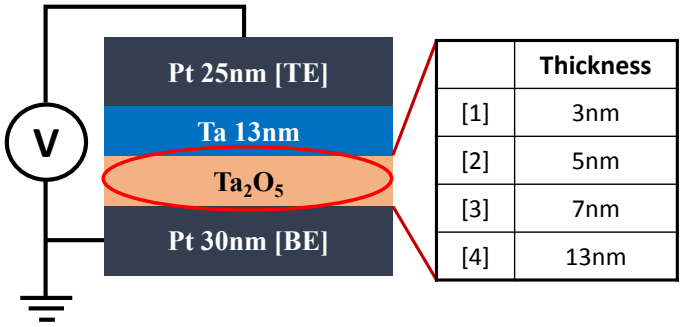


Figure 3.13: A schematic cross-sectional diagram of ReRAM device with 4 different experimental conditions of Ta_2O_5 thickness (3 nm, 5 nm, 7 nm, 13 nm) at fixed thickness of Ta-ohmic electrode and Pt-BE.

vacuum, 13 nm-thick Ta ohmic electrode and 25 nm-thick Pt are deposited by RF and DC sputtering, respectively regardless of Ta_2O_5 thickness. All depositions are performed at room temperature. Next, the top electrode (TE) is etched down with Reactive Ion Beam Etching (RIBE). A device schematic represents the thickness of each stacked layer and 4 different Ta_2O_5 thickness conditions in Fig. 3.13.

3.2.2 R_{initial} and V_{FORM}

The influence of the Ta_2O_5 thickness on the initial resistance and V_{FORM} was statistically investigated by measuring 48 devices from each Ta_2O_5 thickness split as shown in Fig. 3.14(a). The initial resistance was measured at $V_{\text{read}} = 0.1\,\text{V}$. A clear trend between the Ta_2O_5 thickness and R_{initial} was observed. The thinnest 3 nm-thick Ta_2O_5 ReRAM shows 20 $k\Omega$ resistance while the 13 nm-thick Ta_2O_5 ReRAM has the resistance of 25 $G\Omega$. On other hand, the 5 nm and 7 nm-thick Ta_2O_5 ReRAMs show 3 $M\Omega$ and 79 $M\Omega$. The forming process was performed by a positive DC voltage sweep applied to the TE with I_{CC} of 1.0 mA . The forming statistics of the four different Ta_2O_5 thickness splits are given in Fig. 3.14(b). A clear dependence of the V_{FORM} on the Ta_2O_5 thickness is observed. The lowest V_{FORM} is observed from the thinnest switching layer 3 nm (0.70 V in median), followed by the 5 nm

(1.16 V in median) and the 7 nm (1.80 V in median). The 13 nm-thick Ta_2O_5 ReRAM devices show the highest V_{FORM} (2.96 V in median).

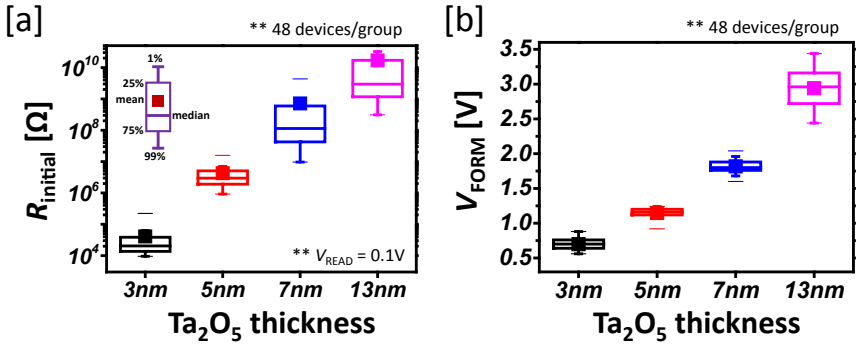


Figure 3.14: (a) Initial resistance measured at V_{read} = 0.1 V for Pt/Ta_2O_5/Ta/Pt ReRAM device for different switching thicknesses. (b) V_{FORM} of the Ta_2O_5 ReRAM device with four different thickness splits.

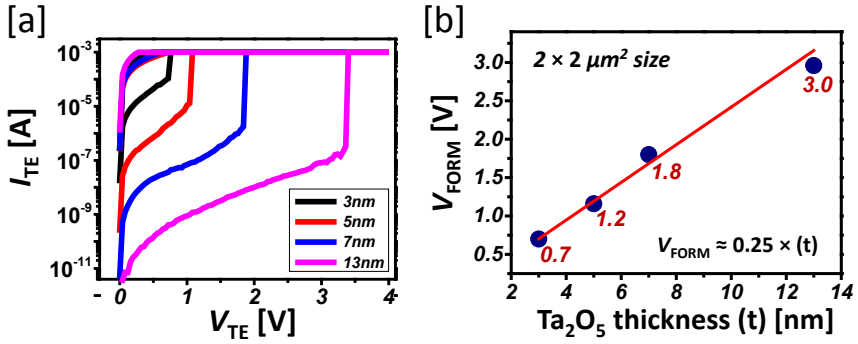


Figure 3.15: (a) Forming I-V curve up to +4.0 V DC sweep with 4 different Ta_2O_5 thicknesses (b) A correlation between the V_{FORM} and the Ta_2O_5 thickness showing a good linear fitting in red.

Fig. 3.15(a) shows the typical forming I-V curves from all different Ta_2O_5 thicknesses based on +4.0 V DC sweep with I_{CC} level of 1.0 mA . The correlation between the Ta_2O_5 thickness and V_{FORM} is plotted in order to

find out if the correlation is a linear or not in Fig. 3.15(b) and it shows a good linear fitting. From the data fitting in Fig. 3.15, a threshold electrical field to initiate the forming in 2 × 2 μm^2 Ta_2O_5 ReRAM is calculated to be 2.3 MV/cm. It might be claimed that by reducing the Ta_2O_5 thickness, the V_{FORM} can be reduced up to regular SET switching voltages [19], [18]. However, as the Ta_2O_5 thickness becomes thinner, the ReRAM devices will suffer performance degradation such as increased current leakage (lowered R_{OFF}) for off-state, earlier failure for reliability test and etc..

3.2.3 $V_{RESET-STOP}$ Effects on Device Performance

Fig. 3.16 shows the typical I-V curves of SET/RESET for all Ta_2O_5 thicknesses under identical measurement conditions of I_{CC} = 1.0 mA and $V_{RESET-STOP}$ = -2.0 V. It is clearly observed that as the Ta_2O_5 thickness increases, the corresponding off-leakage current (I_{OFF}) and V_{SET} increase.

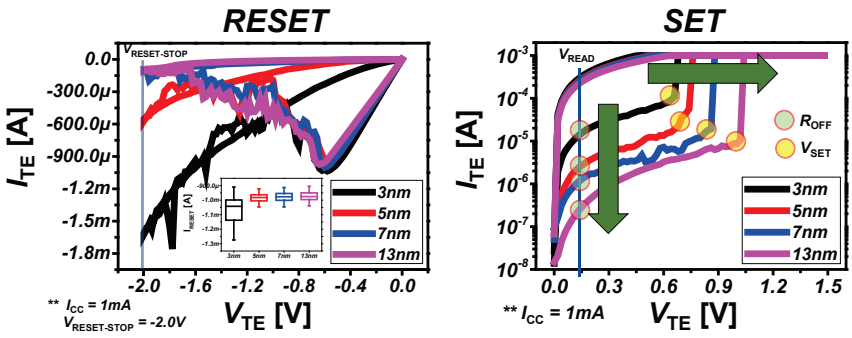


Figure 3.16: Typical RESET-SET I-V curves of Pt/Ta_2O_5/Ta/Pt for different switching layer thicknesses under identical measurement conditions ($V_{RESET-STOP}$ = -2.0 V, I_{CC} = 1.0 mA)

The I_{OFF} (measured at 0.1 V) for the 3 nm-thick Ta_2O_5 ReRAM is 10.0 μA in comparison to 150 nA for the 13 nm-thick,which is × 65 times lower. Both devices having 3 nm- and 5 nm-thick switching layers show the increase of reset current starting from -0.8 V and -1.2 V respectively during reset voltage sweep up to -2.0 V while continuous decrease of the reset current from the

7 nm- and the 13 nm-thick switching layers was observed after reset initiation at -0.6 V up to $V_{\mathrm{RESET-STOP}}$. The statistical analysis in DC-mode (based on 10 devices with 50 switching cycles for each switching layer thickness) has been made to compare the electrical performances such as R_{OFF}, R_{ON}, V_{SET} between Ta_2O_5 thickness splits in terms of $V_{\mathrm{RESET-STOP}}$ effect and I_{CC} effect.

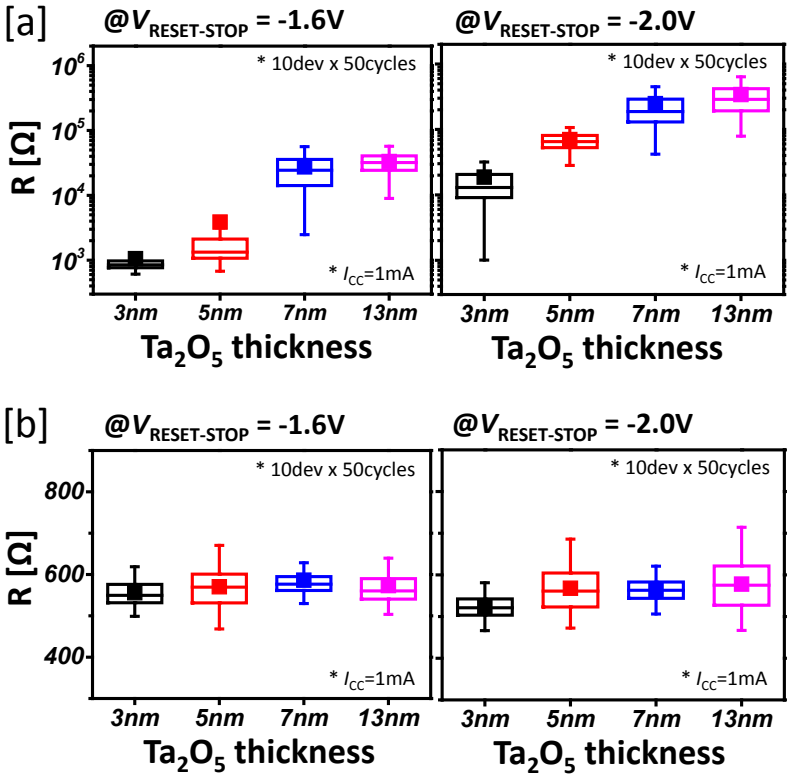


Figure 3.17: (a) R_{OFF} comparison at $V_{\mathrm{RESET-STOP}}$ = -1.6 V and -2.0 V (I_{CC} = 1.0 mA) for the Pt/Ta_2O_5/Ta/Pt ReRAM devices, (b) R_{ON} comparison at $V_{\mathrm{RESET-STOP}}$ = -1.6 V and -2.0 V (I_{CC} = 1.0 mA) for the Pt/Ta_2O_5/Ta/Pt ReRAM devices.

First, the effect of $V_{\mathrm{RESET-STOP}}$ is investigated. During the reset process, oxygen vacancies are depleted at the Pt-BE interface increasing the Schottky

barrier height and hence the resistance increases. A higher $V_{\mathrm{RESET-STOP}}$ leads to a stronger depletion of oxygen vacancies close to the BE, i.e. the effective gap between filament and BE is increased, and thus the R_{OFF} further increases. Two different comparisons of R_{OFF} have been made depending on applied $V_{\mathrm{RESET-STOP}}$ (-1.6 V and -2.0 V) under identical $I_{\mathrm{CC}} = 1.0\,m$A in Fig. 3.17 (a). At $V_{\mathrm{RESET-STOP}}$ = -1.6 V, the lowest R_{OFF} is observed from the 3 nm-thick Ta_2O_5 device (848 Ω in median) while the highest R_{OFF} is achieved from the 13 nm-thick Ta_2O_5 device (32 $k\Omega$ in median). And for the 5 nm- and 7 nm-thick Ta_2O_5 devices, the median values of R_{OFF} are 1.3 $k\Omega$ and 24.4 $k\Omega$ respectively. At $V_{\mathrm{RESET-STOP}}$ = -2.0 V, as expected, the 3 nm-thick device shows the lowest R_{OFF} (12.9 $k\Omega$ in median) while the highest R_{OFF} is observed from the 13 nm-thick device (288.3 $k\Omega$ in median). And for the the 5 nm- and 7 nm-thick Ta_2O_5 devices, the median values of R_{OFF} are 65.3 $k\Omega$ and 187.9 $k\Omega$ respectively. The R_{OFF} results from both $V_{\mathrm{RESET-STOP}}$ conditions clearly indicate that as the Ta_2O_5 thickness decreases the corresponding I_{OFF} at given $V_{\mathrm{RESET-STOP}}$ increases and vice versa. The R_{ON} is also analyzed depending on applied $V_{\mathrm{RESET-STOP}}$ (-1.6 V and -2.0 V) under identical $I_{\mathrm{CC}} = 1.0\,m$A in Fig. 3.17(b). Regardless of the Ta_2O_5 thickness, no difference in the R_{ON} was observed for both $V_{\mathrm{RESET-STOP}}$ (-1.6 V and -2.0 V). All thickness splits have the R_{ON} states between 500 Ω and 600 Ω without any trend. And the R_{ON} was not

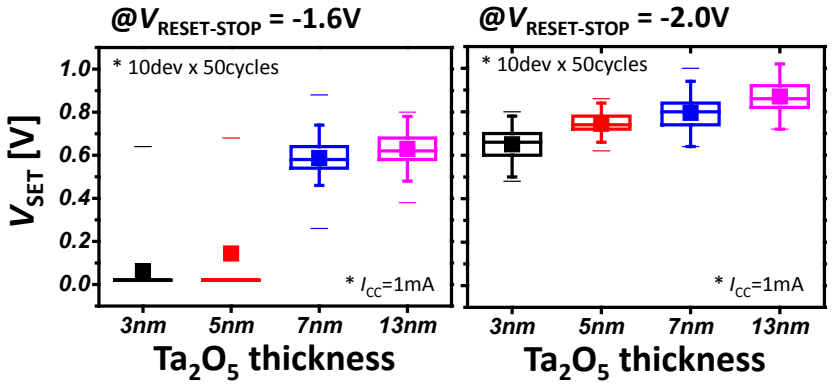


Figure 3.18: V_{SET} change at $V_{\mathrm{RESET-STOP}}$ = -1.6 V and -2.0 V ($I_{\mathrm{CC}} = 1.0\,m$A) for the Pt/Ta_2O_5/Ta/Pt ReRAM devices

influenced by the $V_{\mathrm{RESET-STOP}}$ since it will be dominantly affected by the I_{CC} level during the set process. Since the effective gap between conductive filament and the BE during the reset process becomes widened, the R_{OFF} further increases with higher $V_{\mathrm{RESET-STOP}}$. In Fig. 3.18, the statistical analysis of the V_{SET} has been made with two different $V_{\mathrm{RESET-STOP}}$ (-1.4 V, -2.0 V). At the $V_{\mathrm{RESET-STOP}}$ = -1.6 V, both 3 nm- and 5 nm-thick Ta_2O_5 devices don't show stable set switching, while quite stable set switching was observed from 7 nm- (V_{SET} = 0.58 V in median) and 13 nm-thick devices (V_{SET} = 0.62 V in median). At the $V_{\mathrm{RESET-STOP}}$ = -2.0 V, it is clearly observed that the V_{SET} increases with thicker Ta_2O_5 . The lowest V_{SET} (0.67 V) from 3 nm-thick device is observed and then the V_{SET} starts increasing to 0.74 V (@5 nm), 0.80 V (@7 nm) and 0.86 V (@13 nm).

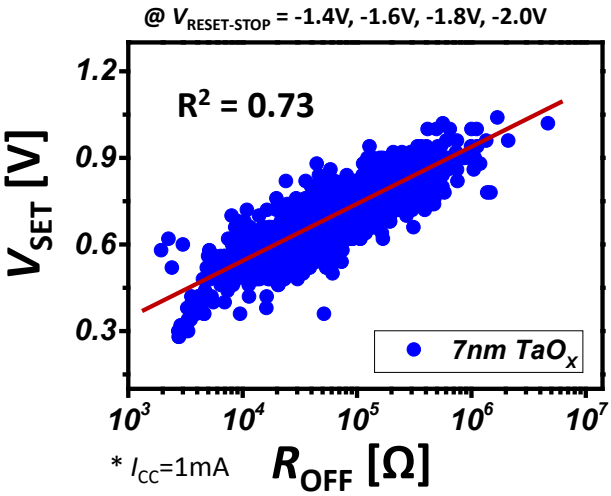


Figure 3.19: A correlation between the R_{OFF} and its corresponding V_{SET} for the 7 nm-thick Ta_2O_5 ReRAM device.

The R_{OFF} shows a strong correlation with Ta_2O_5 thickness as shown in Fig. 3.16 and Fig. 3.17(a). Therefore, it is expected that the V_{SET} can depend on the Ta_2O_5 thickness since the V_{SET} is expected to increase with higher R_{OFF}. The correlation between the R_{OFF} and the V_{SET} for 7 nm-thick Ta_2O_5 ReRAM device has been systematically analyzed in Fig. 3.19. The R_{OFF} and the V_{SET} have been extracted based on DC switching measurements from 10 devices by

varying the $V_{\mathrm{RESET-STOP}}$ from -1.4 V to -2.0 V with the increment of -0.2 V under the I_{CC} of 1.0 mA and each device has 50 switching cycles at given the $V_{\mathrm{RESET-STOP}}$ condition. A strong fitting with $R^2 = 0.73$ is observed. It is expected that similar fittings will be observed from the other Ta_2O_5 thicknesses (3 nm, 5 nm, 13 nm) as well as under different $V_{\mathrm{RESET-STOP}}$ conditions.

* 10dev. x 50cycles / grp

	V_{FORM}	V_{SET} @-2.0V	R_{OFF} / R_{ON} @-2.0V	V_{SET} @-1.6V	R_{OFF} / R_{ON} @-1.6V
3nm	**0.7**	**0.67**	**27**	**0.00**	**1**
5nm	**1.2**	**0.74**	**117**	**0.00**	**2**
7nm	**1.8**	**0.80**	**336**	**0.58**	**42**
13nm	**3.0**	**0.86**	**526**	**0.62**	**45**

** based on medians
** V_{READ} = 0.1V

Figure 3.20: Median Values of V_{FORM}, V_{SET} and $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ for different Ta_2O_5 thickness at $V_{\mathrm{RESET-STOP}}$ = -1.6 V and -2.0 V ($I_{\mathrm{CC}} = 1.0\,m$A)

Fig. 3.20 shows V_{FORM}, V_{SET} and $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ for the different Ta_2O_5 thickness at the $V_{\mathrm{RESET-STOP}}$ = -1.6 V and -2.0 V. The 3 nm-thick device shows the V_{SET} values close to the V_{FORM} at the $V_{\mathrm{RESET-STOP}}$ = -2.0 V meaning forming-free devices can be achieved with 3 nm-thick Ta_2O_5 since you can apply V_{SET} condition for the forming. However, this adversely affect the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ which is reduced to 27 in comparison of 526 for 13 nm-thick devices. Since the forming-free devices with 3 nm-thick device shows leaky R_{OFF} properties resulting in worsening the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$, the R_{ON} performance also was investigated by I_{CC} effect.

3.2.4 I_{CC} Effects on Device Performance

The I_{CC} level strongly affects the R_{ON} state and two distinct I_{CC} levels (400 μA, 1.0 mA) are applied in order to find out how the I_{CC} levels can impact the R_{ON}

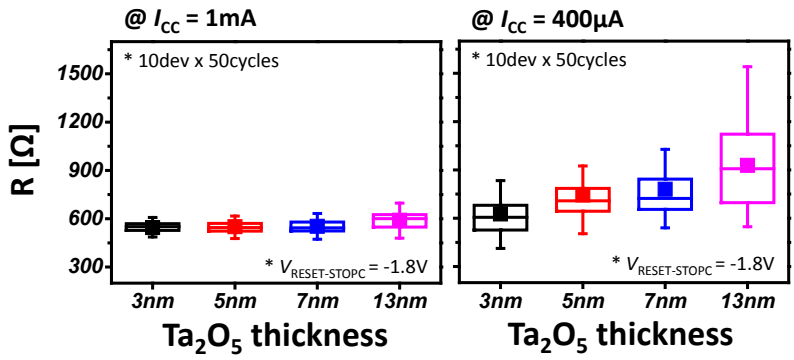


Figure 3.21: Dependence of R_{ON} for the different thickness of $Pt/Ta_2O_5/Ta/Pt$ ReRAM devices at I_{CC} = 1.0 mA, 400 μA (@$V_{RESET-STOP}$ = -1.8 V)

depending on the Ta_2O_5 thickness as shown in Fig. 3.21. At I_{CC} = 1.0 mA, no difference of R_{ON} is observed. However, at reduced I_{CC} = 400 μA, the R_{ON} increases with thicker Ta_2O_5 . 3 nm-thick ReRAM device shows the lowest R_{ON} (600 Ω), while the highest R_{ON} (900 Ω) is observed from 13 nm-thick switching layer with wider R_{ON} distribution. The R_{ON} = 700 Ω, 720 Ω are observed from 5 nm- and 7 nm-thick ReRAM devices, respectively.

3.2.5 Data Retention Comparison at 125°C

Retention test at 125 °C has been carried out for the devices with different Ta_2O_5 thickness as shown in Fig. 3.22. Since retention failure in our Ta_2O_5 devices is only observed starting from the R_{OFF}, the retention from R_{ON} is not shown for all conditions. Each line corresponds to the retention behavior of individual device. While the 13 nm- and 7 nm-thick Ta_2O_5 devices show fairly robust retention performance (with only single failure out of 20 devices), 50% devices of the 5 nm-thick Ta_2O_5 devices and 100% of the 3 nm-thick Ta_2O_5 devices show early retention failures.

3.2.6 Summary of this section

In summary, the impact of the switching layer thickness (3 nm, 5 nm, 7 nm, 13 nm) was analyzed on $Pt/Ta_2O_5/Ta/Pt$ ReRAM device. The $R_{initial}$ and

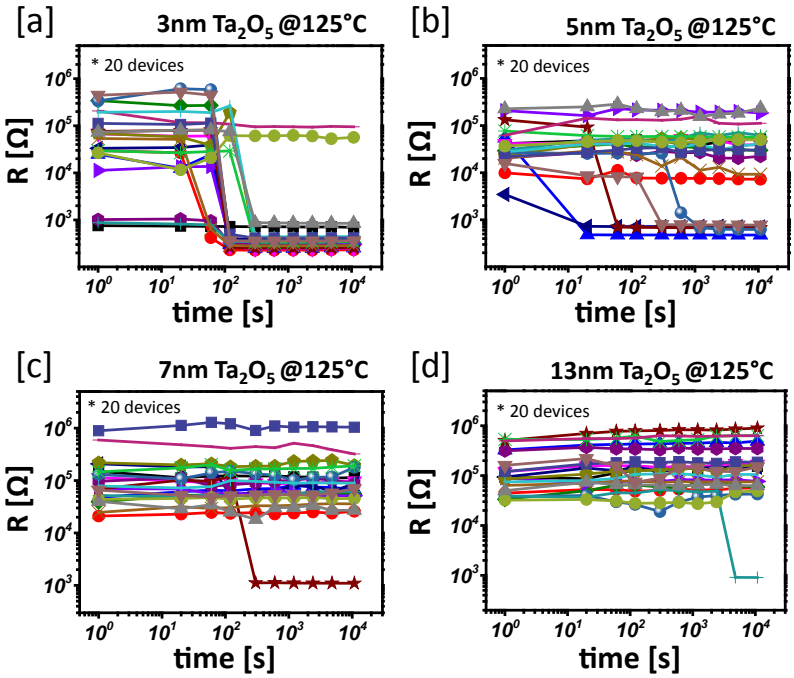


Figure 3.22: Retention data of 3 nm-, 5 nm-, 7 nm- and 13 nm-thick Ta_2O_5 ReRAM devices (20 devices from each split) at 125 °C for 10^4 seconds.

V_{FORM} decrease with thinner Ta_2O_5 layer. The V_{FORM} has a good linear fitting with the Ta_2O_5 thickness and a threshold electrical field to initiate the forming in 2×2 μm^2 Ta_2O_5 ReRAM was 2.3 MV/cm. Since the I_{OFF} reduces with thicker Ta_2O_5 layer, the R_{OFF} increases with thicker Ta_2O_5 at given $V_{RESET-STOP}$ while the R_{ON} remains similar regardless of Ta_2O_5 thickness. At the $V_{RESET-STOP}$ lower than -1.6 V, both 3 nm- and 5 nm- thick Ta_2O_5 layers didn't have stable set switching while robust set switching were observed from 7 nm- and 13 nm- thick Ta_2O_5 layers. The V_{SET} increases with thicker Ta_2O_5 layer as expected from R_{OFF} correlation with Ta_2O_5 thickness. At lower I_{CC} level (400 μA), the R_{ON} also increases with thicker Ta_2O_5 layer. Majority of devices from 3 nm- and 5 nm-thick Ta_2O_5 splits show early retention failures at at 125 °C, while excellent retention performance up to

10^4 seconds at 125 °C was observed from 7 nm- and 13 nm-thick Ta_2O_5 devices.

3.3 Bi-layer (Ta_2O_5/TaO_x) ReRAM Device

Since the ReRAM does not require electron charging/discharging for switching operation, the ReRAM has advantages in device scale-down [1, 13]. Especially, researchers have focused on ReRAM device because of its local switching and fast switching speed, which are the favorable characteristics for nano-device scaling. In order to realize low operation current and stable variability of switching parameters, various approaches such as bi-layer stacks and doping of switching oxide have been proposed and the main concept of those proposed approaches is an optimization of conducting filament [1, 56–58]. Because the conductive filament is made of defects (oxygen vacancies), the defects in switching layer can affect conduction property of filament. Therefore, neighboring defects in switching layer can affect device stability and proper amount of defects can realize more stable switching characteristics [59–62]. To optimize the defect engineering, bilayer structure (metallic oxide layer/switching layer) was chosen for this study. During the deposition of additional metallic oxide layer, the additional layer starts absorbing oxygen from the switching oxide layer. So, the amount of defect (oxygen vacancy) in switching oxide layer can be controlled by optimizing oxygen absorption rate of the metallic oxide layer. In the Ta_2O_5 ReRAM, a highly conducting oxide layer (TaO_x) has been inserted to modify the ReRAM device stack to $Pt/Ta_2O_5/TaO_x/Ta/Pt$. The effect of the TaO_x conducting layer has been studied on the ReRAM device characteristics such as R_{OFF}/R_{ON}, endurance and data retention.

3.3.1 Device Fabrication

In this study, 5 nm-thick Titanium (Ti) and 30 nm-thick Platinum (Pt) layers are deposited by sputtering on a thermally grown 450 nm-thick SiO_2 layer on Si substrate. Next, e-beam lithography and dry-etching processes are used to pattern the Pt layer with 80 nm line width acting as BE. After the nano-size patterning, 7 nm-thick Ta_2O_5 is deposited by reactive sputtering under the

Splits / Layers	Bi-20nm	No-Ta	REF
Top-Electrode	Pt (25nm)		
Capping	Ta (13nm)	**None**	Ta (13nm)
TaOx	**20nm**	**20nm**	None
Ta_2O_5	Ta_2O_5 (7nm)		
Bottom-Electrode	Pt (30nm)		
Stacks	Pt (25nm) Ta (13nm) TaO_x (20nm) Ta_2O_5 (7nm) Pt (30nm)	Pt (25nm) TaO_x (20nm) Ta_2O_5 (7nm) Pt (30nm)	Pt (25nm) Ta (13nm) Ta_2O_5 (7nm) Pt (30nm)

Figure 3.23: Split conditions for Bi-layer (Ta_2O_5/TaO_x) and Ta-ohmic electrode

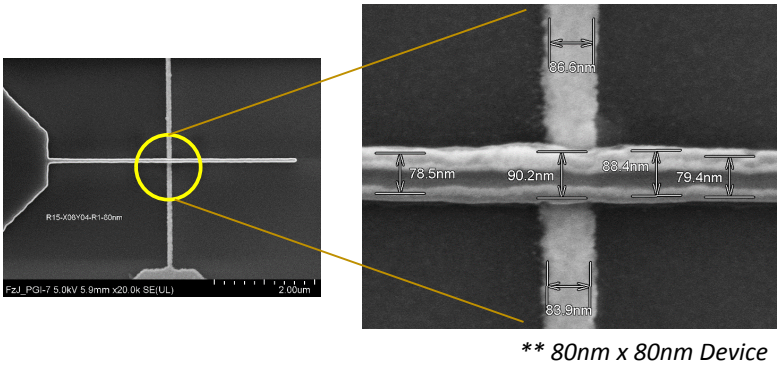


Figure 3.24: SEM image of 80 nm × 80 nm device having the 20 nm-thick TaO_x and and 7 nm-thick Ta_2O_5 layer in Bi-layer structure in $Pt/Ta_2O_5/TaO_x/Ta/Pt$ ReRAM device

gas mixture of argon (77 %) and oxygen (23 %) with an RF power of 236 W at a chamber pressure of 2.3 $\times 10^{-2}$ mbar. And then, TaO_x layer with two splits (20 nm vs. none) is deposited with the gas mixture of argon (97 %) and

oxygen (3 %) under 236 W RF power. After the TaO_x deposition, Ta-ohmic electrode is deposited with two splits (13 nm-thick Ta vs. no Ta) for the fixed 20 nm-thick TaO_x layer and then, 25 nm-thick Pt is deposited by DC sputtering. After the BE, all stacked layers are deposited without breaking the vacuum. In order to create the TE, the e-beam lithography and dry-etch processes are used. The dry-etch continues until the bottom Pt is fully exposed. The detailed split conditions of stacked layers are shown in Fig. 3.23. The patterned nano crossbar structure with 20 nm TaO_x layer is verified by SEM images as shown in Fig. 3.24. There are two purpose for the splits. First, the effect of additional TaO_x is verified with 20 nm-thick TaO_x and second, the effect of Ta ohmic electode is investigated combined with 20 nm-thick TaO_x layer. The device characterization is performed using the Keithley 4200SCS and Agilent B1500 under atmospheric condition at room temperature. During the characterization, active voltage is applied to the TE, keeping the BE is grounded.

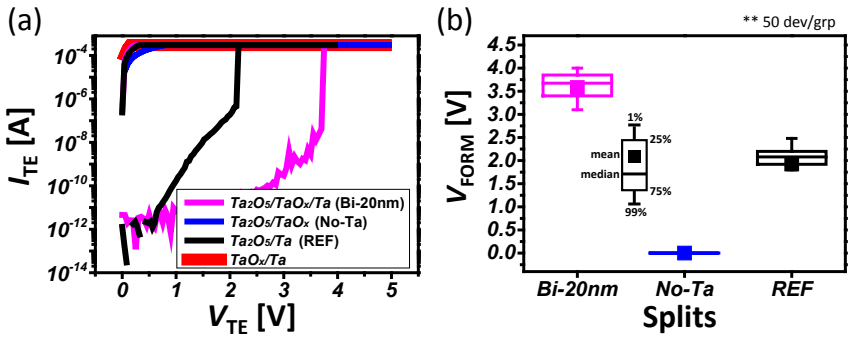


Figure 3.25: (a) Typical forming curves of the Bi-layer Ta_2O_5/TaO_x devices having different switching layer stack, (b) Statistical comparison of the V_{FORM} based on 50 devices per each condition.

3.3.2 $R_{initial}$ and V_{FORM}

The typical forming I-V-curves of different device stacks are compared in Fig. 3.25(a). The Bi-20 nm in magenta ($Ta_2O_5/TaO_x/Ta$) showed higher forming voltage than reference in black (Ta_2O_5/Ta), whereas the No-Ta in

blue (Ta_2O_5/TaO_x) was initially R_{ON}. The layer stack of TaO_x/Ta depicted ohmic behavior implying the TaO_x layer is metallic shown in thick red line. Therefore, in the Bi-20 nm split, resistive switching takes place in Ta_2O_5 layer, not in metallic TaO_x layer. Statistical comparisons of the V_{FORM} based on 50 devices per group are shown in Fig. 3.25(b). Since the No-Ta showed initially R_{ON} state even before the forming, its V_{FORM} is shown as zero. However, the No-Ta experiences severe failures on the 1st RESET and SET as shown in Fig. 3.26(a). Most of devices could not have the proper the 1st RESET and their resistance states were stuck to on-state resistance level (R_{ON} in gray) during negative sweep. Only few devices manage to have the 1st RESET with abrupt current reduction (in blue) and those devices with abrupt hard 1st RESET could not have proper SET as shown in Fig. 3.26(b). This clearly shows that the ohmic Ta electrode is required for Ta_2O_5/TaO_x Bi-layer stacks in order to realize stable RESET-SET switching. We could not continue the electrical characterizations of the devices having the No-Ta electrode due to the switching failures. Further, electrical characterizations are made on two splits, Bi-20 nm and REF samples.

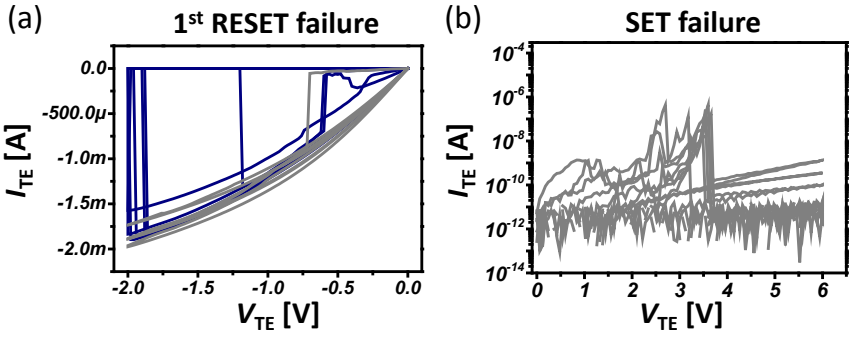


Figure 3.26: Typical switching failures of the ReRAM device having No-Ta electrode during *I-V* sweeps of (a) the 1st RESET in gray and blue, (b) SET in gray.

3.3.3 $V_{RESET-STOP}$ Effects on Device Performance

The $V_{RESET-STOP}$ effect has been investigated from -1.4 V to -2.2 V with 200 mV increment at fixed I_{CC} = 300 μA based on DC measurement. The

resistance states are verified at V_{read}= 0.1 V. The R_{OFF} is expected to increase with higher $V_{\mathrm{RESET-STOP}}$ application. A statistical comparison of R_{OFF} is made based on 10 devices with 30 cycles per each $V_{\mathrm{RESET-STOP}}$ condition as shown in Fig. 3.27(a). There is no significant difference observed between splits over all ranges. The insertion of TaO_x did not affect the R_{OFF} performance over the $V_{\mathrm{RESET-STOP}}$ ranges. Fig. 3.27(b) shows the similar R_{ON} performance between the Bi-20 nm split and REF samples.

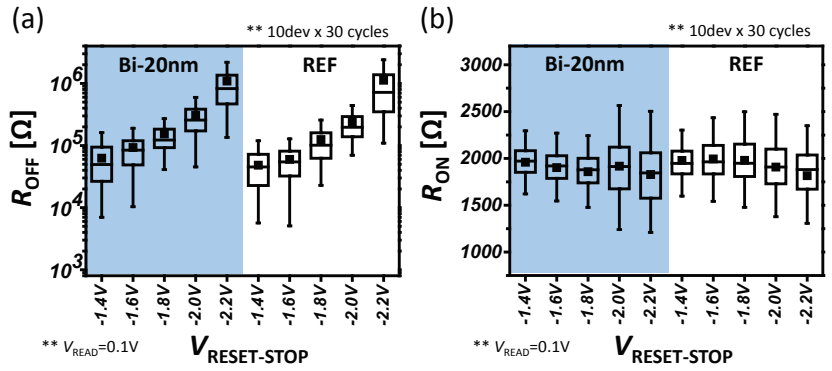


Figure 3.27: Statistical comparison of $V_{\mathrm{RESET-STOP}}$ effect ranging from -1.4 V to -2.2 V for (a) R_{OFF}, (b) R_{ON} .

3.3.4 I_{CC} Effects on Device Performance

The R_{OFF} and the R_{ON} has been statistically analyzed over I_{CC} ranges from 50 μA to 500 μA at fixed $V_{\mathrm{RESET-STOP}}$ = -2.0 V during the DC measurement for the 10 devices with 30 switching cycles for each $V_{\mathrm{RESET-STOP}}$ condition. In general, the R_{OFF} increases as the I_{CC} decreases, but the amount of R_{OFF} increase with I_{OFF} change is much smaller than one with $V_{\mathrm{RESET-STOP}}$ change. The Bi-20 nm sample shows constantly higher R_{OFF} than the REF device over all I_{CC} ranges as shown in Fig. 3.28(a). Especially at low I_{CC} regimes (50 μA, 100 μA), the continuous R_{OFF} increase was observed from the Bi-20 nm, whereas the REF sample showed the saturated R_{OFF} starting from I_{CC} = 100 μA. The Bi-20 nm kept increasing its R_{OFF} from 500 $k\Omega$ at I_{CC} = 100 μA to 600 $k\Omega$ at I_{CC} = 50 μA, while the REF showed the saturated R_{OFF} = 300 $k\Omega$ from I_{CC} = 100 μA. Fig. 3.28(b) shows the R_{ON}

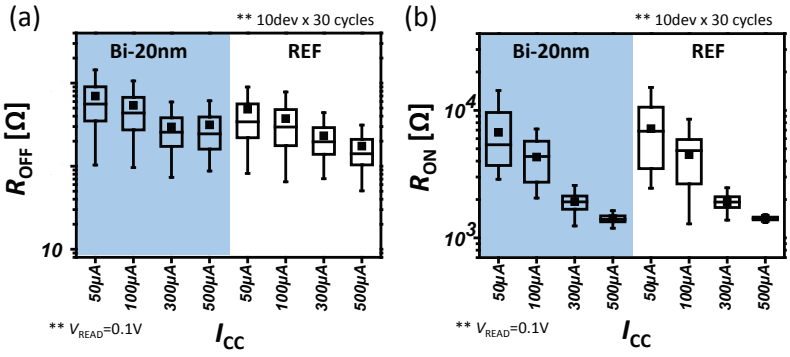


Figure 3.28: Statistical analysis of I_{CC} effect for Bi-layer and single layer Ta_2O_5 ReRAM ranging from 50 μA to 500 μA for (a) R_{OFF}, (b) R_{ON} .

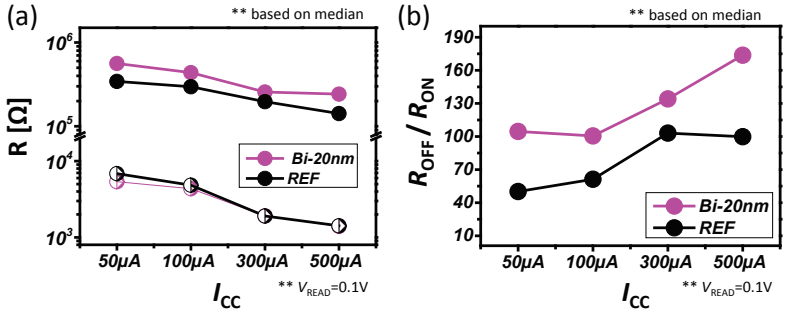


Figure 3.29: (a) Median R_{OFF} and R_{ON} for Bi-layer and single layer Ta_2O_5 ReRAM depending on I_{CC} ranging from 50 μA to 500 μA, (b) R_{OFF} / R_{ON} ratio for bilayer and single layer Ta_2O_5 ReRAM depending on I_{CC} ranging from 50 μA to 500 μA.

comparison and both splits have a similar trend of R_{ON} over the I_{CC} changes. Since the Bi-20 nm sample achieves the increased R_{OFF} with similar R_{ON} compared with the REF sample over all I_{CC} ranges as shown in Fig. 3.29(a), an improved R_{OFF} / R_{ON} ratio is achieved with Bi-20 nm TaO_x device in Fig. 3.29(b). Even at the low I_{CC} (=50 μA), the Bi-20 nm could maintain the R_{OFF} / R_{ON} ratio higher than 100, whereas the REF had less than 60.

Simplified model to explain why the R_{OFF} increases with the TaO_x layer, keeping the R_{ON} constant is depicted in Fig. 3.30 [63]. At initial state, the

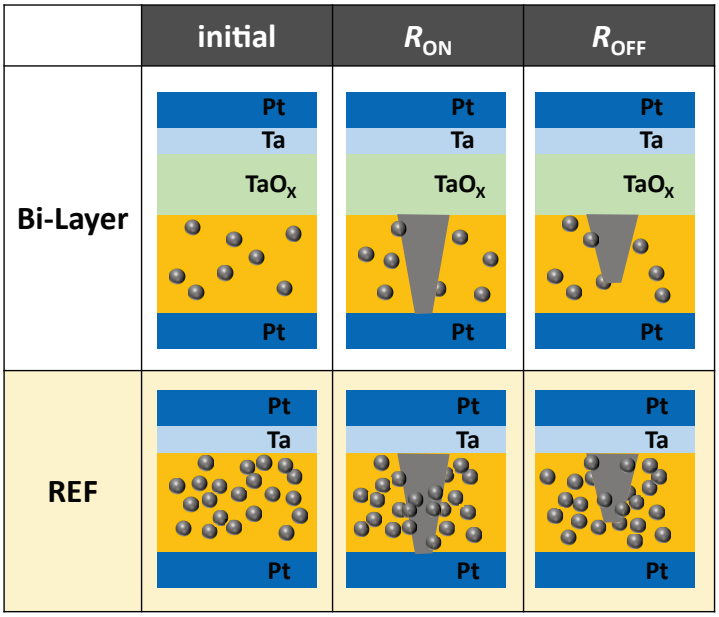


Figure 3.30: Simplified model to explain the R_{OFF} difference between Bi-layer and REF (Single-layer) sample [63].

REF device has more defects (oxygen vacancies) in the Ta_2O_5 switching layer than the Bi-20 nm device. It is due to the Ta ohmic electrode layer making a direct contact to the Ta_2O_5 layer absorbing more oxygen. During switching operations (SET and RESET), the initially generated defects can affect switching characteristics. Since the switching characteristics are governed by the current flowing through the conductive filament during on-state, the R_{ON} of both splits showed the similar I_{CC} dependence in Fig. 3.28(b). However, for the R_{OFF}, the switching characteristics are dominated by the neighboring defects in the Ta_2O_5 layer. It means that the switching characteristics of R_{OFF} are more sensitive to the neighboring defects than the R_{ON}. As operation current is reduced by I_{CC}, the formed filament becomes thinner and weaker so that the influence of neighboring defects will become stronger.

Fig. 3.31 shows the expected distribution of oxygen vacancies under the electric

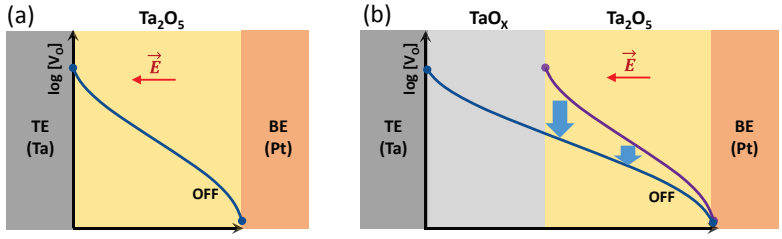


Figure 3.31: Distribution of oxygen vacancies under the electric field (E) during the RESET process. The sketches are based on expected concentration profiles of oxygen vacancy (V_O) during the ReRAM switching cycle (a) from reference device ($Pt/Ta_2O_5/Ta/Pt$), (b) from 20nm-thick Bi-layer device ($Pt/Ta_2O_5/TaO_x/Ta/Pt$)

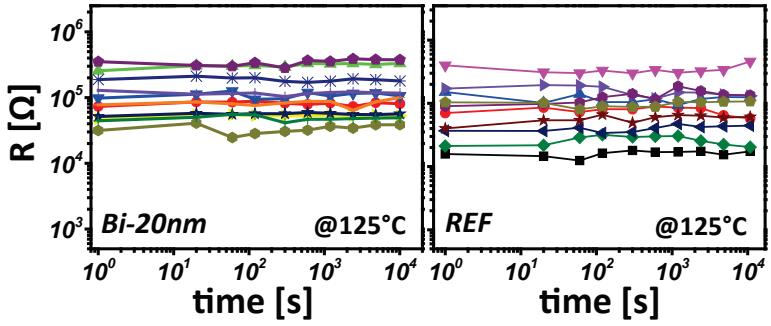


Figure 3.32: Data retention performance for Bi-layer and single layer (REF) Ta_2O_5 ReRAM devices at 125 °C up to 10^4 seconds.

field (E) during the RESET process from both the reference device and 20 nm-thick Bi-layer device. During the RESET process, the oxygen vacancies are depleted near the high work-function Pt electrode (BE) and pile up at the ohmic electrode interface by redistribution of charged oxygen vacancies (V_O) under the electrical field. The depletion at the high work-function Pt electrode results in a space charge region and a high barrier height blocking the electron conduction as shown in Fig. 3.31(a). However, by adding conductive TaO_x layer, the distribution of V_O becomes lowered in the TaO_x switching layer during the R_{OFF} state in Fig. 3.31(b). Therefore, the Bi-20 nm device with

reduced number of defects could maintain the stable and thinner filament resulting in continuously increasing R_{OFF} even at low I_{CC} levels.

3.3.5 Retention Comparison at 125°C

A retention measurement has been made at 125 °C based on $9 \sim 11$ devices for each split as shown in Fig. 3.32. Good retention was observed from all splits up to 10^4 seconds. There was no difference observed in retention performance with TaO_x Bi-layer devices.

3.3.6 Summary of this section

In summary, the effect of additional TaO_x layer insertion in the conventional ReRAM stack has been analyzed for 80 nm × 80 nm device size. The V_{FORM} increased up to 3.6 V from 2.0 V with inserted TaO_x layer. However, the split without Ta-ohmic electrode didn't show any increased V_{FORM} even with additional 20 nm-thick TaO_x layer and it has catastrophic switching failures during the 1st RESET and SET processes. No stable switching was observed from the devices without the Ta ohmic electrode with 20 nm-thick TaO_x. Both Bi-20 nm and REF devices showed comparable performance for the R_{OFF} and R_{ON} with respective to the $V_{RESET-STOP}$ effect ranging from -1.4 V to -2.2 V. However, in the I_{CC} effect, the Bi-20 nm device achieved continuously increasing R_{OFF} even at low I_{CC} regime (50 μA), while the REF device showed an early saturation of R_{OFF} starting from I_{CC} = 100 μA. For the R_{ON}, both had a comparable performance over all I_{CC} ranges from 50 μA to 500 μA. Therefore, an improved R_{OFF} / R_{ON} ratio was achieved with the Bi-20 nm TaO_x device and its ratio was maintained over 100 even at low I_{CC} = 50 μA, whereas the REF device showed less than 60 of R_{OFF} / R_{ON} ratio under the same condition. A good retention was obtained from both splits at 125 °C up to 10^4 seconds. There was no performance degradation in retention with the additional TaO_x layer. It seems that Bi-20 nm TaO_x layer is a good option to improve the memory window (R_{OFF} / R_{ON}) especially at low current condition (50 μA).

3.4 Conclusion of this chapter

In this chapter, impact of the process parameters of the Ta_2O_5 switching layer on the electrical performance of the ReRAM has been studied including the effects of RF sputtering power, the thickness effect of Ta_2O_5 switching layer, and the Bi-layer (Ta_2O_5/TaO_x) structure. For the effect of RF sputtering power, the RF40% (236W) condition shows the best R_{OFF}/R_{ON} performance with stable endurance up to 10^6 cycles (@1.0 μs) and good retention at 125 °C for 10^4 seconds. For the thickness effect of Ta_2O_5 switching layer, the good R_{OFF}/R_{ON} ratio was achieved from the 7 nm-thick Ta_2O_5 with relatively lower V_{FORM} (1.8 V) compared with the 13 nm-thick Ta_2O_5 (3.0 V). The improved R_{OFF} performance was observed with 7.0 nm-thick Ta_2O_5/ 20 nm-thick TaO_x Bi-layer structure at low I_{CC} level (50 μA) due to a better control of defects in the Ta_2O_5 switching layer.

Chapter 4

Ohmic electrode for Ta_2O_5 ReRAM

In this chapter, effects of ohmic electrode (Ta, W, Hf, Ti) and thickness variation of Ta-ohmic electrode in Ta_2O_5 ReRAM will be discussed in detail. Defect formation energy for each ohmic electrode in Ta_2O_5 will be discussed. Difference of defect formation energy can affect the switching parameters such V_{FORM}, V_{SET}, V_{RESET} and the switching speed of RESET and SET process.

4.1 Role of ohmic electrodes (Ta, W, Hf, Ti)

Metal-oxide based bipolar ReRAM devices consist of an insulating switching layer stacked between two asymmetric metal electrodes: one low work function (WF) ohmic electrode (OE) (which is also easily oxidizable), such as W, Ti, Hf, or Ta, and a high WF (inert) metal electrode, such as Pt. The resistive switching mechanism relies on the motion of mobile ionic defects under the applied electrical field. While motion of metal cations has been evidenced and their role cannot be excluded [64], the most widely accepted model is based on (double) positively charged oxygen vacancy defects Vö. These Vo's are introduced in the switching layer during the initial forming step, which results in the formation of a filamentary region with a high concentration of oxygen vacancies between these two electrodes. The main process of Vo defect generation during forming is thought to be extrinsic

defect generation due to oxygen excorporation (Equation 1, following the Kröger-Vink notation [22]):

$$O_O^x \longleftrightarrow Vö + 2e' + \tfrac{1}{2}O_2(g) \qquad (1) \qquad [65]$$

When the electrons are localized at the metal cations, (1) becomes:

$$O_O^x + 2M_M^x \longleftrightarrow Vö + 2M_M' + \tfrac{1}{2}O_2(g) \qquad (2)$$

The presence of the Vö, by a local redox reaction, changes the valence of the neighbouring metal cations in the metal oxide film (note that the Kröger-Vink notation only lists relative charges, with the metal here changing from neutral to negative. In absolute charge notation, the cation may go e.g. from charge state 5+ to 4+), hence, it is termed as valence change memory or VCM [30, 66].
Besides the forming process (Eq. 1), the V_O's are also introduced during processing by oxygen exchange between the oxide layer and the OE layer, i.e. oxygen is extracted from the metal oxide (MO) and oxidizes the OE metal (=M*) to the formation of M*-oxide, see Equation 3 (for notation, $M_{M(MO)}$ stands for an M atom on a M-metal site in the MO metal-oxide, while $M^*_{M^*(M^*)}$ stands for an M* atom on a M*-metal site in the M* metal etc.). Here, it is assumed that the M* oxidizes to valence +4, i.e. forms a new phase M^*O_2:

$$2O^x_{O(MO)} + 4M^x_{M(MO)} + M^{*x}_{M^*(M^*)} \longleftrightarrow$$

$$2Vö_{(MO)} + 4M'_{M(MO)} + M^*O_2 + V''''_{M^*(M^*)} + 4h^\bullet \qquad (3),$$

In case, the cap layer is already partly oxidized at the interface (to $M^*O_{2-\delta}$), as e.g. during device operation, the oxygen exchange corresponds to a reverse V_O exchange, see equation (4):

$$O^x_{O(MO)} + 2M^x_{M(MO)} + Vö_{(M^*O)} + 2M^{*\prime}_{M^*(M^*O)} \longleftrightarrow$$

$$\mathrm{V\ddot{o}_{(MO)}} + 2\mathrm{M'_{M(MO)}} + 2\mathrm{M^{*x}_{M^*(M^*O)}} + \mathrm{O^{x}_{O(M^*O)}} \qquad (4)$$

The oxygen exchange with the OE during deposition introduces a high concentration of the V_O located in the oxide film near the OE electrode (so called defect 'reservoir'). The resultant introduction of V_O in the oxide film lowers theR_{initial} and the V_{FORM} of the device. For a $Pt/SrTiO_3/Ti$ VCM cell, it is demonstrated that the V_{FORM} depends on $SrTiO_3$/Ti layer thickness ratio [67]. The $SrTiO_3$ layer is further chemically reduced by a thicker Ti layer, which finally leads to an electroforming-free device. Most switching models, however, presume that during the RESET/SET switching process, only a redistribution of the V_O within the oxide layer takes place keeping the total amount of the V_O's constant, i.e. no further oxygen exchange with the OE takes place during the switching process.

As mobile donors, the Vö can influence the overall resistance of the ReRAM cell in two ways. First, the local conductivity of the metal-oxide film increases with increasing V_O concentration [V_O] [68–70]. Second, the electrostatic barrier heights at the high WF metal/oxide interface are modulated by the local V_O concentration due to the Schottky effect [30], [71, 72]. During the RESET/SET switching (applying positive/negative bias to the inert electrode), the V_O's move away/towards the interface with the high WF electrode (in accordance with disrupting/restoring the filament). It is assumed that the OE forms an Ohmic contact with the metal-oxide layer, whereas in absence of a high concentration of Vö (disrupted filament) the high WF metal forms high Schottky barrier that dominates the overall resistance in the HRS. During the SET operation, the V_O's move to the high WF, where the increased V_O concentration lowers the Schottky barrier and the device switches to the LRS. Hence, interfacial conduction strongly affects the resistive values in the different states of the oxide ReRAM [73], [74]. In this study, we analyzed Ta_2O_5-based ReRAM devices using different OE materials (W, Ta, Ti and Hf). Among various oxide switching materials, the Ta_2O_5-based ReRAMs exhibit excellent performance in switching speed [2], endurance [1], [75], retention [76] and low power [77], [78], [79]. The OE materials are chosen for the defect formation energy of oxygen vacancy (E_{VO}) with respect to the Ta_2O_5 layer. For the Hf and the Ti, this E_{VO} is

negative, whereas it is positive for the Ta and the W. In this experiment, we have observed that the OE not only affects the V_{FORM} but also the RESET process. The devices with the Hf and the Ti electrode show an early RESET failure, whereas the devices with the Ta and the W OE show highly reliable switching behaviour. The Pt/Ta_2O_5/W ReRAM devices show faster RESET process than the Pt/Ta_2O_5/Ta, which leads to higher R_{OFF}/R_{ON} ratio under the same bias conditions. These observations indicate that oxygen interchange with the OE plays an important role during the resistive switching process. Based on these findings, an advanced resistive switching model, where the oxygen exchange reaction at the OE interface plays a vital role in determining of the resistance states, is presented.

4.1.1 Fabrication

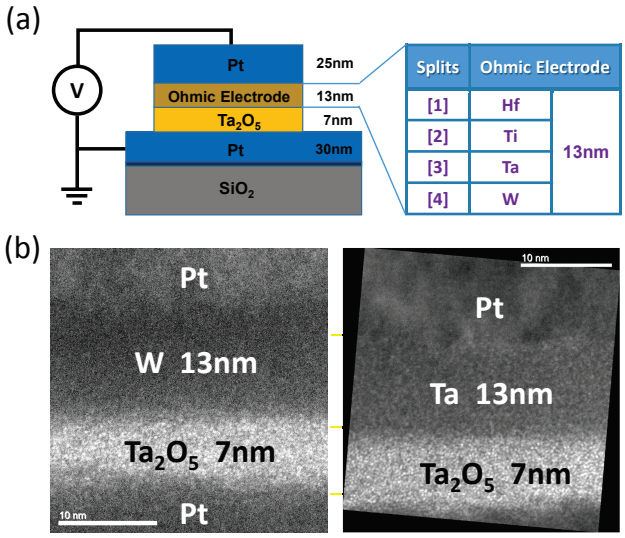


Figure 4.1: (a) A schematic cross-sectional diagram with experimental split conditions with different OE materials (W, Ta, Ti and Hf). (b) TEM images of W-electrode and Ta-electrode devices confirming target thickness of the corresponding layers.

In this study, $2 \times 2\mu m^2$ size device with 30 nm-thick BE (Pt), 7 nm-thick Ta_2O_5

, 4 different types of OE with 13 nm-thick layer and 25 nm-thick Pt (TE) is used and these stacks lead to the Pt(BE)/Ta_2O_5/OE(OE)/Pt ReRAM device sketched in 4.1(a). The cross sectional TEM images of the ReRAM devices with the Ta-OE and the W-OE layer confirm the thicknesses of corresponding device stacks in Fig. 4.1(b). The device characterization is performed using the Keithley 4200SCS under atmospheric conditions at room temperature.

4.1.2 V_O defect formation energies and V_{FORM}

The driving force of the interfacial chemical reaction (see eq. 3) is related to the energy of oxygen vacancy defect formation (E_{VO}) in the metal oxide at the OE interface [80],[81],[82]. Recently, Guo et al. calculated the E_{VO} in different metal oxides, and for different metal cap layers [83],[84]. In these defect energy calculations, they made a difference between O-rich and O-poor conditions. The O-rich conditions actually apply to the metal oxide exposed to an oxygen ambient (with a certain pO_2). The O-poor condition corresponds to the metal-oxide in contact with an OE layer of the same metal as the oxide host metal (M*=M).

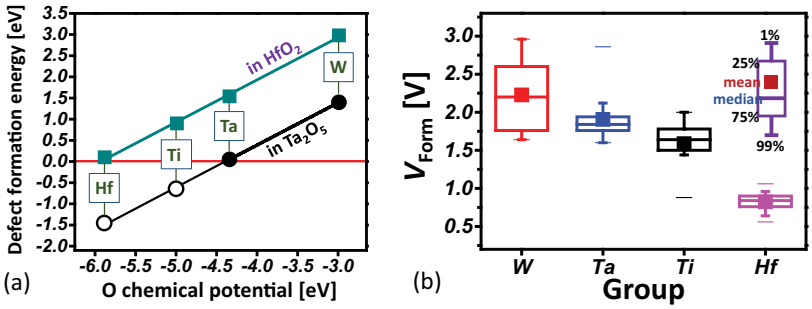


Figure 4.2: (a) Interfacial defect formation energy for oxygen vacancy defects E_{VO} in Ta_2O_5 and HfO_2 as function of the oxygen chemical potential. This chemical potential is determined by the OE present as indicated here for Ta, W, Ti and Hf. (b) V_{FORM} of the Ta_2O_5 ReRAM device for each ohmic metal electrode (W, Ta, Ti and Hf)

In that case, the energy required for removing the O from the metal oxide is nearly completely compensated by the (negative) free energy of oxidation

of the metal cap, and the resultant defect formation energy is approximately 0. Fig. 4.2(a) shows the calculated E_{VO} values in HfO_2 and Ta_2O_5 in contact with different OE (based on Fig. 5 of [85], where the energy values for the Hf and the Ti with respect to the Ta_2O_5 have been extrapolated based on available data in the reference [83],[84]. Based on these calculations, the E_{VO} for the Ta_2O_5 layer is estimated to be 1.4 eV for W-electrode, 0.1 eV for Ta-electrode. -0.6 eV for Ti-electrode and -1.5 eV for Hf-electrode. In general, as depicted in Fig. 4.2(a), the E_{VO} increases with the stability (i.e. free energy of oxide formation) of the host oxide (cf. parallel shift of defect energy for Ta_2O_5 and HfO_2), and decreases according to the stability of the metal cap oxide (horizontal shift according to OE metal used. The O chemical potential corresponds to the equilibrium oxygen partial pressure of the M*/M*O couple, reflecting the relative M*O stability). It can be observed that a cap metal that has a more stable oxide than the oxide host metal (e.g., Ta_2O_5 capped with Hf and Ti) results in a negative regime. A positive E_{VO} is required for stable switching [85], as the negative E_{VO} would result in a continuous increase of the V_O in the switching film, resulting in a non-switchable, conducting film. The influence of the OE on the V_{FORM} was investigated by measuring 50 devices for each device stack. The forming process was performed by a positive DC voltage sweep (+3.0 V) applied to the OE with I_{CC} = 1.0 mA. The forming statistics of the four different device stacks are given in Fig. 4.2(b). A clear dependence of the V_{FORM} on the OE material is observed. The lowest V_{FORM} is observed for the Hf-electrode devices (0.84 V in median), followed by the Ti-electrode devices (V_{FORM} = 1.64 V in median). The W-electrode devices show the highest V_{FORM} (2.21 V in median) followed by the Ta-electrode ones (V_{FORM} = 1.84 V in median). The V_{FORM} trend as shown in Fig. 4.2(b) clearly correspond with the oxygen vacancy defect formation energies at the respective OE/Ta_2O_5 interfaces as shown in Fig. 4.2(a).

4.1.3 V_O defect formation energies and early RESET failures

During the switching, the ReRAM devices with the Ti- and the Hf-OE show a failure in the RESET process within the first 20 cycles.

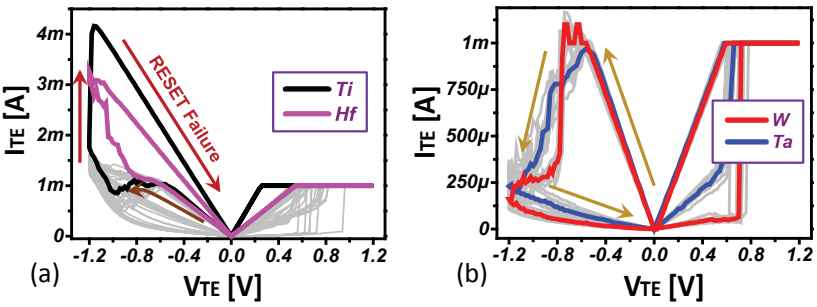


Figure 4.3: At the given I_{CC} of 1.0 mA, the switching curves of Ta_2O_5 ReRAM with different OE and the maximum RESET voltage of -1.2 V are examined. (a) Early RESET failures from Hf and Ti electrodes, (b) Stable switching cycles of SET and RESET from Ta and W electrodes.

This early RESET failure is shown in Fig. 4.3(a). The gray lines show the switching behavior of the Ta_2O_5 ReRAM with the Ti- and the Hf-OE before failure. After the RESET failure the ReRAM devices exhibit ohmic *I-V* behavior and are stuck in the LRS regime. In contrast, stable switching operation has been observed with the W- and the Ta-OE under the same biasing conditions as shown in Fig. 4.3(b). Average switching curves are shown in red for the W-OE and in blue for the Ta-OE devices. The occurrence of RESET failure or stable switching clearly correlates with (the sign of) E_{VO} at the OE/Ta_2O_5 interface, suggesting that oxygen exchange takes place at this OE/Ta_2O_5 interfaces during the switching process. This will be discussed with more details in the latter part of this study.

4.1.4 RESET process ($V_{RESET-STOP}$ vs. R_{OFF})

4.1.4.1 RESET performance for DC analysis

Since the Hf- and Ti-based devices show the early RESET failure, only the W- and Ta-OE based Ta_2O_5 ReRAM devices are further investigated and compared under identical bias conditions.

Fig. 4.4(a) shows a typical *I-V* characteristics of Ta_2O_5 device at I_{CC} of 1.0 mA exhibiting the gradual RESET transition for two different RESET

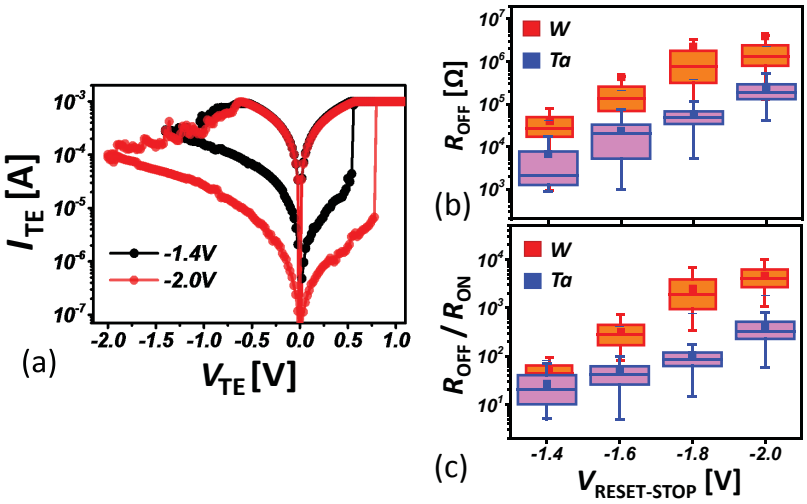


Figure 4.4: (a) Typical *I-V* characteristics of the Ta_2O_5 ReRAM device for two different $V_{\mathrm{RESET-STOP}}$ conditions (-1.4 V, -2.0 V), (b) R_{OFF} change depending on $V_{\mathrm{RESET-STOP}}$ increment for two OE materials (W and Ta), (c) Comparison of $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio as a function of the $V_{\mathrm{RESET-STOP}}$ increment for the Ta- and the W-OE ReRAM device.

stop voltages ($V_{\mathrm{RESET-STOP}}$ = -1.4 V & -2.0 V). The higher RESET voltage toggles the device into a higher R_{OFF} value [50],[51],[52], which subsequently results in a higher SET voltage. This phenomenon is attributed to the fact that under the electric field during RESET, the V_O's drift away from the high WF metal electrode resulting in an increase of the effective Schottky barrier height. This drift, however, builds up a concentration gradient giving rise to an opposite diffusion flow of V_O. Hence, the V_O distribution approaches an equilibrium (balance) over time [74]. This equilibrium profile is frozen, when the voltage is switched off and depends on the maximum applied RESET voltage. When the RESET voltage increases, the Ta_2O_5 close to the high WF metal electrode becomes more depleted from V_O's and, thus, the resulting R_{OFF} value becomes higher [44],[45],[46],[47]. The effects of the $V_{\mathrm{RESET-STOP}}$ on the R_{OFF} for the W- and the Ta-OE based Ta_2O_5 devices are investigated in the range of -1.4 V to -2.0 V with -0.2 V increment

under identical SET I_{CC} of 1.0 mA using quasi-static voltage sweeps. The W-OE devices consistently yield higher R_{OFF} than the Ta-OE devices, shown in Fig. 4.4(b). For the $V_{RESET-STOP}$ = -1.4 V, the R_{OFF} value of the Ta_2O_5 ReRAM with the W-OE is 23 $k\Omega$ in comparison with 2.0 $k\Omega$ for the Ta-OE devices. At the $V_{RESET-STOP}$ = -2.0 V, the R_{OFF} value is further increased to 1.2 $M\Omega$ and 200 $k\Omega$ for the W- and the Ta-OE device, respectively. Due to the high R_{OFF} for the W-OE device with similar R_{ON}, the R_{OFF}/R_{ON} ratio of the W-OE based Ta_2O_5 device is more than 1,000 at $V_{RESET-STOP}$ = -1.8 V. This is about 12 times higher than the one for the Ta-OE device as shown in Fig. 4.4(c).

4.1.4.2 RESET performance for AC analysis

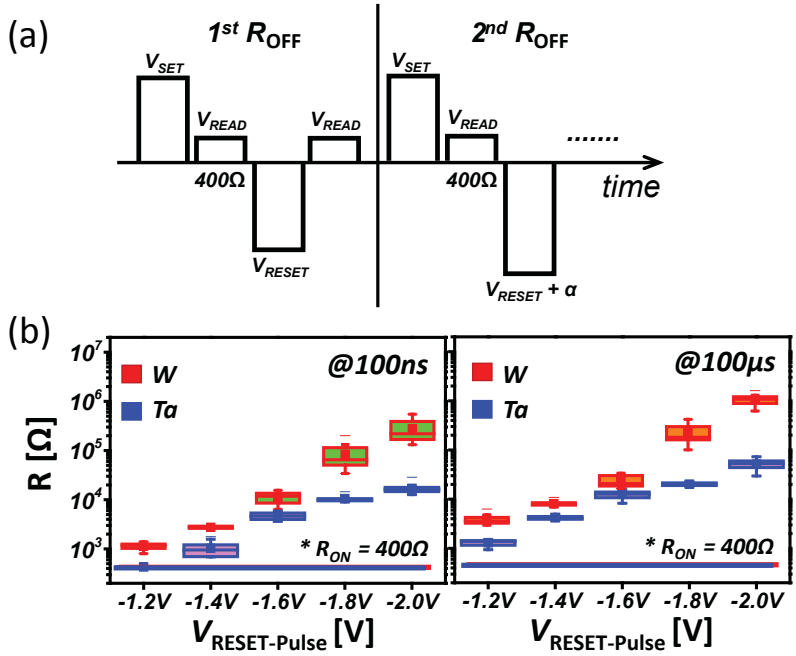


Figure 4.5: (a) Schematics of pulse application during the AC measurement, (b) Comparison of the RESET kinetics between the W- and Ta-OE with 100 ns and 100 μs pulse width showing resistance change over applied RESET voltage.

The AC RESET behavior of the Ta- and W-OE based Ta_2O_5 devices is further investigated using voltage pulses of 100 ns and 100 μs length. The measurement schematics of AC pulse sequences are shown in Fig. 4.5(a). The R_{ON} of all devices is always kept constant to about 400 Ω, which is verified by a 0.1 V read pulse with 1.0 μs width before the RESET pulse application. Fig. 4.5(b) shows the R_{OFF} change for different RESET voltages ranging from -1.2 V to -2.0 V at both 100 ns and 100 μs pulse widths. For both, the W- and Ta-OE devices, the R_{OFF} state varies with the pulse voltage amplitude. For both pulse widths, the rate of resistance change over voltage amplitude is steeper for the W-OE than that of the Ta-OE device. For the 100 ns pulse width, at the $V_{RESET-Pulse}$ = -2.0 V, the R_{OFF} of the W-OE based Ta_2O_5 device was approximately 15 times (221 $k\Omega$ for W vs. 16 $k\Omega$ for Ta) higher than that of Ta-OE device. For the longer RESET pulse (100 μs) at $V_{RESET-Pulse}$ = -2.0 V, the resistance of the W-OE device was about 20 times (1.1 $M\Omega$ for W vs. 53 $k\Omega$ for Ta) higher than that of Ta-OE device. As expected, longer pulses (100 μs) result in a higher resistance change than the short pulses (100 ns) for both device stacks at given voltage amplitude [86]. The RESET pulse experiment is consistent with the DC-RESET results, where the W-OE shows higher R_{OFF} at any given RESET voltage. The results from both AC and DC measurements thus confirm that the OE material affects the RESET switching speed and equilibrium in the device, which verifies the presumption that oxygen exchange at the OE/metal-oxide interface actively contributes to the switching process.

4.1.5 SET performance

Next, the SET kinetics of the Ta_2O_5 device for both OE have been investigated with varying amplitudes $V_{SET-Pulse}$, as shown in Fig. 4.6(a). The transient SET pulse (in gray) and its corresponding transient SET current ($I_{SET-Pulse}$) in blue is measured for $V_{SET-Pulse}$ = 1.2 V and 1.45 V with Ta-OE device. Prior to the SET pulse application, the R_{OFF} value for both conditions was kept between 150 $k\Omega$, to 200 $k\Omega$.

In the beginning of the $V_{SET-Pulse}$, the corresponding $I_{SET-Pulse}$ is relatively low. However, after some time the current level shows a sudden increase. The point in time at which this abrupt increase in the current is observed, is defined

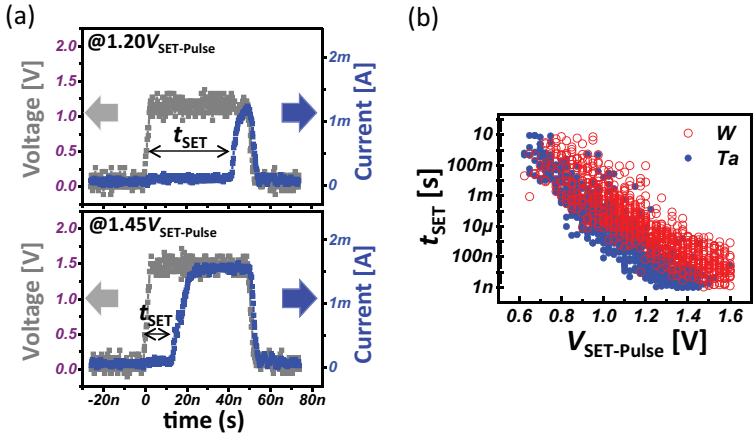


Figure 4.6: (a) Examples of the measured transient current (in blue) and the applied SET pulse (in gray) of $V_{\mathrm{SET}} = 1.3\,\mathrm{V}$ and $1.75\,\mathrm{V}$. The abrupt increase of current is identified as the SET process. The SET time (t_{SET}) is obtained depending on the amplitude of SET pulse. (b) A correlation between the t_{SET} and the SET Pulse amplitude for both W- (in red) and Ta-OE (in blue) illustrating the ultra-high nonlinearity of the SET kinetics.

as SET switching time, t_{SET}. For the lower $V_{\mathrm{SET-Pulse}}$ (1.2 V), a longer t_{SET} (45 ns) is required to switch the device to the LRS whereas a shorter t_{SET} (15 ns) is observed at the higher $V_{\mathrm{SET-Pulse}}$ (1.45 V). This measurement has been carried out over a wide $V_{\mathrm{SET-Pulse}}$ range spanning from 0.6 V to 1.6 V with 25 mV increment for each OE, shown in Fig. 4.6(b). A clear correlation between $V_{\mathrm{SET-Pulse}}$ and t_{SET} is observed for both devices. As the $V_{\mathrm{SET-Pulse}}$ increases, the t_{SET} becomes shorter as reported for other devices [87],[88],[89]. For the complete voltage range the Ta-OE devices show the shorter t_{SET} i.e. faster SET process. So, the transition from R_{OFF} to R_{ON} for the SET process appears faster with Ta-OE, which is the exactly opposite to the RESET process of the device (that is faster for the W-OE). This outcome further supports the assumption that the OE plays an active role during the switching process.

4.1.6 Theoretical explanation

The experimental results indicate that the OE plays an active role during the switching process in the VCM ReRAM devices. In analogy to the forming

process, an oxygen exchange reaction occurs during switching at the OE/metal-oxide interfaces. Thus, the former assumptions of the switching process, in which the amount of V_O in the filament stays constant needs to be modified [90]. In addition to the movement of the V_O's in the filament, an oxygen exchange takes place at the OE/oxide interface. Hence, the total amount of the V_O's within the filament changes during the switching process. This modified switching model is illustrated in Fig. 4.7.

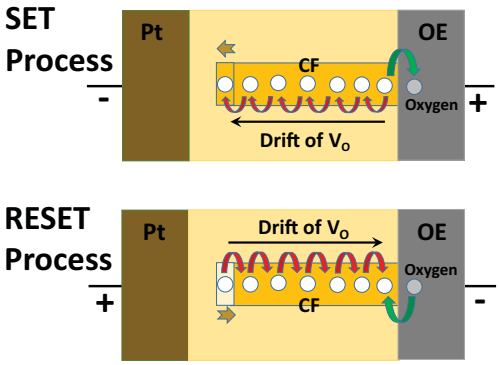


Figure 4.7: Illustration showing the movements of oxygen vacancies and oxygen ions during the SET and the RESET process

During the SET transition, the oxygen vacancies drift towards the high WF metal electrode and decrease the Schottky barrier height. This is corresponding to oxygen moving towards the OE interface, where due to the oxygen exchange reaction oxygen is extracted from the metal-oxide and incorporated in the OE. By this, the electrode may be locally oxidized forming a sub-oxide (which would be still be very conductive), while the total amount of the V_O in the metal-oxide increases (cf. equation 3, proceeding to the left). During the RESET process, the opposite movement of the V_O's result in their depletion at the high WF metal electrode and accumulation at the OE electrode. Due to the oxygen exchange reaction at the electrode, oxygen is incorporated in the oxide layer lowering the amount of vacancies at the OE interface. Thus, the total amount of the V_O's decreases in the oxide layer. The rate of this oxygen exchange reaction depends on the E_{VO}. A faster extraction of the oxygen ion from the switching oxide layer (SET) is achieved for a lower (positive) E_{VO}

values. In contrast, the re-incorporation of oxygen ions into the switching oxide layer (RESET) is faster for higher (positive) E_{VO}. Thus, a higher E_{VO} is beneficial for faster RESET operation. The experimental observations can now be explained in the context of the modified model.
The early RESET failure occurs in the Ti- and Hf-OE devices. For those two electrodes, E_{VO} is negative, i.e. there is a continuous thermodynamic drive for V_O formation. Kinetic barriers to this may be lowered due to Joule heating during the switching process, with oxygen extraction from the Ta_2O_5 strongly enhanced during the SET process while O re-incorporation during RESET process is strongly reduced. Hence, the total amount of the oxygen vacancies is increasing from cycle to cycle, reducing the film resistivity. Eventually, the current and the dissipated power during the RESET process is so high that oxygen may get excorporated at the opposite Pt electrode (i.e., we get a spurious SET at this Pt electrode), resulting in an overall RESET failure. For the Ta- and W-OE devices, the oxygen exchange during the SET and the RESET process is better balanced and thus stable switching is obtained. The different speed of the RESET process for these devices can also be explained with the oxygen exchange model. Fig. 4.8 explains the change in the profile of the oxygen vacancy during the RESET process [91].

During the RESET process, the oxygen vacancies are depleted near the high WF Pt electrode and pile up at the OE interface by redistribution of charged oxygen vacancies (Vö) under the electric field (E), as shown in Fig. 4.8(a). The depletion at the high WF Pt electrode results in a space charge region and a high barrier height blocking the electron conduction. The diffusion (D) of the V_O will counteract the concentration gradient build-up by the drift, resulting in equilibrium in Fig. 4.8(b). By that, the V_O accumulation at the OE will be reduced. However, these amount of the V_O will diffuse towards the high WF Pt electrode, decreasing the depletion and increasing the current in the R_{OFF}. The oxygen (O) exchange with the OE will reduce the high V_O concentration lowering the back-diffusion force (D), shown in Fig. 4.8(c). As the result, a lowered concentration of the V_O at the high WF Pt interface can be maintained and the leakage current at R_{OFF} remains low. The W-OE can release oxygen (O) back easier than Ta-OE due to its higher energy for defect formation. This is why the W-OE can achieve lower leakage current (higher

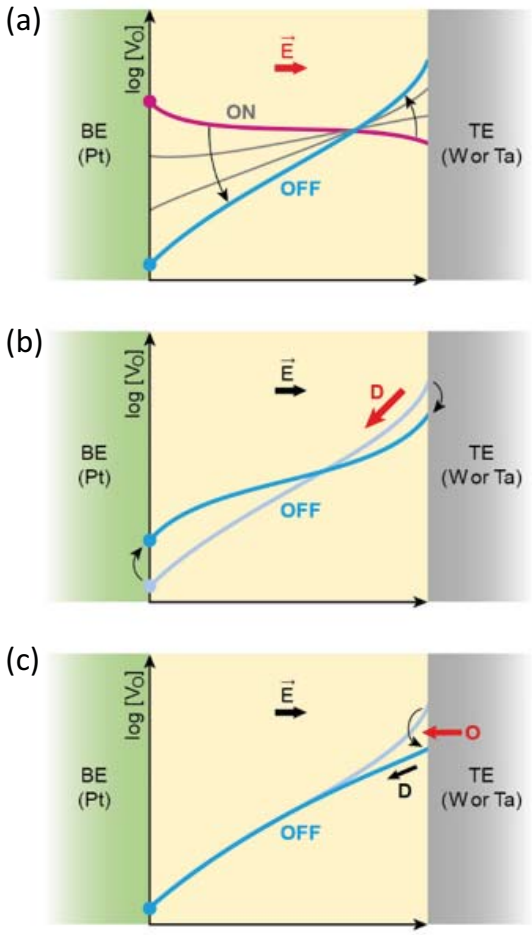


Figure 4.8: (a) Redistribution of oxygen vacancies under the electric field (E) during the RESET process. Sketch based on simulations of V_O concentration profiles during ReRAM switching (b) Diffusion of oxygen vacancies counteracting the concentration gradient by the drift process. (c) Oxygen exchange with the OE resulting in lower concentration of oxygen vacancy at the Pt interface.

R_{OFF}) with the same V_{RESET} application. In contrast, for the switching speed of the SET process, the Ta-OE is faster than the W-OE. This is attributed to the speed of the oxygen exchange reaction at the interface. The extraction of the oxygen ions at the OE electrode is faster for the Ta-OE because it has the lower E_{VO}.

4.1.7 Endurance and retention

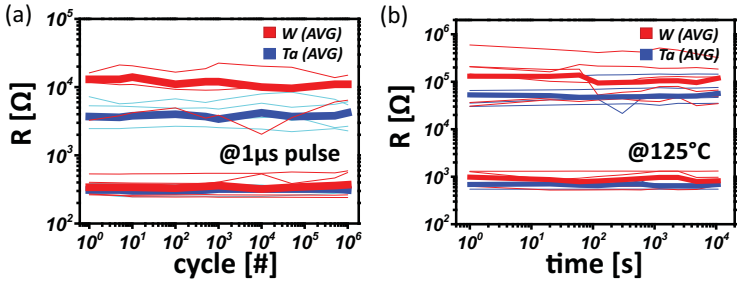


Figure 4.9: (a) Endurance for both electrodes up to 10^6 cycles (@1μs pulse width). (b) The data retention time for both electrodes at 125°C up to 10^4 seconds.

Successful endurance up to 10^6 cycles from 5 devices of each OE (W, Ta) has been achieved as shown in Fig. 4.9(a) and the applied reset condition is -1.6 V with 1.0 μs pulse width. The thin line is corresponding to each individual endurance and the bold line (blue, red) represents the average value of thin lines for both R_{OFF} and R_{ON} . The resistance state is verified with 0.1 V pulse. Both electrodes (W, Ta) shows the good retention performance up to 10^4 seconds at 125°C in Fig. 4.9(b).

4.1.8 3-Bit Multi-Level-Cell with W-OE

A higher memory window (R_{OFF} /R_{ON} ratio) at given reset voltage can be achieved with W-OE, which facilitates the realization of Multi-Level-Cell (MLC) in this ReRAM device. Fig. 4.10(a) shows the cumulative distribution of the 3-bit MLC operation with 100 ns single pulse operation for 100 cycles. Prior to the reset pulse, the starting resistance level always maintains at the $R_{\mathrm{ON}} \sim 400\,\Omega$ for all resistance states. Each of high resistance states is achieved with the reset pulse and then the resistance state returns to the R_{ON} state with the set pulse. The next higher resistance state is achieved with the increased amplitude of the reset pulse. The states distribution shows slight overlap, which can further be improved by using state-correction algorithms. The excellent data retention time of corresponding 8-states up to 10^4 seconds at 125°C, shown in Fig. 4.10(b) proves the feasibility of 3-bit

MLC in the Ta_2O_5/W ReRAM devices.

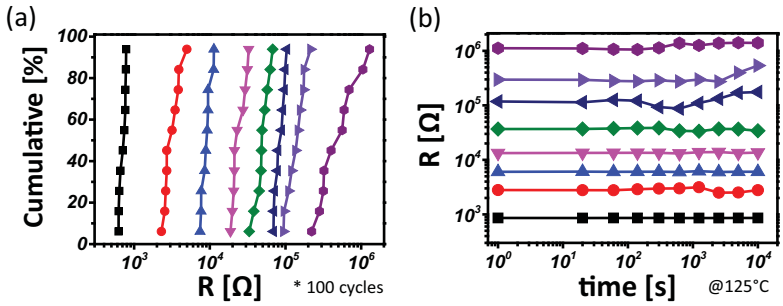


Figure 4.10: W-electrode based Ta_2O_5 ReRAM device for (a) 3-bit MLC operation with 100 ns pulse width. (b) Data retention time of the corresponding 8-states at 125°C up to 10^4 seconds.

4.1.9 Summary of this section

In this study, Ta_2O_5-based ReRAM devices have been studied with W-, Ta-, Ti- and Hf-OEs. Based on our experimental observations, a modified switching model is proposed. In contrast to the previous models, the experimental results show that oxygen exchange reactions with the OE not only occur during the electroforming process, but also during each SET and RESET process. The relevant design property presumably is the interfacial oxygen defect formation energy E_{VO} at the OE/oxide interface. The Ti- and Hf-OE devices suffer from an early RESET failure due to an accumulation of the V_O's during the switching cycles. This is explained by their negative E_{VO}, which favors the reduction of the switching oxide layer. In contrast, the positive E_{VO} for the Ta- and W-OE leads to highly stable switching process in the Ta_2O_5 ReRAM. The W-OE devices show an increased R_{OFF} compared with the Ta-electrode under identical RESET conditions. This difference of the R_{OFF} value can also be explained by the oxygen exchange reaction. The E_{VO} of Ta_2O_5/W favors incorporation of the oxygen ions into the switching oxide layer decreasing the total amount of the V_O inside the switching oxide, which will lower the current in high resistance state under the given biasing conditions of the RESET process. On the opposite side, the lower E_{VO} for Ta-OE results in faster SET processes than its counterpart W-OE. These

observations indicate that oxygen interchange with the OE plays an important role during the resistive switching, leading to extended modified switching model. The proposed model can explain the experimental dependence of the resistive switching properties as RESET depth and SET speed on the used material stack, and so will be beneficial for the future material's design of optimized ReRAM devices. Both W- and Ta-OEs show good endurance up to 10^6 cycles and retention time of 10^4 seconds at 125°C based on 2-states.
The $Pt/Ta_2O_5/W/Pt$ ReRAM devices shows a higher R_{OFF} value (at given $V_{RESET-STOP}$) than $Pt/Ta_2O_5/Ta/Pt$ devices. This higher R_{OFF}/R_{ON} window with the W electrode device helps to achieve the MLC operation. 3-bit (8 states) MLC operation has been successfully demonstrated in the $Pt/Ta_2O_5/W/Pt$ ReRAM device within $\pm 2.0\,V$ operation window, and all 8-states show an excellent retention time of 10^4 seconds at 125°C without state overlapping.

4.2 Role of Ta-OE thickness

In order to achieve bipolar resistive switching in ReRAM, it is required to have asymmetrical structures especially between TE and BE. The cell asymmetry can be explained in a difference of metal work function in TE and BE. The BE should be an inert metal, while the TE is an oxygen scavenging layer. This oxygen scavenging layer introduces oxygen vacancy (V_O) defects in the cell (and reduces the V_{FORM}) and this in an asymmetric way, forming a kind of V_O reservoir at the TE interface [1, 2]. In this section, the thickness effect of Ta-OE in the Ta_2O_5 based ReRAM is analyzed.

4.2.1 Device fabrication

In this study, nano-scale 80×80 nm^2 size ReRAM device were fabricated using Ta_2O_5 oxide thin film, deposited by physical vapor deposition (PVD).
Fig. 4.11(a) shows the layer stacks consisting of 30 nm-thick Pt (Bottom Electrode), 7 nm-thick Ta_2O_5 , thickness splits of Ta-OE (3 nm, 7 nm, 13 nm, 30 nm) and 25 nm-thick Pt (Top Electrode). A top-down SEM image of nano-crossbar structure is also shown in Fig 4.11(b).

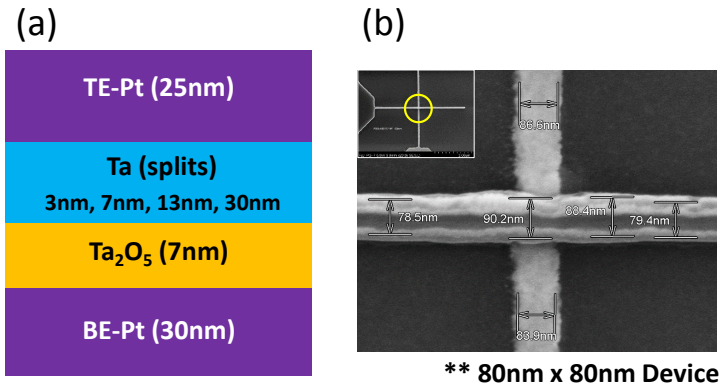


Figure 4.11: (a) A schematic cross-sectional diagram with experimental split conditions with different Ta-OE thickness (3 nm, 7 nm, 13 nm, 30 nm). (b) Scanning electron microscope image of the 80 × 80 nm^2 ReRAM device in passive crossbar configuration.

4.2.2 Forming voltage

V_{FORM} is compared depending on different Ta-OE thickness as shown in 4.12(a). It decreases as the Ta-OE increases. The 3nm-thick Ta showes the highest V_{FORM} (= 3.0 V), while the lowest V_{FORM} (= 2.0 V) was observed from the 30 nm-thick Ta.

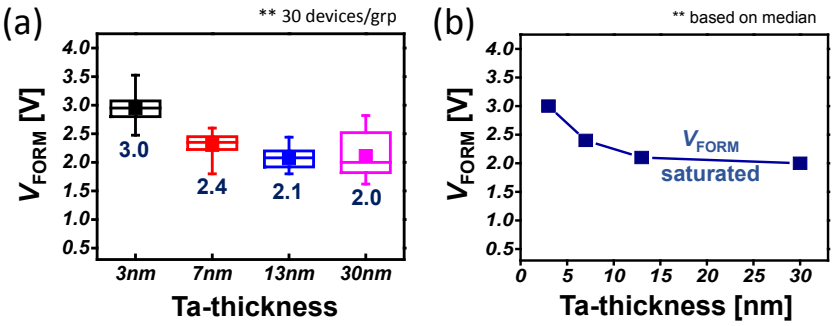


Figure 4.12: (a) V_{FORM} change with different Ta-OE thickness (3 nm, 7 nm, 13 nm, 30 nm). (b) Saturation of the V_{FORM} with thicker Ta-OE in real scale plot.

It seems that the V_{FORM} decreases abruptly from 3 nm to 7 nm, however, the

V_{FORM} change becomes saturated from 13 nm-thick Ta ($V_{FORM} = 2.1$ V) as shown in 4.12(b). The decrease of V_{FORM} is related to the amount of V_O generated in Ta_2O_5 film implying that the increase of Ta-OE thickness does not continuously proliferate the oxygen exchange [19, 92].

4.2.3 Current compliance effect

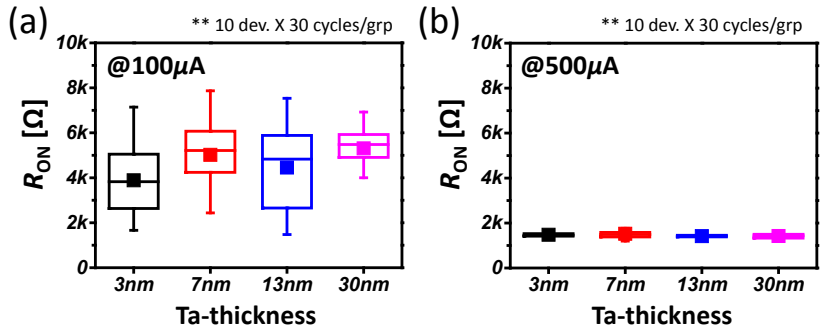


Figure 4.13: R_{ON} change with different Ta-OE thickness (3 nm, 7 nm, 13 nm, 30 nm) (a) at the $I_{CC} = 100\,\mu$A (b) at the $I_{CC} = 500\,\mu$A.

An impact of I_{CC} change on performance of ReRAM devices was analyzed over different thickness of Ta-OEs. Two distinctively different I_{CC} levels (100 μA, 500 μA) are applied for electrical characterization based on DC measurement. Since it is well known that as the I_{CC} levels directly impact the R_{ON} states, the R_{ON} performance was analyzed first. As you can observe from Fig. 4.13(a), all split thicknesses show relatively increased R_{ON} states ($> 4\,k\Omega$) as expected at low I_{CC}(@100 μA) . There was no trend found with the thickness change of Ta-OE at the $I_{CC} = 100\,\mu$A. When the I_{CC} level increases up to 500 μA, overall resistance levels decrease from $\sim$5.0 $k\Omega$ to $\sim$1.5 $k\Omega$ without any correlation with the Ta-OE thickness as shown in Fig. 4.13(b). The distribution of R_{ON} becomes wider with lower I_{CC} level. Regardless of Ta-OE thickness, standard deviation for the $I_{CC} = 100\,\mu$A was about 1.5 $k\Omega$ while the standard deviation for the $I_{CC} = 500\,\mu$A is about 100 Ω implying the increased I_{CC} could produce tighter distribution of R_{ON} performance.

No impact of Ta-OE thickness was found for the R_{ON} performance regardless of I_{CC} levels. R_{OFF} performance was also compared, shown in Fig.4.14. For both

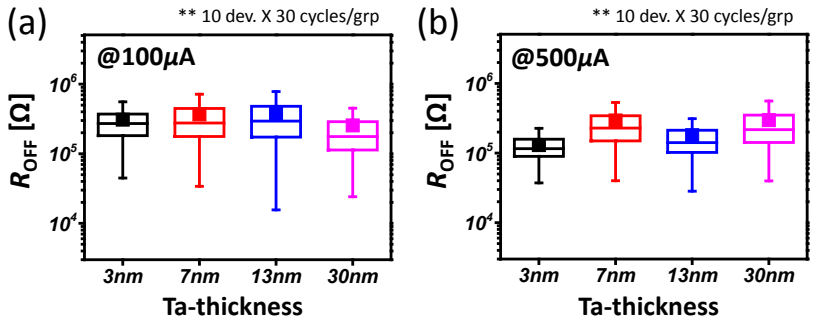


Figure 4.14: R_{OFF} change with different Ta-OE thickness (a) at the I_{CC} = 100 μA (b) at the I_{CC} = 500 μA.

I_{CC} conditions, there was difference of R_{OFF} performance found irrespective of Ta-OE thickness. Unilike the improvement of R_{ON} distribution with higher I_{CC} level, there was no such an improvement observed in R_{OFF} distribution with higher I_{CC} application. Next, the impact of the Ta-OE on the I_{RESET} has been analyzed. For this analysis, the applied $V_{\mathrm{RESET-STOP}}$ was fixed to be -2.0 V. The I_{RESET} is the highest current (in negative) during the RESET voltage sweep.

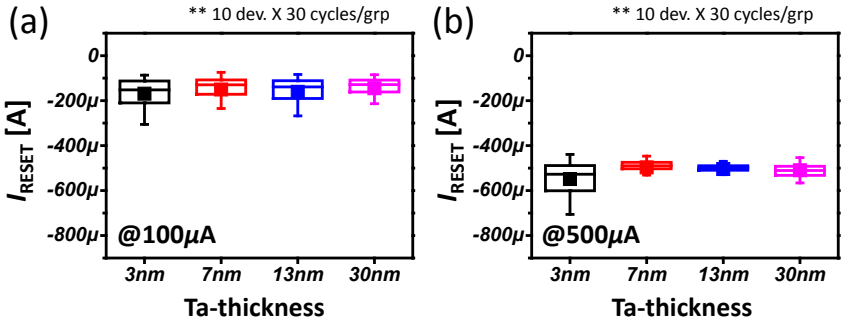


Figure 4.15: I_{RESET} change with different Ta-OE thickness (3 nm, 7 nm, 13 nm, 30 nm) (a) at the I_{CC} = 100 μA (b) at the I_{CC} = 500 μA.

The Fig. 4.15(a) shows the I_{RESET} comparison for the I_{CC} = 100 μA. The 3nm-thickness shows a bit increased I_{RESET} (-170 μA vs. -150 μA) compared with the others under identical I_{CC} = 100 μA condition. For the I_{CC} =

500 μA also, higher I_{RESET} (-550 μA vs. -500 μA) is observed with wider distribution (σ: 76 μA vs. 40 μA) in Fig. 4.15(b). Overall the 3nm-thickness shows an increased I_{RESET} with wider distribution compared with the others. And this analysis also clearly shows that as the I_{CC} increases, the corresponding I_{RESET} also increases (in negative). This is due to the fact the conductive filament size is proportional to the I_{CC} [93, 94] and it will require higher energy to break this filament.

4.2.4 $V_{\mathrm{RESET\text{-}STOP}}$ effect

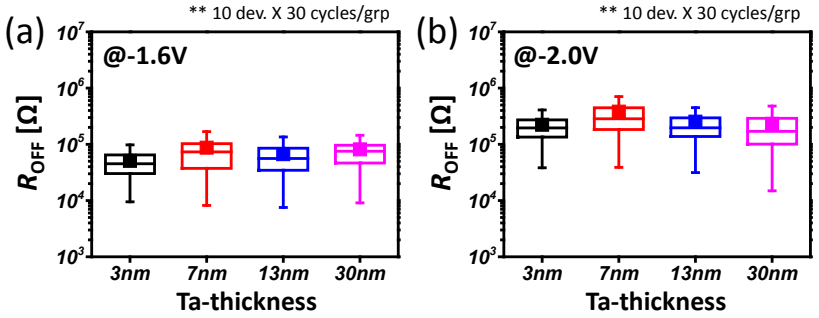


Figure 4.16: R_{OFF} change with different Ta-OE thickness (3 nm, 7 nm, 13 nm, 30 nm) (a) at the $V_{\mathrm{RESET-STOP}}$ =-1.6 V (b) at the $V_{\mathrm{RESET-STOP}}$ =-2.0 V

An impact of the $V_{\mathrm{RESET-STOP}}$ change on performance of ReRAM devices was analyzed over different thickness of the Ta-OEs. Two distinctively different $V_{\mathrm{RESET-STOP}}$ levels (-1.6 V, -2.0 V) are applied for electrical characterization based on DC measurement. It is well known that as the $V_{\mathrm{RESET-STOP}}$ can impact the R_{OFF} states and V_{SET}. As you can observe from Fig. 4.16(a), there was no difference in R_{OFF} levels regardless of Ta-OE thickness. When the $V_{\mathrm{RESET-STOP}}$ is raised up to -2.0 V, overall R_{OFF} levels increase as shown in Fig. 4.16(b). R_{ON} performance for both $V_{\mathrm{RESET-STOP}}$ =-1.6 V and -2.0 V was also comparable irrespective of the Ta-OE thickness. Therefore, there was no difference in R_{ON} / R_{OFF} ratio for both $V_{\mathrm{RESET-STOP}}$ conditions in Fig. 4.17. However, it was clearly shown that as the $V_{\mathrm{RESET-STOP}}$ increases, the R_{ON}

/ R_{OFF} ratio improves due to the higher R_{OFF} state which corresponds to larger gap between the high WF electrode and the conductive filament.

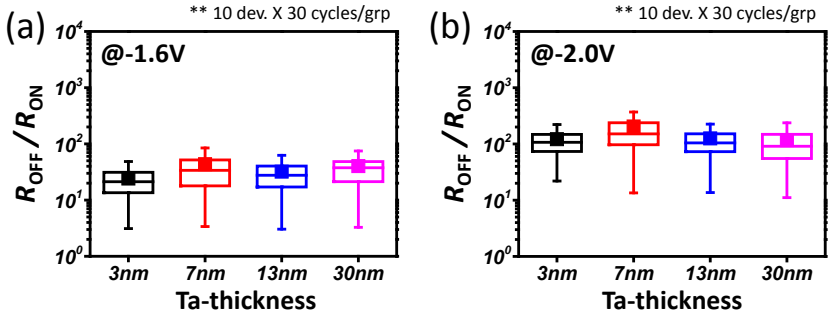


Figure 4.17: R_{OFF}/R_{ON} change with different Ta-OE thickness (3 nm, 7 nm, 13 nm, 30 nm) (a) at the $V_{RESET-STOP}$ =-1.6 V (b) at the $V_{RESET-STOP}$ =-2.0 V

4.2.5 Data retention time

The retention at 125 °C is compared in Fig. 4.18. Since major failure of retention for the Ta_2O_5 based ReRAM devices are from the R_{OFF} to the R_{ON} , our analysis on the data retention is focused only on the R_{OFF} states. All thicknesses show robust retention performance without any failure at 125 °C up to 10^4 seconds.

4.2.6 Summary of this section

The Ta-OE thickness affects the $V_{FORM}$of the Ta_2O_5 ReRAM device. As the Ta-OE becomes thicker, the corresponding V_{FORM} decreases. However, the reduction of V_{FORM} becomes saturated at 13 nm thickness. The V_{FORM} reduction is related to the amount of the V_O generated in the Ta_2O_5 film implying that the increase of the Ta-OE thickness does not continuously proliferate the oxygen exchange. Based on electrical characterization of DC sweeps for the SET and the RESET process, there was no correlation found between the thickness change of Ta-OE and measurement characteristics

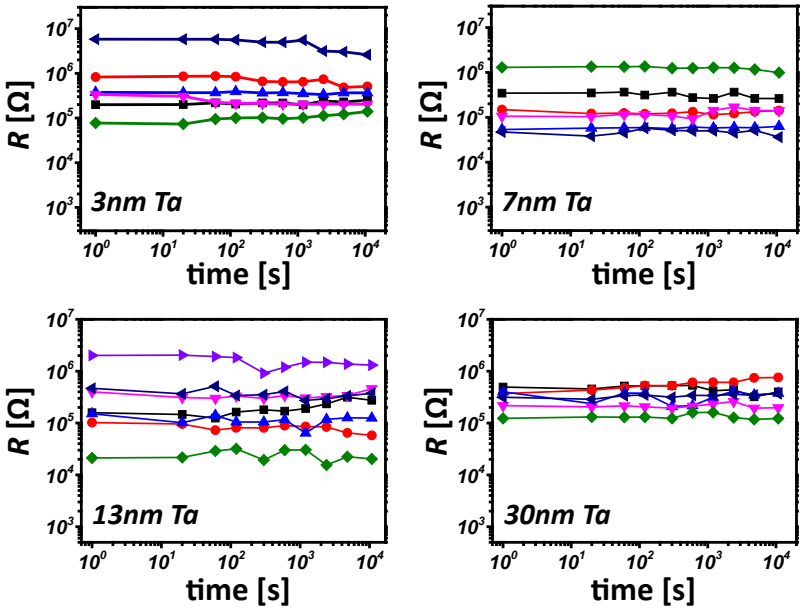


Figure 4.18: Analysis of data retention time for all Ta-OE thicknesses at 125 °C up to 10^4 seconds

such as R_{ON}, R_{OFF}, memory window (R_{OFF} / R_{ON}) and I_{RESET} for both I_{CC} effects and $V_{RESET-STOP}$ effects. However, this analysis helps to optimize the thickness of Ta-OE in order to reduce the V_{FORM} in the Ta_2O_5 based ReRAM devices.

4.3 Conclusion of this chapter

In this chapter, effects of the OE in the Ta_2O_5 ReRAM devices have been analyzed for different OE-materials and Ta-OE thickness. For the OE-material investigation, the impact of four different OE materials (W, Ta, Ti, and Hf) was studied on the characteristics of Ta_2O_5 ReRAM. Early RESET failures were observed from the Ti- and Hf-OE devices due to an accumulation of the V_O's during the switching cycles while highly stable switching processes were achieved with the W- and Ta-OE devices. The W-OE devices show an increased R_{OFF} compared with the Ta-electrode

under identical RESET conditions and the difference can be explained by higher E_{VO} of W-OE. On the other hand, the lower E_{VO} for Ta-OE results in faster SET processes than W-OE.

For the study on the Ta-OE thickness change, as the Ta-OE becomes thicker, the corresponding V_{FORM} decreases due to the increased amount of V_O generated in Ta_2O_5 layer. However, there was no further difference observed in electrical characterizations such as R_{ON}, R_{OFF} in terms of $V_{RESET-STOP}$ and I_{CC} effects by changing the Ta-OE thickness.

Chapter 5

Forming Free ReRAM Device

Here, in this chapter, we have investigated various device fabrication parameters of Ta_2O_5 ReRAM devices, which might lower the V_{FORM} such as switching layer thickness and OE thickness, rapid thermal annealing (RTA) at different temperature in oxygen ambient. Next, we investigate the impact of oxygen/nitrogen implantation on the V_{FORM} and other switching characteristics parameter. In the end, we propose the mechanism of forming-free ReRAM devices resulted from the oxygen ion implantation process.

5.1 Stack engineering of Ta_2O_5 ReRAM for V_{FORM} lowering

A possibility to reduce V_{FORM} by controlling the layer thickness of Ta_2O_5 switching oxide and Ta-OE is investigated in this section.

5.1.1 Thickness reduction: Ta-OE vs. Ta_2O_5

V_{FORM} is generally affected by the thickness of the active switching layer and corresponding OE ,which is demonstrated by the forming- free HfO_2 based ReRAM device [19]. In previous chapter, we have studied the impact of the switching layer and OE thickness on the V_{FORM} in detail and concluded the same trends of lowering the V_{FORM} with the Ta_2O_5 layer thickness.
Fig. 5.1 shows the dependence of V_{FORM} on the Ta_2O_5 thickness and Ta-OE

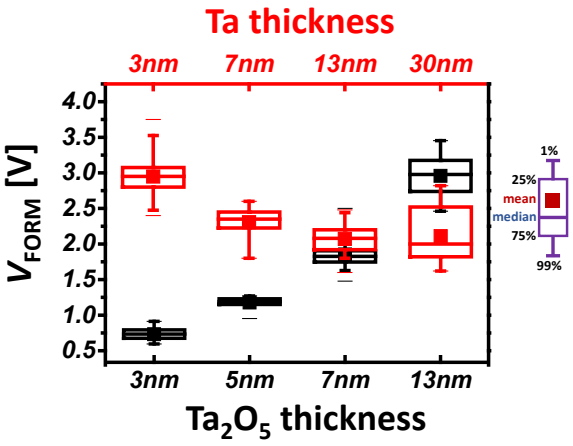


Figure 5.1: V_{FORM} variations (30 cells from each group) depending on thickness change of Ta-OE and Ta_2O_5 switching layer for $2 \times 2\,\mu m^2$ Pt/Ta_2O_5/Ta/Pt ReRAM device

thickness for the Pt/Ta_2O_5/Ta/Pt ReRAM device. The Ta-electrode thickness varied from 3 nm up to 30 nm with fixed 7 nm-thick Ta_2O_5, while the Ta_2O_5 thickness ranged from 3 nm to 13 nm for fixed Ta-electrode thickness of 13 nm. For the Ta-OE (shown in red), as the electrode thickness increases, the corresponding V_{FORM} decreases. However, the V_{FORM} saturates around 2.0 V for the Ta thicknesses at or above 7 nm, and the forming process is still required even for the 30 nm-thick Ta-electrode. For the Ta_2O_5 switching layer, as the thickness decreases, the V_{FORM} decreases below 1.5 V at 5 nm-thick and even below 1.0 V for 3 nm-thick Ta_2O_5. So, thinning the switching layer seems a more viable route for reducing V_{FORM} .

5.1.2 Device performance: Ta_2O_5 thickness reduction

The off-state resistance (R_{OFF}) and on-state resistance (R_{ON}) depending on the thickness of the Ta_2O_5 switching layer thickness is shown in Fig. 5.2(a). However, the ratio ($R_{\mathrm{OFF}}/R_{\mathrm{ON}}$) significantly drops for the 3 nm-thick Ta_2O_5 device as it cannot maintain reasonable R_{OFF} during the reset cycles. Also, retention at 125 °C has been measured for the devices with different Ta_2O_5 thickness as shown in Fig. 5.2(b). While the 13 nm- and 7 nm-thick Ta_2O_5

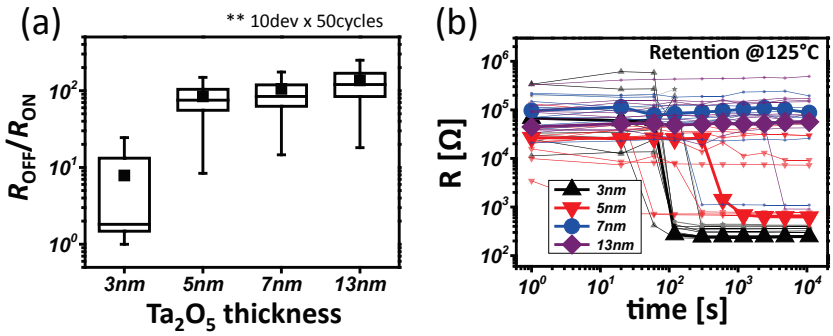


Figure 5.2: (a) Dependence of the R_{OFF}/R_{ON} on the Ta_2O_5 switching thickness for $2 \times 2\,\mu m^2$ Pt/Ta_2O_5/Ta/Pt ReRAM device, (b) Data retention time of 3 nm-, 5 nm-, 7 nm- and 13 nm-thick Ta_2O_5 ReRAM devices (10 devices from each split) at 125 °C for 10^4 seconds

devices show fairly robust retention performance (with only single failure out of 10 devices), 50% devices of the 5 nm-thick Ta_2O_5 devices and 100% of the 3 nm-thick Ta_2O_5 devices show early retention failures.
This analysis shows that the reduction of the V_{FORM} as the result of switching layer thickness leads to degradation of device performance. Therefore, a novel way for reduction of the V_{FORM} or even complete elimination of the forming process, i.e forming free device, is required. In next section, we investigate the effect of rapid thermal annealing process on the forming behavior of the Ta_2O_5 ReRAM device.

5.2 Lowering V_{FORM} with RTA process

Here, in this section, we investigated how rapid thermal annealing (RTA) on the Ta_2O_5 switching layer during device fabrication can impact the performance of Ta_2O_5 ReRAM devices including V_{FORM} at different temperature in oxygen ambient. In this experiment, nano-crossbar structures of $80 \times 80\,nm^2$ ReRAM have been fabricated with 30 nm-thick Pt (Bottom Electrode), 3.5 nm-thick Ta_2O_5 (Bottom Layer), 3.5 nm-thick Ta_2O_5 (Top Layer), 13 nm-thick Ta and 25 nm-thick Pt (Top Electrode), as shown in

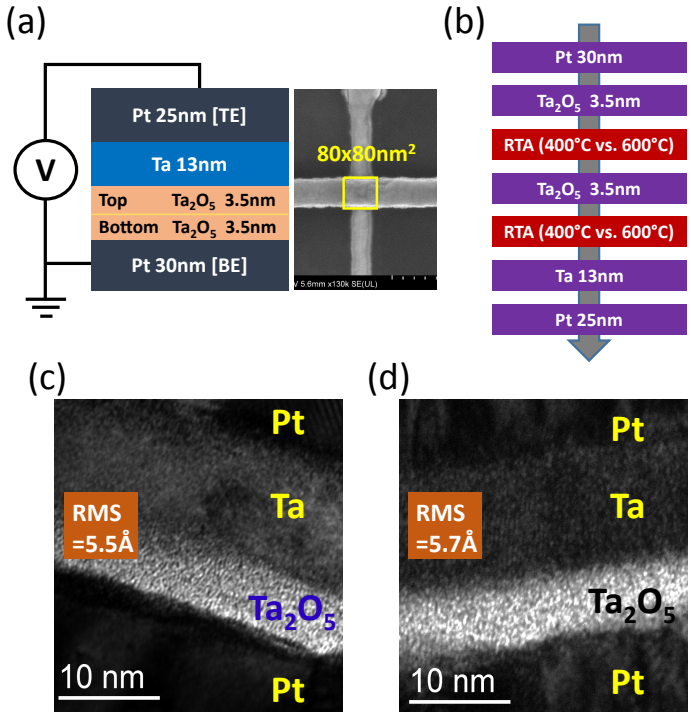


Figure 5.3: (a) A cross-sectional schematic of device and its corresponding SEM image of 80×80 nm^2 Pt/Ta_2O_5/Ta/Pt ReRAM device, (b) Process flow of nano-structure fabrication with RTA process. TEM images and surface roughness measured by AFM from, (c) Device with RTA at 600 °C for both Ta_2O_5 layers (Top, Bottom) and (d) Reference device.

Fig. 5.3(a). Both Ta_2O_5 layers were deposited by the reactive sputtering. RTA for the Ta_2O_5 switching layer were applied in oxygen atmosphere. The RTA processes were applied to either top or bottom Ta_2O_5 layers or both (B: bottom, T: top, D: dual) shown in Fig. 5.3(b). TEM and AFM images of RTA-600D and non-heat-treated reference (Ref) device, shown in Fig. 5.3(c, d) confirm that the Ta_2O_5 film thickness and surface roughness after the RTA treatment remains unchanged (RTA-600D: rms = 5.5 Å and Ref: rms = 5.7 Å). The electrical characterization of the device was performed with

Keithley 4200SCS parameter analyzer at room temperature.

5.2.1 Electrical characteristics

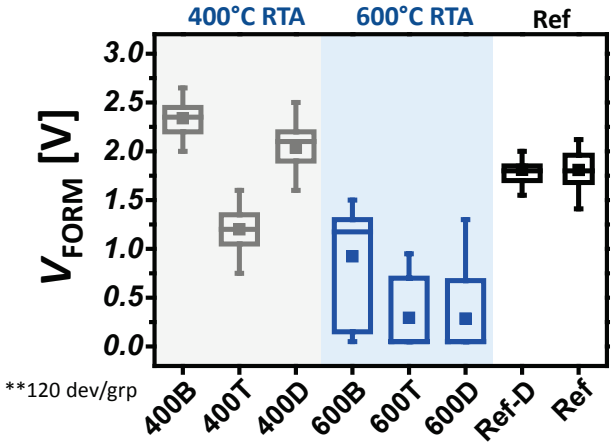


Figure 5.4: Effect of the RTA on the V_{FORM} of $80 \times 80\,nm^2$ $Pt/Ta_2O_5/Ta/Pt$ ReRAM device. For each condition, 120 devices were measured. At 600 °C, most of the devices shows significant reduction of the V_{FORM}.

The device 400B shows an increased V_{FORM} while a reduction for sample 400T is observed in Fig. 5.4. Nevertheless, all samples of 400 °C splits require forming procedure varying from 2.3 V to 1.3 V. However, the devices with 600T and 600D conditions show radical V_{FORM} reduction compared with the Reference (Ref-D with dual layers, Ref with single 7.0 nm-thick layer) groups. For both splits, the median V_{FORM} is 0.0 V (forming-free) and mean V_{FORM} is 0.2 V. More than 70 % of measured devices from both groups (600T and 600D) show the forming-free behaviors. The devices with 600B condition has relatively higher V_{FORM} ($\sim$ 1.2 V based on median) with wider distribution. Hence, overall 600 °C RTA condition significantly reduces the V_{FORM} effectively.

5.2.2 RESET behaviors

Generally, the reset behavior after the forming process is related to the overshoot phenomena [95, 96]. Higher 1st reset current corresponds to the

larger overshoot in the device. The I-V curves in Fig. 5.5(a) show the (typical) 1st reset behavior after forming for the 600 °C RTA splits and reference device. Since the devices with 600T (in red) and with 600D condition (in blue) do not require the forming, the maximum 1st RESET currents (I_{RESET}) are relatively lower (300 μA $\sim$ 400 μA). The samples with 600B (in magenta) needs forming and the 1st $I_{\mathrm{RESET}} \approx 1.0\,m$A. Based on 120 devices from each split, the statistical comparison on the 1st I_{RESET} after the forming process is shown in Fig. 5.5(b).

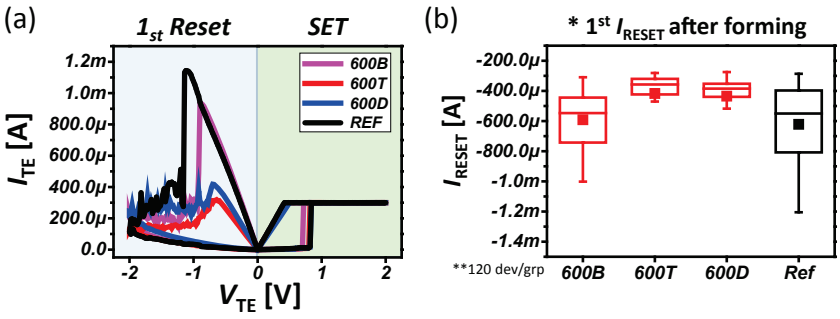


Figure 5.5: Based on the the $80 \times 80\,n\mathrm{m}^2$ Pt/Ta_2O_5/Ta/Pt ReRAM devices (a) Forming characteristics and the 1st reset behavior of for thermally treated and reference devices, (b)The 1st RESET current under different thermal conditions. At 600 °C, the ReRAM device shows the reduction of 1st RESET current.

The forming current compliance for all splits was 300 μA. The 1st I_{RESETS} of 600B, 600T and 600D are 530 μA, 330 μA, and 350 μA (median value) respectively. Also, 600T and 600D shows much tighter distribution than 600B and reference devices.

5.2.3 Effects of I_{CC}

The R_{OFF} and R_{ON} are compared under identical SET-RESET switching conditions with 2 different I_{CC} conditions (100 μA, 300 μA) as shown in Fig. 5.6. For the SET process, the I_{CC} levels were kept at 100 μA and 300 μA. For the RESET process, the maximum applied voltage ($V_{\mathrm{RESET-STOP}}$) for DC sweep was -2.0 V.

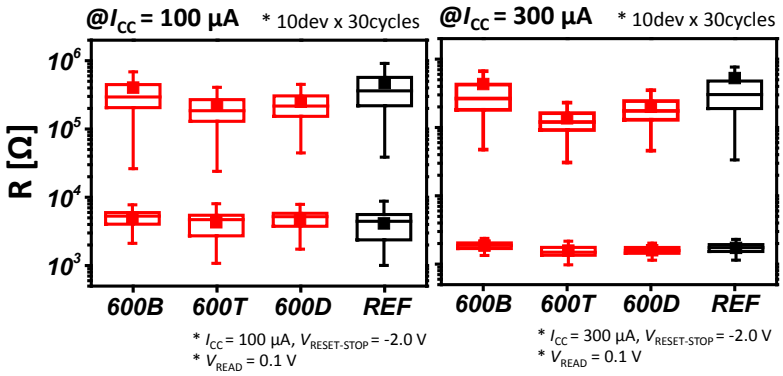


Figure 5.6: I_{CC} effects (100 μA, 300 μA) of $80 \times 80\,nm^2$ Pt/Ta_2O_5/Ta/Pt ReRAM devices

The devices of 600B show the $R_{OFF} \approx 270\,k\Omega$, which is similar to the reference samples for both I_{CC} conditions. The samples of 600T and 600D show the $R_{OFF} \approx 150\,k\Omega$ and $200\,k\Omega$ respectively for both I_{CC} conditions. The R_{OFF} performance among the splits is quite close to each other with only small difference. For the R_{ON}, obviously all devices including the REF show increased R_{ON} at $I_{CC} = 100\,\mu$A compared with 300 μA and this is due to the fact that lower I_{CC} generates the thinner conductive filament. However. there was no difference observed among the splits as the I_{CC} is kept constant. Therefore, the comparable memory window (R_{OFF}/R_{ON}) can be maintained with the 600T and 600D conditions.

5.2.4 Endurance and retention

Since the 600D samples have undergone to a larger thermal budget than those of the 600T, the 600D was chosen for reliability testing (both endurance and retention).

Successful endurance of 10 devices up to 10^6 cycles has been achieved for the 600D samples, shown in Fig. 5.7(a) (applied pulse conditions are -1.6 V for the reset and 1.2 V for the set process at 1.0 μs pulse width). The resistance states in Fig. 10(a) are verified with an AC read pulse of 0.1 V with 1.0 μs pulse-width. Also, excellent retention up to 10^4 seconds for the samples 600D

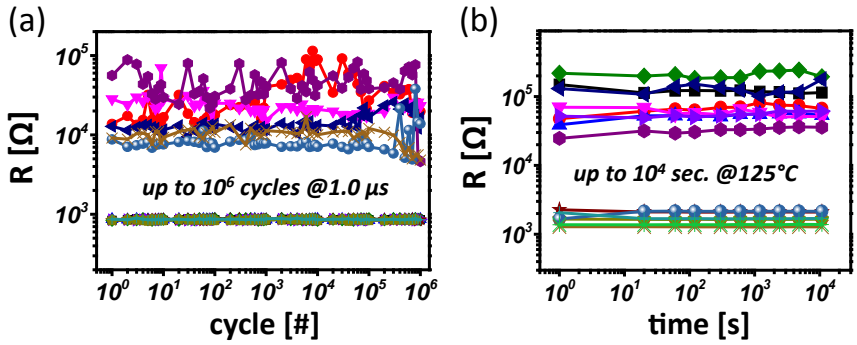


Figure 5.7: Reliability measurement of 600D (a) AC endurance up to 10^6 cycles with 1.0 μs pulse width with $V_{\mathrm{SET}} = 1.2\,\mathrm{V}$ and $V_{\mathrm{RESET}} = -1.6\,\mathrm{V}$. (b) Robust data retention at 125 °C up to 10^4 seconds.

is achieved at 125 °C, shown for 8 devices in Fig. 5.7(b). The resistance states for the retention are verified with the DC V_{read} of 0.1 V.

5.2.5 Summary of this section

In summary, we have demonstrated the impact of the switching layer thickness and OE thickness on the Pt/Ta_2O_5/Ta/Pt ReRAM device. The V_{FORM} decreases with thinner switching layer and thicker OEs. However, the effect of thicker Ta layer already saturates at the Ta thickness (7 nm), and thinner Ta_2O_5 degrades the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ and retention performance of the ReRAM device. On the other hand, RTA of the switching layer reduces the R_{initial} and V_{FORM} of the ReRAM devices. At 600 °C, 65% of the characterized devices show the forming-free behavior. These forming-free devices show highly reliable switching operation up to 10^6 cycles with $R_{\mathrm{OFF}}/R_{\mathrm{ON}} > 10$ and excellent retention time of 10^4 s at 125 °C.

5.3 Forming-free ReRAM devices

In previous section, we have demonstrated the forming-free ReRAM devices with the RTA process. However, this method is not compatible to advanced CMOS technology due to higher thermal budget (600 °C) and only 70% devices

show the forming-free behavior. Therefore, it is highly important to investigate an alternative method which has lower thermal budget and gives 100% yield for forming-free behavior. Here, we demonstrate the forming-free Ta_2O_5 and HfO_2 ReRAM device by oxygen ion implantation (O_2 IIP) and nitrogen ion implantation (N_2 IIP) in the respective switching oxide layer.

5.3.1 Device fabrication with O_2 IIP

In this study, two types of nano-scale $80 \times 80\,n\text{m}^2$ size ReRAM devices were fabricated using different oxide thin films (Ta_2O_5 and HfO_2), deposited by reactive physical-vapor-deposition (PVD) and plasma enhanced atomic-layer -deposition (PEALD) respectively.

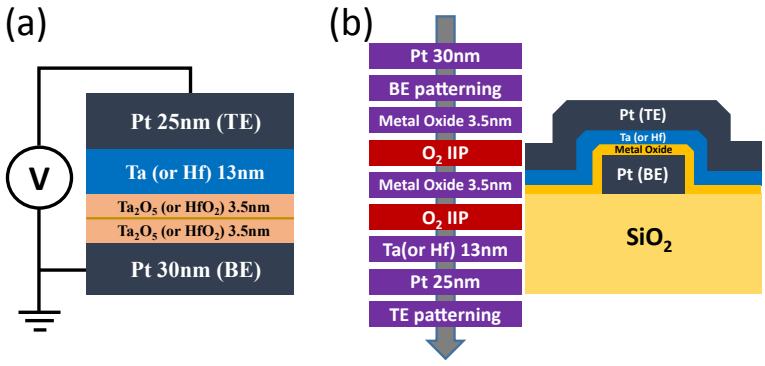


Figure 5.8: (a) Cross-sectional structure of Ta_2O_5, HfO_2 ReRAM device with $80 \times 80\,n\text{m}^2$ size, (b) Process flow of nano-structure fabrication with O_2 IIP and cross-sectional schematic along TE

Fig. 5.8(a) shows the layer stacks consisting of 30 nm-thick Pt (BE), 7 nm-thick Ta_2O_5 (or 7 nm-thick HfO_2), 13 nm-thick Ta (or 13 nm-thick Hf, OE) and 25 nm-thick Pt (TE). The O_2 ion implantation (O_2 IIP) with different doses and fixed energy of 30 keV was applied directly after the deposition of metal oxide layer, as shown in Fig. 5.8(b). No thermal treatment was carried out after the implantation. Reference devices without the O_2 IIP were also fabricated in this process. Fig. 5.9 shows the simulated oxygen implanted profiles in 7 nm-thick Ta_2O_5 / 30 nm-thick Pt(BE) / 430 nm-thick SiO_2 stacks. Fig. 5.10 shows that the reference device and forming-free device have similar Ta_2O_5 thickness

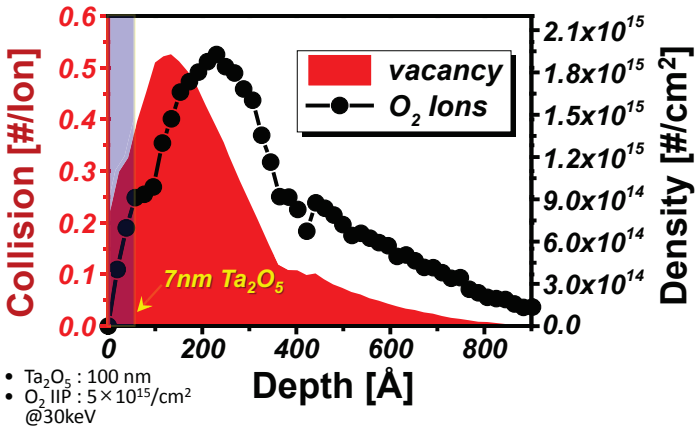


Figure 5.9: Simulation results of defect generation and ion penetration depending on depth due to the O_2 IIP with $5.0 \times 10^{15}/\mathrm{cm}^2$ at 30 keV energy

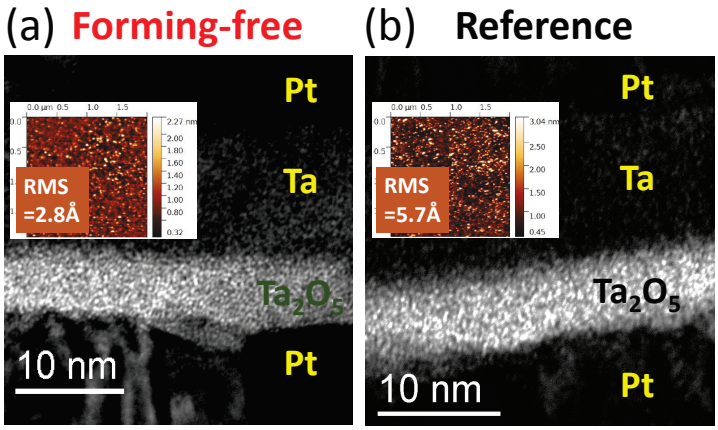


Figure 5.10: TEM and AFM images of the Ta_2O_5 ReRAM from (a) Forming-free device with O_2 IIP, (b) Reference

and surface roughness based on TEM images and AFM images confirming no negative effects such as surface roughening and oxide thickness reduction from the O_2 IIP.

5.3.2 Reactive PVD-Ta_2O_5 ReRAM device: forming behavior

The O_2 IIP in the Ta_2O_5 ReRAM was applied with 2 separate doses, D_1 and D_2 ($D_2 = 5 \times D_1$) at fixed energy of 30 keV with EATON-Implanter. The used doses are $1.0 \times 10^{15}/cm^2$ (D_1), $5.0 \times 10^{15}/cm^2$ (D_2) respectively. The D_2 IIP condition at EATON-Implanter is equivalent to oxygen etch with O_2-Low condition (acceleration current: 3 mA, acceleration voltage: 187 V) for 60 seconds at RIBE tool.

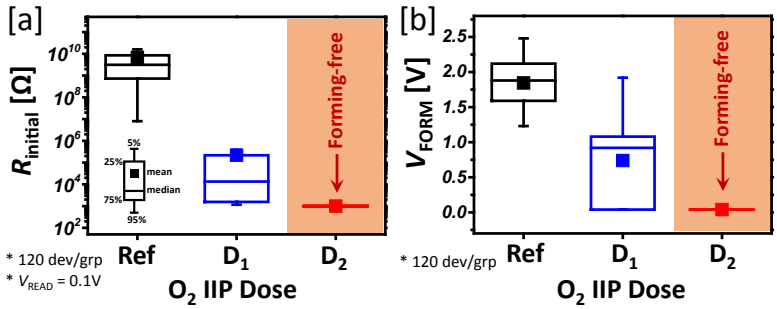


Figure 5.11: Dependence of (a) R_{initial} comparison and (b) V_{FORM} of the $Pt/Ta_2O_5/Ta/Pt$ on the implantation dose and condition

Fig. 5.11(a) shows that the R_{initial} decreases as the O_2 IIP dose increases. In comparison with the reference device (3 $G\Omega$), the R_{initial} of O_2 IIP devices is greatly reduced to 25 $k\Omega$ and 1.3 $k\Omega$ with doses D_1 and D_2, respectively. The V_{FORM} is compared in Fig. 5.11(b). It decreases abruptly from 1.8 V (reference) to 0.9 V with the dose D_1 and ultimately, the forming-free state for all devices were obtained with dose D_2. The typical I-V forming curves for all implantation conditions are shown in Fig. 5.12.

A correlation between the R_{initial} of forming-free devices and their device sizes has been analyzed in Fig. 5.13. The R_{initial} decreases as the device size increases. As for the initial conduction, a uniform conduction over the area would be expected from the O_2 IIP process. While the conduction indeed scales with area, there is no 1:1 correlation observed in Fig. 5.13(b). This may be explained by the device topography caused by non-planarized bottom electrode line, causing most critical areas for higher conduction at the edge

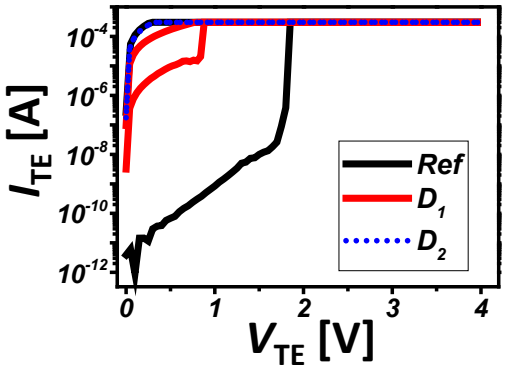


Figure 5.12: Forming behavior of the Ta_2O_5 ReRAM for different implantation dose

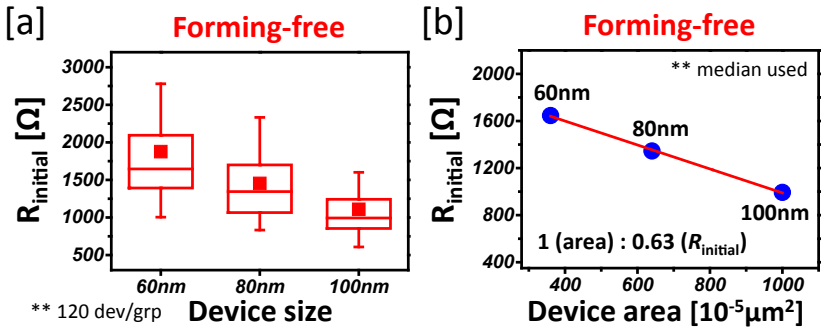


Figure 5.13: Dependence of R_{initial} on the device (a) size and (b) area for the Ta_2O_5 based forming-free device.

steps. Thus, the more localized conduction explains the rather easier 1st RESET with a similar V_{RESET} to that of filamentary switching. Detailed comparisons of the R_{initial} distributions is made in Fig. 5.14. Similar tight resistance state distributions are observed for the R_{initial} of forming-free devices and the R_{ON} of reference device after SET based on I_{CC} of 300 μA. This shows the possibility of an accurate control of the R_{initial} with the O_2 IIP. High V_{FORM} in ReRAM devices generally causes current overshoots and high 1st RESET currents. Fig. 5.15 shows the comparison of 1st RESET current and typical 1st RESET behavior for forming-free and reference devices. On average, the forming-free devices show 41% reduction in the 1st

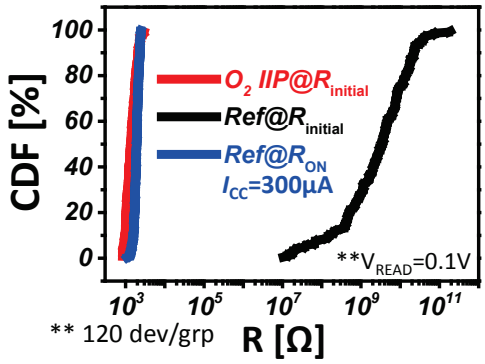


Figure 5.14: Cumulative distribution of the R_{initial} for the forming-free and reference in Ta_2O_5 ReRAM device. The R_{ON} of reference device is estimated at SET (I_{CC} = 300 μA).

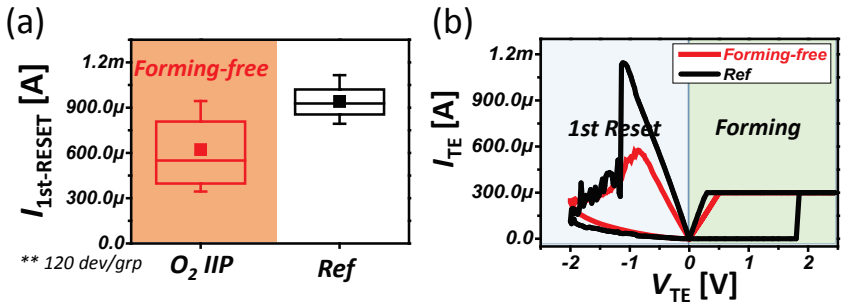


Figure 5.15: The reduced 1$^{\text{st}}$ RESET current with O_2 IIP (a) in bar plots with distribution, (b) in typical I-V curves after forming for the Ta_2O_5 ReRAMs.

RESET current.

5.3.3 Reactive PVD-Ta_2O_5 ReRAM device: I_{CC} and V_{RESET} effects

The I_{CC} effect at fixed $V_{\text{RESET-STOP}}$ (= -2.0 V) has been compared from 50 μA to 500 μA, in Fig. 5.16. For overall I_{CC} ranges, there was no difference observed in R_{ON} between the forming-free and the reference.

The $V_{\text{RESET-STOP}}$ effect from -1.4 V to -2.0 V at fixed I_{CC} = 300 μA is shown

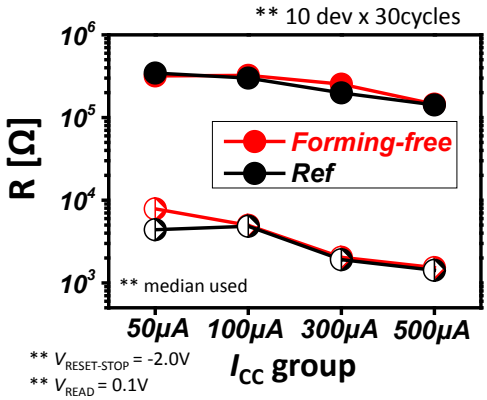


Figure 5.16: Dependence of the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ on the I_{CC} for Ta_2O_5 ReRAMs

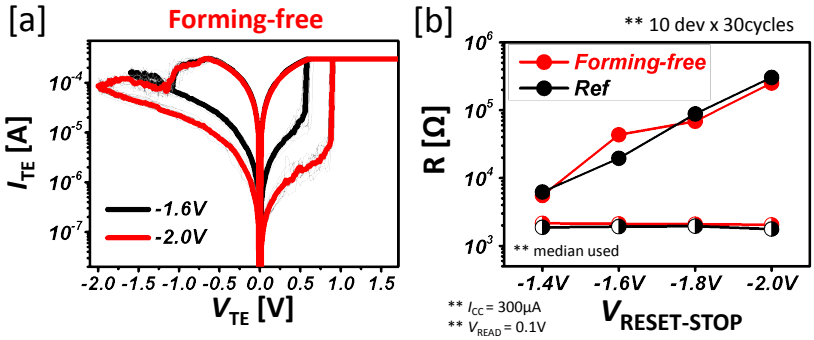


Figure 5.17: (a) I-V characteristic of the Ta_2O_5 forming-free ReRAM device for different $V_{\mathrm{RESET-STOP}}$ (b) Dependence of the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ on the $V_{\mathrm{RESET-STOP}}$ for the forming-free and reference devices.

in Fig. 5.17. The R_{OFF} increases with higher $V_{\mathrm{RESET-STOP}}$, keeping the R_{ON} constant. No difference in the R_{OFF} between the forming-free and the reference was observed. Additionally, high $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio ($\sim$200) for the forming-free Ta_2O_5 ReRAM shows the MLC capability.

5.3.4 Reactive PVD-Ta_2O_5 ReRAM device: endurance and retention

Finally, the reliability of the forming-free Ta_2O_5 devices was evaluated. AC endurance with 1.0 μs pulse width up to 10^6 cycles and data retention time up to 10^4 seconds at 125 °C are demonstrated in Fig. 5.18 and Fig. 5.19, respectively, showing no difference between the forming-free and the reference devices.

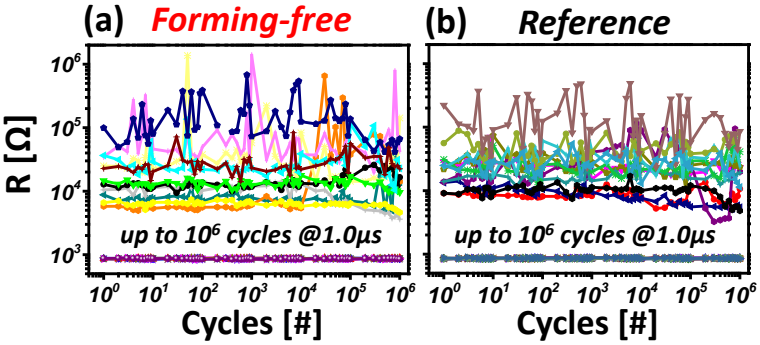


Figure 5.18: Excellent endurance characteristics up to 10^6 cycles with 1.0 μs pulse width for (a) the forming-free devices, (b) the reference devices

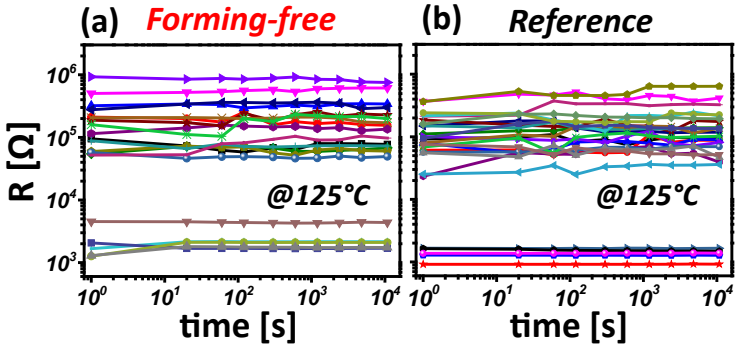


Figure 5.19: Good data retention up to 10^4 seconds at 125 °C for (a) the forming-free devices, (b) the reference devices

5.3.5 Plasma enhanced ALD-HfO_2 ReRAM device: forming behavior

Fig. 5.20(a) shows the V_{FORM} of the HfO_2 ReRAM for three O_2 IIP doses. The baseline O_2 IIP dose for the forming-free Ta_2O_5 layer is D_2. For the HfO_2 layer, the dose is increased by $\times 2$ and $\times 3$ times of D_2 with fixed implantation energy. Again, as the O_2 IIP dose increases, the V_{FORM} decreases and the forming-free HfO_2 ReRAMs are obtained with $2 \times D_2$ and $3 \times D_2$ doses. The typical I-V forming curves are compared in Fig. 5.20(b).

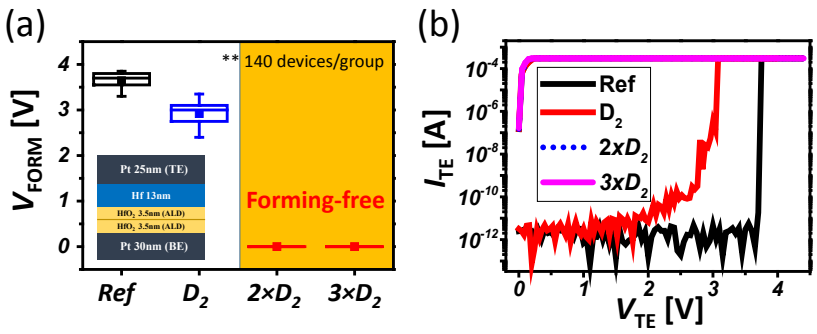


Figure 5.20: (a) Dependence of the V_{FORM} on the O_2 IIP dose for the HfO_2 ReRAMs, (b) Typical forming curves for different O_2 IIP dose of HfO_2 ReRAMs at the $I_{\mathrm{CC}} = 300\,\mu\mathrm{A}$

The 1st RESET switching in the HfO_2 devices is influenced by the O_2 IIP process. The 1st RESET behaviors with dose splits are compared in Fig. 5.21. A much deeper RESET is obtained for the reference HfO_2 sample. The higher HRS compared to the Ta_2O_5 is attributed to a better stoichiometry of the ALD HfO_2 vs PVD Ta_2O_5. The 1st RESET in the reference HfO_2 is very abrupt with a high subsequent SET failure rate. Typical curves of SET failure from the reference are shown in Fig. 5.22 and the SET failure decreases up to 10% as the O_2 IIP dose increases. However, further increasing the dose ($3 \times D_2$) again made the voltage and current of the 1st RESET higher and making it more abrupt as shown in Fig. 5.21. Hence, a careful dose optimization is required for each material. Lower $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ with more gradual RESET and low SET failure rate was obtained for the forming-free HfO_2 devices at the O_2 IIP.

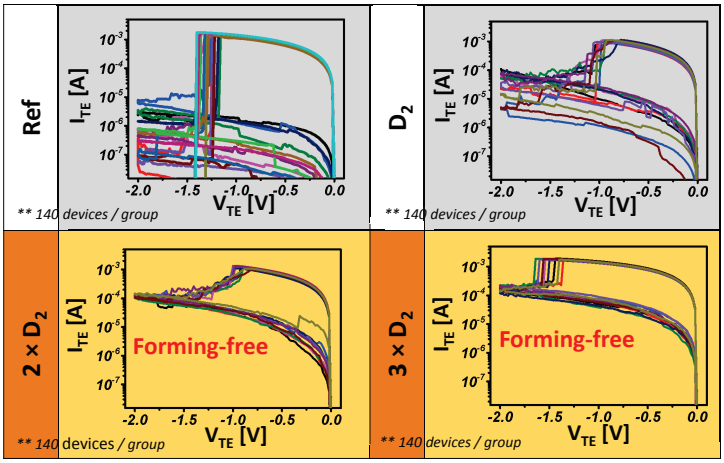


Figure 5.21: Changes of the 1st RESET I-V curves after forming depending on O_2 IIP dose for the HfO_2 ReRAMs at the $I_{CC} = 300\,\mu$A (at forming).

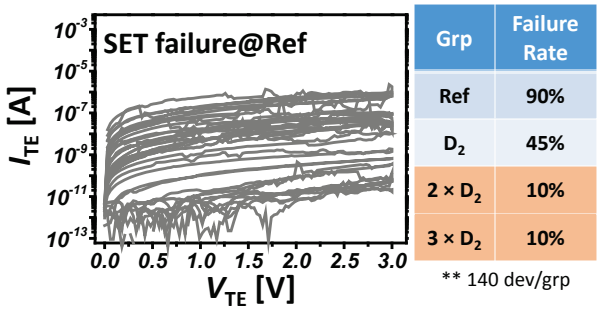


Figure 5.22: SET failures after the 1st hard-RESET for the reference device and comparison of SET failure rates between groups.

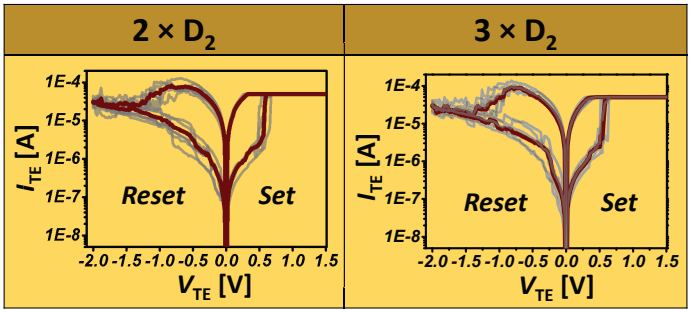


Figure 5.23: Stable I-V characteristics of the forming-free HfO_2 ReRAM devices for different O_2 IIP dose at the $I_{CC} = 50\,\mu A$.

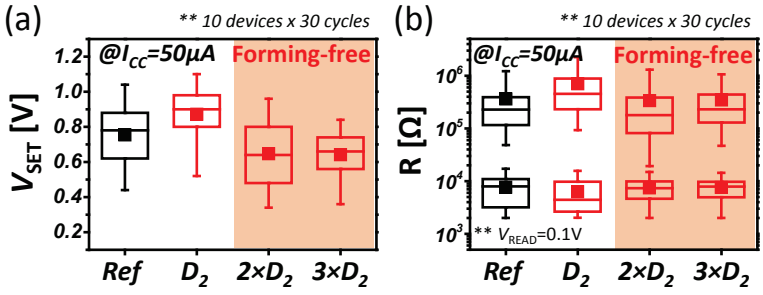


Figure 5.24: Comparable performance under $I_{CC} = 50\,\mu A$, $V_{RESET-STOP} = -2.0\,V$ in HfO_2 ReRAMs for (a) V_{SET} and (b) R_{OFF}/R_{ON}

5.3.6 Plasma enhanced ALD-HfO_2 ReRAM device: R_{OFF}/R_{ON} and V_{SET} at $I_{CC} = 50\,\mu A$

Stable switching cycles of the forming-free devices are shown in Fig. 5.23. A good memory window ($R_{OFF}/R_{ON} > 20$) at low I_{CC} of $50\,\mu A$ is observed from the forming-free devices in Fig. 5.24.

5.3.7 Physical effect of O_2 IIP

Ion bombardment with low kinetic energy has been used extensively in surface cleaning and surface analytical techniques and can produce a chemical composition change at the surface. For the metal oxides, it is well known that the ion bombardment can cause a preferential oxygen sputtering resulting in chemical reduction of oxide film. This preferential sputtering of oxides is explained in terms of the stability and decomposition of the various oxides at the spike temperature [97]. The metallic oxides such as Ta_2O_5, TiO_2, WO and Al_2O_3 used as switching layers in ReRAM devices also show the same reduction behaviors with the ion bombardment. The leakage current through the metallic oxide is expected to increase with higher reduction, and was indeed found to be dependent on the amount of bombarding ion current [98]. Using Ar^+ ion irradiation, TaO_x/Ta_2O_5 hetero-structure for ReRAMs has been realized. The TaO_x sub-oxide was formed on top of the Ta_2O_5 and the thickness of sub-oxide was controlled by the irradiation kinetic energy and irradiation time [99]. On the other hand, when bombarding with non-neutral oxygen ions, one could expect incorporation of extra oxygen. Thus, when oxygen ions were implanted into Ta metal layer, Ta_2O_5/TaO_x hetero-structure is created even without any thermal treatment implying a possible chemical interaction at room temperature [100].

In order to understand which effect prevails in our films, Fig. 5.9 compares the simulated depth profiles of the incorporated oxygen and of the atomic collisions as result of the O_2 IIP at $5 \times 10^{15}/cm^2$ dose into the Ta_2O_5 layer (film density = 7.65 g/cm^3). It can be observed that the implantation range is much deeper than the 7 nm-thick metal oxide film, with nearly no O incorporation close to the surface, while a high number of collisions is present at the surface of the layer. Therefore, the main impact of the O_2 IIP in our thin films is the reduction of the metal-oxide layer. Similar reduction effect is expected with implantation of other ions, however, heavier ions (such as Ar^+) might physically etch the metal oxide film. This reduction causes both the conduction increase and lowering of the V_{FORM}. The higher (double) dose required to obtain forming-free HfO_2 ReRAM compared to Ta_2O_5 ReRAM, can then be explained by the higher stability of HfO_2 film against the

reduction process, as explained above [97].

5.3.8 Forming-free with N_2 IIP

The O_2 IIP was effective method to make the ReRAM devices forming-free regardless of switching oxide (Ta_2O_5, HfO_2) and thin-film deposition method (PVD, ALD). The theoretical background for the forming-free results was explained with Mote-Carlo simulation of O_2 IIP in Fig. 5.9. Another experiment with different ion species was chosen to verify if our theoretical interpretation of IIP effect is still valid. Due to the similarity of size between oxygen and nitrogen, N_2 IIP was chosen for this experiment since the size of implanted ion can affect ion penetration depth and defect generation.
The N_2 IIP in the Ta_2O_5 ReRAM was applied with 2 separate doses, D_1 and D_2 ($D_2 = 5 \times D_1$) at fixed energy of 30 keV with EATON-Implanter. The used doses are $1.0 \times 10^{15}/cm^2$ (D_1), $5.0 \times 10^{15}/cm^2$ (D_2) respectively.

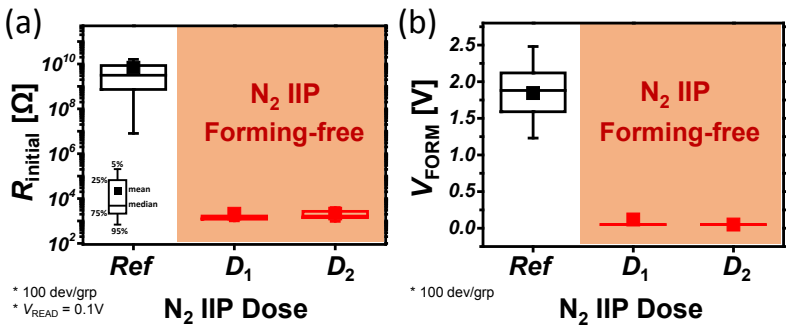


Figure 5.25: Dependence of (a) R_{initial} comparison and (b) V_{FORM} of the $Pt/Ta_2O_5/Ta/Pt$ on the N_2 implantation dose

The R_{initial} decreases as the N_2 IIP dose increases as shown in Fig. 5.25(a). In comparison with the reference device ($3\,G\Omega$), the R_{initial} of N_2 IIP devices is greatly reduced to $1.3\,k\Omega$ for both dose D_1 and dose D_2. The V_{FORM} is compared in Fig. 5.25(b). The forming-free conditions were obtained by both dose D_1 and dose D_2. Fig. 5.26(a) shows the comparison of 1st RESET current and the 1st RESET current decreases as the dose of N_2 IIP increases. Stable

1st switching curves (I-V) of the forming-free devices with dose D_2 are shown in Fig. 5.26(b).

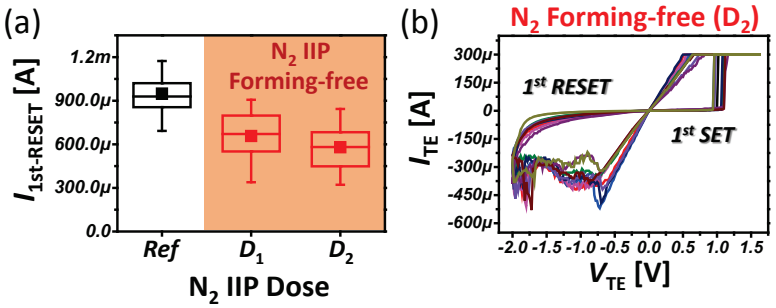


Figure 5.26: The reduced 1st RESET current with N_2 IIP (a) in bar plots with distribution, (b) in typical I-V curves of the 1st RESET and the 1st SET with $5.0 \times 10^{15}/\text{cm}^2$ (D_2).

5.3.9 Summary of this section

Forming-free Ta_2O_5 and HfO_2 nanoscaled ReRAM devices are obtained by a new versatile process of O_2 IIP and N_2 IIP. With material-specific optimized implantation dose, as-fabricated devices are initially in the ON state with a narrow R_{ON} distribution, and show the lower current overshoot than reference devices during the 1st RESET cycle. While avoiding the need for a high voltage forming step, the devices show similar resistive switching properties as reference devices without any degradation of electrical performance. For both Ta_2O_5 and HfO_2 forming-free ReRAMs, a high $R_{OFF}/R_{ON} > 20$ at the I_{CC} of 50 μA is observed. Excellent AC endurance of 10^6 cycles and good retention of 10^4 sec at 125 °C for forming-free Ta_2O_5 ReRAM is obtained. This newly developed method is of high importance for possible commercialization of ReRAM technology.

5.4 Conclusion of this chapter

In this chapter, how the process parameters such as Ta_2O_5 thickness, Ta-OE thickness, RTA in O_2 and ion implantation can impact the V_{FORM} and the

other electrical performance of ReRAM device has been studied. For the thickness effect of Ta_2O_5 switching layer, the V_{FORM} was reduced effectively with 3 nm-thick Ta_2O_5, however, the performance of R_{OFF}/R_{ON} ratio and the data retention at 125 °C became seriously degraded. For the thicker Ta-OE, the V_{FORM} was reduced with a limitation since the reduction of V_{FORM} became saturated at 13 nm-thick Ta-OE. There was no more reduction of V_{FORM} observed starting from above 13 nm-thick Ta-OE. The majority ($\sim 70\%$) of ReRAM devices with 600 °C RTA showed forming-free behaviors. However, 600 °C is too high for Back-End-Of-Line (BEOL) process, therefore it is not a practical option for CMOS application. Finally, we could realize the forming-free ReRAM devices (100%) regardless of switching oxide type (Ta_2O_5, HfO_2) and its deposition methods (PVD, ALD) with optimized O_2 IIP and N_2 IIP. And the forming-free ReRAM devices with the O_2 IIP showed comparable electrical performances in R_{OFF}/R_{ON} ratio, data retention and endurance.

Chapter 6

MOSFET-ReRAM Integration

Overshoot phenomena in ReRAM device is a major concern as it degrades the device characteristics. In this chapter, the ReRAM device is integrated with MOSFET device and the different characteristics of Ta_2O_5 based ReRAM in 1T-1R configuration are studied. The device parameters such as V_{FORM} , Non-Linearity (NL) and resistance ratio ($R_{\mathrm{OFF}}/R_{\mathrm{ON}}$) are analyzed at various I_{CC} levels for different device sizes and switching layer thicknesses.

6.1 Device Fabrication in 1T-1R

Ta_2O_5 based ReRAM devices have been integrated with n-channel MOSFETs fabricated in a 65-nm process technology. During the backend processing, a planarized BE of 40 nm-thick PVD TiN is defined. Afterwards, 7.0 nm- or 3.5 nm-thick (amorphous) Ta_2O_5 layer is deposited on top of TiN by reactive sputtering at room temperature under process gas mixture of Ar (23%) and oxygen (7%). RF power used is 116W with base chamber pressure of 2.3×10^{-2} mbar. Then, 10 nm-thick Ta and 25 nm-thick Pt are deposited on top of Ta_2O_5 layer. The TE is patterned with e-beam lithography and Reactive Ion Beam Etching process. In this work, the ReRAM device area ranges from 85×85 nm^2 to 135×135 nm^2 and long channel MOSFET devices (W/L = 1.0 μm/1.0 μm) are used to control the current. TEM cross-sectional view of integrated 1T-1R structure and the top-down SEM image on the 1T-1R structure with top contacts for V_{SL}, V_{GS} and V_{BL} are shown in Fig. 6.1(a) and Fig. 6.1(b). Fig. 6.1(c) shows the enhanced TEM cross-section image of

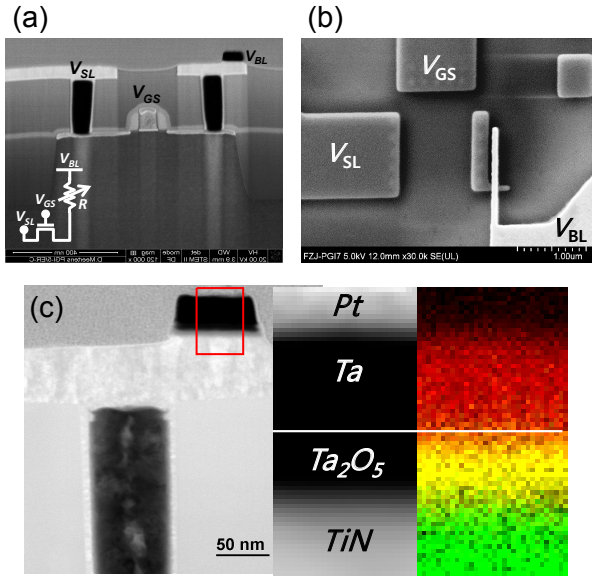


Figure 6.1: (a) Cross-sectional TEM image of ReRAM device in the 1T-1R configuration. (b) Top-down SEM view of the 1T-1R structure showing contacts for V_{SL}, V_{GS} and V_{BL}. (c) Enhanced TEM cross-section of the ReRAM device stacks (TiN/Ta_2O_5/Ta/Pt) and the device stack is confirmed with energy-dispersive X-ray (EDX) analysis.

Mode		Operation Range		
		V_{GS} (V)	V_{BL}(V)	V_{SL} (V)
DC	Forming	1.4	0.0~4.5	GND
	Reset	2.5	GND	0.0~1.5
	Set	1.0/1.2/1.4	0.0~1.5	GND
	Read	1.4	0.2	GND
AC	Reset	2.5	GND	2.0@1µs
	Read	1.4	0.1@100µs	GND

Figure 6.2: Operation conditions of Forming, Reset and Set process for DC, AC mode of the integrated TiN/Ta_2O_5/Ta/Pt ReRAM device in the 1T-1R configuration

ReRAM device stacks and its corresponding energy dispersive X-ray (EDX) from the red-boxed area.

The electrical characterization of the integrated 1T-1R device is performed using the Keithley 4200SCS parameter analyzer. The voltage is applied to either bit-line (V_{BL}) or source line (V_{SL}) with a constant voltage on the gate electrode (V_{GS}). The AC pulse mode is used to determine the transient I-V characteristics and estimate the NL of the ReRAM devices. The operating conditions of the 1T-1R device for write/read are explained in Fig. 6.2.

6.2 *I-V* Characteristics of ReRAM

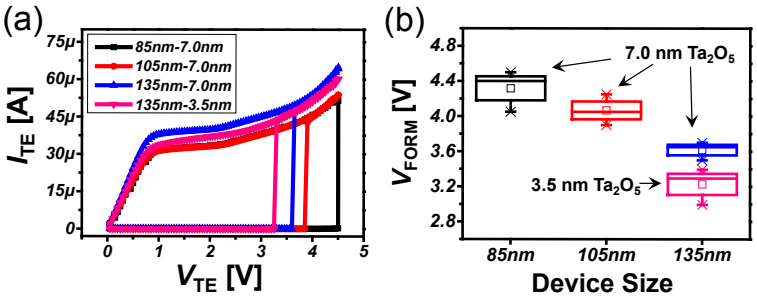


Figure 6.3: Dependence of the V_{FORM} on device area (85×85 nm^2, 105×105 nm^2, 135×135 nm^2) with different Ta_2O_5 thickness (3.5 nm vs. 7.0 nm), shown in (a) typical *I-V* curves and (b) statistical bar plots.

Fig. 6.3 shows the effect of ReRAM device dimensions and switching layer thicknesses on the V_{FORM}. For 7.0 nm-thick Ta_2O_5 device, the highest V_{FORM} of 4.3 V for the $85 \times 85\,\mathrm{nm}^2$ device area is observed, which decreases to 3.6 V for the 135×135 nm^2 device area. The V_{FORM} further decreases to 3.2 V for the thinner Ta_2O_5 (3.5 nm) with same device area [19]. Fig. 6.4(a) shows the *I-V* characteristics of integrated TiN/(7.0 nm) Ta_2O_5/Ta/Pt ReRAM in the 1T-1R configuration of $85 \times 85\,\mathrm{nm}^2$ device dimension for different I_{CC} levels. The channel resistance of the MOSFET at $V_{\mathrm{GS}} = 1.4$ V for Read was measured to be 4.1 $k\Omega$. The different I_{CC} levels in Fig. 6.4(a) have been categorized into low, medium and high. The low and medium I_{CC} levels correspond to 30 μA@ $V_{\mathrm{GS}} = 1.0$ V, and 60μA@ $V_{\mathrm{GS}} = 1.2$ V, whereas high I_{CC}

level is denoted by $90\mu A@V_{GS}=1.4\,V$. Fig. 6.4(b) shows the I-V characteristics of the Ta_2O_5 ReRAM device with extremely low I_{CC} level. The maximum switching current of $4.5\,\mu A$ (I_{RESET}) is observed in this case, while keeping the I_{CC} level to $3.0\,\mu$ A. The impact of I_{CC} levels on R_{OFF}, R_{ON} and the R_{OFF}/R_{ON} ratio is shown in Fig. 6.5(a) for 7.0 nm-thick Ta_2O_5 ($85\times85\,nm^2$)and in Fig. 6.5(b) for 3.5 nm-thick Ta_2O_5 ($135\times135\,nm^2$). The R_{OFF}, R_{ON} are measured at $V_{read}=0.2\,V$. The R_{ON} becomes lower as the I_{CC} level increases and the lowered R_{ON} improves the R_{OFF}/R_{ON} for both Ta_2O_5 thicknesses.

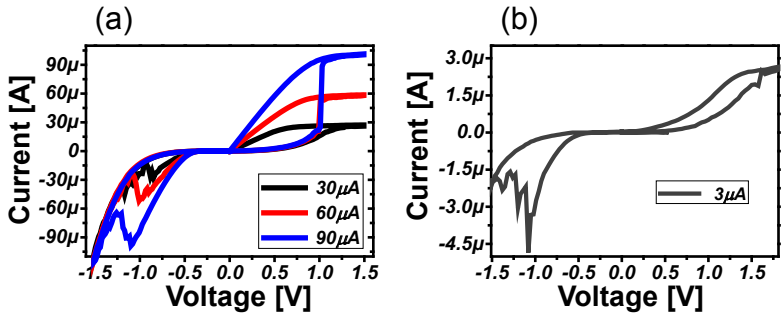


Figure 6.4: I-V characteristics of 7.0 nm-thick Ta_2O_5 ReRAM having the 85×85 nm^2 device area (a) for different I_{CC} levels (b) for extremely low I_{CC} $=3.0\,\mu A$.

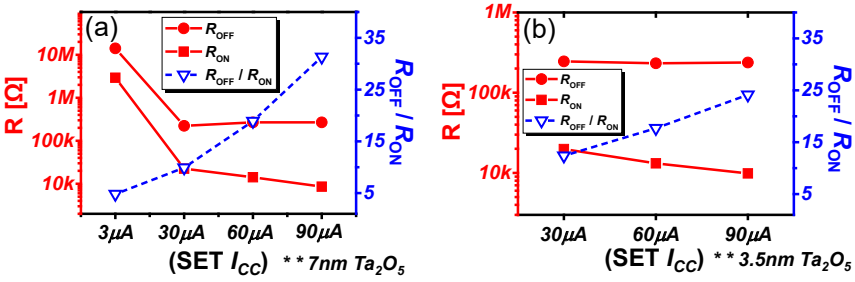


Figure 6.5: (a) Impact of the I_{CC} levels on the R_{OFF}, R_{ON}, and R_{OFF}/R_{ON} for 7 nm-thick Ta_2O_5 (85×85 nm^2). (b) Impact of the I_{CC} levels on the R_{OFF}, R_{ON}, and R_{OFF}/R_{ON} for 3.5 nm-thick Ta_2O_5 (135×135 nm^2)

6.3 AC Non-Linearity (AC-NL) Analysis

6.3.1 Definition of NL

The highest memory density could be obtained in the passive cross-point array with $4F^2$ configuration in ReRAM device and it results in a high sneak path current [101]. This leads to both WRITE and READ failure in the ReRAM memory. Generally, this problem can be solved by introducing strong non-linearity in the cell, e.g. by integrating the ReRAM device with a non-linear selector device such as diode [102] or MOSFET [19], however this trades off with density and impedes three dimensional (3D) ReRAM integration. An alternative solution is to build a ReRAM device with intrinsic non-linear *I-V* characteristics. The required Non-Linearity (NL) depends both on the array size and the addressing schemes [103]. Common electrical addressing schemes for the passive cross-point array operation are *V/2* and *V/3* [104],[105],[106]. The *V/2* scheme uses *V/2* bias condition for both unselected wordlines and bitlines while the *V/3* scheme adopts *V/3* bias for unselected wordlines and *2V/3* bias for unselected bitlines. Comparing these two methods, the *V/2* scheme offers low power consumption and simple WRITE/READ protocols [107] for the cross-point array. However, the scheme has unwanted sneak current flow through selected *V/2* cells in the passive array. A ratio of I_{RESET} at V_{RESET} to I_{RESET} at $V_{\mathrm{RESET}}/2$ is defined as write Non-Linearity, given by following equation [108]:

$$WRITE\ nonlinearity\ (NL) = \frac{I@V_{\mathrm{RESET}}}{I@½V_{\mathrm{RESET}}} .....(1)$$

Most publications calculate this NL from the DC *I-V* characteristics, however as pulse operation is more relevant for the application, here the NL is calculated based on the AC *I-V* characteristics with the V_{RESET} defined as the (minimum) pulse amplitude for which the full RESET occurs.

6.3.2 AC-NL Measurement

Fig. 6.6(a) shows the pulse reset characteristics of 85×85 nm^2 device area at the V_{RESET} and the $\frac{1}{2}$ V_{RESET} with 1.0 μs pulse width. A circle in blue is marked indicating the I_{RESET} peak taken for the AC NL analysis. Prior to the pulse reset process, the ReRAM device was toggled to SET at 30 μA@$V_{\mathrm{GS}} = 1.0$ V. The black lines are for the applied voltages, whereas the red lines correspond to the currents. The applied pulse amplitude (V_{SL}) for the V_{RESET} and $\frac{1}{2}$ V_{RESET} is 2.0 V and 1.0 V respectively. The I_{RESET} at the V_{RESET} is 72 μA while the I_{RESET} at the $\frac{1}{2}V_{\mathrm{RESET}}$ is 28 μA. Therefore, the corresponding AC-NL is 2.6. Prior to the V_{RESET} pulse, the device resistance

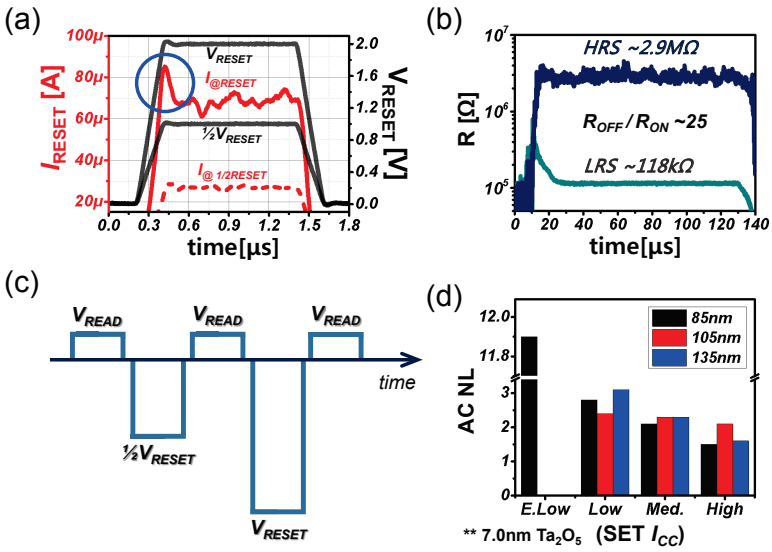


Figure 6.6: All figures are based on 7 nm-thick Ta_2O_5 ReRAM. (a) Pulse reset characteristics with 85×85 nm^2 device area at the V_{RESET} and $\frac{1}{2}V_{\mathrm{RESET}}$ with 1.0 μs pulse width after SET application based on Low I_{CC} group. (b) $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ measured for the same device before and after the V_{RESET} application during the NL analysis. (c) The sequence of applied pulses for AC-NL measurement. (d) Dependence of the AC-NL on the I_{CC} levels including all device sizes.

was 118 $k\Omega$ (R_{ON}), whereas after the V_{RESET} pulse, the device resistance changes to 2.9 $M\Omega$ (R_{OFF}). This is verified at the $V_{read} = 0.1$ V with 100 μs pulse width. The R_{OFF}/R_{ON} in this case was estimated to be 25, as shown in Fig. 6.6(b). The Fig. 6.6(c) shows the sequence of applied pulses for AC-NL measurement. The 1st V_{read} gathers an $R_{initial}$ state and the 2nd V_{read} verifies if the $R_{initial}$ state changes with the $\frac{1}{2}V_{RESET}$ or not. No resistance change is expected with $\frac{1}{2}V_{RESET}$. The changed resistance state is verified with the 3rd V_{read}. The AC-NL values shown in Fig. 6.6(d) are extracted using the equation (1) and they are average values based on multiple data points from each device area and each SET I_{CC} . The NL decreases with higher SET I_{CC} for all device sizes. However, the NLs do not show any trend with device sizes at given I_{CC} . The maximum AC-NL of 12 was observed at the I_{CC} = 3.0 μA. This is attributed to the fact that lower I_{CC} generates a thinner filament in the ReRAM device, which constraints the current flow and generally changes the conduction mechanism from linear (metallic, Ohmic) to non-linear (semiconducting, hopping, tunneling or quantum confined) [109]. Due to this conduction mechanism change, the abrupt changes for R_{ON} and R_{OFF} at Extremely Low I_{CC} group are observed in Fig. 6.5(a).

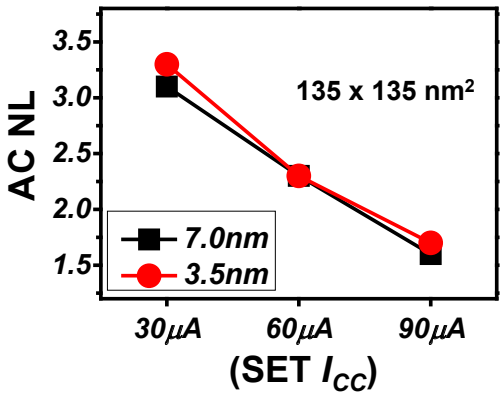


Figure 6.7: Dependence of the AC-NL on the SET I_{CC} levels for 3.5 nm-thick and 7.0 nm-thick Ta_2O_5 ReRAM devices.

Further, the impact of the switching layer thickness (3.5 nm-thick and 7.0 nm-thick Ta_2O_5) on the NL is investigated with different I_{CC} levels. The AC-NL does not show any dependence on the switching layer thickness as shown in

the Fig. 6.7 and the similar trend (as shown in Fig. 6.6(d)) of the AC-NL is observed with increase of NL at lower I_{CC} levels. From this analysis (Fig. 6.5, Fig. 6.6), it can be concluded that the NL and the R_{OFF}/R_{ON} are the competing parameters, which are affected by the I_{CC} levels in the opposite manner i.e. one increases and another decreases. It is therefore highly required to select the right I_{CC} level of the ReRAM device so that required NL and R_{OFF}/R_{ON} can be achieved for the desired memory operations.

6.4 Conclusion of this chapter

I_{CC} plays an important role on resistive-switching behavior of ReRAM devices, especially for R_{ON} and I_{RESET} (the peak current duing RESET). In the passive 1R array structure, it is difficult to control I_{CC} precisely due to current overshoot from parasitic capacitance [96, 110]. Therefore, based on 1T-1R configuration, the overshoot can be suppressed efficiently [95, 111] making the stable switching at low current regime.

The NL in the 1T-1R Ta_2O_5 ReRAM improves at lower I_{CC} level regardless of the device area while the R_{OFF}/R_{ON} degrades. This is attributed to the fact that higher I_{CC} generates a stronger filament in the ReRAM device and the stronger filament deteriorates the NL value. For the $I_{CC} = 3.0\,\mu$A, the highest NL value of 12 for the AC mode is achieved. On the contrary, the R_{OFF}/R_{ON} degrades with lower I_{CC} level as the R_{ON} is directly affected with the I_{CC} level. The switching layer thickness of the ReRAM device does not show an impact on the the R_{OFF}/R_{ON} ratio and the NL value.

Chapter 7

Resistor logic: Ternary Arithmetic

Recently, the capability of ReRAMs to implement Boolean logic functionality based on 2 state resistance levels gained wide interest [112]. Here, in this chapter, we enable the realization of an intrinsic modular arithmetic using a ternary number system report based on 7-states resistance levels of Ta_2O_5 ReRAM device. Modular arithmetic, a fundamental system for operating on numbers within the limit of a modulus, is known to mathematicians since the days of Euclid and finds applications in diverse areas ranging from e-commerce to musical notations.

7.1 Concept of Modular Arithmetic

In this work, a rigorous mathematical framework of modular arithmetic was developed by Carl Friedrich Gauss [10] by defining a congruence relation between integers. Two integers, a and b are said to be congruent modulo n, when their difference (a-b) is divisible by n. In this case, n is known to be the modulus of this relation.

$$a \equiv b \pmod{n} \qquad (1)$$

The properties of integer numbers for a specific modulus, spanning addition,

subtraction and multiplication are written as following.

Given $a_1 \equiv b_1 \pmod{n}$, and $a_2 \equiv b_2 \pmod{n}$, we have

$$\begin{aligned} a_1 + a_2 &\equiv (b_1 + b_2) \pmod{n} \\ a_1 - a_2 &\equiv (b_1 - b_2) \pmod{n} \\ a_1\, a_2 &\equiv (b_1\, b_2) \end{aligned} \tag{2}$$

Apart from applications in mathematics, modular arithmetic plays a fundamental role in modern computer arithmetic. Here, a ring of integers modulo 2 is termed as a Boolean ring and every Boolean ring gives rise to Boolean algebra, where the ring multiplication is conjunction operator ($\wedge$) and the ring addition is exclusive disjunction operator ($\vee$). Furthermore, the idea of secure and fault-tolerant data communication relies on the principles of public-key cryptography and error-correcting codes, respectively. Both of these fields require efficient implementations of modular arithmetic.

Modular arithmetic is also useful for reducing the complexity of standard arithmetic circuits [7, 113] and is essential for building the residue numeral systems (RNS). RNS representation allows overflow-free addition, subtraction and multiplication, thereby enabling high degree of parallelism.

State-of-the-art modular arithmetic circuits in CMOS technology are implemented using two-state Boolean arithmetic operations, which follows directly from the two-level switching algebra introduced by Shannon [8]. Memristive devices were suggested to replace register files in conventional signed-digit adders [9] or to be used in conjunction with complex quantization circuits [114]. This chapter reports the first implementation of modular arithmetic using multi-state ReRAM devices, which is fully crossbar array compatible in conjunction with a selector device. Whereas most previous memristive circuit studies are based on over simplistic memristor models [115], we use real memristive devices fabricated in word structures to verify the proposed functionality. It should also be noted that we perceive no theoretical limit in scaling the number of states for memristive devices,

thereby, opening a new research direction on multi-state storage and computing devices.

7.2 Device Fabrication

A 30 nm-thick Pt BE is patterned on top of 430 nm-thick thermally grown SiO_2 layer from silicon wafer and 7 nm-thick Ta_2O_5 is deposited by reactive sputtering under process gas mixture of Ar (77%) and oxygen (23%) with 236W RF power at the chamber pressure of 2.3×10^{-2} mbar.

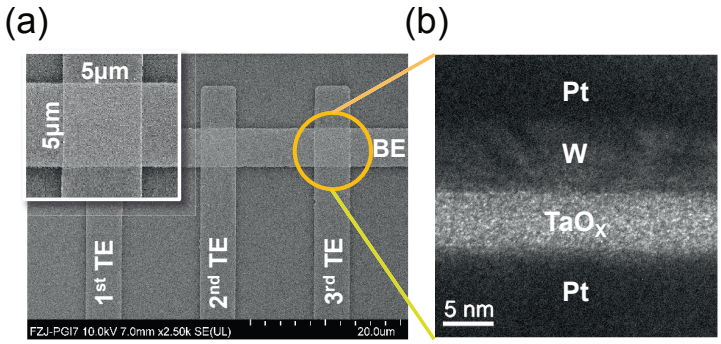


Figure 7.1: Resistive switching device structures (a) Scanning electron microscopy image of 1×3 array with the inset showing $5 \times 5\mu m^2$ single device (b) Transmission electron microscopy image of single device cross-section, 7-nm-thick Ta_2O_5 switching layer and 13-nm-thick tungsten ohmic electrode.

Without breaking the vacuum, 13 nm-thick W-OE and 25 nm-thick Pt are deposited by RF and DC sputtering, respectively. All depositions are performed at room temperature. Next, TE is etched down with Reactive Ion Beam Etching (RIBE). $5 \times 5\,\mu m^2$ Pt/W/Ta_2O_5/Pt cross-point devices arranged in word structures are used to realize the three Trit (**tr**inary digi**t**) modular addition as shown in Fig. 7.1(a). A TEM image of device stack from is shown in Fig. 7.1(b) confirming the amorphous nature of the Ta_2O_5 layer and its thickness.

7.3 Basic ReRAM Funcitonality

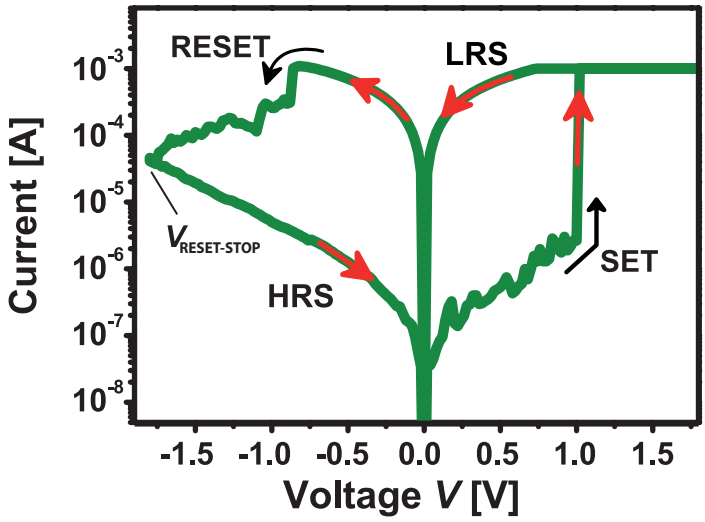


Figure 7.2: Typical bipolar operation of SET-RESET switching in DC sweep mode for a single ReRAM ($5 \times 5\mu m^2$) device within the 1×3 array.

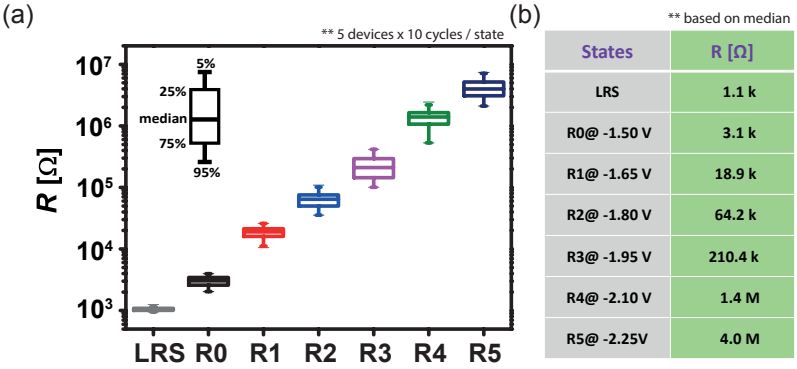


Figure 7.3: Resistance distribution (a) Pulses of 200 ns and pulse height in the range of -1.5 V to -2.25 V (0.15 V steps) enable highly accurate resistive state control. (b) Median values of the final resistance levels.

The typical *I-V* characteristic of this device is shown in Fig. 7.2. During RESET process, the maximum applied voltage, $|V_{\mathrm{RESET-STOP}}|$, defines the final resistive state (1.8 V in Fig. 7.2). This feature is also present in pulse mode, thus can be used in memory and logic operations for controlling the multi-level states. Fig. 7.3(a) shows the statistical data of low resistance state (LRS) and six multi-level resistive states, which are obtained for 200 ns pulses in the range of $V_{\mathrm{RESET-STOP}}$ = -1.5 V to -2.2 V. The distribution is very tight, highlighting the excellent switching properties of this device. In Fig. 7.3(b), the median value for each of the resistive state R0 to R5 is given. For the proposed arithmetic operation, the input operands are applied to the TE and BE electrode, respectively. To enable an equidistant voltage stepping, we use a predefined OFFSET voltage (V_{OFFSET}) for each pulse. The operand voltages are V_{op}= 0.00 V to 0.75 V with increment of 0.15 V. The actual pulse applied at the bottom electrode is therefore $V_{\mathrm{BE}} = V_{\mathrm{OFFSET}} + V_{\mathrm{op1}}$ and V_{TE} = -(V_{OFFSET} + V_{op2}) for the top electrode. Thus, the overall potential difference is $V_{\mathrm{RESET-STOP}} = V_{\mathrm{TE}}$ - V_{BE} = -(2V_{OFFSET} + V_{op1} + V_{op2}). Since the overall device voltage is always negative, a logic operation corresponds to a RESET pulse whose amplitude depends on the actual operands.

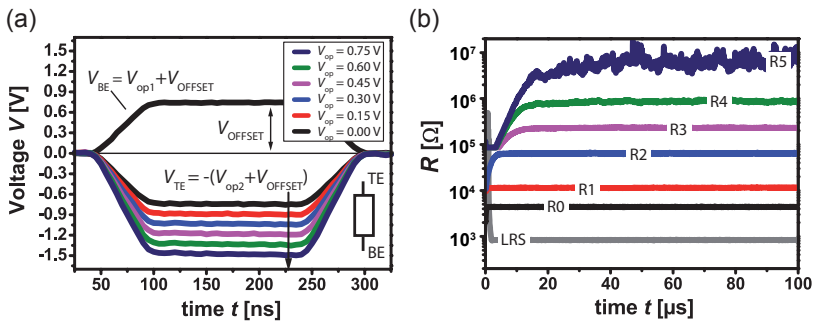


Figure 7.4: Basic logic functionality (a) The logic operands p and q are applied to TE and BE, respectively. An OFFSET voltage (V_{OFFSET}) is used to enable an equal stepping of operand voltages. In this example, $V_{\mathrm{op1}} = 0.0$ V holds while V_{op2} is varied from 0.0 V to 0.75 V. (b) Depending on the pulse height, R0...R5 are written to the device. Here, a read-out voltage of 0.1 V was used to show the actual resistance states.

To show the multi-level pulse operation mode, we set V_{BE} = 0.75 V and vary V_{TE} from -0.75 V to -1.5 V (Fig. 7.4(a)). The resulting resistances are depicted in Fig. 7.4(b). Depending on the overall device voltage ($V_{\mathrm{RESET-STOP}}$ = -1.5 V to -2.25 V) six different resistance states (R0, R1, R2, R3, R4 and R5) are accessible (Fig. 7.4(b)). Note that three resistive states would be sufficient to represent a ternary numeral system (Trit). This multi-level device property is used for the modular arithmetic operation. To enable highly reproducible RESET operation, we always apply a DC SET operation before each pulsed RESET operation. Note that also nanosecond pulsed SET operations are feasible, but not applied in this work. Details on the pulsed SET operation can be found in Fig. 7.5 of pulsed SET operation.

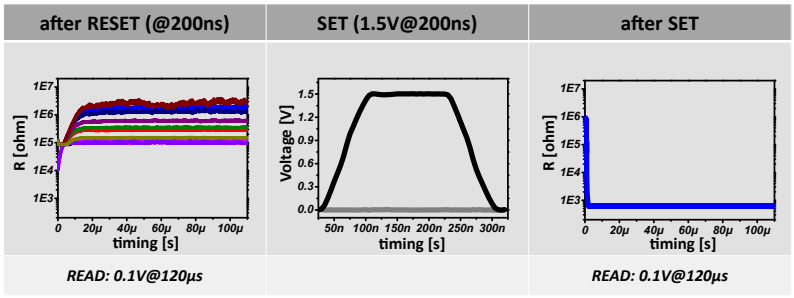


Figure 7.5: Feasibility of pulsed SET operation. After the RESET operation, the ReRAM device is in a multi-level state (left). A SET pulse of 1.5 V (middle) sets the device to the LRS (right).

7.4 Development of modular arithmetic working principle

The new developed algorithm calculates the carries and sums directly in the ReRAM devices, which store the results until they are read out.

Initially, all the devices in a wordline are initialized, i.e. written to the LRS. Starting from this state the sum bit of significance 0 (s_0) can be directly calculated in the device of significance 0 while the other devices are

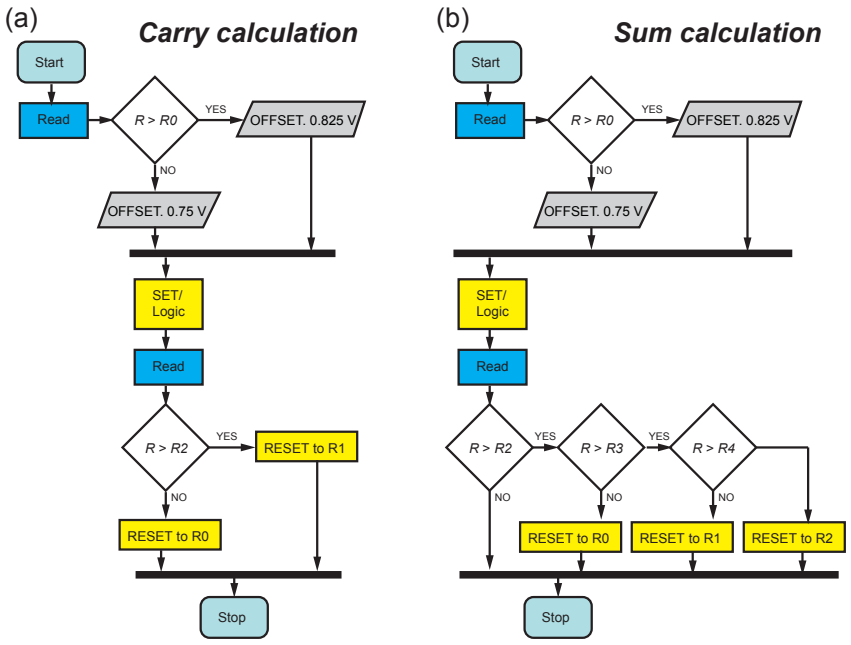


Figure 7.6: State machine (a) Algorithm for carry calculation. First, the input carry is read and OFFSET is adjusted correspondingly. Next, the logic operation is conducted and high resistive states > R2 are mapped to R1 otherwise to R0. (b) Algorithm for sum calculation. The OFFSET evaluation and logic signal application is the same as for carry. The mapping is as follows: R3 → R0, R4 → R1 and R5 → R2. Start and stop of the algorithm are marked by light blue color, Read by blue color, and logic and RESET steps by yellow color.

calculating the first output carry c_1. The actual sum or carry calculating devices are shifted for each significance one device to the left.

In general, for the carry algorithm (Fig. 7.6(a)), first the device state of the actual device is read, to check whether the input carry c_{in} is 0 or 1. In case of 1, V_{OFFSET} is set to 0.875 V whereas in case of 0, the OFFSET remains V_{OFFSET} = 0.75 V. Next, the logic operation is conducted after a SET operation using the evaluated OFFSET. We apply V_{TE} = -(V_{OFFSET} + V_{op1}) to the top electrode and V_{BE} = V_{OFFSET} + V_{op2} to the bottom electrode. Finally, the resistive state of the device is read and evaluated. To enable a

proper modulus operation the ReRAM device has to provide 2n states for an n-ary number system. The background is that in a n-ary number system the operands at each specific significance are in the range of 0...n-1, i.e., the sum of two operands is at most 2n-1. Since, an input carry of 1 from may also occur, the totally required number of states per device is 2n. Thus, for a ternary number system six states (R0...R5) are required. If the state is R $\leq$ R2, the output carry c_{out} is 0 and R0 is written back. For R > R2, the device is written to R1, i.e. $c_{out} = 1$. Note that prior to the write back operation, the SET operation is conducted to enable a highly controlled R1 state. Based on the input carry, the final sum can be calculated (Fig. 7.6b). As for the carry calculation, the required level of the V_{OFFSET} (either 0.75 V or 0.875 V) is first evaluated. Next, the operand voltages V_{TE} = -(V_{OFFSET} + V_{op1}) and V_{BE} = V_{OFFSET} + V_{op2} are applied after the SET operation. Based on a final readout, the mapping R3 $\rightarrow$ R0, R4 $\rightarrow$ R1 and R5 $\rightarrow$ R2 has to be conducted to complete the modulo sum operation. The corresponding write back operation is done subsequently after the SET operation. Since the signals which are applied to the TE are the same in both algorithm, these can be conducted in parallel on devices of different significance. Thus the cycle count can be kept low.

7.5 Proof-of-concept

For the proof-of-concept measurement, a two Trit modular addition is selected, adding the ternary numbers $\mathbf{p} = p_1p_0$ and $\mathbf{q} = q_1q_0$. Since the sum output $\mathbf{z} = z_1z_2z_3$ needs three Trit digits, three ReRAM devices are required for this operation and initialized to LRS firstly. The addition is performed in a word-line structure (cf. Fig. 7.1(a)). For the exemplary addition, operand 1 is $\mathbf{p}$ = 21 (= 7) and operand 2 is $\mathbf{q}$ = 22 (= 8). Note that input 0 corresponds to V_{op}= 0.00 V, input 1 corresponds to V_{op}= 0.15 V and input 2 corresponds to V_{op}= 0.30 V, using the earlier described incremental stepping of 0.15 V. In Fig. 7.7(a-c), the sequentially obtained resistive states are shown. The arrows mark the order of steps without showing the in between SET-steps. The algorithm described in Fig. 7.6 realizes the following

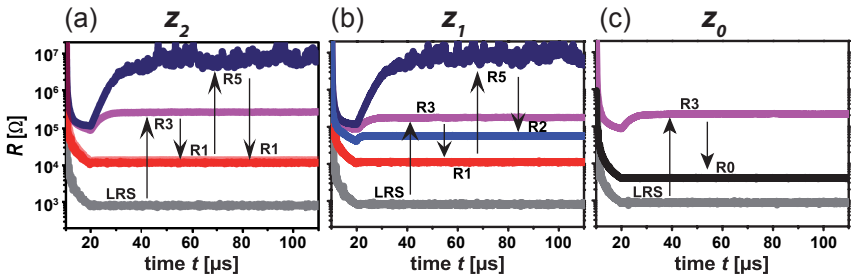


Figure 7.7: Proof of concept measurement. This example is for p = 21($2 \cdot 3 + 1 \cdot 1$ = 7) and q = 22($2 \cdot 3 + 2 \cdot 1$ = 8). (a) The sequence of resistive states in ReRAM device z_2, (b) ReRAM device z_1 and (c)ReRAM device z_0. The final values are: z_2 = R1, z_1 = R2 and z_0 = R0. This corresponds to $1 \cdot 9 + 2 \cdot 3 + 0 \cdot 1 = 15$. Numbers and arrows indicate the state changes.

mathematical modulo sum operation. In device z_0, the sum operation is conducted directly:

- z_0 = (1+2) rem 3 = 0 (s_0)

Note that the function rem returns the remainder. Starting from LRS, the device is reset ($p_0 = 1 => V_{TE}$ = -0.9 V and $q_0 = 2 => V_{BE}$ = 1.05 V, i.e. -1.95 V). According to Fig. 7.3(b), this voltage leads to state R3, as can be also seen in Fig. 7.7(c) directly. According to the sum algorithm (Fig. 7.6(b)), R3 is finally mapped to R0, see Fig. 7.7(c).

In device z_1, first the carry operation is conducted:

- z_1 = (1+2) div 3 = 1 ($c_1 = 1$)

The function 'div' returns the floor quotient. Starting from LRS, the device is toggled to R3 state by applying p_0 and q_0 to calculate the carry c_1. According to the carry algorithm (Fig. 7.6(a)), R3 is then mapped to R1, see Fig. 7.7(b).

Next, the second cell sum Trit is obtained by the following operation:

- $z_1 = (2+2+c_1)$ rem $3 = 2$ (s_1)

Since $c_1 = 1$ holds the $V_{\mathrm{OFFSET}} = 0.875$ V is applied, and the accessed state is R5. According to the sum algorithm (Fig. 7.6(b)), R5 is then mapped to R2, see Fig. 7.7(b).

For cell z2 (Fig. 7.7(a), again the carry operation is conducted first:

- $z_2 = (1+2)$ div $3 = 1$ ($c_1 = 1$)

Starting from LRS, R1 state is accessed via R3.

Since we consider a two Trit addition, the final sum bit equals the carry c_2:

- $z_2 = (2+2+c_1)$ div $3 = 1$ ($c_2 = s_2 = 1$)

According to the carry algorithm (Fig. 7.6(a)), R5 is then mapped to R1, see Fig. 7.7(c).

The final sum is stored directly in memory:

- Sum $\mathbf{z} = z_2\ z_1\ z_0 = 120$ (= 15)

7.6 Schematics of Operation and Truth Table

In Fig. 7.8, the schematics of applied operation voltages and corresponding states are depicted. The first line shows the voltages at the common BE acting as a wordline (WL). The second, fourth and sixth lines show the voltages applied to the three separate top electrodes ($V_{\mathrm{TE2}}, V_{\mathrm{TE1}}, V_{\mathrm{TE0}}$) acting as bitlines (BL) while the third, fifth and seventh lines represent the resistance states ($R_{\mathrm{TE2}}, R_{\mathrm{TE1}}, R_{\mathrm{TE0}}$) at each BL. The three background colors are used. The gray shows the LRS after SET. The yellow depicts the logic implementations

and the blue shows the corresponding states after the logic implementation. Overall twelve steps are presented. Step 1-2 show the initialized LRS and logic implementation of carry. Step 3-4 depict the corresponding resistance states with the carry implementation and the LRS after SET. Step 5-6 show

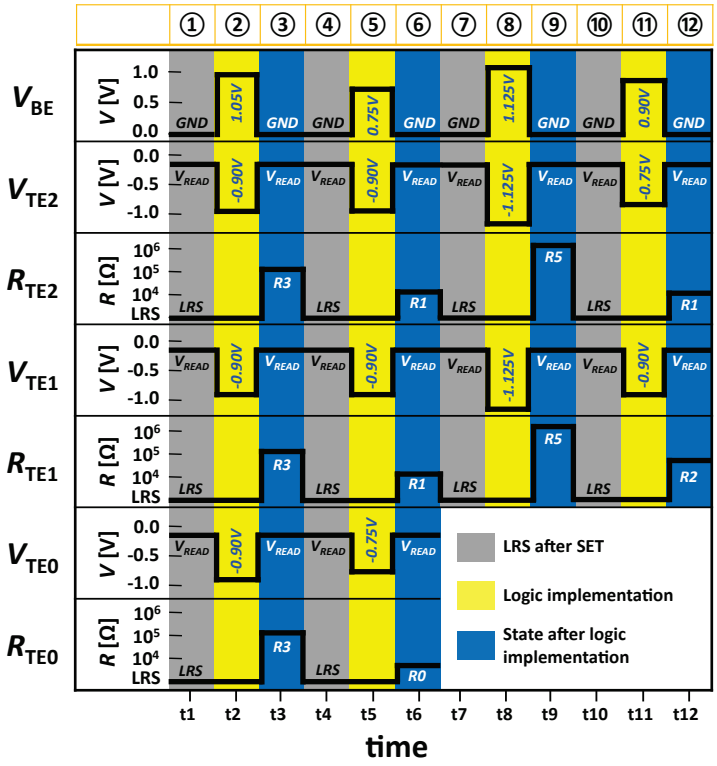


Figure 7.8: Schematics of operation. Schematics of operation for applied voltages (V_{TE}, V_{BE}) are shown. The gray shows the LRS after SET. The yellow depicts the logic implementations and the blue shows the corresponding states after the logic implementation. Step 1 is the LRS after initialization and Step 2 is carry logic implementation. Step 3 is the resistance states based on Step 2. Step 4 is the LRS after SET and Step 5 implements the logics. Step 6 is the corresponding resistance states and Step 7 is the LRS after SET. Step 8 is the logic implementation with adjusted OFFSET and Step 9 is the corresponding resistance states. Step 10 is the LRS after SET. Step 11 is the logic implementation and Step 12 is the corresponding resistance states.

logic implementations and the corresponding states. The state is set to LRS in Step 7. The logic is implemented with adjusted OFFSEET in Step 8 and the corresponding states are shown in Step 9. The LRS after SET is shown in Step 10. Step 11-12 show the logic implementations and the corresponding resistance states. The states ($R_{\mathrm{TE2}}, R_{\mathrm{TE1}}, R_{\mathrm{TE0}}$) shown in Step 12 and Step 6 depict the final sum stored in memory (Sum z = z2 z1 z0 = 120). The details of the applied voltage steps are given in supplementary Fig. S1, S2, S3. A truth table for the overall state definition (R0 - R5) is shown in the Fig. 7.9. Each combination of p (TE) and q (BE) sets the corresponding state with and without the adjustment of OFFSET.

0.4cm

q \ p	0	1	2
0	R0	R1	R2
	R1	R2	R3
1	R1	R2	R3
	R2	R3	R4
2	R2	R3	R4
	R3	R4	R5

without adjustment of OFFSET

with adjustment of OFFSET

Figure 7.9: Truth table for state definition. Truth table of p and q to realize each corresponding state with and without the OFFSET adjustment.

7.7 Discussion

We have demonstrated a ternary number system implementation, using multi-states Tantalum Oxide devices in word structures. Depending on the available number of resistive states, higher order number systems can also be implemented in the same way. For n-ary systems, we would need 2n resistive states, hence further progress in ReRAM memory technology will directly enable arithmetic operations using higher radix number systems.

On the other hand, the choice of radix for a number representation can be motivated from the perspective of underlying implementation as well as the

analysis of radix economy. A quantifiable measure of radix economy proposed in [116] is as following:

$$E(b,N) = b \cdot [\log_b(N) + 1],$$

Where, b is the radix and N is the number to be represented. This metric yields E as the most economical real-valued radix. It also turns out that the radix value of 3 (ternary) is more economical compared to binary. We argue that the above measure does not take the growth of the implementation media into account. For several device technologies, the area requirement grows linearly with the radix size and make the radix implementation very tough. However, in this is not true for multistate memristive devices such as the $Pt/Ta_2O_5/W/Pt$ ReRAM, since the implementable radix size depends on the number of resistance states. Considering, a k-state device can be realized at the same cost of a two-state device, a more appropriate metric would be

$$E(b,N) = [\tfrac{b}{k}] \cdot [\log_b(N) + 1]$$

Compared to binary arithmetic, an n-ary number representation reduces the space complexity in a logarithmic ratio. Given comparable performance for the base devices, the gain in arithmetic circuits, such as, integer addition is also expected to be in logarithmic scale. However, the actual gain will be somehow smaller due to need for better sense amplifiers and more control circuitry.

The presented approach is not limited to a specific multistate ReRAM device, but would work for any memristive device offering multiple resistance levels induced by different RESET voltages $V_{\mathrm{RESET-STOP}}$. The proposed algorithm could further be simplified by avoiding in between SET operations, however this requires ultra-low variance ReRAM devices. For the considered ReRAM device only RESET pulses were allowed as logic inputs. Appropriate SET pulses enabling step-by-step decrease of the resistance could be used to implement also subtraction within the same device similar to the here shown addition operation.

The presented approach is compatible to the passive crossbar array

configuration, by integrating a selector device to each Ta_2O_5 junction. The implementation of the arithmetic functionality within the resistive memory device using the available multi-resistance levels is a highly attractive option for future functionality enhanced hybrid CMOS/ReRAM chips. This approach enables a reduction of cycle count compared to Boolean logic based ReRAM approaches [117–120]. For example, a recently proposed cipher application could be decisively improved using multi-level ReRAMs [121], enabling efficient in-hardware encryption and decryption for future smart devices. In summary, low-variance multi-level ReRAM could play a key role for implementation of public-key cryptography and error-correcting codes in smart devices.

7.8 Conclusion of this chapter

$Pt/Ta_2O_5/W/Pt$ devices enable highly reliable multi states, which can be accessed reproducibly by pulses of specific height, starting from a defined LRS. By using word and bit lines as inputs for pulses, the resistive multi-levels can be used to store and calculate in-memory logic operations. To avoid an overflow in individual devices, a modulus arithmetic is implemented, assuring the device to be always in a valid 0, 1, 2 (Trit) state. By using a ternary number system, the amount of devices and cycles can be reduced significantly. In contrast to two-state devices, multistate devices provide better radix economy with the option for further scaling. Therefore, establishing multi-state ReRAM for non-volatile memory opens the door to novel storage and in-memory computer arithmetic options.

7.9 Supplementary

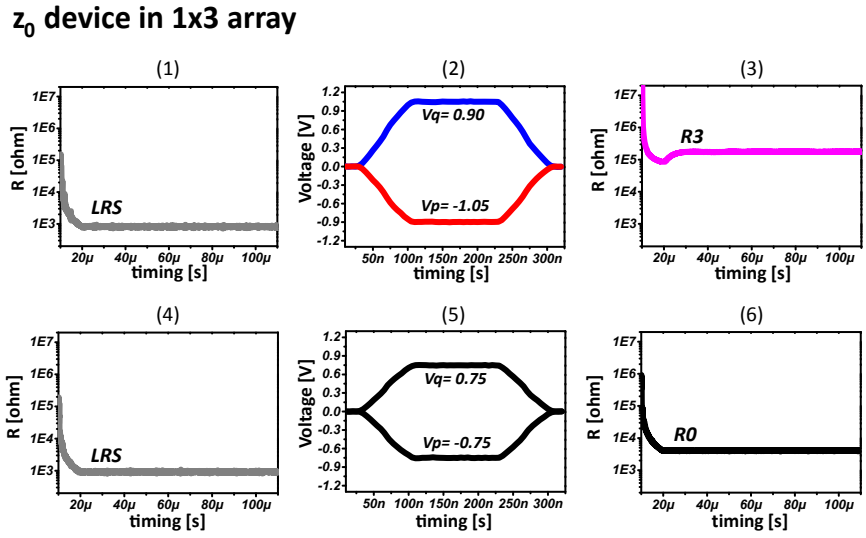


Figure S1: Sum calculation in z_0 device in 1×3 array by step-by-step (1) Initialization: SET to LRS. (2) Sum calculation. (3) State is R3 $\rightarrow$ Mapping to R0 required. (4) LRS after SET. (5) Write to R0. (6) Final state R0. Color code for voltages: see Fig. 7.4(a). Color code for resistances: see Fig. 7.4(b).

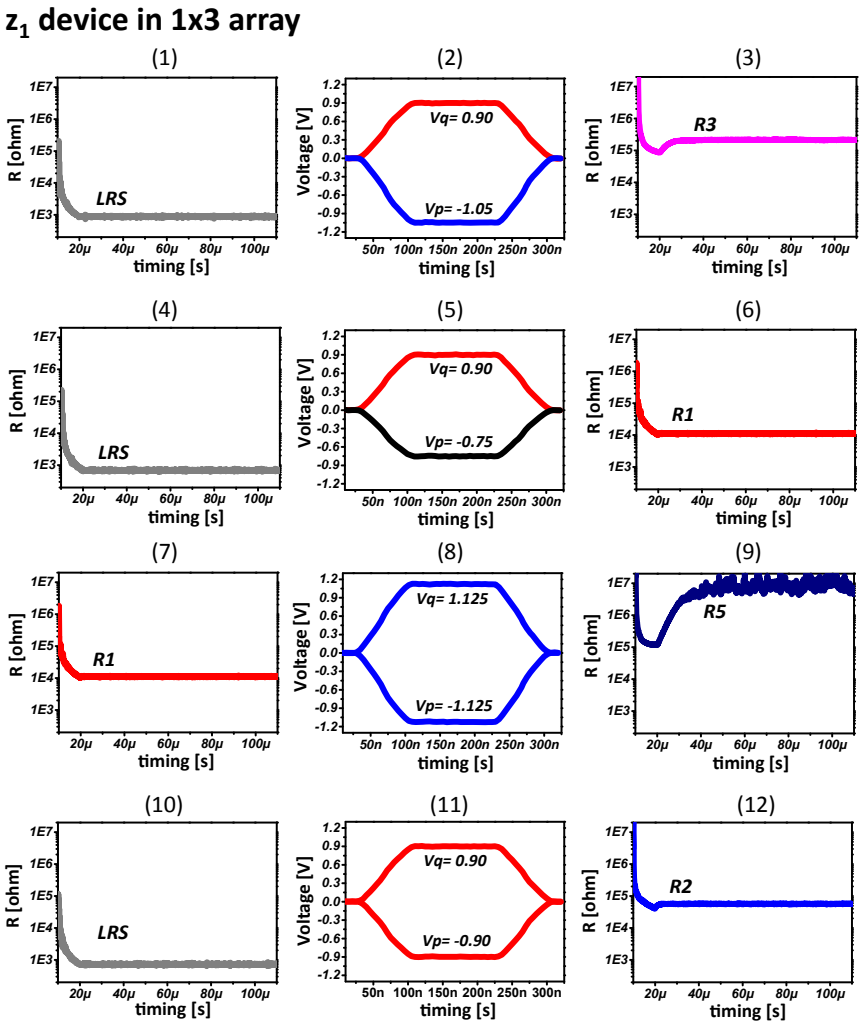


Figure S2: Sum calculation in z_1 step-by-step. (1) Initialization: SET to LRS. (2) Carry calculation. (3) State is R3 → Mapping to R1 required. (4) LRS after SET. (5) Write to R1. (6,7) State is R1. Note: Set to LRS is performed after this step. (8) Sum calculation. (9) State is R5 → Mapping to R2 required. (10) LRS after SET. (11) Write R2. (12) Final state R2. Color code for voltages: see Fig. 7.4(a). Color code for resistances: see Fig. 7.4(b).

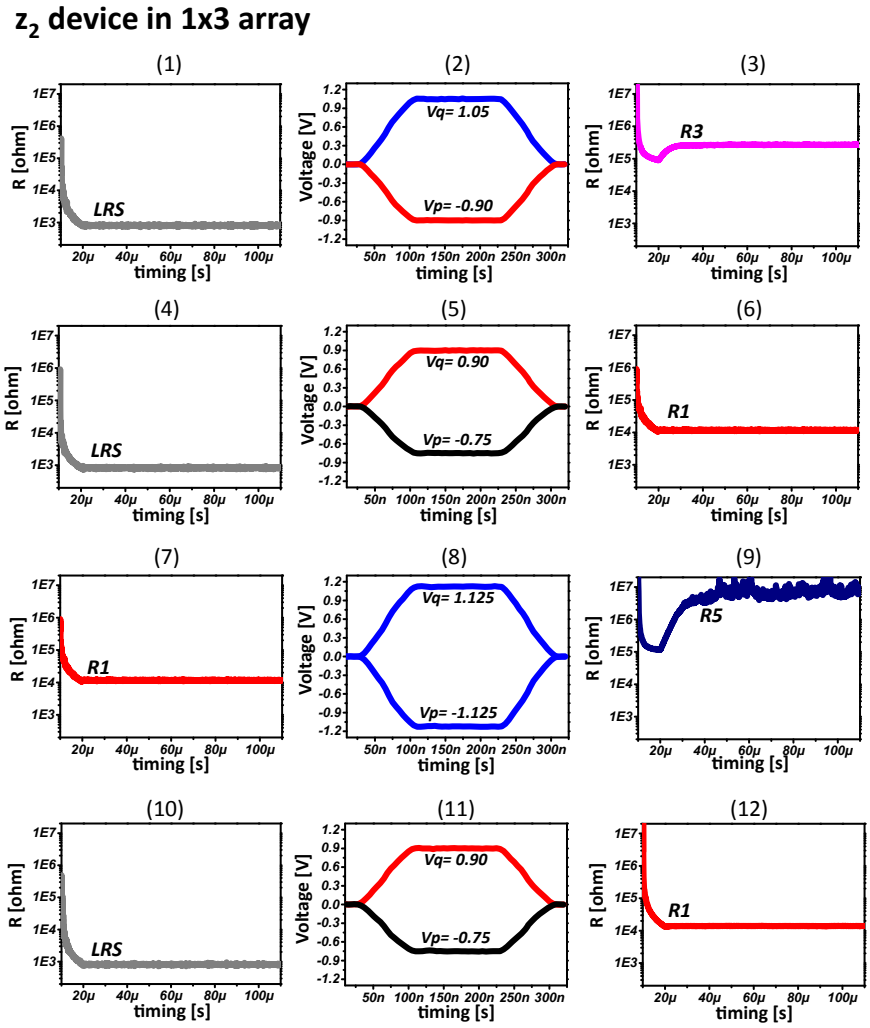


Figure S3: Sum calculation in z_2 step-by-step. (1) Initialization: SET to LRS. (2) Carry calculation. (3) State is R3 → Mapping to R1 required. (4) LRS after SET. (5) Write to R1. (6,7) State is R1. Note: Set to LRS is performed after this step. (8) Carry calculation. (9) State is R5 → Mapping to R1 required. (10) LRS after SET. (11) Write R1. (12) Final state R1. Color code for voltages: see Fig. 7.4(a). Color code for resistances: see Fig. 7.4(b).

Chapter 8

Conclusions

The investigation of Ta_2O_5 ReRAM in microscale and nanoscale devices was a main scope of this research work for advanced non-volatile memory applications. In order to find out the best properties of Ta_2O_5 switching oxide, various approaches such as sputtering power change of Ta_2O_5 layer, Ta_2O_5 thickness change and Bi-layer (Ta_2O_5 - TaO_x) were made. Also, the role of OE was investigated in terms of thickness change (Ta) and materials change (Hf, Ti, Ta, W) in Ta_2O_5 ReRAM.
The high V_{FORM} is not compatible to low-voltage CMOS technology. Therefore, a stack engineering and thermal process with RTA were made to reduce the V_{FORM} as low as the SET voltage. And successfully, the forming-free ReRAM devices were achieved by O_2 IIP and N_2 IIP. Non-Linearity (NL) and resistance ratio (R_{OFF}/R_{ON}) are analyzed at various I_{CC} levels for different device sizes and switching layer thicknesses in 1T-1R configuration. Also, an intrinsic modular arithmetic was realized using a ternary number system based on 7-states resistance levels of Ta_2O_5 ReRAM device.

8.1 Development of Ta_2O_5 switching oxide

Optimization of the Ta_2O_5 switching layer has been studied based on the effects of RF sputtering power, the thickness effect of Ta_2O_5 switching layer, and the Bi-layer (Ta_2O_5/TaO_x) structure. For the effect of RF sputtering power, the RF40% (236W) condition shows the best R_{OFF}/R_{ON} performance with stable

endurance up to 10^6 cycles (@1.0 μs) and good retention at 125 °C for 10^4 seconds. The good memory window (R_{OFF}/R_{ON} ratio) was achieved from the 7 nm-thick Ta_2O_5 with relatively lower V_{FORM} (1.8 V) compared with the 13 nm-thick Ta_2O_5 (3.0 V) for the thickness effect of Ta_2O_5 switching layer. For the Bi-layer (Ta_2O_5/TaO_x) effect, the R_{OFF} performance was improved with 7.0 nm-thick Ta_2O_5/ 20 nm-thick TaO_x at low I_{CC} level (50 μA) due to a better control of defects in the Ta_2O_5 switching layer.

8.2 Ohmic electrode for Ta_2O_5 ReRAM

Effects of the OE in the Ta_2O_5 ReRAM devices have been analyzed for different OE-materials and Ta-OE thickness. For the OE-material study, the impact of four different OE materials (W, Ta, Ti, and Hf) was analyzed. Early RESET failures were observed from the Ti- and Hf-OE devices due to an accumulation of the V_O's during the switching cycles while highly stable switching processes were achieved with the W- and Ta-OE devices. The W-OE devices show an increased R_{OFF} compared with the Ta-electrode under identical RESET conditions and the difference can be explained by higher E_{VO} of W-OE. On the other hand, the lower E_{VO} for Ta-OE results in faster SET processes than W-OE. For the investigation on the Ta-OE thickness change, the V_{FORM} decreases due to the increased amount of V_O generated in Ta_2O_5 layer with thicker Ta-OE. However, there was no further difference observed in electrical characterizations such as R_{ON}, R_{OFF} in terms of $V_{RESET-STOP}$ and I_{CC} effects by changing the Ta-OE thickness.

8.3 Forming free ReRAM device

The process parameters such as Ta_2O_5 thickness, Ta-OE thickness, RTA in O_2 and ion implantations (O_2, N_2) have been investigated in order to find out if they can impact the V_{FORM} and the other electrical performance of ReRAM device. For the thin Ta_2O_5 switching layer, the V_{FORM} was reduced effectively with 3 nm-thick Ta_2O_5, however, the performance of R_{OFF}/R_{ON} ratio and the data retention at 125 °C became seriously degraded. For the thicker Ta-OE, the V_{FORM} was reduced with a limitation since the reduction

of V_{FORM} became saturated at 13 nm-thick Ta-OE. There was no more reduction of V_{FORM} observed starting from above 13 nm-thick Ta-OE.
The majority ($\sim 70\%$) of ReRAM devices with 600 °C RTA showed forming-free behaviors. However, 600 °C is too high for Back-End-Of-Line (BEOL) process in CMOS application, therefore it is not a practical option. We could realize the forming-free ReRAM devices (100%) regardless of switching oxide material (Ta_2O_5, HfO_2) and its deposition methods (PVD, ALD) by both O_2 IIP and N_2 IIP. And the forming-free ReRAM devices with the O_2 IIP showed comparable electrical performances in $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio, data retention and endurance.

8.4 MOSFET-ReRAM integration

In 1T-1R configuration, the current overshoot from parasitic capacitance typically shown in the passive 1R structure can be effectively suppressed making the stable switching at low current regime. Therefore, Ta_2O_5 ReRAM in 1T-1R configuration was used for intrinsic property study of NL with controlled I_{CC} levels.
The NL in the 1T-1R Ta_2O_5 ReRAM improves at lower I_{CC} level regardless of the device area while the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ degrades. This is attributed to the fact that higher I_{CC} generates a stronger filament in the ReRAM device and the stronger filament deteriorates the NL value. For the $I_{\mathrm{CC}} = 3.0\,\mu$A, the highest NL value of 12 for the AC mode is achieved. On the contrary, the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ degrades with lower I_{CC} level as the R_{ON} is directly affected with the I_{CC} level. The switching layer thickness of the ReRAM device does not show an impact on the the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio and the NL value.

8.5 Resistor logic: ternary arithmetic

The new concept is successfully proven with sum of two Trit modular addition with the ternary numbers, $\mathbf{p} = \mathrm{p_1p_0} = 21$ and $\mathbf{q} = \mathrm{q_1q_0} = 22$. Since the sum output $\mathrm{z} = \mathrm{z_2z_1z_0}$ needs three Trit digits, three ReRAM devices are

required for this operation. Therefore, the implementation of modular arithmetic is achieved based on reliable multi-state (7-states) of W-OE based Ta_2O_5 ReRAM array (1×3). The sum calculation is carried out by proposed state machine for the calculation of carry and sum. For the calculation, the logic operands p and q (pre-defined by truth table for state definition) are applied to top electrode (TE) and bottom electrode (BE), respectively. A V_{OFFSET} is used to enable an equal stepping of operand voltages. The operation signal applied for HRS (6-states, R0, R1, R2, R3, R4, R5) has 200 ns pulse width based on full width half maximum (FWHM) with 40 ns rising/falling times.

8.6 Outlook

The Ta_2O_5 based ReRAM devices have been systematically analyzed based on effects of Ta_2O_5 switching layer, effects of OE. And also, the process parameters to reduce the V_{FORM} were studied and a method to make the forming-free ReRAM devices was achieved.

However, in order to achieve highly reliable ReRAM devices, further studies are required for switching mechanism of the forming free ReRAM with ion implantation, further optimized Bi-layer stacks, stable switching with sub µA current regime in 1T-1R configuration and etc.. And the different switching oxides such as HfO_2, TiO_2 combined with the developed technology from this dissertation could be a potential candidate for further improvement of the device characteristics. Also, systematic research on selector devices in ReRAM array is needed especially for high density vertical 3D-ReRAM in order to compete against current 3D-NAND Flash memory, which is available now in the market. Furthermore, additional characterization in precisely controlled test environment can reveal more meaningful insight for ReRAM devices.

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