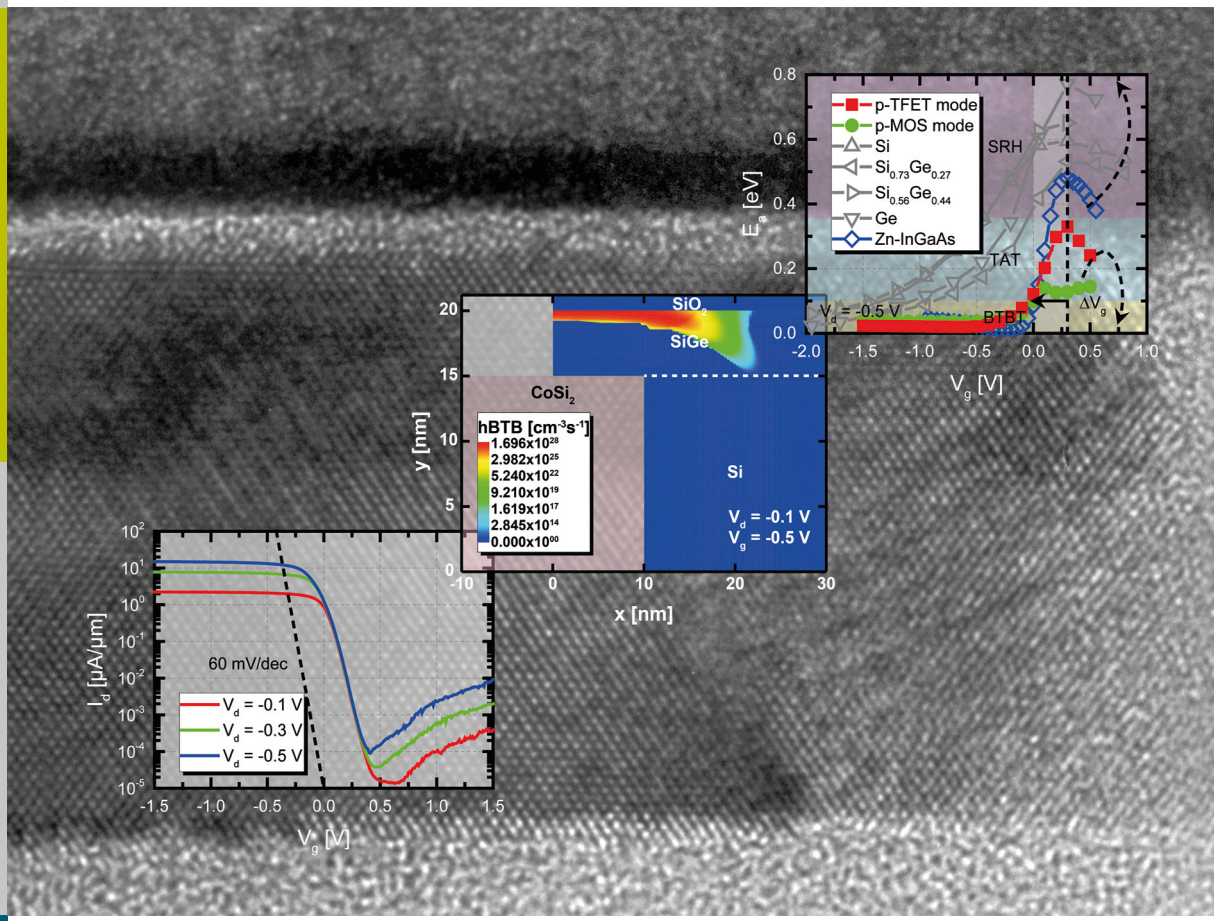
Strained Silicon-Germanium / Silicon Heterostructure Tunnel FETs for Low Power Applications

Sebastian Blaeser



Member of the Helmholtz Association

Schlüsseltechnologien / Key Technologies
Band / Volume 124
ISBN 978-3-95806-135-4

JÜLICH FORSCHUNGSZENTRUM

Schriften des Forschungszentrums Jülich
Reihe Schlüsseltechnologien / Key Technologies Band / Volume 124

Forschungszentrum Jülich GmbH
Peter Grünberg Institute
Semiconductor Nanoelectronics (PGI-9)

Strained Silicon-Germanium/Silicon Heterostructure Tunnel FETs for Low Power Applications

Sebastian Blaeser

Schriften des Forschungszentrums Jülich
Reihe Schlüsseltechnologien / Key Technologies Band / Volume 124

ISSN 1866-1807 ISBN 978-3-95806-135-4

Bibliographic information published by the Deutsche Nationalbibliothek.
The Deutsche Nationalbibliothek lists this publication in the Deutsche
Nationalbibliografie; detailed bibliographic data are available in the
Internet at http://dnb.d-nb.de.

Publisher and Distributor:	Forschungszentrum Jülich GmbH Zentralbibliothek 52425 Jülich Tel: +49 2461 61-5368 Fax: +49 2461 61-6103 Email: zb-publikation@fz-juelich.de www.fz-juelich.de/zb
Cover Design:	Grafische Medien, Forschungszentrum Jülich GmbH
Printer:	Grafische Medien, Forschungszentrum Jülich GmbH
Copyright:	Forschungszentrum Jülich 2016

Schriften des Forschungszentrums Jülich
Reihe Schlüsseltechnologien / Key Technologies, Band / Volume 124

D 82 (Diss. RWTH Aachen University, 2016)

ISSN 1866-1807
ISBN 978-3-95806-135-4

The complete volume is freely available on the Internet on the Jülicher Open Access Server (JuSER)
at www.fz-juelich.de/zb/openaccess.

Abstract

Scaling of nanoelectronics consequently comes along with power consumption in integrated circuits, either in terms of static power consumption P_{static} due to different leakage contributions or in terms of dynamic power consumption P_{dynamic}, accounting for the power density arising in an integrated circuit and thus, restricting an arbitrary miniaturization. Since dynamic power consumption scales with the second power of the supply voltage, $P_{\mathrm{dynamic}} \propto V_{\mathrm{DD}}^2$, a reduction of the latter represents a promising approach in order to enable low power electronics. However, a reduction of the supply voltage V_{DD} inevitably results in an either lowered on-current I_{on} or increased off-current I_{off} of a metal-oxide-semiconductor field-effect transistor (MOSFET). A reduction of the subthreshold swing SS of the transistor as a measure of the steepness of its transition from the off- to the on-state in turn allows for a reduction of the supply voltage V_{DD} without accepting an either lowered on-current I_{on} or increased off-current I_{off}. However, since charge transport in a MOSFET is based on thermionic emission over a potential barrier due to a broadened FERMI distribution function, its subthreshold swing SS is limited to 60 mV/dec at room temperature $T = 300\,\mathrm{K}$. In order to overcome this inherent limitation of a MOSFET and allow for a smaller subthreshold swing SS, the tunnel field-effect transistor (TFET) has been suggested as a promising alternative due to its charge transport realized by means of quantum mechanical band-to-band tunneling (BTBT).

Within the framework of this thesis, two different proposals of a TFET device concept allowing for low power applications are investigated. As a first approach, a vertical Silicon-Germanium/Silicon (SiGe/Si) heterostructure TFET is considered which makes use of strained SiGe as a material with smaller band gap E_{g} at the source tunnel junction in order to increase the probability for BTBT while suppressing the ambipolar switching characteristics in parallel due to the use of Si with its higher band gap E_{g} as compared to SiGe at the drain tunnel junction, thus enabling a heterostructure device concept. As a second approach, a planar SiGe/Si heterostructure TFET is presented which not only makes use of strained SiGe as a material with smaller band gap E_{g} at the source tunnel junction, but also benefits from a selective and self-adjusted silicidation in combination with a counter doped pocket at the source tunnel junction in order to enable line tunneling aligned with the gate electric field lines in an enlarged area directly underneath the gate. In addition, for both types of TFETs, technology computer aided design (TCAD) simulations are consulted in order to evaluate the respective experimental results as well as to illustrate potential improvements of each device concept.

However, the vertical SiGe/Si heterostructure n-TFET suffers from a high subthreshold swing SS, a weak onset of the drain current I_{d} with a pronounced S-shape as well as no visible saturation of the drain current I_{d} due to a strong degradation of both tunnel junctions which may stem from poor electrostatic control caused by a defective interface between

semiconductor and high-κ dielectrics as well as a pronounced surface roughness at the side walls of the fin, both favoring trap assisted tunneling (TAT). In addition, a pronounced ambipolar switching characteristics despite a heterostructure device concept becomes obvious, resulting from a much stronger contribution from TAT at the p^{++}-SiGe tunnel junction as compared to the n^{+}-Si tunnel junction, caused by the different chemical compositions of their respective interfacial oxide layers on the one hand and a much higher carrier concentration n within the SiGe layer on the other hand, scaling TAT.

The planar SiGe/Si heterostructure p-TFET in turn reveals a high on-current I_{on} of $6.7\,\mu A/\mu m$ at a supply voltage V_{DD} of $0.5\,V$ in parallel with an average subthreshold swing SS of about $80\,mV/dec$ over four orders of magnitude of drain current I_d. Benchmarking the planar SiGe/Si heterostructure p-TFET with published state of the art TFETs in terms of on-current I_{on} and average subthreshold swing SS over four orders of magnitude of drain current I_d highlights the planar SiGe/Si heterostructure p-TFET outperforming other devices due to line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT. Pulsed measurements allow for an identification of TAT being responsible for a degradation of the subthreshold swing SS. A sharp transition of the activation energy E_a from both Shockley-Read-Hall (SRH) and TAT to BTBT regime within a small gate voltage window ΔV_g of less than $0.4\,V$ is revealed by means of low temperature T measurements, being much steeper as compared to state of the art Si, SiGe or Ge TFETs, thus facilitating high on-currents I_{on} at a low supply voltage V_{DD} and a constant subthreshold swing SS in parallel. Finally, p-logic Not-AND (NAND) operation is demonstrated by means of two planar SiGe/Si heterostructure p-TFETs connected in series, highlighting their ability for both low power electronics and logic applications down to ultra-low supply voltages V_{DD} of $0.1\,V$.

Kurzfassung

Skalierung in der Nanoelektronik geht unweigerlich einher mit dem Energieverbrauch eines integrierten Schaltkreises, sei es in Form von statischem Energieverbrauch P_{static} aufgrund unterschiedlicher Leckstrompfade oder in Form von dynamischem Energieverbrauch P_{dynamic}, der die Energiedichte in einem integrierten Schaltkreis bestimmt und so einer beliebigen Miniaturisierung Grenzen setzt. Da der dynamische Energieverbrauch mit dem Quadrat der Versorgungsspannung skaliert, $P_{\text{dynamic}} \propto V_{\text{DD}}^2$, stellt die Verringerung letzterer einen vielversprechenden Ansatz für die Realisierung elektronischer Anwendungen mit niedrigem Energieverbrauch dar. Jedoch hat eine Verringerung der Versorgungsspannung V_{DD} unvermeidlich einen entweder reduzierten An-Strom I_{on} oder erhöhten Aus-Strom I_{off} eines Metall-Oxid-Halbleiter-Feldeffekttransistors (MOSFET) zur Folge. Dagegen ermöglicht eine Verringerung der Unterschwellenspannung SS des Transistors als Maß für die Steilheit des Überganges zwischen Aus- und An-Zustand eine Verringerung der Versorgungsspannung V_{DD}, ohne einen entweder reduzierten An-Strom I_{on} oder erhöhten Aus-Strom I_{off} in Kauf nehmen zu müssen. Da der Ladungstransport in einem MOSFET jedoch auf thermischer Emission über eine Potentialbarriere aufgrund einer aufgeweiteten Fermi Verteilungsfunktion beruht, ist seine Unterschwellenspannung SS auf 60 mV/dec bei Raumtemperatur $T = 300\,\text{K}$ begrenzt. Um diese inhärente Limitierung des MOSFETs zu überwinden und eine kleinere Unterschwellenspannung SS zu ermöglichen, wird der Tunnel-Feldeffekttransistor (TFET) als vielversprechende Alternative in Betracht gezogen, da dessen Ladungstransport auf quantenmechanischem Band-zu-Band Tunneln (BTBT) beruht.

Im Rahmen dieser Dissertation werden zwei unterschiedliche Vorschläge eines TFET-Bauelementkonzeptes unter dem Gesichtspunkt der Realisierung elektronischer Anwendungen mit niedrigem Energieverbrauch diskutiert. Als erster Ansatz wird ein vertikaler Silizium-Germanium/Silizium (SiGe/Si) Heterostruktur TFET untersucht, der von verspanntem SiGe als einem Material mit kleinerer Bandlücke E_{g} an der Tunnelverbindung der Quelle profitiert, um die Wahrscheinlichkeit für BTBT zu erhöhen, und gleichzeitig ein ambipolares Schaltverhalten unterdrückt, indem auf Si mit seiner größeren Bandlücke E_{g} an der Tunnelverbindung der Senke zurückgegriffen wird, um auf diese Weise das Konzept einer Heterostruktur zu realisieren. Als zweiter Ansatz wird ein planarer SiGe/Si Heterostruktur TFET vorgestellt, der nicht nur auf verspanntes SiGe als ein Material mit kleinerer Bandlücke E_{g} an der Tunnelverbindung der Quelle zurückgreift, sondern auch von einer selektiven und selbstjustierenden Silizidierung in Kombination mit einer gegendotierten Tasche an der Tunnelverbindung der Quelle profitiert, so dass Linientunneln in Richtung der elektrischen Feldlinien in einem vergrößerten Bereich direkt unterhalb der Steuerelektrode ermöglicht wird. Zusätzlich wird bei beiden TFETs auf Simulationen mittels technologischem, rechnerunterstütztem Konstruierens (TCAD) zurückgegriffen, um sowohl die jeweiligen experi-

mentellen Ergebnisse beurteilen als auch Raum für potentielle Verbesserungen des jeweiligen Bauelementkonzeptes aufzeigen zu können.

Jedoch wird der vertikale SiGe/Si Heterostruktur n-TFET durch eine hohe Unterschwellenspannung SS, einen schwachen Anstieg des Senkenstromes I_d mit einer ausgeprägten S-Form sowie keiner sichtbaren Sättigung des Senkenstromes I_d limitiert, die auf eine starke Schädigung beider Tunnelverbindungen schließen lassen. Diese Schädigung beider Tunnelverbindungen kann sowohl von schwacher elektrostatischer Kontrolle aufgrund einer defektreichen Grenzfläche zwischen Halbleiter und high-κ Dielektrikum als auch einer ausgebildeten Oberflächenrauheit an den Seitenwänden der Finne herrühren, so dass Tunneln über Störstellen (TAT) begünstigt wird. Zudem tritt ein ausgeprägtes ambipolares Schaltverhalten trotz des Konzepts einer Heterostruktur zu Tage, das in einem stärkeren Beitrag von TAT an der p^{++}-SiGe Tunnelverbindung im Vergleich zur n^{+}-Si Tunnelverbindung begründet liegt. Diese unterschiedlich starke Ausprägung von TAT lässt sich einerseits auf Unterschiede in der chemischen Zusammensetzung der jeweiligen Grenzflächenoxide und andererseits auf eine deutlich höhere Ladungsträgerkonzentration n innerhalb der SiGe-Schicht, die TAT skaliert, zurückführen.

Der planare SiGe/Si Heterostruktur p-TFET dagegen weist einen hohen An-Strom I_on von $6.7\,\mu\mathrm{A}/\mu\mathrm{m}$ für eine Versorgungsspannung V_DD von $0.5\,\mathrm{V}$ bei einer gleichzeitig mittleren Unterschwellenspannung SS von ungefähr $80\,\mathrm{mV/dec}$ über vier Größenordnungen des Senkenstromes I_d auf. Ein Vergleichsmaßstab des planaren SiGe/Si Heterostruktur p-TFETs mit publizierten TFETs nach aktuellem Stand der Technik in Bezug auf An-Strom I_on und mittlere Unterschwellenspannung SS über vier Größenordnungen des Senkenstromes I_d offenbart die Überlegenheit des planaren SiGe/Si Heterostruktur p-TFETs, die im Linientunneln in Richtung der elektrischen Feldlinien als maßgeblichen Anteil zum BTBT begründet liegt. Mithilfe von Pulsmessungen kann TAT als Ursprung der erhöhten Unterschwellenspannung SS ausgemacht werden. Messungen bei tiefen Temperaturen T zeigen einen scharfen Übergang der Aktivierungsenergie E_a von einem durch Shockley-Read-Hall (SRH) und TAT bestimmten Ladungstransport hin zu einem durch BTBT dominierten auf. Dieser Übergang wird in einer geringen Spannungsdifferenz ΔV_g der Steuerelektrode von weniger als $0.4\,\mathrm{V}$ vollzogen, ist deutlich schärfer als bei anderen publizierten TFETs nach aktuellem Stand der Technik auf Basis von Si, SiGe oder Ge und begünstigt so hohe An-Ströme I_on für niedrige Versorgungsspannungen V_DD bei einer gleichzeitig konstanten Unterschwellenspannung SS. Abschließend wird ein Nicht-UND (NAND)-Gatter in p-Logik mithilfe von zwei in Serie verschalteten planaren SiGe/Si Heterostruktur p-TFETs realisiert, die damit ihre Eignung sowohl im Bereich elektronischer Anwendungen mit niedrigem Energieverbrauch als auch im Bereich von Logikanwendungen für Niedrigst-Versorgungsspannungen V_DD von $0.1\,\mathrm{V}$ unter Beweis stellen.

Contents

1 Introduction

Whenever discussing scaling of nanoelectronics, MOORE's empirical law from 1965 comes into play, suggesting a doubling of the number of transistors in a highly integrated circuit approximately every two years [1]. Due to steady progress in technology such as the introduction of high-κ dielectrics in the 45 nm node in 2007 or the establishment of tri-gate fin-shaped field-effect transistors (FinFETs) as one step towards a three-dimensional device geometry in the 22 nm node in 2012 [2, 3], a premature ending of MOORE's prediction could be postponed over and over again and is valid for more than 50 years now. However, the more the dimensions of a metal-oxide-semiconductor field-effect transistor (MOSFET) as the key component of state of the art complementary metal-oxide-semiconductor (CMOS) technology shrink, the more contributions from leakage have to be taken into account, resulting in an increased static power consumption P_{static} of the integrated circuit and thus, degraded performance. Recently, Intel Corporation had to admit a slowdown of their cadence for technology transitions from two to two and a half years [4], resulting in a pronounced delay of their 10 nm node, first announced for 2015, now expected to show up in 2017. But on the contrary, a research alliance consisting of IBM, Globalfoundries and Samsung Corporation recently demonstrated a transistor incorporating a SiGe channel based on a 7 nm node utilizing extreme ultraviolet (EUV) lithography [5], once more postponing the limits of miniaturization and thus, further approaching the fundamental physical limits arising from quantum mechanics. Besides static power consumption P_{static} due to leakage contributions, dynamic power consumption P_{dynamic} must also be taken into account. Dense packaging of transistors in highly integrated circuits results in a considerable energy dissipation, making a restriction to an arbitrary miniaturization due to the limit of power density at a value of about $100\,\mathrm{W/cm^2}$ much more probable than due to quantum mechanical effects [6]. Thus, a reduction of dynamic power consumption P_{dynamic} is indispensable if MOORE's empirical law should not come to its end. Since dynamic power consumption scales with the second power of the supply voltage, $P_{\mathrm{dynamic}} \propto V_{\mathrm{DD}}^2$, a reduction of the latter represents a promising approach in order to enable low power electronics as one key requirement for both mobility and context-aware computing [7].

However, a reduction of the supply voltage V_{DD} inevitably results in an either lowered on-current I_{on} or increased off-current I_{off} of the transistor. In this regard, a steeper transition from the off- to the on-state of a transistor may encounter this issue, thus bringing the subthreshold swing SS as a further figure of merit of a transistor into focus of consideration. Since charge transport in a MOSFET is based on thermionic emission over a potential barrier due to a broadened FERMI distribution function, its subthreshold swing SS is limited to $60\,\mathrm{mV/dec}$ at room temperature $T = 300\,\mathrm{K}$. In order to overcome this inherent limitation of a MOSFET and allow for a smaller subthreshold swing SS, new device concepts enabling a different mechanism of charge transport are needed. As one example of such a new device

concept, a SCHOTTKY barrier FET making use of impact ionization was recently experimentally demonstrated, allowing for a steep subthreshold swing SS far below 60 mV/dec [8]. However, Monte-Carlo simulations suggest a reduced switching speed in case of impact ionization due to a considerable time required in order to activate the process of carrier multiplication [9], claiming one major drawback of this novel device concept. With respect to the switching speed of a transistor, the tunnel field-effect transistor (TFET) as the most promising candidate for steep-slope devices comes into play. Charge transport in a TFET is not based on thermionic emission over but on quantum mechanical band-to-band tunneling (BTBT) through a potential barrier. The mechanism of BTBT was already experimentally observed and discussed by ESAKI in narrow Ge p-n junctions in 1958 [10], exhibiting a negative differential resistance (NDR) at forward bias in the corresponding current-voltage (IV) characteristics, whereas first concepts for a transistor making use of BTBT date back to the late 1980s [11, 12]. Finally, the first TFET enabling a subthreshold swing SS below 60 mV/dec was experimentally realized in 2005 by means of a carbon nanotube transistor (CNT) [13], whereas the first TFET experimentally revealing a subthreshold swing SS below 60 mV/dec, but based on Si technology, came up in 2007 [14]. However, TFETs still suffer from low on-currents I_{on} as compared to state of the art MOSFETs since the probability for BTBT yields to $T(E) < 1$ and thus, limits charge transport in a TFET, whereas in case of (short-channel) MOSFETs, charge transport within the channel can be assumed as ballistic, enabling a transmission probability $T(E) = 1$ [15]. One possibility to encounter the issue of low on-currents I_{on} is the introduction of materials with small band gap E_{g} such as strained Ge or GeSn which allow for a direct band gap E_{g} transition in order to enhance the transmission probability $T(E)$. In this regard, the first TFET employing GeSn was experimentally realized in 2012 [16, 17], providing high on-currents I_{on}, but still lacking in terms of a direct band gap E_{g} transition due to the actual Sn content not exceeding the critical concentration yet. However, in 2015 GeSn finally was proven to enable a direct band gap E_{g} transition by means of lasing for Sn concentrations above 9% while maintaining a Si compatible technology [18]. In summary, the recent usability of TFETs as a replacement for MOSFETs is still quite limited, but theoretical calculations predict superior performance, higher switching speed and less power consumption of TFETs as compared to MOSFETs for supply voltages V_{DD} below 0.5 V, revealing their promising potential even more pronounced in complementary metal-oxide-semiconductor (CMOS) logic applications [19, 20], but also in analog and sensor applications [21, 22, 23, 24].

Within the framework of this thesis, two different proposals of a TFET device concept allowing for low power applications will be investigated. As a first approach, a vertical Silicon-Germanium/Silicon (SiGe/Si) heterostructure TFET will be considered which makes use of strained SiGe as a material with smaller band gap E_{g} at the source tunnel junction in order to increase the probability for BTBT while suppressing the ambipolar switching characteristics in parallel due to the use of Si with its higher band gap E_{g} as compared to SiGe at the drain tunnel junction, thus enabling a heterostructure device concept. As a second approach, a planar SiGe/Si heterostructure TFET will be presented which not only makes use of strained SiGe as a material with smaller band gap E_{g} at the source tunnel junction, but also benefits from a selective and self-adjusted silicidation in combination with a counter doped pocket at the source tunnel junction in order to enable line tunneling aligned with the gate electric field lines in an enlarged area directly underneath the gate. In

addition, for both types of TFETs, technology computer aided design (TCAD) simulations will be consulted in order to evaluate the respective experimental results as well as illustrate potential improvements of each device concept.

The content of this thesis is divided into five chapters. Subsequent to this introductory chapter, chapter 2 provides the theoretical background which is needed to describe the physics of the experimental work presented in this thesis, highlighting the different working principles of a MOSFET and a TFET respectively as well as discussing strain engineering and equivalent oxide thickness (EOT) scaling as two possibilities in order to improve subthreshold swing SS and on-current I_{on} of a TFET. The vertical SiGe/Si heterostructure n-TFET will be introduced in chapter 3, first motivating this device concept by means of TCAD simulations, then presenting the experimental results obtained by direct current (DC) characterization. Chapter 4 presents the experimental results obtained from the planar SiGe/Si heterostructure p-TFET. Besides DC characterization, pulsed measurements and low temperature T analysis are performed in order to describe the physics emerging in this TFET structure. TCAD simulations assist in evaluating the experimental results and identifying critical process parameters. In addition, as a first step towards logic applications, a Not-AND (NAND) gate is presented, realized by means of p-TFET logic. Finally, chapter 5 concludes by summarizing the different results derived within the framework of this thesis and by giving an outlook by means of TCAD simulations for an optimized TFET device concept based on the planar SiGe/Si heterostructure p-TFET in order to demonstrate TFETs as a fierce competitor of MOSFETs in terms of low power electronics as well as low power CMOS logic applications.

2 Theoretical Background

This chapter provides the theoretical background which is needed in order to describe the physics of the experimental work presented in this thesis. At first, basic principles concerning power consumption in integrated circuits are highlighted in order to motivate the focus of this thesis on low power electronics. The MOSFET as the key component of state of the art CMOS technology is discussed, briefly deriving its subthreshold characteristics. Subsequently, the TFET as one candidate to overcome the inherent limitations of a MOSFET is introduced. KANE's BTBT model as well as different BTBT mechanisms and additional properties emerging in a TFET are deduced and discussed in order to describe its physics. Finally, strain engineering and EOT scaling as two possible techniques in order to optimize design and operation of a TFET are considered.

2.1 Power Consumption in Integrated Circuits

Power consumption in integrated circuits arises from dynamic power P_{dynamic}, short-circuit power $P_{\text{short-circuit}}$ and static power P_{static} as three independent contributions [25]. Figure 2.1.1 sketches these different components of power consumption in an integrated circuit. Dynamic power P_{dynamic} and short-circuit power $P_{\text{short-circuit}}$ are also known as the switching power of an integrated circuit. Both are consumed whenever transistors change their logic

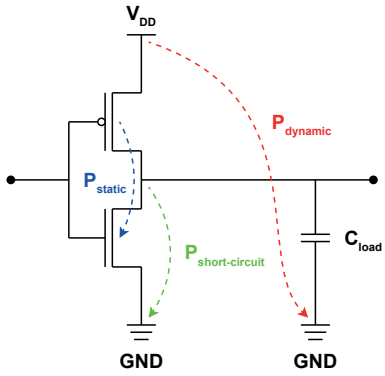


Figure 2.1.1: Schematic illustration of the different contributions to power consumption arising in integrated circuits. Dynamic power P_{dynamic} and short-circuit power $P_{\text{short-circuit}}$ are consumed when transistors change their logic state due to charging and discharging of load capacitors C_{load} whereas static power P_{static} in turn dissipates due to different leakage contributions.

state due to charging and discharging of load capacitors C_{load}. The dependency of the dynamic power P_{dynamic} on the supply voltage V_{DD} can be described as

$$P_{\text{dynamic}} = AC_{\text{load}}V_{\text{DD}}^2 f, \tag{2.1.1}$$

where A denotes the activity factor, ranging between 0 and 1, as a measure of the average switching activity in the integrated circuit and f is the corresponding switching frequency. Static power P_{static} in turn dissipates due to different leakage contributions like reverse biased diode leakage, gate induced drain leakage, gate oxide tunneling and subthreshold leakage and depends linearly on the off-current I_{off} of a transistor:

$$P_{\text{static}} = I_{\text{off}}V_{\text{DD}}. \tag{2.1.2}$$

The off-current I_{off} of a transistor in turn is mainly dominated by the subthreshold leakage. As a consequence, the dependency of the off-current I_{off} on the supply voltage V_{DD} can also be approximated by the subthreshold swing SS as a figure of merit of a transistor, allowing for the evaluation of the steepness of its transition from the off- to the on-state [15]:

$$SS \approx \frac{V_{\text{DD}}}{\log\left(\frac{I_{\text{on}}}{I_{\text{off}}}\right)}, \tag{2.1.3}$$

which is equivalent to

$$I_{\text{off}} = I_{\text{on}} \cdot 10^{-\frac{V_{\text{DD}}}{SS}}. \tag{2.1.4}$$

Equation (2.1.4) reveals an exponential increase of the off-current I_{off} of a transistor for a reduction of the supply voltage V_{DD} but keeping the on-current I_{on} constant. This unfavorable behavior becomes visible in the corresponding transfer characteristics plotting the drain current I_{d} of the transistor as a function of the gate voltage V_{g} as illustrated in figure 2.1.2. A reduction of the supply voltage V_{DD} without accepting an either lowered on-current I_{on} or increased off-current I_{off} can only be achieved by a smaller subthreshold swing SS enabling a sharper transition from the off- to the on-state of the transistor as already indicated in chapter 1.

2.2 Physics of a MOSFET

A MOSFET is a three-terminal device making use of the electrical field-effect in order to control charge transport from a doped source to a doped drain through an intrinsic channel. The electrostatic potential within the channel is controlled by an electrically isolated gate electrode determining the metal-oxide-semiconductor (MOS) capacitor of the transistor. Injection of carriers from the source into the channel is based on thermionic emission over a potential barrier due to a broadened FERMI distribution function in the source. In case of n-MOSFET operation as depicted in figure 2.2.1, source and drain are n^+-doped and a positive voltage $V_{\text{d}} > 0$ at the drain is applied, resulting in the conduction band edge of the channel being a potential barrier for electrons from source and drain respectively. By applying a positive voltage $V_{\text{g}} > 0$ at the gate electrode, conduction and valence band in the channel are lowered in energy, allowing for charge transport between source and drain

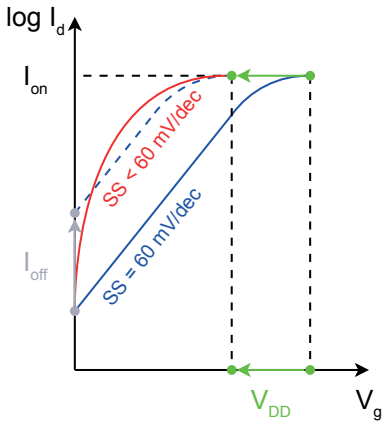


Figure 2.1.2: Schematic illustration of the transfer characteristics of a MOSFET, revealing an exponential increase of the off-current I_{off} of a transistor for a reduction of the supply voltage V_{DD} but keeping the on-current I_{on} constant. A reduction of the supply voltage V_{DD} without either accepting a lowered on-current I_{on} or increased off-current I_{off} can only be achieved by a subthreshold swing SS below 60 mV/dec enabling a sharper transition from the off- to the on-state as provided in case of a TFET.

due to a reduced potential barrier, indicated by the surface potential Φ_{ch} of the channel. Thereby, the characteristics of the drain current I_{d} depend exponentially on the broadening of the FERMI distribution function as deduced in chapter 2.2.1.

2.2.1 Subthreshold Characteristics

Charge transport in a MOSFET can be derived by means of the LANDAUER-BÜTTIKER formalism interpreting conduction in a one-dimensional system as a transmission problem [26]:

$$I_{\text{d}} = \frac{2e}{h} \int_{E} \mathrm{d}E\, T(E) \left[f_{\text{s}}(E) - f_{\text{d}}(E) \right], \tag{2.2.1}$$

where e is the elementary charge, h the PLANCK constant, $T(E)$ the transmission probability and f_{s} and f_{d} represent the FERMI distribution functions of source and drain respectively. As already suggested in chapter 1, assuming ballistic transport within the channel yields a transmission probability $T(E) = 1$ for energies $E > \Phi_{\text{ch}}$ greater than the surface potential of the channel and $T(E) = 0$ for all other energies, simplifying the integral in equation (2.2.1) to:

$$I_{\text{d}} \approx \frac{2e}{h} \int_{\Phi_{\text{ch}}}^{\infty} \mathrm{d}E \left[f_{\text{s}}(E) - f_{\text{d}}(E) \right]. \tag{2.2.2}$$

Applying a positive drain voltage $V_{\text{d}} > 0$ causes a lowered chemical potential $\mu_{\text{d}} < \mu_{\text{s}}$ at the drain as compared to the source. As a consequence, the contribution of the FERMI

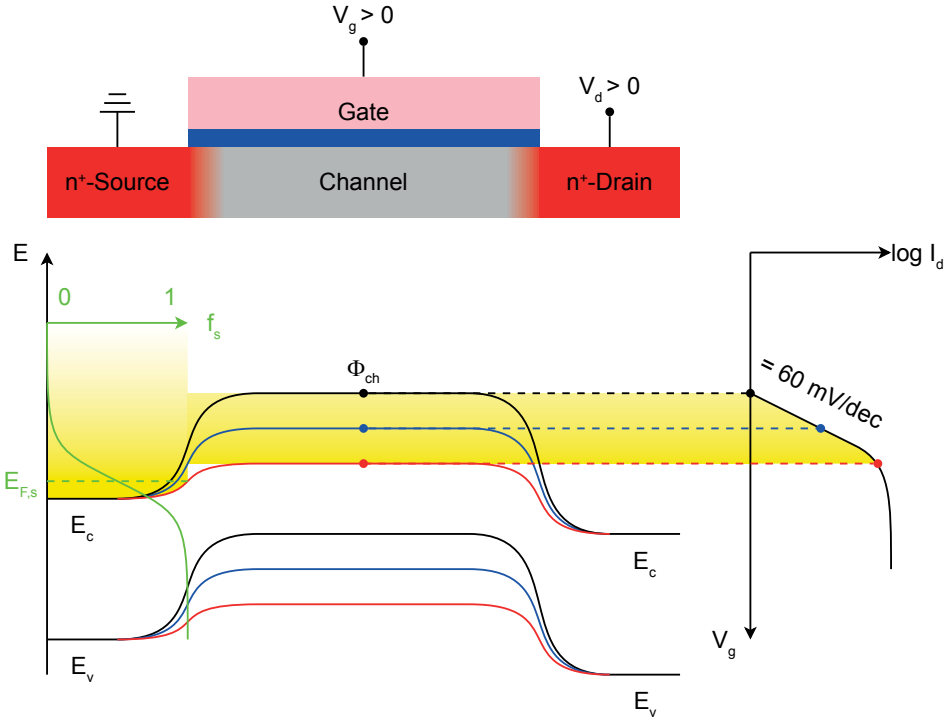


Figure 2.2.1: Schematic illustration of the band structure and corresponding transfer characteristics in case of n-MOSFET operation with source and drain being n^+-doped and a positive voltage $V_d > 0$ at the drain applied. By applying a positive voltage $V_g > 0$ at the gate electrode, conduction and valence band in the channel are lowered in energy, allowing for charge transport based on thermionic emission between source and drain due to a reduced potential barrier, indicated by the surface potential Φ_{ch} of the channel.

distribution function of the drain becomes negligible with respect to that of the source, $f_d \ll f_s$, further simplifying the integral in equation (2.2.2) to:

$$I_d \approx \frac{2e}{h} \int_{\Phi_{ch}}^{\infty} dE \, f_s(E) \,. \tag{2.2.3}$$

Assuming charge transport in the subthreshold regime of a MOSFET, the FERMI distribution function f_s of the source can be approximated by the BOLTZMANN distribution function since the surface potential of the channel is much greater than the chemical potential of the source, $\Phi_{ch} \gg \mu_s$, thus allowing for an analytic solution of the integral in equation (2.2.3):

$$I_d \approx \frac{2e}{h} \int_{\Phi_{ch}}^{\infty} dE \, \exp\left(-\frac{E-\mu_s}{k_B T}\right) = \frac{2e}{h} k_B T \exp\left(-\frac{\Phi_{ch}-\mu_s}{k_B T}\right). \tag{2.2.4}$$

In order to evaluate the steepness of the transition of a MOSFET from its off- to its on-state, the subthreshold swing SS as one figure of merit is defined:

$$SS = \left[\frac{\partial \log I_\mathrm{d}}{\partial V_\mathrm{g}}\right]^{-1} = \ln(10)\left[\frac{1}{I_\mathrm{d}}\frac{\partial I_\mathrm{d}}{\partial V_\mathrm{g}}\right]^{-1} = \ln(10)\left[\frac{1}{I_\mathrm{d}}\frac{\partial I_\mathrm{d}}{\partial \Phi_\mathrm{ch}}\frac{\partial \Phi_\mathrm{ch}}{\partial V_\mathrm{g}}\right]^{-1}, \tag{2.2.5}$$

where the first derivative of the drain current I_d with respect to the surface potential Φ_ch of the channel can be calculated from equation (2.2.4). In order to evaluate the influence of the gate voltage V_g on the surface potential Φ_ch of the channel, the gate capacitance C of a MOSFET has to be taken into account [6]:

$$C = \frac{\partial Q_\mathrm{depl}}{\partial V_\mathrm{g}} + \frac{\partial Q_\mathrm{inv}}{\partial V_\mathrm{g}} = \left(\frac{\partial Q_\mathrm{depl}}{\partial \Phi_\mathrm{ch}} + \frac{\partial Q_\mathrm{inv}}{\partial \Phi_\mathrm{ch}}\right)\frac{\partial \Phi_\mathrm{ch}}{\partial V_\mathrm{g}} = \frac{C_\mathrm{depl} + C_\mathrm{inv}}{e}\frac{\partial \Phi_\mathrm{ch}}{\partial V_\mathrm{g}}, \tag{2.2.6}$$

with C_depl and C_inv being the capacitances in depletion and inversion respectively. In addition, the gate capacitance C can be described as a combination of a parallel and a series connection of depletion, inversion and oxide capacitances C_depl, C_inv and C_ox:

$$C = \frac{(C_\mathrm{depl} + C_\mathrm{inv})\, C_\mathrm{ox}}{C_\mathrm{ox} + C_\mathrm{depl} + C_\mathrm{inv}}. \tag{2.2.7}$$

Combining equations (2.2.6) and (2.2.7) yields the dependency of the surface potential Φ_ch of the channel on the gate voltage V_g:

$$\frac{\partial \Phi_\mathrm{ch}}{\partial V_\mathrm{g}} = e\left(\frac{C_\mathrm{ox}}{C_\mathrm{ox} + C_\mathrm{depl} + C_\mathrm{inv}}\right). \tag{2.2.8}$$

As a consequence, the subthreshold swing SS of a MOSFET becomes a function of the temperature T and the different contributions from the gate capacitance C:

$$SS = \ln(10)\frac{k_\mathrm{B}T}{e}\left(1 + \frac{C_\mathrm{depl} + C_\mathrm{inv}}{C_\mathrm{ox}}\right). \tag{2.2.9}$$

Assuming the oxide capacitance is much greater than the capacitances in depletion and inversion, $C_\mathrm{ox} \gg C_\mathrm{depl} + C_\mathrm{inv}$, the lower limit of the subthreshold swing SS of a MOSFET at room temperature $T = 300\,\mathrm{K}$ can be calculated as:

$$SS = \ln(10)\frac{k_\mathrm{B}T}{e} \approx 60\,\mathrm{mV/dec}. \tag{2.2.10}$$

2.3 Physics of a TFET

In contrast to a MOSFET, charge transport in a TFET is not based on thermionic emission over a potential barrier but on quantum mechanical BTBT. Therefore, source and drain are doped with opposite dopant species, resulting in a gated p-i-n structure which is operated in reverse bias conditions. In case of p-TFET operation as illustrated in figure 2.3.1, the source is n^+-doped whereas the drain is p^+-doped and a negative voltage $V_\mathrm{d} < 0$ at the drain is applied, resulting in the conduction band edge of the channel being a potential

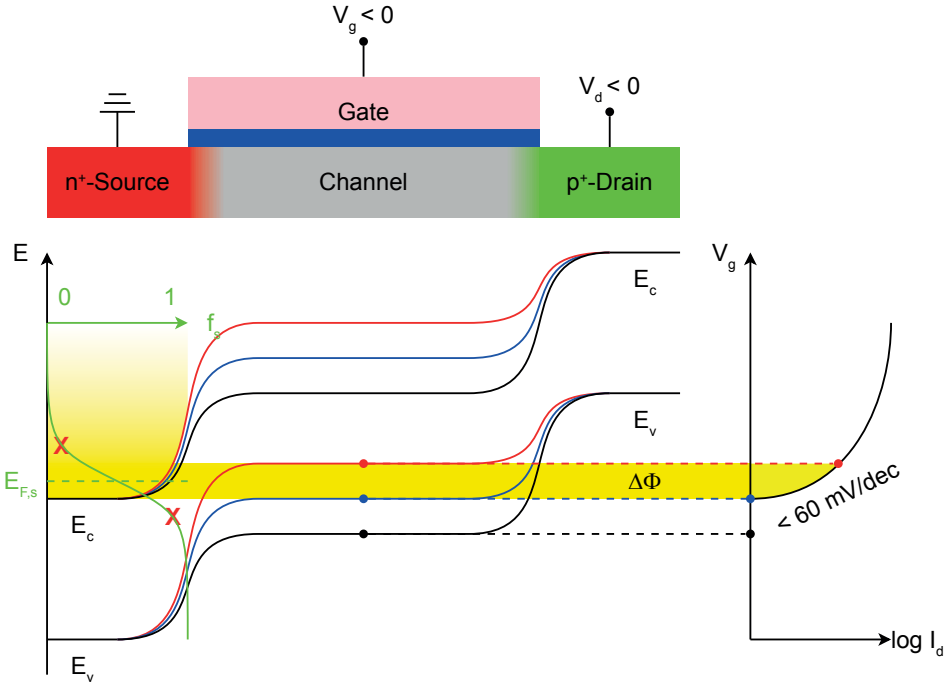


Figure 2.3.1: Schematic illustration of the band structure and corresponding transfer characteristics in case of p-TFET operation with the source being n^+-doped, the drain being p^+-doped and a negative voltage $V_d < 0$ at the drain applied. By applying a negative voltage $V_g < 0$ at the gate electrode, conduction and valence band in the channel are raised in energy, causing an energy overlap $\Delta\Phi$ between the conduction band of the source and the valence band of the channel. This energy overlap $\Delta\Phi$ defines the tunneling window for BTBT from the source into the channel.

barrier for electrons from the source and the valence band edge of the channel being a potential barrier for holes from the drain. By applying a negative voltage $V_g < 0$ at the gate electrode, conduction and valence band in the channel are raised in energy, causing an energy overlap $\Delta\Phi$ between the conduction band of the source and the valence band of the channel. This energy overlap $\Delta\Phi$ defines the tunneling window for BTBT from the source into the channel. Thereby, the confinement of the tunneling windows gives rise to a band-pass filter like behavior of the TFET due to a cut off of the high and low energy tale of the FERMI distribution function, allowing for a subthreshold swing SS lower than 60 mV/dec as in case of a MOSFET.

2.3.1 Kane's BTBT Model

BTBT as a quantum mechanical process is based on the assumption that electrons can not only be described as particles but also as wave functions. In contrast to classical mechanics,

these wave functions are not fully reflected at a potential barrier but have a finite probability to penetrate through and continue after the potential barrier. In case of BTBT, this potential barrier is represented by the band gap E_g of a semiconductor. Whenever an electron tunnels from the valence into the conduction band through the band gap E_g, an electron-hole pair is generated.

The probability for this tunneling process can be sufficiently described by Kane's semiclassical, local BTBT model which translates BTBT currents into generation rates G of electrons and holes respectively. In case of a local model, the electric field as the gradient of the electrostatic potential, $F = -\frac{\partial \Phi}{\partial x}$, is supposed to be both constant and uniform, being a valid assumption as long as the electrostatic potential Φ does not change rapidly along a certain direction x according to the so-called Wentzel-Kramers-Brillouin (WKB) approximation [27]. Thus, the generation rates G of electrons and holes can be described as a function of the first derivative of the current density J with respect to the energy E by means of the relation $E = -e\Phi$:

$$G = \frac{1}{e}\frac{\partial J}{\partial x} = -\frac{F}{e}\frac{\partial J}{\partial \Phi} = F\frac{\mathrm{d}J}{\mathrm{d}E}. \tag{2.3.1}$$

In contrast to the current density J, the generation rates G of electrons and holes are not dependent on the position x as long as the electric field F is constant as assumed in case of a local model. The current density J in turn can be derived by means of the already discussed Landauer-Büttiker formalism according to:

$$J = \frac{2e}{h}\frac{1}{A}\int_E \mathrm{d}E \sum_{\boldsymbol{k}_\perp} T\left(E, \boldsymbol{k}_\perp\right)\left[f_\mathrm{v}\left(E\right) - f_\mathrm{c}\left(E\right)\right], \tag{2.3.2}$$

where A denotes a normalized area and f_v and f_c are the Fermi distribution functions of valence and conduction band respectively. Furthermore, the transmission probability $T\left(E, \boldsymbol{k}_\perp\right)$ is not only a function of the energy E but also of the wave vector $\boldsymbol{k}_\perp = \boldsymbol{k}_y + \boldsymbol{k}_z$ perpendicular to the tunneling direction. Assuming an electron tunnels from a fully occupied valence into an empty conduction band, the Fermi distribution functions of valence and conduction band can be set to $f_\mathrm{v} = 1$ and $f_\mathrm{c} = 0$ respectively, simplifying equation (2.3.2) to:

$$J \approx \frac{2e}{h}\frac{1}{A}\int_E \mathrm{d}E \sum_{\boldsymbol{k}_\perp} T\left(E, \boldsymbol{k}_\perp\right). \tag{2.3.3}$$

Taking the first derivative of the current density J given in equation (2.3.3) with respect to the energy E and multiplying with the electric field F yields the generation rates G of electrons and holes as follows:

$$G = \frac{2e}{h}\frac{F}{A}\sum_{\boldsymbol{k}_\perp} T\left(E, \boldsymbol{k}_\perp\right). \tag{2.3.4}$$

The sum over the transmission probabilities $T\left(E, \boldsymbol{k}_\perp\right)$ as a function of the wave vector $\boldsymbol{k}_\perp$ perpendicular to the tunneling direction as stated in equation (2.3.4) can be converted into an integral over the whole momentum space of $\boldsymbol{k}_\perp$ multiplied with its two-dimensional density of states $\frac{A}{(2\pi)^2}$:

$$G = \frac{e}{2\pi^2 h}F\iint_{\boldsymbol{k}_\perp} \mathrm{d}^2\boldsymbol{k}_\perp\, T\left(E, \boldsymbol{k}_\perp\right). \tag{2.3.5}$$

The transmission probability $T(E, \boldsymbol{k}_\perp)$ in turn can be calculated according to the WKB approximation as follows [28]:

$$T(E, \boldsymbol{k}_\perp) = \frac{\pi^2}{9} \exp\left(-2 \int_{x_1}^{x_2} \mathrm{d}x \ \mathrm{Im}\left(k_x\right)\right), \tag{2.3.6}$$

with x_1 and x_2 being the classical turning points of the tunneling process and k_x denoting the norm of the wave vector $\boldsymbol{k}_x$ parallel to the tunneling direction. Moreover, the norm of the wave vector $\boldsymbol{k}_x$ parallel to the tunneling direction must be a function of the position, $k_x = k_x(x)$, due to energy conservation. Thus, the transmission probability $T(E, \boldsymbol{k}_\perp)$ as stated in equation (2.3.6) has to be integrated over a path conserving the energy E on the one hand and the wave-vector $\boldsymbol{k}_\perp$ perpendicular to the tunneling direction on the other hand. A dispersion relation $E(k)$ as a function of the norm k of the wave-vector $\boldsymbol{k}$ is required which links the states of the valence band to the states of the conduction band and is valid within the band gap E_g in parallel [29]:

$$E_\pm = \frac{E_\mathrm{g}}{2} + \frac{\hbar^2 k^2}{2m_0} \pm \frac{1}{2}\sqrt{E_\mathrm{g}^2 + \frac{E_\mathrm{g}\hbar^2 k^2}{m_\mathrm{r}}}, \tag{2.3.7}$$

where $\hbar = \frac{h}{2\pi}$ denotes the reduced PLANCK constant. The energy of valence and conduction band respectively is given as the difference of the total energy and the energy arising from the electric field, $E_\pm = E - eFx$. The reduced tunneling mass in turn can be expressed by the reciprocal of the effective masses of valence and conduction band, $m_r = \left(\frac{1}{m_v} + \frac{1}{m_c}\right)^{-1}$. Assuming the contribution from the kinetic energy $\frac{\hbar^2 k^2}{2m_0}$ as negligible within the band gap E_g, equation (2.3.7) simplifies to:

$$E_\pm \approx \frac{E_\mathrm{g}}{2} \pm \frac{1}{2}\sqrt{E_\mathrm{g}^2 + \frac{E_\mathrm{g}\hbar^2 k^2}{m_\mathrm{r}}}, \tag{2.3.8}$$

where the norm of the total wave-vector $\boldsymbol{k} = \boldsymbol{k}_x + \boldsymbol{k}_\perp$ can be expressed as $k^2 = k_x^2 + k_\perp^2 = \mathrm{Re}\left(k_x\right)^2 + \mathrm{Im}\left(k_x\right)^2 + k_\perp^2$ with k_x being solely imaginary within the band gap E_g. The non-zero contribution of $k_\perp$ keeps k_x imaginary over an even longer path as compared to the classical tunneling distance $\frac{E_\mathrm{g}}{eF}$, resulting in a larger effective band gap E_g and thus, in a reduced transmission probability $T(E, \boldsymbol{k}_\perp)$ for large values of $k_\perp$. In order to enable tunneling, the energy of valence and conduction band respectively has be compensated by the energy of the electric field, $E_\pm = eFx$, allowing for equation (2.3.8) to be transformed into:

$$\mathrm{Im}\left(k_x\right) = \sqrt{\frac{m_\mathrm{r}}{E_\mathrm{g}\hbar^2}}\sqrt{E_\mathrm{g}^2 + \frac{E_\mathrm{g}\hbar^2 k_\perp^2}{m_\mathrm{r}} - 4\left(eFx - \frac{E_\mathrm{g}}{2}\right)^2}. \tag{2.3.9}$$

Plugging equation (2.3.9) into equation (2.3.6) and setting the limits of the integral to $x_1 = 0$ and $x_2 = \frac{E_\mathrm{g}}{eF}$ finally allows for an evaluation of the transmission probability $T(E, \boldsymbol{k}_\perp)$:

$$T(E, \boldsymbol{k}_\perp) = \frac{\pi^2}{9} \exp\left(-\frac{\pi^2\sqrt{m_\mathrm{r}}E_\mathrm{g}^{3/2}}{ehF}\right) \exp\left(-\frac{h\sqrt{E_\mathrm{g}}}{4e\sqrt{m_\mathrm{r}}F}k_\perp^2\right). \tag{2.3.10}$$

Combining equations (2.3.5) and (2.3.10) yields an integral which can be solved analytically by means of the relation $\int_{-\infty}^{\infty} \mathrm{d}x \, \exp\left(-ax^2\right) = \sqrt{\frac{\pi}{a}}$. Thus, the generation rates G of electrons and holes in the limit of both a constant and uniform electric field F can be expressed as:

$$G = \frac{2\pi e^2 \sqrt{m_\mathrm{r}}}{9h^2\sqrt{E_\mathrm{g}}} F^2 \exp\left(-\frac{\pi^2\sqrt{m_\mathrm{r}} E_\mathrm{g}^{3/2}}{ehF}\right) = AF^2 \exp\left(-B/F\right), \tag{2.3.11}$$

with $A = A\left(E_\mathrm{g}, m_\mathrm{r}\right)$ and $B = B\left(E_\mathrm{g}, m_\mathrm{r}\right)$ being material dependent parameters. Thus, equation (2.3.11) provides a sufficient approach in comparing BTBT in different semiconductors as a function of the material dependent parameters A and B. However, the corresponding BTBT currents derived from KANE's semiclassical, local model tend to be overestimated due to the assumption of both a constant and uniform electric field F, allowing for BTBT currents flowing even when no drain voltage V_d is applied since generation rates G of electrons and holes are only a function of the electric field F, but not of the drain voltage V_d. Non-local models as implemented in TCAD may encounter this issue by numerical integration. In this concept, the tunneling distance is no longer determined by a local electric field F, but by the bending of valence and conduction band due to a gradient of the electrostatic potential Φ [30]. As a consequence, a local model does not distinguish between the generation rate G_h of holes and the generation rate G_e of electrons, resulting in the highest generation rates G of electrons and holes occurring within the band gap E_g, whereas a non-local model enables a generation rate G_h of holes at the beginning and a generation rate G_e of electrons at the end of the tunneling path as presented in figure 2.3.2.

2.3.2 Phonon Assisted BTBT

The tunneling probability as derived from KANE's semiclassical, local model describes BTBT in semiconductors exhibiting a direct band gap E_g. This direct band gap E_g can be overcome by proceeding along the imaginary axis ik while keeping the same point k in momentum space $\boldsymbol{k}$ as indicated in figure 2.3.3. In this concept, valence and conduction bands meet at a branch point k_d on the imaginary axis where a direct transition from the one into the other band takes place. However, in semiconductors with an indirect band gap E_g such as Si or Ge, an interaction with phonons is required in order to enable a transition between valence and conduction band in accordance with momentum conservation. Thus, phonon scattering bridges the gap between the two branch points k_i and k_i' and allows for indirect BTBT. In case of Si and Ge, the main contribution to phonon assisted BTBT arises from the interaction with transverse acoustic phonons due to their highest phonon occupation number and smallest phonon energy [31]. Phonon scattering results in an earlier onset of phonon assisted BTBT as compared to direct BTBT, introducing a stronger dependency of the generation rates G of electrons and holes on the electric field F as considered in equation (2.3.11) by changing the exponent from 2 to 2.5 as follows:

$$G = A_\mathrm{ind} F^{2.5} \exp\left(-B_\mathrm{ind}/F\right). \tag{2.3.12}$$

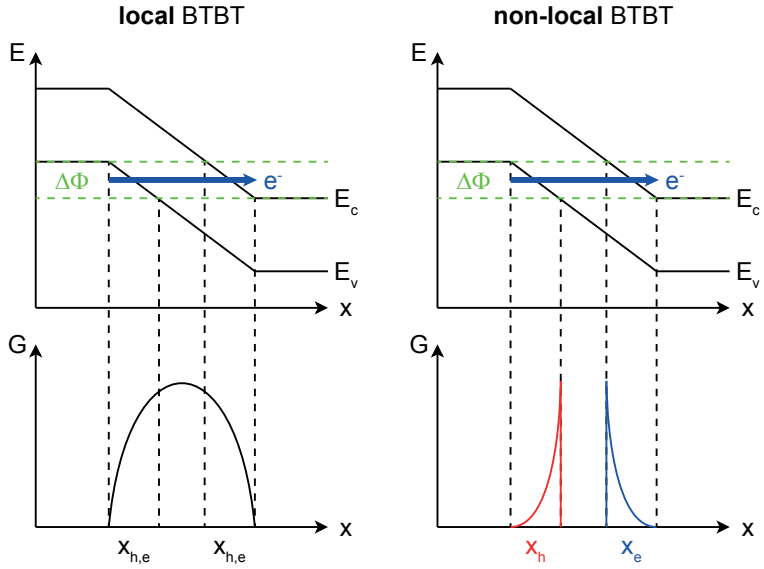


Figure 2.3.2: Schematic illustration of the respective generation rates G of electrons and holes as a function of the position x in case of a local or a non-local BTBT model. A local model does not distinguish between the generation G_h of holes and the generation G_e of electrons, resulting in the highest generation rates G of electrons and holes occurring within the band gap E_g, whereas a non-local model enables a generation G_h of holes at the beginning and a generation G_e of electrons at the end of the tunneling path.

The material dependent parameters A_ind and B_ind have to be adjusted as well in order to account for the interaction with phonons:

$$A_\mathrm{ind} = \frac{g e^{5/2} \left(1 + 2N_\mathrm{ta}\right) D_\mathrm{ta}^2 \left(m_\mathrm{DOS,v} m_\mathrm{DOS,c}\right)^{3/2}}{2^{21/4} h^{5/2} \rho E_\mathrm{ta} m_\mathrm{r}^{5/4} E_\mathrm{g}^{7/4}} \quad \text{and} \quad B_\mathrm{ind} = \frac{2^{7/2} \pi m_\mathrm{r}^{1/2} E_\mathrm{g}^{3/2}}{3eh}, \tag{2.3.13}$$

with N_ta being the phonon occupation number, D_ta the phonon deformation potential and E_ta the energy of transverse acoustic phonons. The density of the semiconductor itself is denoted by ρ. In addition, a degeneracy factor $g = 2g_\mathrm{v}g_\mathrm{c}$ is introduced in order to account for the degeneracy of spin and the degeneracy of different valleys in valence and conduction band respectively with the latter requiring an introduction of effective density of state (DOS) masses $m_\mathrm{DOS,v}$ and $m_\mathrm{DOS,c}$ of valence and conduction band respectively.

2.3.3 Trap Assisted Tunneling

Similar to phonon assisted BTBT, trap assisted tunneling (TAT) enables a tunneling process without an energy overlap $\Delta\Phi$ of valence and conduction band already established by an external electrical field F, also resulting in an earlier onset of TAT as compared to direct

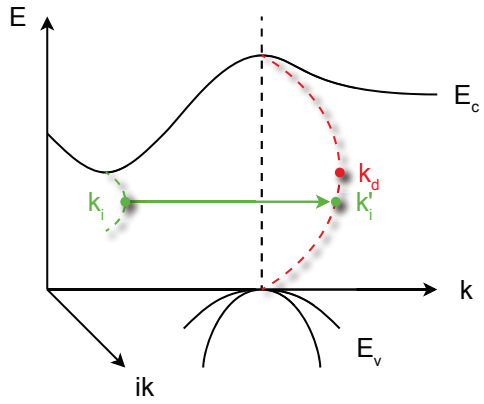


Figure 2.3.3: Schematic illustration of a direct and an indirect BTBT process. A direct band gap E_g can be overcome by proceeding along the imaginary axis ik while keeping the same point k in momentum space $\boldsymbol{k}$. Valence and conduction band meet at a branch point k_d on the imaginary axis where a direct transition from the one into the other band takes place. In case of an indirect band gap E_g, an interaction with phonons is required in order to enable a transition between valence and conduction band in accordance with momentum conservation. Thus, phonon scattering bridges the gap between the two branch points k_i and k_i' and allows for indirect BTBT.

BTBT. Carriers from the source tunnel into trap states of an energy E_t within the band gap E_g of the channel and reach its bands by thermal excitation from these trap states as shown in figure 2.3.4 [32]. Trap states can be introduced by traps at the interface of the oxide, defects due to ion implantation at the tunneling junction or dopants themselves. TAT arising from the latter will be discussed in more detail in chapter 3.2.2.

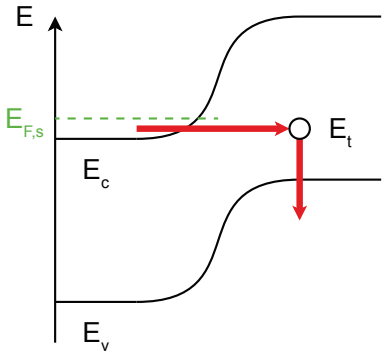


Figure 2.3.4: Schematic illustration of a TAT process. Carriers from the source tunnel into trap states of an energy E_t within the band gap E_g of the channel and reach its bands by thermal excitation from these trap states.

Since the excitation of carriers from trap states into the channel is based on thermionic emission, a dependency on the FERMI distribution function arises. As a consequence, the band-pass filter like behavior of a TFET is lost, degrading the lower limit of the subthreshold swing SS to 60 mV/dec as in case of a MOSFET.

2.3.4 Shockley-Read-Hall Recombination

The recombination of electrons from the conduction band with holes from the valence band by means of trap states of an energy E_t within the band gap E_g is known as SHOCKLEY-READ-HALL (SRH) recombination [33, 34]. The process describes a non-radiative recombination, being much more probable than direct recombination since less energy is needed for activation. The energy released during this recombination process is consumed by lattice vibrations. The resulting recombination rate R can be calculated as:

$$R = \frac{np - n_\mathrm{i}^2}{(n + n_0)\,\tau_\mathrm{p} + (p + p_0)\,\tau_\mathrm{n}}, \tag{2.3.14}$$

with

$$n_0 = n_\mathrm{i} \exp\left(\frac{E_\mathrm{t} - E_\mathrm{F}}{k_\mathrm{B}T}\right) \quad \text{and} \quad p_0 = n_\mathrm{i} \exp\left(\frac{E_\mathrm{F} - E_\mathrm{t}}{k_\mathrm{B}T}\right), \tag{2.3.15}$$

where n and p denote the carrier concentrations of electrons and holes respectively and τ_n and τ_p their corresponding lifetimes. The energy E_t of the trap states is given with respect to the FERMI energy E_F. Moreover, the intrinsic carrier concentration n_i of a semiconductor can be expressed as [27]:

$$n_\mathrm{i} = \sqrt{N_\mathrm{c} N_\mathrm{v}} \exp\left(-\frac{E_\mathrm{g}}{2k_\mathrm{B}T}\right), \tag{2.3.16}$$

with N_c and N_v being the DOS in conduction and valence band respectively. Equation (2.3.16) reveals an increase of the intrinsic carrier concentration n_i of the semiconductor with decreasing band gap E_g [35].

In case of TFET operation as described in chapter 2.3, the p-i-n structure is operated in reverse bias conditions, resulting in electrons from the channel flowing to the n^+-doped region and holes from the channel to the p^+-doped region respectively as depicted in figure 2.3.5. Subsequently, the carrier concentrations n and p of electrons and holes are decreased below the intrinsic carrier concentration n_i of the channel, enabling a negative recombination rate R as visible from equation (2.3.14). For this particular case, SRH generation exceeds SRH recombination and thus, determines the lower limit of the off-current I_off in a TFET. As a consequence, taking equation (2.3.16) into account, the use of materials with small(er) band gap E_g such as strained SiGe, Ge or GeSn requires a trade-off between an increased off-current I_off due to enabled SRH generation and an increased on-current I_on due to an improved probability for BTBT.

2.3.5 BTBT Mechanisms

The BTBT mechanism as described in chapter 2.3 is referred to in literature as point tunneling. Point tunneling occurs at the interface between source and channel with the latter

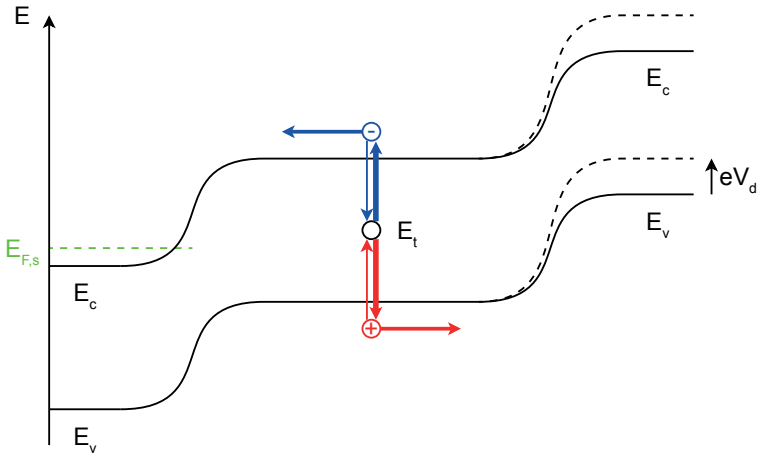


Figure 2.3.5: Schematic illustration of a SRH generation-recombination process. In case of TFET operation, the p-i-n structure is operated in reverse bias conditions, resulting in electrons from the channel flowing to the n^+-doped region and holes from the channel to the p^+-doped region respectively. Subsequently, the carrier concentrations n and p of electrons and holes are decreased below the intrinsic carrier concentration n_i of the channel, enabling a negative recombination rate R. For this particular case, SRH generation exceeds SRH recombination.

controlled by a gate and thus, is confined to a local area. In addition, when parts of the source region are also overlapped by the gate, line tunneling into a depleted region within the source as a second contribution to BTBT may set in. Naming of both BTBT mechanisms arises from the area where each tunneling process has its origin: While point tunneling starts from a single point at the interface between source and channel, the area for line tunneling resembles a line perpendicular to the gate electric field lines as illustrated in figure 2.3.6. As a consequence, line tunneling occurs in direction parallel with the gate electric field lines,

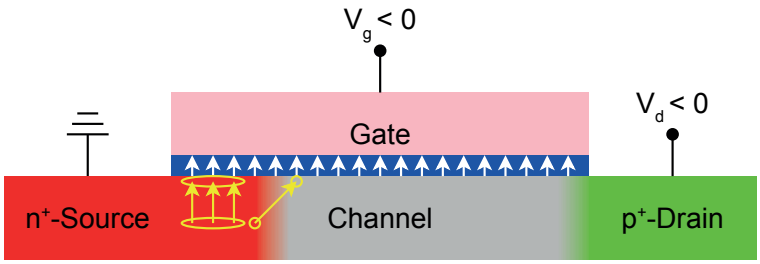


Figure 2.3.6: Schematic illustration of the point and line tunneling mechanism. Point tunneling starts from a single point at the interface between source and channel whereas the area for line tunneling resembles a line perpendicular to the gate electric field lines. As a consequence, line tunneling occurs in direction parallel with the gate electric field lines into a depleted region within the source overlapped by the gate.

enabling a diminished influence of the latter as compared to point tunneling and thus, accounting for the strong dependency of the generation rates G of electrons and holes on the electric field F in case of phonon assisted BTBT as already discussed in chapter 2.3.2.

In order to be able to quantify the respective dependencies of both BTBT mechanisms on the electric field F, their corresponding dependencies of the drain current I_d on the gate voltage V_g are derived by integrating the generation rates G of electrons and holes as stated in equation (2.3.11) over the volume V of the p-i-n structure:

$$I_\mathrm{d} = e \int_V \mathrm{d}V\, G = e \int_V \mathrm{d}V\, AF^2 \exp\left(-B/F\right). \tag{2.3.17}$$

Assuming direct BTBT as indicated in equation (2.3.17) due to the exponent of the electric field F being equal to 2, the dependency of the drain current I_d on the gate voltage V_g in case of point tunneling can be approximated as [36]:

$$I_\mathrm{d} \propto V_\mathrm{g}^4 \exp\left(1/V_\mathrm{g}\right), \tag{2.3.18}$$

resulting in a dependency of the subthreshold swing SS on the gate voltage V_g as follows:

$$SS = \left[\frac{\partial \log I_\mathrm{d}}{\partial V_\mathrm{g}}\right]^{-1} \propto V_\mathrm{g}. \tag{2.3.19}$$

Equation (2.3.19) reveals a linear increase of the subthreshold swing SS as a function of the gate voltage V_g, allowing for small values of the subthreshold swing SS only for small gate voltages V_g. In contrast to point tunneling, the dependency of the drain current I_d on the gate voltage V_g in case of line tunneling can be approximated as [37, 36]:

$$I_\mathrm{d} \propto \sqrt{V_\mathrm{g} - V_\mathrm{onset}} \exp\left(\sqrt{V_\mathrm{g} - V_\mathrm{onset}}\right), \tag{2.3.20}$$

where V_onset denotes the onset voltage as a measure of the gate voltage V_g required in order to deplete parts of the source region directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines. The corresponding dependency of the subthreshold swing SS on the gate voltage V_g yields:

$$SS = \left[\frac{\partial \log I_\mathrm{d}}{\partial V_\mathrm{g}}\right]^{-1} \propto \sqrt{V_\mathrm{g} - V_\mathrm{onset}} \approx \sqrt{V_\mathrm{onset}} + \mathcal{O}\left(V_\mathrm{g}\right). \tag{2.3.21}$$

As already indicated, equation (2.3.21) reveals a less pronounced dependency of the subthreshold swing SS on the gate voltage V_g in case of line tunneling as compared to point tunneling due to a root dependency instead of a linear relation. Taking the Taylor series for an expansion at small gate voltages V_g into account, the subthreshold swing SS in case of line tunneling can be assumed as constant with its lower limit depending only on the root of the onset voltage $\sqrt{V_\mathrm{onset}}$. Thus, good electrostatic control is required in order to minimize the value of the onset voltage V_onset with the latter mainly determined by the band gap E_g, the thickness t_ox of the gate oxide and the carrier concentration n_s of the source which has to be depleted in a region directly underneath the gate in order to allow for line

tunneling aligned with the gate electric field lines [37, 36]. For both BTBT mechanisms, no direct dependency of the subthreshold swing SS on the temperature T is obvious due to the band-pass filter like behavior of a TFET, being a major difference as compared to a MOSFET where the lower limit of the subthreshold swing SS is determined by the high and low energy tale of the FERMI distribution function.

2.4 Design Considerations

TFETs are discussed as a promising concept for low-power electronics, but still suffer from low on-currents I_{on} as compared to state of the art MOSFETs. In addition, their usage in CMOS applications is still quite limited due to the inherent ambipolar switching of TFETs. This ambipolar switching arises from the symmetry of the p-i-n structure that defines a TFET. Thus, BTBT in a TFET occurs not only at the source junction but also at the drain junction depending on the actual gate voltage V_g applied to the channel. The ambipolarity of a TFET becomes even more pronounced when contributions from phonon assisted BTBT and TAT come into play. Due to their earlier onset as compared to direct BTBT, the resulting n- and p-branch of the transfer characteristics move closer together. For n- and p-branch intersecting, the off-current I_{off} of the TFET is increased as compared to pure SRH generation, resulting in a degraded static power consumption P_{static} as visible from equation (2.1.2).

Both problems of low on-currents I_{on} as well as the ambipolar switching can be tackled in parallel by introducing materials with small(er) band gap E_g such as strained SiGe, Ge or GeSn at the source tunnel junction of the TFET, allowing for a heterostructure device concept. In contrast to a homostructure, a heterostructure may suppress the ambipolar switching due to the symmetry of the p-i-n structure lifted while enabling an enhanced probability for BTBT and increased on-current I_{on} due to a reduction of the band gap E_g in parallel. However, this reduced band gap E_g might increase the off-current I_{off} of the TFET due to increased SRH generation as already pointed out in chapter 2.3.4. Within the framework of this thesis, compressively strained SiGe as the material with smaller band gap E_g of choice and its influence on the performance of a TFET will be examined. As a further possibility to tune the probability for BTBT and the on-current I_{on} of a TFET without a simultaneous increase of the off-current I_{off}, an optimization of the electrostatic control with respect to the gate oxide is suggested. As already highlighted in chapter (2.3.5), especially line tunneling aligned with the gate electric field lines requires optimized electrostatic control due to its dependency on an onset voltage V_{onset}, allowing for an improved subthreshold swing SS as compared to point tunneling.

2.4.1 Strain Engineering

When growing SiGe pseudomorphically on Si, compressive, biaxial strain ε is introduced into the SiGe layer due to the lattice mismatch between Si and Ge. In this regard, the lattice

constant $a_{0,\mathrm{SiGe}}(x)$ of relaxed SiGe as a function of the Ge mole fraction x can be obtained by the following analytical expression based on VEGARD's empirical law [38]:

$$a_{0,\mathrm{SiGe}}(x) = a_{0,\mathrm{Si}} + 0.200326x(1-x) + (a_{0,\mathrm{Ge}} - a_{0,\mathrm{Si}})x^2, \tag{2.4.1}$$

with $a_{0,\mathrm{Si}} = 5.43\,\text{Å}$ and $a_{0,\mathrm{Ge}} = 5.65\,\text{Å}$ denoting the lattice constants of Si and Ge respectively at room temperature $T = 300\,\mathrm{K}$. The resulting band structure of relaxed SiGe can be approximated as Si-like for Ge mole fractions up to $x \leq 0.85$ [39], enabling an indirect transition stemming from the band gap E_g between Γ and Δ being the dominant contribution to BTBT. The according band gap $E_{\mathrm{g,SiGe}}(x)$ of relaxed SiGe as a function of the Ge mole fraction x can be approximated as [40]:

$$E_{\mathrm{g,SiGe}}(x) = E_{\mathrm{g,Si}} - 0.454x + 0.208x^2, \tag{2.4.2}$$

where $E_{\mathrm{g,Si}} = 1.11\,\mathrm{eV}$ denotes the band gap of relaxed Si at room temperature $T = 300\,\mathrm{K}$. Equation (2.4.2) reveals a decreasing band gap $E_{\mathrm{g,SiGe}}(x)$ for increasing Ge mole fractions x. The compressive, biaxial strain ε introduced by the pseudomorphic growth breaks the lattice symmetry of the relaxed SiGe layer, lifting both the degeneracy of the Δ_6 conduction band valleys as well as the degeneracy of LH and HH bands stemming from the Γ valley. The Δ_6 conduction band valleys split into Δ_4 and Δ_2 valleys with the former lowered in energy whereas the HH band is increased in energy with respect to the LH band. Thus, the band gap E_g of compressively, biaxially strained SiGe is determined by the difference of the Δ_4 conduction band valleys and the HH band as presented in figure 2.4.1. While the conduction band offset ΔE_c between the strained SiGe layer and the Si substrate is mainly determined by the difference in their electron affinities χ and thus, can be assumed as negligible, the valence band offset at room temperature $T = 300\,\mathrm{K}$ scales linearly as a function of the Ge mole fraction according to $\Delta E_\mathrm{v} \approx 0.74x$ [42], resulting in a p-type configuration being the more favorable one in terms of an energy overlap $\Delta\Phi$ as a tunneling window to be established. In addition, the electron effective masses m_c of the Δ_4 valleys do not change significantly as a function of the Ge mole fraction x or strain ε [43]. Even though the band gap E_g of compressively, biaxially strained SiGe is further reduced as compared to relaxed SiGe, phonon assisted BTBT still remains the dominant transition for Ge mole fractions up to $x \leq 0.7$ with higher Ge mole fractions $x > 0.7$ constrained due to the critical thickness caused by the lattice mismatch between Si and Ge [42]. The resulting degeneracy factor for phonon assisted BTBT according to equation (2.3.13) can be specified as $g = 2g_\mathrm{v}g_\mathrm{c} = 2 \cdot 1 \cdot 4 = 8$ with respect to spin, the non-degenerate HH band and the fourfold degenerate Δ_4 conduction band valleys.

2.4.2 EOT Scaling

In order to quantify the electrostatic control in a single-gate transistor with respect to the gate oxide, the screening length λ_ch as one solution of POISSON's equation can be taken into account [44]:

$$\lambda_\mathrm{ch} = \sqrt{\frac{\kappa_\mathrm{sc}}{\kappa_\mathrm{ox}} t_\mathrm{sc} t_\mathrm{ox}}, \tag{2.4.3}$$

with κ_sc and κ_ox being the dielectric constants of the semiconductor and the gate oxide respectively and t_sc and t_ox denoting their respective layer thicknesses. Equation (2.4.3)

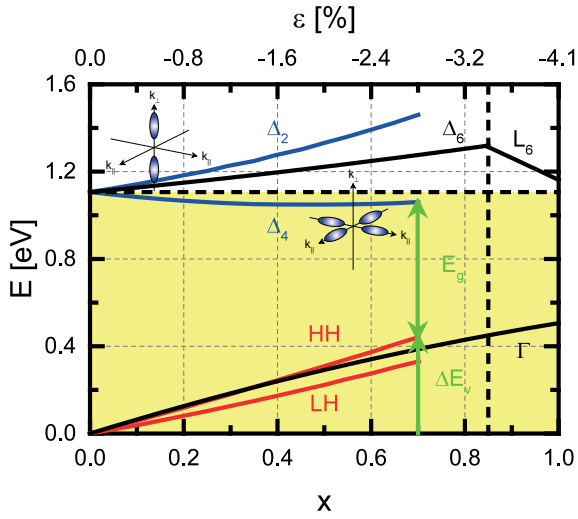


Figure 2.4.1: Schematic illustration of the band structures of relaxed and strained SiGe as a function of the Ge mole fraction x and the corresponding compressive biaxial strain ε within the SiGe layer based on nonlocal empirical pseudopotential method (EPM) calculations [41, 40, 42]. The band structure of relaxed SiGe changes from Si-like into Ge-like at a Ge mole fraction x of about 0.85 as indicated by a dashed vertical line. The dashed horizontal line in turn depicts the band gap E_g of Si at room temperature $T = 300\,\mathrm{K}$ as a reference level for the valence band offset ΔE_v. Compressive, biaxial strain ε introduced by the pseudomorphic growth breaks the lattice symmetry of the relaxed SiGe layer, lifting both the degeneracy of the Δ_6 conduction band valleys as well as the degeneracy of LH and HH bands stemming from the Γ valley. The Δ_6 conduction band valleys split into Δ_4 and Δ_2 valleys with the former lowered in energy whereas the HH band is increased in energy with respect to the LH band. Thus, the band gap E_g of compressively, biaxially strained SiGe is determined by the difference of the Δ_4 conduction band valleys and the HH band.

reveals a reduced screening length λ_{ch} for either a decreased thickness t_{sc} of the semiconductor, a decreased thickness t_{ox} of the gate oxide or an increased dielectric constant κ_{ox} of the gate oxide itself. However, decreasing the thickness t_{ox} of the gate oxide may result in an increased gate leakage, degrading the off-current I_{off} and consequently, the subthreshold characteristics of a TFET. In this regard, the introduction of dielectrics with a higher relative permittivity κ_{ox} enables an appropriate way to reduce the screening length λ_{ch} while keeping the thickness t_{ox} of the gate oxide layer constant, allowing for an overall improved electrostatic control. In 2007, HfO_2 as such a high-κ dielectrics with a relative permittivity of $\kappa_{HfO_2} \approx 25$ was introduced by Intel Corporation in their 45 nm node [2]. However, the growth of high-κ dielectric layers still remains challenging due to the formation of an interfacial oxide layer. In case of Si, this interfacial oxide layer consists of SiO_2 with its low relative permittivity of $\kappa_{SiO_2} \approx 3.9$, diminishing the intended effect of a high-κ dielectric.

Within the framework of this thesis, the introduction of Al_2O_3 as an interlayer between Si and HfO_2 is investigated. On the one hand, Al_2O_3 provides a relative permittivity of $\kappa_{Al_2O_3} \approx 9$ being more than two times larger than in case of pure SiO_2 and on the other

hand, Aluminium (Al) is known to act as a diffusion barrier, resulting in a decreased thickness of the interfacial oxide layer in ideal case [45, 46]. In order to evaluate the influence of an Al_2O_3 interlayer on the electrostatic control, capacitance-voltage (CV) measurements on MOS capacitors incorporating three different gate oxide compositions, namely 3 nm Al_2O_3, 3 nm HfO_2 and 1 nm Al_2O_3 + 2 nm HfO_2, are performed, granting information about both the gate capacitance C as well as the leakage current I of each MOS capacitor. In this regard, the respective capacitance C_{acc} in accumulation of each MOS capacitor corresponds to the capacitance C_{ox} of its gate oxide and can be assumed as:

$$C_{\mathrm{acc}} = C_{\mathrm{ox}} = \kappa_0 \kappa_{\mathrm{ox}} \frac{A}{t_{\mathrm{ox}}}, \tag{2.4.4}$$

with κ_0 being the vacuum permittivity and A denoting the area of the capacitor. Equation (2.4.4) reveals an increased capacitance C_{ox} of the gate oxide for an increased dielectric constant κ_{ox}. Both the resulting area-normalized gate capacitance $\frac{C}{A}$ of the MOS capacitor and its area-normalized leakage current $\frac{I}{A}$ are plotted as a function of the gate voltage V_{g} corrected by the respective flat-band voltage V_{fb} of each gate stack composition at a frequency f of 100 kHz as shown in figure 2.4.2. In this regard, the flat-band voltage V_{fb} as a measure of the difference of the work functions of the gate metal and the semiconductor can be determined as the maximum of the reciprocal of the second derivative of the gate capacitance C with respect to the gate voltage V_{g} [47]. In addition, in order to account for a possible frequency dispersion arising in accumulation, a compensation of the series resistance is applied beforehand [48]. Pure HfO_2 reveals not only the highest area-normalized capacitance $\frac{C_{\mathrm{acc}}}{A}$ in accumulation at a gate voltage of $V_{\mathrm{g}} = V_{\mathrm{fb}} - 1\,\mathrm{V}$ but also the highest area-normalized leakage current $\frac{I_{\mathrm{acc}}}{A}$ in accumulation. Instead of the area-normalized capacitance

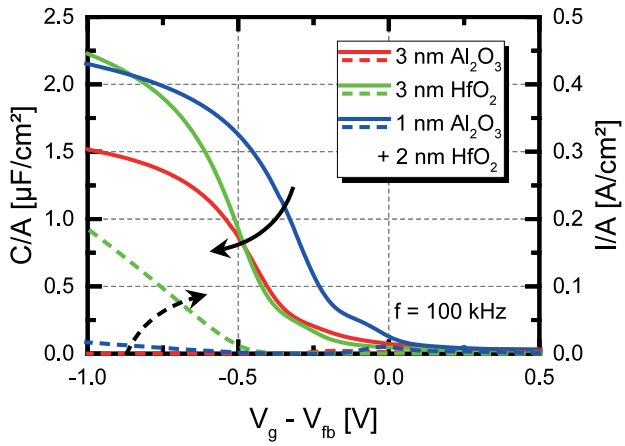


Figure 2.4.2: Measured area-normalized gate capacitance $\frac{C}{A}$ of the MOS capacitor as well as its area-normalized leakage current $\frac{I}{A}$ as a function of the gate voltage V_{g} corrected by the respective flat-band voltage V_{fb} of each gate stack composition at a frequency f of 100 kHz. Pure HfO_2 reveals not only the highest area-normalized capacitance $\frac{C_{\mathrm{acc}}}{A}$ in accumulation at a gate voltage of $V_{\mathrm{g}} = V_{\mathrm{fb}} - 1\,\mathrm{V}$ but also the highest area-normalized leakage current $\frac{I_{\mathrm{acc}}}{A}$ in accumulation.

$\frac{C_{acc}}{A}$ in accumulation, the use of the equivalent oxide thickness (EOT) is more convenient in order to compare the three different gate stack compositions. In this regard, the EOT is a measure of how thick a gate stack consisting of pure SiO_2 needs to be in order to reach the same area-normalized capacitance $\frac{C_{acc}}{A}$ in accumulation as the gate stack having high-κ dielectrics incorporated and can be calculated from the capacitance equivalent thickness (CET) plus a quantum mechanical correction as follows:

$$\mathrm{EOT} = \mathrm{CET} - \mathrm{QM_{corr}} = \frac{\kappa_0 \kappa_{SiO_2}}{\frac{C_{acc}}{A}} - 0.4\,\mathrm{nm}, \tag{2.4.5}$$

with $\mathrm{QM_{corr}} = 0.4\,\mathrm{nm}$ being the quantum mechanical correction in case of Si [49]. Figure 2.4.3 summarizes the obtained values of the EOT, plotting the area-normalized leakage current $\frac{I_{acc}}{A}$ in accumulation as a function of the EOT for all three different gate oxide compositions. At first, the values of the EOT in case of pure HfO_2 and the combination of Al_2O_3 and HfO_2 are comparable in the range of 1.2 nm, suggesting a reduction of the interfacial layer by the presence of Al_2O_3 in order to compensate for its lower relative permittivity as compared to pure HfO_2, $\kappa_{Al_2O_3} < \kappa_{HfO_2}$. Even more important, the combination of Al_2O_3 and HfO_2 reveals an one order of magnitude lower area-normalized leakage current $\frac{I_{acc}}{A}$ in accumulation as compared to pure HfO_2, allowing for a decreased off-current I_{off} and thus, improved subthreshold characteristics as a key advantage for TFET operation.

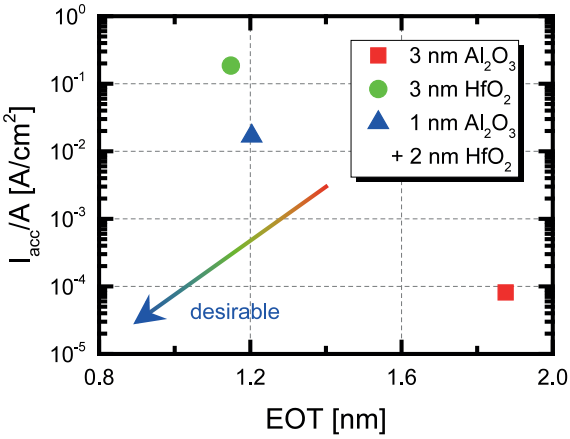


Figure 2.4.3: Measured area-normalized leakage current $\frac{I_{acc}}{A}$ in accumulation as a function of the EOT for all three different gate oxide compositions. At first, the values of the EOT in case of pure HfO_2 and the combination of Al_2O_3 and HfO_2 are comparable in the range of 1.2 nm, suggesting a reduction of the interfacial layer by the presence of Al_2O_3 in order to compensate for its lower relative permittivity as compared to pure HfO_2, $\kappa_{Al_2O_3} < \kappa_{HfO_2}$. Even more important, the combination of Al_2O_3 and HfO_2 reveals an one order of magnitude lower area-normalized leakage current $\frac{I_{acc}}{A}$ in accumulation as compared to pure HfO_2, allowing for a decreased off-current I_{off} and thus, improved subthreshold characteristics as a key advantage for TFET operation.

3 Vertical SiGe/Si Heterostructure TFETs

This chapter deals with the concept of a vertical SiGe/Si heterostructure TFET which makes use of strained SiGe as a material with smaller band gap E_g at the source tunnel junction in order to increase the probability for BTBT while suppressing the ambipolar switching characteristics in parallel due to the use of Si with its higher band gap E_g as compared to SiGe at the drain tunnel junction, enabling a heterostructure device concept. In addition, the vertical SiGe/Si heterostructure TFET benefits from in-situ doping of source and drain during growth in order to allow for a low density of defects at the source tunnel junction and thus, a diminished influence of TAT as compared to common ion implantation. Furthermore, the vertical SiGe/Si heterostructure TFET serves as a proof of concept for further integration of materials with small band gap E_g such as strained Ge or GeSn which allow for a direct band gap E_g transition into a three-dimensional device structure while maintaining a Si compatible technology [18].

3.1 Device Fabrication

Vertical SiGe/Si heterostructure n-TFETs were fabricated on a Si/SiGe layer stack pseudomorphically grown on a 15 nm Silicon on insulator (SOI) substrate by means of a reduced pressure chemical vapor deposition (RPCVD) reactor [50]. The source of the vertical SiGe/Si heterostructure n-TFET is defined by 15 nm p^+-Si, followed by 20 nm compressively, biaxially strained p^{++}-$Si_{0.45}Ge_{0.55}$. Intrinsic Si with a thickness of 60 nm serves as the channel whereas the drain is realized by 20 nm n^+-Si, thus realizing a heterostructure device concept. Due to in-situ doping of source and drain during growth, both a high carrier concentration n and a low density of defects are enabled as compared to common ion implantation. In this regard, the active carrier concentration n is characterized by means of secondary ion mass spectrometry (SIMS) and electrochemical capacitance-voltage (ECV) measurements as depicted in figure 3.1.1, highlighting both a sharp doping profile with a steepness λ_s of about 3 nm/dec in direction to the Si channel and a high carrier concentration n up to $4 \times 10^{20}\,\mathrm{cm}^{-3}$ within the SiGe source. The compressive, biaxial strain ε of about $-2\,\%$ in the SiGe layer due to the pseudomorphic growth further reduces the band gap E_g as compared to relaxed SiGe, allowing for an overall enhanced probability for BTBT as already discussed in chapter 2.4.1. In order to enable high Ge mole fractions x incorporated into the lattice, the layers were grown at a low temperature T of 500 °C, defining the upper thermal budget for subsequent annealing steps. The subsequent process flow for the vertical SiGe/Si heterostructure n-TFET is sketched in detail in figure 3.1.2, being applicable to a p-TFET structure as well just by changing dopant types during growth of source and drain. However, the use of PH_3 as a precursor results in a higher background doping as compared to B_2H_6,

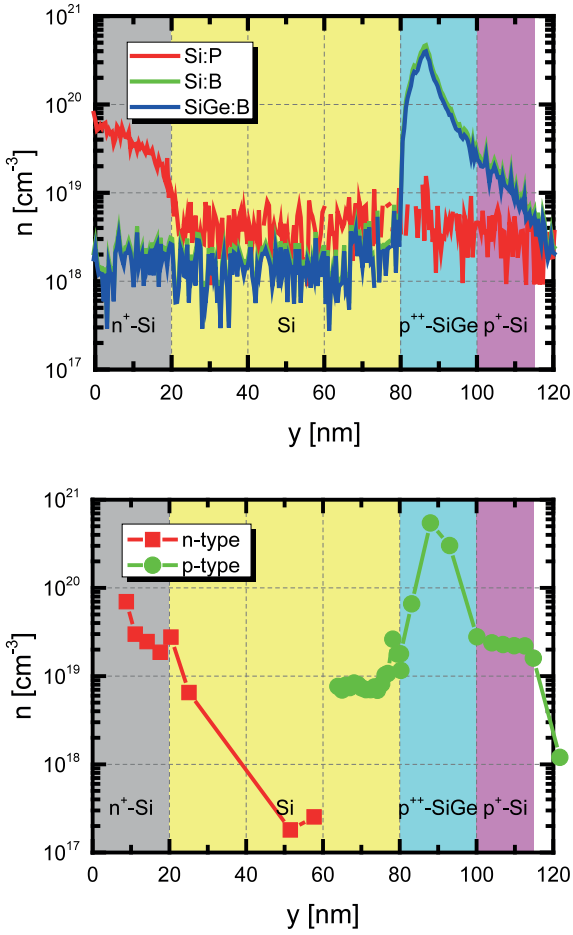


Figure 3.1.1: Doping profile of the vertical SiGe/Si heterostructure n-TFET measured by SIMS and ECV, revealing both a sharp doping profile with a steepness λ_s of about 3 nm/dec in direction to the Si channel and a high carrier concentration n up to $4 \times 10^{20}\,\mathrm{cm}^{-3}$ within the SiGe source.

thus facilitating growth of a n^+-doped SiGe layer in case of a p-TFET structure at the end of the process.

1. Pre-cleaning of the substrate was performed by rinsing in acetone and isopropyl alcohol (IPA) as organic solvents in an ultrasonic bath in order to remove photoresist covering the sample as a protection during sawing of the wafer into pieces with a size of 1.95 cm x 1.95 cm each. Subsequently, the sample was cleaned wet-chemically in Piranha etch solution consisting of $H_2SO_4 : H_2O_2$ (2 : 1) for 10 min, removing remaining photoresist residues as well as organic particles.

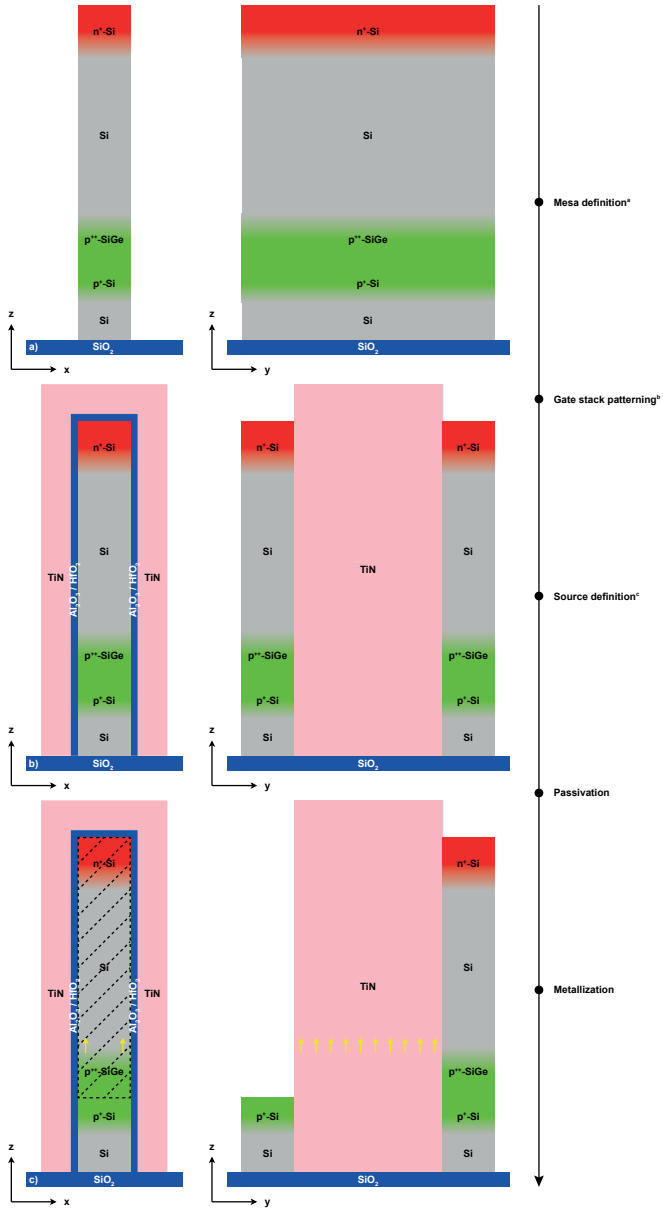


Figure 3.1.2: Process flow for the vertical SiGe/Si heterostructure n-TFET, highlighting mesa definition, gate stack patterning and source definition.

2. The sample was patterned with positive deep ultraviolet (DUV) photoresist UV6.06 in order to create marker squares with a size of 15 µm x 15 µm as a coordinate system for subsequent electron beam lithography steps. The marker pattern was etched by means of reactive ion etching (RIE) using a three step process consisting of a SF_6/O_2 plasma etching the top Si/SiGe layer stack, a CHF_3 plasma etching the buried oxide and a SF_6/Ar plasma etching parts of the Si substrate. The resulting marker depth is in the range of 900 nm to 1 µm.

3. Mesa definition in order to electrically isolate each transistor was realized by means of electron beam lithography. The sample was patterned with negative electron beam resist XR-1541 (HSQ) and subsequently etched by means of RIE in a Cl_2/Ar plasma including inductively coupled plasma (ICP) (see figure 3.1.2a). The use of a Cl_2/Ar plasma including ICP enables a high anisotropy of the etched facets even at room temperature $T = 300\,\mathrm{K}$.

4. The sample was cleaned by RIE in an O_2 plasma, followed by a wet-chemical etch consisting of hydrofluoric acid (HF) 1% and hydrochloric acid (HCl) 1% for 2 min in order to remove interfacial oxide layers as well as metallic residues accumulating at the side walls of the mesa. In this regard, standard RCA cleaning was omitted in order to avoid etching of the exposed parts of the SiGe layer due to an oxidizing reaction with H_2O_2 [51]. Subsequently, a high-κ/metal gate stack consisting of 1 nm Al_2O_3, 2 nm HfO_2 and 60 nm TiN was deposited by atomic layer deposition (ALD) and atomic vapor deposition (AVD) respectively.

5. The gate stack was patterned with negative electron beam resist XR-1541 (HSQ), followed by a dry etch of the TiN gate metal by means of RIE in a Cl_2/SF_6/Ar plasma including ICP. Remaining TiN spacers on the side walls of the mesa were etched wet-chemically by means of SC-1 solution consisting of $NH_3 : H_2O_2 : H_2O$ (1 : 1 : 5), being selective to the embedded HfO_2. Subsequently, HfO_2 and Al_2O_3 were etched wet-chemically making use of HF 1% acid for 2 min (see figure 3.1.2b). A scanning electron microscope (SEM) image as well as a transmission electron microscope (TEM) image of a processed device after gate stack patterning are shown in figures 3.1.3 and 3.1.4 respectively, revealing the TiN gate wrapped around the side walls of the fin with a high aspect ratio of about 1:5 with respect to a fin width W of about 20 nm as well as high crystalline quality of both the Si and the compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ layers.

6. The sample was patterned with positive electron beam resist AR-P 669.07 (PMMA 600K) in order to create an etching window only at the source side of the device. Both the n^+-Si and the intrinsic Si underneath were etched by means of RIE using a Cl_2/Ar plasma omitting ICP (see figure 3.1.2c). In this regard, omitting ICP allows for a slow, controllable etch rate.

7. The sample was passivated with a 50 nm thick layer of SiO_2 by means of a plasma enhanced chemical vapor deposition (PECVD) reactor at a temperature T of 350 °C. Subsequently, the sample was patterned with positive electron beam resist AR-P 669.07 (PMMA 600K) in order to create etching windows enabling contacts to source, gate

and drain. The etching of the SiO_2 layer was performed by means of RIE using a CHF_3 plasma.

8. The sample was patterned with positive electron beam resist AR-P 669.07 (PMMA 600K) in order to open windows for the metallization of source, gate and drain. Before the actual metallization, residual interfacial oxide on top of p^{++}-SiGe, TiN and n^+-Si respectively was removed by sputtering with Ar^+ ions. The metallization was performed by means of a physical vapor deposition (PVD) tool, sputtering layers of 3 nm Nickel (Ni) and 150 nm Al. In this regard, Ni was introduced as an interlayer in order to enable a silicidation of SiGe and Si respectively and thus, to decrease their contact resistance to Al.

9. A forming gas anneal (FGA) in an ambient of 4% H_2 and 96% N_2 was performed at a temperature T of 350 °C for 10 min in order to improve the quality of both the high-κ/metal gate stack and the contacts by saturating dangling bonds on the one hand and by enabling the silicidation of SiGe and Si respectively with Ni on the other hand.

It is worth mentioning that the process flow as just described results in a fin-like TFET structure, realizing electrostatic control by means of a double-gate at the side walls of the fin. Going from a fin to a vertical nanowire enables a gate-all-around (GAA) TFET structure benefiting from ideal electrostatic control due to a by a factor of $\sqrt{2}$ decreased screening length λ_{ch} as compared to a double-gate structure and thus, further boosting BTBT [52, 53].

3.2 Device Characterization and Simulation

This chapter presents the experimental results obtained from DC characterization of the vertical SiGe/Si heterostructure n-TFET. In advance, various TCAD simulations are per-

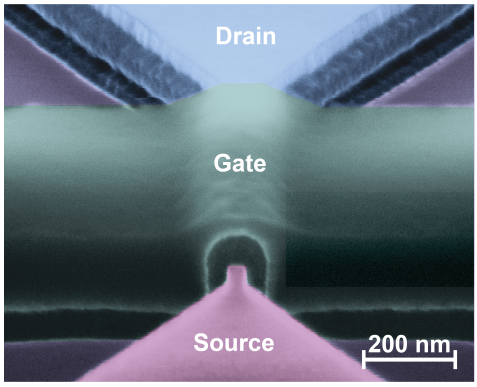


Figure 3.1.3: SEM image of the vertical SiGe/Si heterostructure n-TFET after gate stack patterning, revealing the TiN gate wrapped around the side walls of the fin with a high aspect ratio of about 1:5 with respect to a fin width W of about 20 nm.

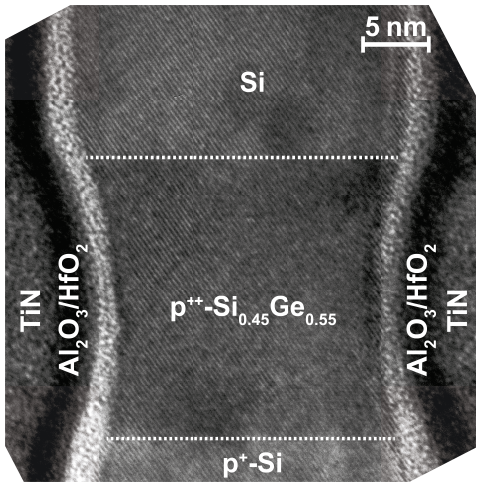


Figure 3.1.4: TEM image of the vertical SiGe/Si heterostructure n-TFET, revealing high crystalline quality of both the Si and the compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ layers.

formed in order to motivate the concept of the vertical SiGe/Si heterostructure n-TFET itself on the one hand and describe the physics emerging in this TFET structure on the other hand. Software of choice for the corresponding TCAD simulations is Sentaurus Device [30]. Models for drift-diffusion transport, FERMI statistics, TAT and doping-dependent SRH generation-recombination as well as dynamic non-local BTBT have been applied to self-consistently solve the POISSON and carrier continuity equations with specified boundary conditions. The corresponding parameters for BTBT in case of compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ are based on calibrations from [42] and have been adjusted by means of linear interpolation in order to match the specific Ge mole fraction x. The influence of the compressive, biaxial strain ε within the SiGe layer due to the pseudomorphic growth on the band structure has been taken into account by means of deformation potential theory based on parameters derived by nonlocal EPM calculations [54, 40], incorporating a multivalley band model including non-parabolicity for the Δ_4 conduction band valleys as well as for HH and LH band. Since the electron effective masses m_c of the Δ_4 conduction band valleys do not change significantly as a function of the Ge mole fraction x or strain ε as already discussed in chapter 2.4.1, only changes of the hole effective masses m_v and their corresponding DOS as a function of the compressive, biaxial strain ε had to be considered by 6-band $k \cdot p$ modeling of LH and HH band.

3.2.1 Design Considerations

A vertical SiGe/Si heterostructure TFET enables the integration of strained SiGe as a material with smaller band gap E_g into a Si compatible technology while maintaining a standardized process flow. Due to a heterostructure device concept, both a material with smaller band gap E_g at the source tunnel junction in order to increase the probability for BTBT and

a suppressed ambipolar switching characteristics can be realized in parallel. TCAD simulations allow for pointing out of these key advantages by comparing the transfer characteristics of a vertical SiGe/Si heterostructure TFET with those of a vertical Si or Ge homostructure TFET as illustrated in figure 3.2.1, assuming a p-type configuration without loss of generality. The corresponding carrier concentrations n_s and n_d of both source and drain were equally set to $1 \times 10^{20}\,\mathrm{cm}^{-3}$ in order to be able to evaluate any ambipolar switching characteristics arising in one of these TFET configurations. As further parameters for the TCAD simulations, the EOT was assumed as 1.2 nm in accordance with the EOT extracted from CV measurements on MOS capacitors as discussed in chapter 2.4.2 and the fin width W was set to 20 nm in accordance with the TEM analysis illustrated in figure 3.1.4. Subsequently, the gate metal work function was adjusted to match the onset of the vertical SiGe/Si heterostructure p-TFET at a gate voltage V_g of about 0 V, yielding a gate metal work function of 5.1 eV. A vertical Si homostructure p-TFET enables a low off-current I_{off} of the device due to its large band gap E_g of 1.11 eV at room temperature $T = 300\,\mathrm{K}$ but consequently, lacks in terms of a high on-current I_{on}, resulting in a still improvable ratio of on- to off-current $\frac{I_{on}}{I_{off}}$. A vertical Ge homostructure p-TFET in turn reveals a contrasting picture in terms of on-current I_{on} and off-current I_{off} respectively due to its much lower band gap E_g of 0.66 eV at room temperature $T = 300\,\mathrm{K}$ as compared to Si. Even though the off-current I_{off} of the vertical Ge homostructure p-TFET increases due to the low band gap E_g, the on-current I_{on} increases even more, thus enabling an improved ratio of on- to off-current $\frac{I_{on}}{I_{off}}$ as compared to the vertical Si homostructure p-TFET. However, the use of a homostructure results in a pronounced ambipolar switching characteristics, especially in case of the vertical Ge homostructure p-TFET, thus diminishing the usability of this kind of TFET device concept for CMOS applications. A vertical SiGe/Si heterostructure p-TFET in turn making use of strained SiGe as a material with smaller band gap E_g at the source tunnel junction combines

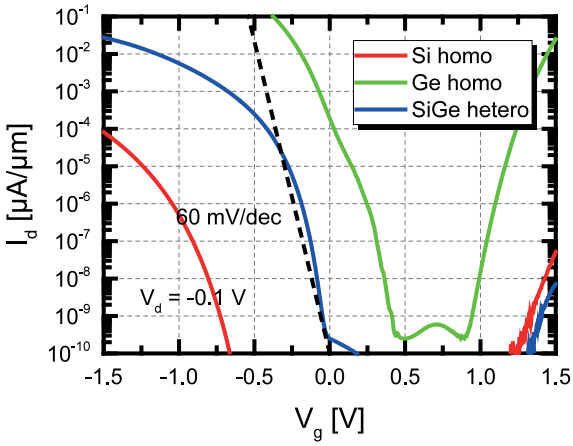


Figure 3.2.1: Simulated transfer characteristics of different vertical homo- and heterostructure p-TFETs at a drain voltage V_d of -0.1 V, highlighting the benefits of a vertical Si/SiGe heterostructure TFET in terms of a promising ratio of on- to off-current $\frac{I_{on}}{I_{off}}$ while suppressing the ambipolar switching characteristics in parallel.

both a high on-current I_{on} as in case of pure Ge and a low off-current I_{off} as in case of pure Si, resulting in a promising ratio of on- to off-current $\frac{I_{on}}{I_{off}}$ while suppressing the ambipolar switching characteristics in parallel.

In this regard, the n^+-SiGe source tunnel junction of the vertical SiGe/Si heterostructure p-TFET can be realized in two ways. On the one hand, a sharp transition between the n^+-SiGe source and the intrinsic Si channel describes the common way to define a heterostructure, while on the other hand, a grading of the Ge mole fraction x over a distinct length is conceivable as well. Grading of the Ge mole fraction x enables a smoothed band structure at the transition between SiGe and Si [55, 56], being beneficial for BTBT as visible from the simulated transfer characteristics and the corresponding band structure presented in figures 3.2.2 and 3.2.3. Especially in case of a p-TFET configuration, grading allows for a remarkable improvement by encountering the pronounced valence band offset ΔE_v between compressively, biaxially strained SiGe and Si as already discussed in chapter 2.4.1. In case of a n-TFET configuration, the beneficial impact of grading is less pronounced due to the negligible conduction band offset ΔE_c between compressively, biaxially strained SiGe and Si, becoming notably relevant for high Ge mole fractions $x > 0.5$ [42].

3.2.2 DC Characteristics

DC characterization at room temperature $T = 300\,\mathrm{K}$ is realized by means of a three terminal setup performed with a Keithley 4200-SCS parameter analyzer [57]. The measured transfer characteristics of both a graded and a non-graded vertical SiGe/Si heterostructure n-TFET are shown in figure 3.2.4. Both types of vertical SiGe/Si heterostructure n-TFETs exhibit

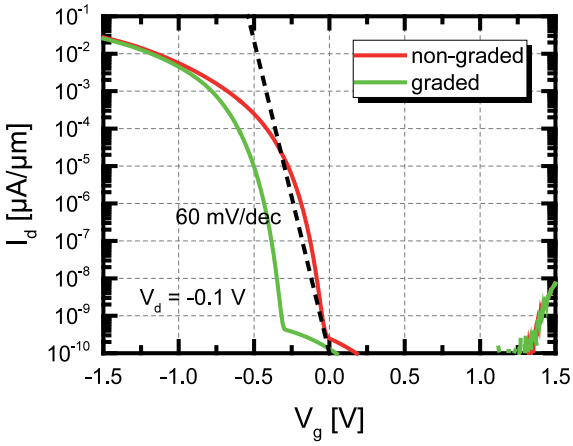


Figure 3.2.2: Simulated transfer characteristics of a non-graded and a graded vertical SiGe/Si heterostructure p-TFET at a drain voltage V_d of $-0.1\,\mathrm{V}$, revealing a higher on-current I_{on} in case of the graded vertical SiGe/Si heterostructure p-TFET due to an increased probability for BTBT.

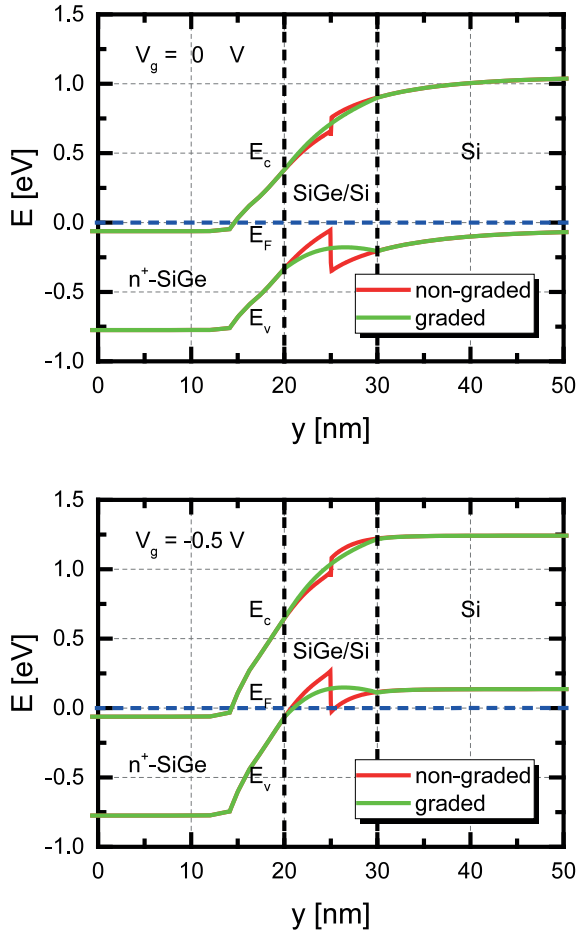


Figure 3.2.3: Simulated band structure of a non-graded and a graded vertical SiGe/Si heterostructure p-TFET at a drain voltage V_d of $-0.1\,\mathrm{V}$ for gate voltages V_g of $0\,\mathrm{V}$ and $-0.5\,\mathrm{V}$, revealing a beneficial impact of a grading of the Ge mole fraction x by encountering the pronounced valence band offset ΔE_v between compressively, biaxially strained SiGe and Si, resulting in a decreased tunneling length and thus, increased probability for BTBT.

poor switching for positive gate voltages $V_\mathrm{g} > 0$, namely the n-branch of the transfer characteristics. In contrast to TCAD simulations, the vertical SiGe/Si heterostructure n-TFET does not benefit from a grading of the Ge mole fraction x at the source tunnel junction even though its positive influence should be more pronounced in case of a p-TFET as already discussed in chapter 3.2.1. However, both types of vertical SiGe/Si heterostructure n-TFETs provide a surprisingly pronounced switching for negative gate voltages $V_\mathrm{g} < 0$, namely the p-branch of the transfer characteristics, negating the expected suppression of

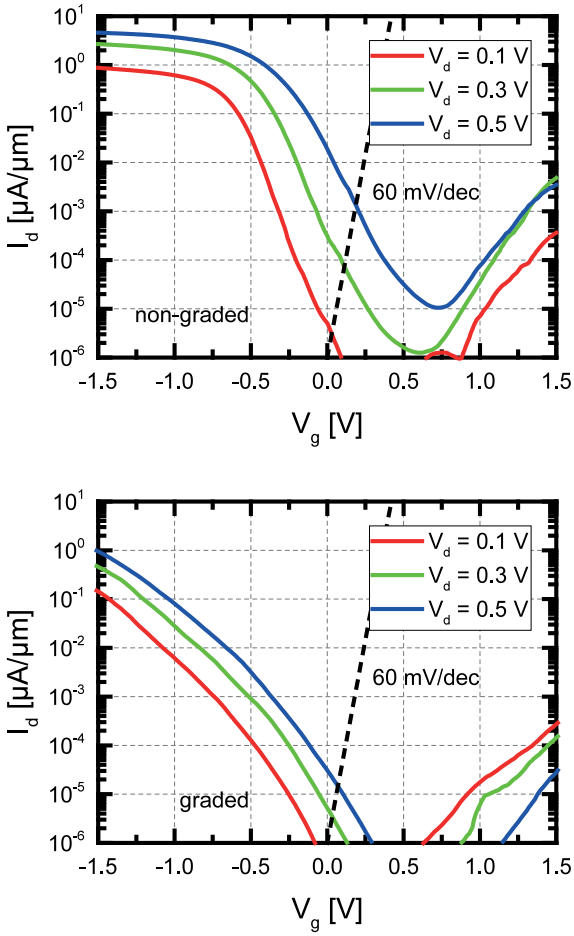


Figure 3.2.4: Measured transfer characteristics of a non-graded and a graded vertical SiGe/Si heterostructure n-TFET, exhibiting poor switching for positive gate voltages $V_g > 0$, namely the n-branch of the transfer characteristics.

the ambipolar switching characteristics as one key feature of this TFET device concept. Taking the weak onset of the n-branch of the transfer characteristics into account, it seems likely that the observed ambipolar switching characteristics might stem from a much more degraded p^{++}-SiGe tunnel junction at the source as compared to the n^{+}-Si tunnel junction at the drain. It is worth mentioning that the n-branch of the transfer characteristics suffers from pronounced noise, being an indication for a degraded contact towards the p^{++}-SiGe layer. On the contrary, the p-branch of the transfer characteristics does not exhibit that pronounced noise, suggesting a lowered contact resistance towards the n^{+}-Si layer due to its silicidation with Ni as already discussed in chapter 3.1. Accordingly, in order to evaluate the

switching characteristics at the n^+-Si tunnel junction in more detail, both the graded and the non-graded vertical SiGe/Si heterostructure n-TFETs are measured in p-TFET mode by swapping source and drain while applying a negative drain voltage V_d. The corresponding transfer characteristics in case of biasing in p-TFET mode are depicted in figure 3.2.5. As expected, the transfer characteristics of the vertical SiGe/Si heterostructure n-TFET in case of biasing in p-TFET mode do not differ from those in n-TFET mode except the shift of the ambipolar response, being a function of the respective applied drain voltage V_d. The sub-

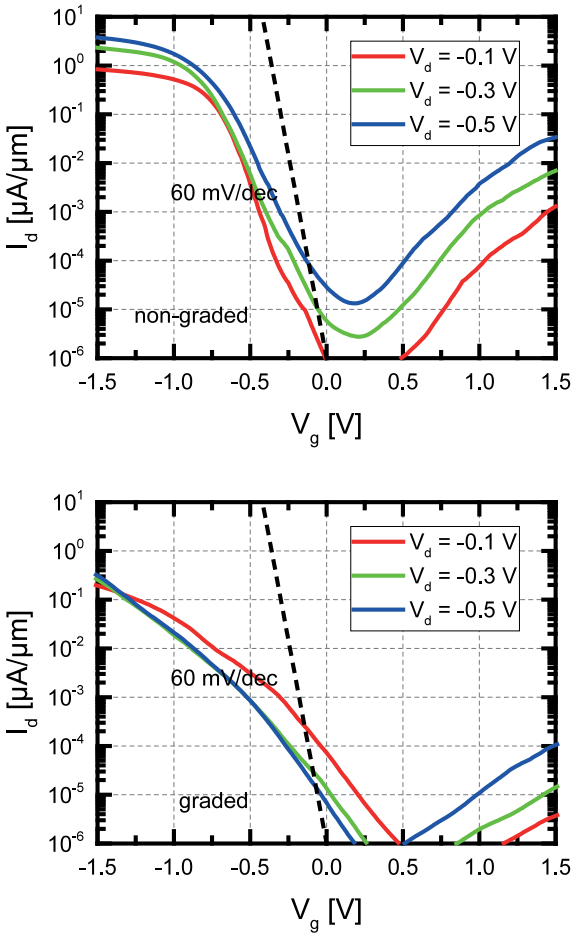


Figure 3.2.5: Measured transfer characteristics of a non-graded and a graded vertical SiGe/Si heterostructure n-TFET in case of biasing in p-TFET mode, providing a surprisingly pronounced switching for negative gate voltages $V_g < 0$, namely the p-branch of the transfer characteristics, negating the expected suppression of the ambipolar switching characteristics as one key feature of this TFET device concept.

threshold swing SS in case of biasing in p-TFET mode yields a value of about 250 mV/dec in case of the graded and a value of about 150 mV/dec in case of the non-graded vertical SiGe/Si heterostructure n-TFET. However, this difference in the subthreshold swing SS cannot be attributed to a grading of the Ge mole fraction x because in case of biasing in p-TFET mode, the source tunnel junction corresponds to a transition between n^+-Si and i-Si for both types of TFETs whereas for this particular case, the p^{++}-SiGe layer acts as the drain tunnel junction.

The corresponding output characteristics of both types of vertical SiGe/Si heterostructure n-TFETs in case of biasing in p-TFET mode reveal a weak onset of the drain current I_d with a pronounced S-shape as well as no visible saturation of the drain current I_d as illustrated in figure 3.2.6, being clear indications of a degraded tunnel junction due to a too low carrier concentration n [58, 59], coinciding with the measured SIMS and ECV profiles as already discussed in chapter 3.1, revealing a low carrier concentration n of about $2 \times 10^{19}\,\mathrm{cm}^{-3}$ at the n^+-Si tunnel junction as compared to the p^{++}-SiGe tunnel junction. However, this low carrier concentration n at the n^+-Si tunnel junction was desired when considering the design of the vertical SiGe/Si heterostructure n-TFET in order to allow for suppression of the ambipolar switching characteristics.

Even though the carrier concentration n of the n^+-Si layer yields a low value of about $2 \times 10^{19}\,\mathrm{cm}^{-3}$, being disadvantageous for BTBT in general, a degradation of the electrical characteristics of both types of vertical SiGe/Si heterostructure n-TFETs due to poor electrostatic control seems much more likely. Defects at the interface between semiconductor and high-κ dielectrics may enable a pronounced contribution from TAT, having a much stronger impact on the p^{++}-SiGe tunnel junction than on the n^+-Si tunnel junction since oxidation of Si results in SiO_2 as a stable, self-limiting interfacial oxide whereas oxidation of SiGe yields thicker interfacial oxide layers, being a compound of mainly SiO_2, but also of GeO_2 and Ge sub-oxides GeO_x in the range of 1% as revealed by X-ray photoelectron spectroscopy (XPS) [60]. In addition, even though Al is known to be quite reactive with O_2, resulting in a decreased thickness of an interfacial oxide layer in ideal case as already discussed in chapter 2.4.2 [45], the TEM image of the vertical SiGe/Si heterostructure n-TFET reveals a quite thick interfacial oxide layer of about 2 nm at the interface between SiGe and high-κ dielectrics, but also at the interface between Si and high-κ dielectrics, suggesting a material independent effect with respect to the thickness of the interfacial oxide layer. In this regard, a rough surface at the side walls of the fin due to etching by means of RIE may come into play, giving disadvantageously rise to an increased thickness of the interfacial oxide layer. In summary, an increased thickness of the interfacial oxide layer arising in the vertical SiGe/Si heterostructure n-TFET may stem from surface roughness at the side walls of the fin which define the tunnel junctions of a vertical TFET whereas defects at the interface between semiconductor and high-κ dielectrics may cause a pronounced contribution from TAT having a much stronger impact on the p^{++}-SiGe tunnel junction than on the n^+-Si tunnel junction due to the different chemical compositions of their respective interfacial oxide layers.

Besides defects at the interface between semiconductor and high-κ dielectrics, dopants themselves give rise to TAT as already indicated in chapter 2.3.3. In this regard, the lifetimes τ

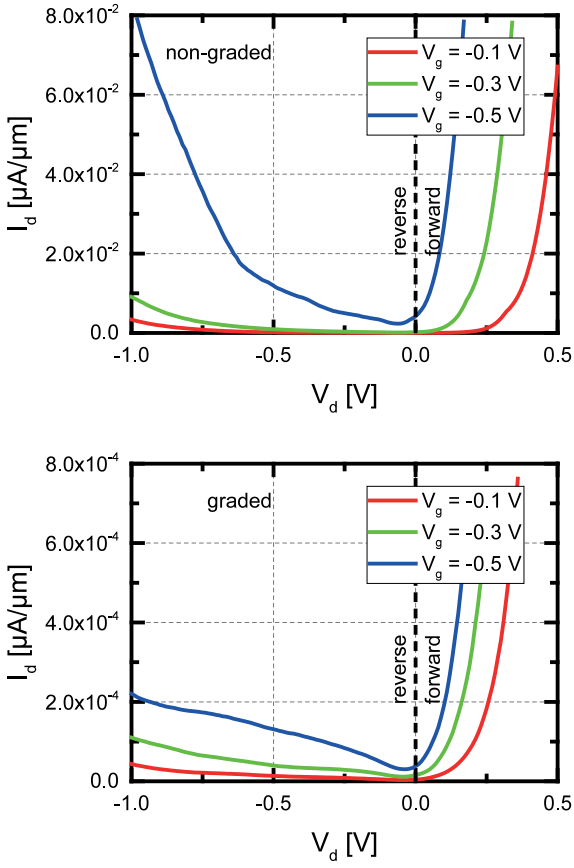


Figure 3.2.6: Measured output characteristics of a non-graded and a graded vertical SiGe/Si heterostructure n-TFET in case of biasing in p-TFET mode, revealing a weak onset of the drain current I_d with a pronounced S-shape as well as no visible saturation of the drain current I_d, being clear indications of a degraded tunnel junction due to a too low carrier concentration n.

of the traps scale with the carrier concentration n and can be approximated by means of the empirical SCHARFETTER relation [61, 62]:

$$\tau = \tau_\mathrm{min} + \frac{\tau_\mathrm{max} - \tau_\mathrm{min}}{1 + \left(\frac{n_\mathrm{s}+n_\mathrm{d}}{n_\mathrm{ref}}\right)^\gamma}, \tag{3.2.1}$$

where n_s and n_d denote the carrier concentrations of source and drain respectively and n_ref defines the reference carrier concentration of the intrinsic channel. The material dependent parameter γ scales with the band gap E_g of the respective semiconductor, enabling an increased lifetime τ of the traps in case of materials with small band gap E_g and thus a diminished influence of TAT, being indispensable for a low subthreshold swing SS. However,

equation (3.2.1) reveals a decreased lifetime τ of the traps for increasing carrier concentrations n_s and n_d of source and drain respectively in parallel, resulting in an increased contribution from TAT as a consequence. Thus, the stronger degradation of the p^{++}-SiGe tunnel junction as compared to the n^{+}-Si tunnel junction may stem from its higher carrier concentration n up to $4 \times 10^{20}\,\mathrm{cm}^{-3}$, coinciding with TCAD simulations presented in figures 3.2.7 and 3.2.8. As suggested by equation (3.2.1), the simulated transfer characteristics of the graded vertical SiGe/Si heterostructure n-TFET reveal a much stronger contribution from TAT at the p^{++}-SiGe tunnel junction than at the n^{+}-Si tunnel junction due to its higher carrier concentration n, i.e. for a minimum of TAT at a gate voltage V_g of $-0.5\,\mathrm{V}$, the trap recombination rates at a gate voltage V_g of $0\,\mathrm{V}$ exceed the ones at the corresponding gate voltage V_g of $-1\,\mathrm{V}$ for nearly two orders of magnitude as indicated by dashed lines. The corresponding contour plots of the trap recombination rates at gate voltages V_g of $-1\,\mathrm{V}$ and $0\,\mathrm{V}$ respectively emphasize this scaling of TAT with the carrier concentration n. In addition, a pronounced ambipolar switching becomes visible in the simulated transfer characteristics stemming from TAT, coinciding with the measured transfer characteristics, thus suggesting TAT and not BTBT being the dominant contribution to charge transport in the vertical SiGe/Si heterostructure n-TFET. In summary, TAT disadvantageously not only causes a degraded subthreshold swing SS, but also diminishes the benefits of a heterostructure device concept.

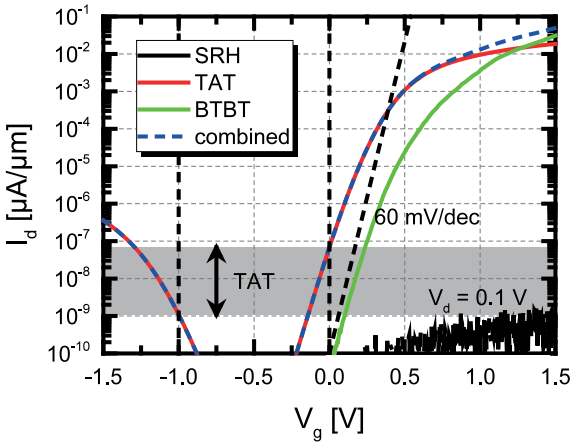


Figure 3.2.7: Simulated transfer characteristics of a graded vertical SiGe/Si heterostructure n-TFET at a drain voltage V_d of 0.1 V, demonstrating a stronger degradation of the p^{++}-SiGe tunnel junction as compared to the n^{+}-Si tunnel junction due to TAT, stemming from its higher carrier concentration n.

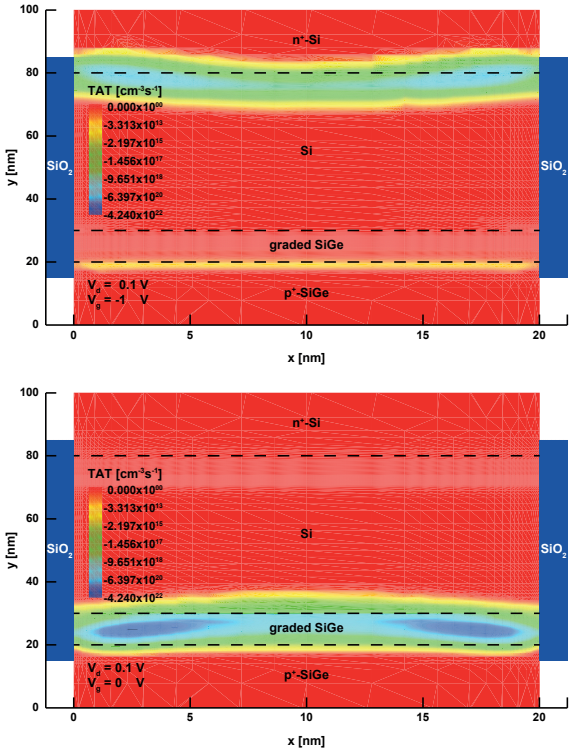


Figure 3.2.8: Contour plots of the simulated trap recombination rates arising in the graded vertical SiGe/Si heterostructure n-TFET at a drain voltage V_d of 0.1 V for gate voltages V_g of -1 V and 0 V, revealing nearly two orders of magnitude higher trap recombination rates at the p^{++}-SiGe tunnel junction as compared to the n^{+}-Si tunnel junction.

3.3 Summary and Discussion

Vertical SiGe/Si heterostructure n-TFETs were presented which make use of strained SiGe as a material with smaller band gap E_g at the source tunnel junction in order to increase the probability of BTBT while suppressing the ambipolar switching characteristics in parallel due to the use of Si with its higher band gap E_g as compared to SiGe at the drain tunnel junction, thus enabling a heterostructure device concept. However, high subthreshold swing SS, weak onset of the drain current I_d with a pronounced S-shape as well as no visible saturation of the drain current I_d became obvious due to a strong degradation of both tunnel junctions which may stem from poor electrostatic control caused by a defective interface between semiconductor and high-κ dielectrics as well as a pronounced surface roughness at the side walls of the fin, both favoring TAT. In this regard, the pronounced ambipolar switching characteristics despite a heterostructure device concept may result from a much stronger contribution from TAT at the p^{++}-SiGe tunnel junction as compared to the n^{+}-Si tunnel

junction, caused by the different chemical compositions of their respective interfacial oxide layers on the one hand and a much higher carrier concentration n within the SiGe layer on the other hand, scaling TAT. In order to allow for such high carrier concentrations n at the source tunnel junction, being beneficial for BTBT in general, a much less defective gate oxide is indispensable, resulting in good electrostatic control while suppressing TAT in parallel. In addition, the problem of a pronounced surface roughness at the side walls of the fin which define the tunnel junctions of a vertical TFET has to be tackled consequently by means of wet-chemical etching and/or oxidation.

However, the vertical SiGe/Si heterostructure n-TFET may serve as a promising proof of concept for further integration of materials with small band gap E_g such as strained Ge or GeSn which allow for a direct band gap E_g transition into a three-dimensional device structure while maintaining a Si compatible technology, but needs careful optimization of its process flow in order to benefit from the versatility grading and in-situ doping enable.

4 Planar SiGe/Si Heterostructure TFETs

This chapter deals with the concept of a planar SiGe/Si heterostructure TFET which benefits from line tunneling aligned with the gate electric field lines by means of a selective and self-adjusted silicidation in order to enlarge the area for BTBT. In addition, a counter doped pocket at the source tunnel junction is introduced in order to reduce the onset voltage V_{onset} as a measure of the gate voltage V_{g} required in order to deplete parts of the source region directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines. In contrast to the vertical SiGe/Si heterostructure TFET presented in chapter 3, this TFET structure relies on asymmetric tunnel junctions at source and drain in order to suppress the ambipolar switching characteristics rather than making use of two different materials at source and drain in order to enable a heterostructure device concept. Similar to the vertical SiGe/Si heterostructure TFET, the planar SiGe/Si heterostructure TFET benefits from strained SiGe as a material with smaller band gap E_g in order to increase the probability for BTBT, but in this particular case, the source tunnel junction is not realized by in-situ doping during growth but by means of ion implantation into silicide (IIS) and subsequent dopant segregation (DS) to the silicide edges in order to form a source tunnel junction with sharp doping profile and high carrier concentration n in parallel.

4.1 Device Fabrication

Planar SiGe/Si heterostructure p-TFETs were fabricated on 5 nm intrinsic $Si_{0.45}Ge_{0.55}$ pseudomorphically grown on a 15 nm SOI substrate with an additional cap of 5 nm intrinsic Si by means of a RPCVD reactor [50]. In this regard, a Si cap is introduced in order to avoid the formation of a thick and defective interfacial oxide layer at the interface between SiGe and high-κ dielectrics as already indicated in chapter 3.2, but to enable a thin SiO_2 layer as a stable interfacial oxide at the interface between Si and high-κ dielectrics, resulting in an improved electrostatic control, being beneficial for BTBT. The compressive, biaxial strain ε of about $-2\,\%$ in the SiGe layer due to the pseudomorphic growth further reduces the band gap E_g as compared to relaxed SiGe, allowing for an overall enhanced probability for BTBT as already discussed in chapter 2.4.1. In order to enable high Ge mole fractions x incorporated into the lattice, the layers were grown at a low temperature T of 500 °C, defining the upper thermal budget for subsequent annealing steps. The subsequent process flow for the planar SiGe/Si heterostructure p-TFET is sketched in detail in figure 4.1.1, being applicable to a n-TFET configuration as well just by interchanging dopant types during the respective implantations of source, counter doped pocket and drain. If no further details are mentioned, respective steps of the process flow correspond to the ones for the vertical SiGe/Si heterostructure n-TFET (see chapter 3.1).

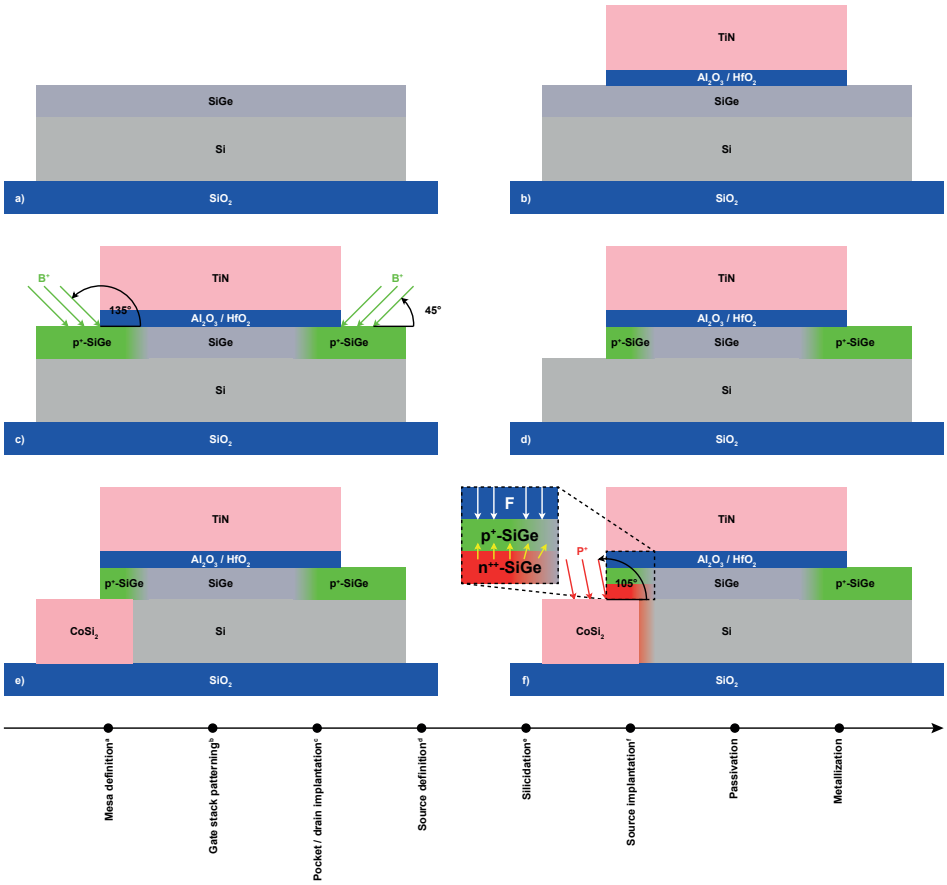


Figure 4.1.1: Process flow for the planar SiGe/Si heterostructure p-TFET, highlighting mesa definition, gate stack patterning, implantation of counter doped pocket and drain respectively, source definition, selective as well as self-adjusted silicidation and IIS in order to define the source.

1. Pre-cleaning of the substrate.
2. Marker patterning for electron beam lithography.
3. Mesa definition (see figure 4.1.1a).
4. Pre gate stack cleaning and deposition.
5. Gate stack patterning (see figure 4.1.1b).
6. Boron ions were implanted at an energy of 0.7 keV at a tilt angle of 45° to a dose of $2 \times 10^{14}\,\mathrm{cm}^{-2}$ and at a tilt angle of 135° to a dose of $2 \times 10^{13}\,\mathrm{cm}^{-2}$ in order to form a p-doped drain and p-doped pocket directly underneath the gate (see figure 4.1.1c). In

this regard, the gate stack served as a shadow mask, allowing for an individual implantation of drain and counter doped pocket without further lithography steps in between required. The implantation energy was chosen that low in order to form a shallow doping only in the SiGe layer and not in the SOI substrate underneath, resulting in the implantation peak of the ion distribution located at the interface between Si cap and SiGe layer according to Transport of Ions in Matter (TRIM) simulations as depicted in figure 4.1.2. Dopant activation of drain and counter doped pocket was carried out at a low temperature T of 500 °C for 1 min in nitrogen atmosphere to sustain the compressive biaxial strain ε within the SiGe layer.

7. The sample was patterned with positive electron beam resist AR-P 669.07 (PMMA 600K) in order to create an etching window only at the source side of the device. Both the remaining Si cap and the SiGe layer underneath were etched by means of RIE using a Cl_2/Ar plasma omitting ICP (see figure 4.1.1d). Subsequent to definition of the source, a metal stack consisting of 5 nm Co and 10 nm Ti was deposited by e-gun evaporation in order to avoid oxidation of the freed SOI substrate. In this regard, the Ti cap served to prevent the Co layer from oxidizing during the following silicidation which was carried out at a low temperature T of 500 °C for 30 s in forming gas to form $CoSi_2$ (see figure 4.1.1e). Co advantageously enables a selective and self-adjusted silicidation and allows $CoSi_2$ to encroach under the gate along the SOI substrate without reaction to the SiGe, resulting in an increased area for line tunneling aligned with the gate electric field lines underneath the gate. The reason for this selective and self-adjusted silicidation can be found in a Ge segregation at the SiGe/Si interface due to the Gibbs free energy difference ΔG between CoSi and CoGe which favors the formation of the former silicide [63]. A formation of epitaxial $CoSi_2$ in a region underneath the gate may be achieved even at that low temperatures T due to Co diffusion along the SOI substrate, resulting in the silicidation being a volume and not a surface effect, similar to the case of Ni silicidation [64]. In this regard, the required thickness for the Co deposition in order to enable diffusion along the SOI substrate underneath the gate was estimated from the remaining thickness of the SOI substrate measured by means of ellipsometry.

8. Patterning of the sample with positive electron beam resist AR-P 669.07 (PMMA 600K) was repeated in order to open an implantation window at the source side of the device. Phosphorus ions were implanted at an energy of 15 keV at a tilt angle of 105° to a dose of $5 \times 10^{15}\,\mathrm{cm}^{-2}$ into Ti/$CoSi_2$ (see figure 4.1.1f), followed by a low temperature T anneal at 400 °C and 500 °C respectively for 1 min in nitrogen atmosphere to drive out the dopants from the silicide edges into the SiGe layer by means of DS and thus, to form a n^{++}-p^{+} tunnel junction with sharp doping profile and high carrier concentration n directly underneath the gate. Since implantation of the source was carried out by means of IIS, residual defects are mainly located within the metallic $CoSi_2$ and less within the SiGe layer, thus avoiding severe contribution from TAT due to a defective source tunnel junction [65]. In order to avoid shortcut between source and gate, the remaining Ti and unreacted Co were etched wet-chemically by means of SC-1 solution consisting of $NH_3 : H_2O_2 : H_2O$ (1 : 1 : 5), being selective to the embedded $CoSi_2$. A SEM image as well as a TEM image of a processed device are shown in figures 4.1.3 and 4.1.4 respectively. The TEM image reveals the $CoSi_2$ layer encroached underneath

the gate for about 10 nm, thus increasing the area for line tunneling aligned with the gate electric field lines as compared to point tunneling as a key advantage of this TFET structure. In addition, even though gate stack cleaning and deposition in case of the planar and the vertical heterostructure TFET are performed the same way, a much thinner interfacial oxide layer in the range of 1 nm at the interface between Si and high-κ dielectrics is observed in case of the planar SiGe/Si heterostructure p-TFET, being beneficial in terms of improved electrostatic control and thus, for BTBT. In this regard, the much rougher surface at the side walls of the fin in case of the vertical heterostructure n-TFET as already discussed in chapter 3.2 may come into play, giving disadvantageously rise to the increased thickness of the interfacial oxide layer. The corresponding source doping profile of the planar SiGe/Si heterostructure p-TFET after DS was obtained by ECV measurements on a bulk Si reference sample, highlighting both a sharp doping profile with a steepness λ_s up to 3 nm/dec and a high carrier concentration n up to $4 \times 10^{20}\,\mathrm{cm}^{-3}$ as illustrated in figure 4.1.5.

9. Passivation with SiO_2.

10. Metallization with Al.

11. FGA.

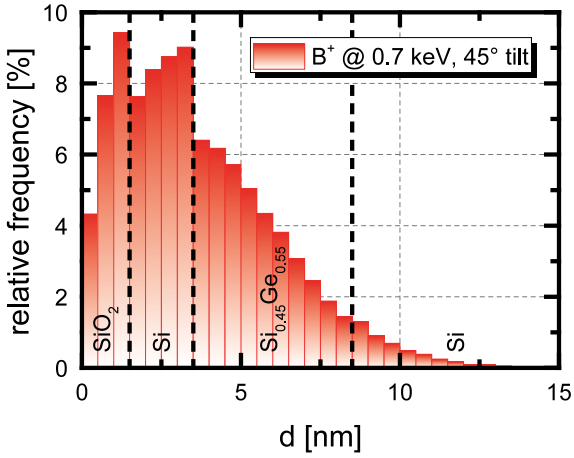


Figure 4.1.2: Simulated ion distribution within the sample after implantation with Boron ions at an energy of 0.7 keV at a tilt angle of 45° in order to form a shallow doping only in the SiGe layer and not in the SOI substrate underneath. The resulting implantation peak of the ion distribution is located at the interface between Si cap and SiGe layer.

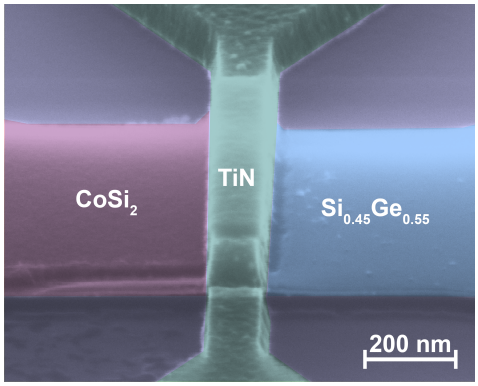


Figure 4.1.3: SEM image of the planar SiGe/Si heterostructure p-TFET after gate stack patterning and selective and self-adjusted silicidation with Co at the source side of the device, resulting in a formation of $CoSi_2$.

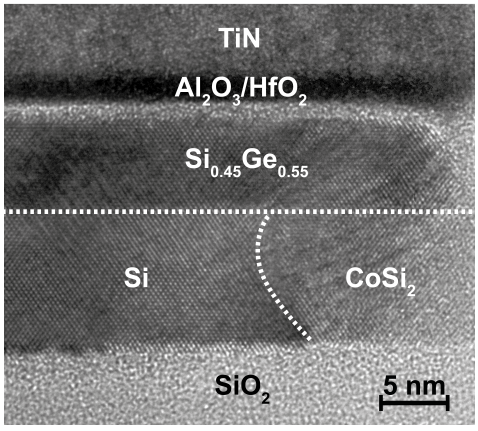


Figure 4.1.4: TEM image of the planar SiGe/Si heterostructure p-TFET, revealing the $CoSi_2$ layer encroached underneath the gate for about 10 nm, thus increasing the area for line tunneling aligned with the gate electric field lines as compared to point tunneling.

4.2 Device Characterization and Simulation

This chapter presents the experimental results obtained from measurements of the planar SiGe/Si heterostructure p-TFET. Besides DC characterization, pulsed measurements and low temperature T analysis are performed in order to describe the physics emerging in this TFET structure. Focus in all measurements is put on low power electronics as the key advantage of TFETs as compared to state-of-the-art MOSFETs. In addition, various TCAD simulations are performed in order to evaluate the experimental results as well as to illustrate potential improvements of the concept of the planar SiGe/Si heterostructure p-TFET itself.

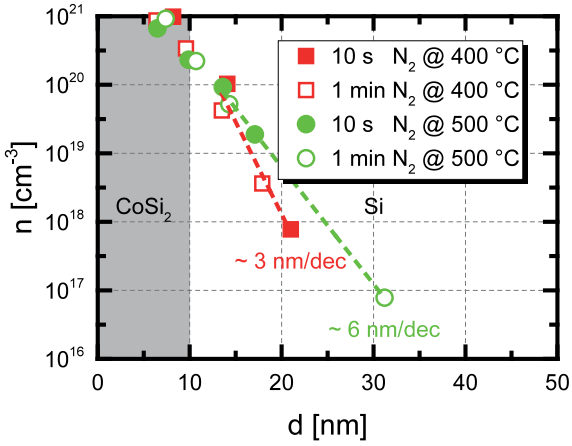


Figure 4.1.5: Source doping profile measured by ECV on a reference Si bulk sample for different temperatures T and different times t of DS. A high carrier concentration n up to $4 \times 10^{20}\,\mathrm{cm}^{-3}$ is revealed, being independent of temperature T and time t for DS, whereas a low temperature T of 400 °C allows for a sharp doping profile with a steepness λ_s up to 3 nm/dec in parallel to the high carrier concentration n.

Finally, as a first step towards logic applications, a NAND gate is realized by means of p-TFET logic, highlighting the potential of the planar SiGe/Si heterostructure p-TFET as a promising concept not only for low power electronics but also for low power applications.

4.2.1 DC Characteristics

DC characterization at room temperature $T = 300\,\mathrm{K}$ is realized by means of a three terminal setup performed with a Keithley 4200-SCS parameter analyzer [57]. The resulting transfer characteristics of the planar SiGe/Si heterostructure p-TFET are presented in figure 4.2.1. A high on-current I_{on} of 6.7 µA/µm at a supply voltage $V_{DD} = |V_d| = |V_{ov}| = |V_g - V_{off}|$ of 0.5 V is revealed where V_{ov} denotes the overdrive voltage accounting for a possible threshold voltage shift of the transfer characteristics and V_{off} corresponds to the respective gate voltage V_g at an off-current I_{off} of 200 pA/µm. Even at a low supply voltage V_{DD} of only 0.3 V the on-current I_{on} of the planar SiGe/Si heterostructure p-TFET still reaches 0.6 µA/µm. The transfer characteristics exhibit a pronounced linear dependency of the logarithmic of the drain current $\log(I_d)$ on the gate voltage V_g in the subthreshold regime, similar to a conventional MOSFET, resulting in an average subthreshold swing SS of about 80 mV/dec over four orders of magnitude of drain current I_d. This linear dependency of the logarithmic of the drain current $\log(I_d)$ on the gate voltage V_g can be attributed to line tunneling aligned with the gate electric field lines as the dominant contribution to BTBT, as already pointed out in chapter 2.3.5. For this particular case, the subthreshold swing SS can be approximated as constant over a distinct region of the gate voltage V_g with the actual value of the subthreshold swing SS being proportional to the root of the onset voltage

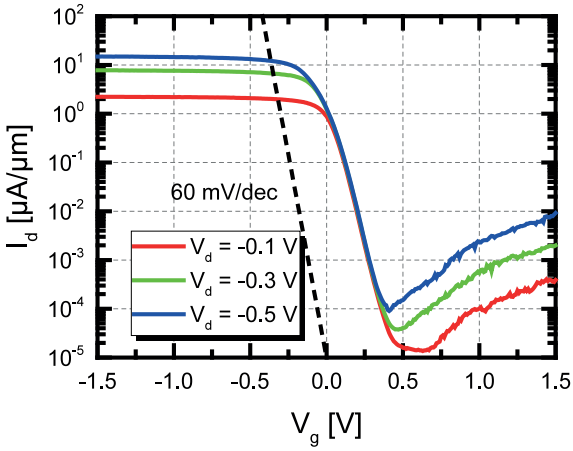


Figure 4.2.1: Measured transfer characteristics of the planar SiGe/Si heterostructure p-TFET, revealing both a high on-current I_{on} of 6.7 µA/µm at a supply voltage V_{DD} of 0.5 V and an average subthreshold swing SS of about 80 mV/dec over four orders of magnitude of drain current I_d in parallel.

$\sqrt{V_{onset}}$. The latter in turn is as a measure of the gate voltage V_g required in order to deplete parts of the source region directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines, thus affording both a small band gap E_g and good electrostatic control in order to minimize its value. Furthermore, the ambipolar switching of the planar SiGe/Si heterostructure p-TFET is strongly suppressed due to the asymmetric tunnel junctions implemented at source and drain. Whereas the drain tunnel junction is realized by common ion implantation and thermal activation, resulting in a broad and defective drain doping profile, the source tunnel junction benefits from IIS and subsequent DS by means of a selective and self-adjusted silicidation in combination with a counter doped pocket in order to enable both a sharp source doping profile and a high carrier concentration n in an enlarged area directly underneath the gate. Thereby, BTBT at the drain tunnel junction is dominated by point tunneling whereas the source tunnel junction benefits from line tunneling aligned with the gate electric field lines with the latter being advantageous in terms of the subthreshold swing SS due to the less pronounced dependency on the gate voltage V_g as visible from equations (2.3.19) and (2.3.21). In this regard, a constant subthreshold swing SS over a distinct region of the gate voltage V_g as provided by line tunneling aligned with the gate electric field lines is highly desired in terms of circuit design in order to avoid nonlinearities in the corresponding output characteristics which degrade rise and fall times and consequently, the dynamic noise margin of a TFET [66, 67]. In addition to the subthreshold swing SS, the switching response of a transistor can be evaluated by means of the transconductance $g_m = \frac{\partial I_d}{\partial V_g}$ as a function of the gate voltage V_g as shown in figure 4.2.2. The transconductance g_m as an important figure of merit in terms of analog circuit design yields to 13.6 µS/µm at a low supply voltage V_{DD} of 0.3 V and even reaches 42.8 µS/µm at a supply voltage V_{DD} of 0.5 V, outperforming state-of-the-art nanowire (NW) n- and p-TFETs with diameters down to 10 nm by a factor of about 1.5 [68, 69]. The

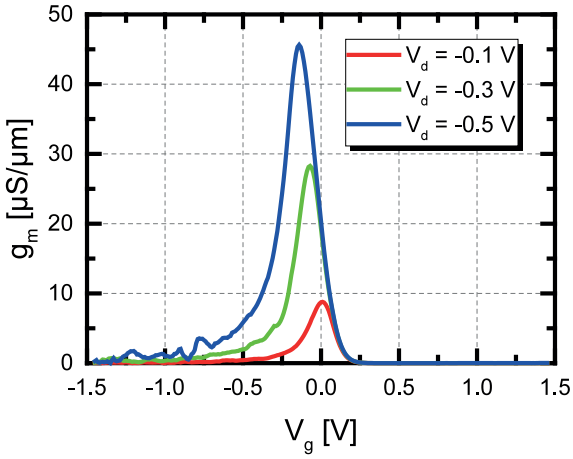


Figure 4.2.2: Transconductance g_m of the planar SiGe/Si heterostructure p-TFET as a function of the gate voltage V_g, yielding to 42.8 µS/µm at a supply voltage V_DD of 0.5 V.

pronounced linear dependency of the logarithmic of the drain current $\log(I_\mathrm{d})$ as a function of the gate voltage V_g becomes even more obvious by plotting either the subthreshold swing SS or the transconductance efficiency $\frac{g_\mathrm{m}}{I_\mathrm{d}} = \frac{1}{I_\mathrm{d}} \frac{\partial I_\mathrm{d}}{\partial V_\mathrm{g}} = \frac{\ln(10)}{SS}$ as a function of the drain current I_d as depicted in figures 4.2.3 and 4.2.4, highlighting a constant subthreshold swing SS and a constant transconductance efficiency $\frac{g_\mathrm{m}}{I_\mathrm{d}}$ respectively over a distinct region of the drain current I_d. The corresponding output characteristics of the planar SiGe/Si heterostructure

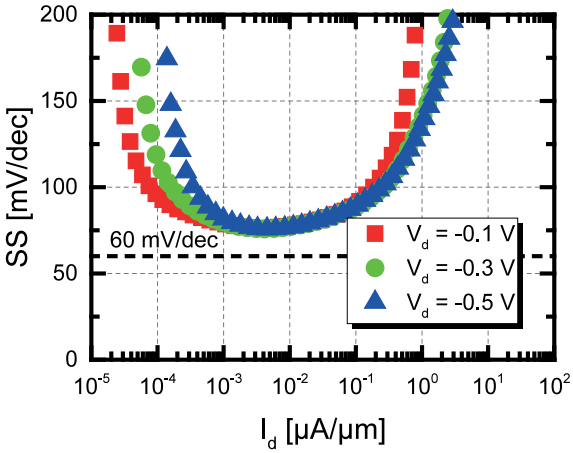


Figure 4.2.3: Subthreshold swing SS of the planar SiGe/Si heterostructure p-TFET as a function of the drain current I_d, highlighting a constant subthreshold swing SS over a distinct region of the drain current I_d.

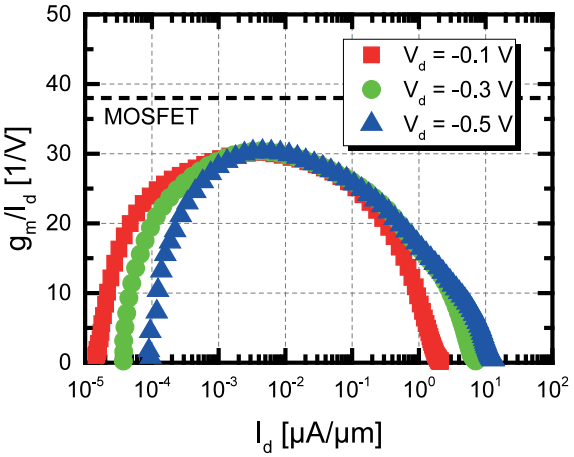


Figure 4.2.4: Transconductance efficiency $\frac{g_\mathrm{m}}{I_\mathrm{d}}$ of the planar SiGe/Si heterostructure p-TFET as a function of the drain current I_d, highlighting a constant transconductance efficiency $\frac{g_\mathrm{m}}{I_\mathrm{d}}$ over a distinct region of the drain current I_d.

p-TFET in reverse direction reveal a linear onset as well as a pronounced saturation of the drain current I_d as visible from figure 4.2.5, being clear indications of a sufficient high carrier concentration n at the source tunnel junction [58, 59]. Thereby, the output characteristics of the planar SiGe/Si heterostructure p-TFET coincide with the sharp source doping profile obtained by ECV measurements on a Si bulk reference sample as already discussed in chapter

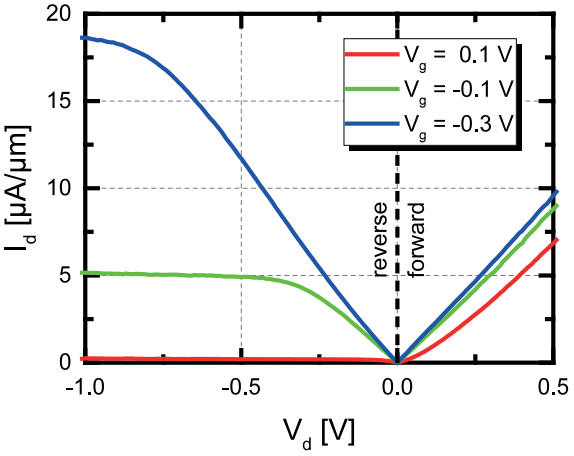


Figure 4.2.5: Measured output characteristics of the planar SiGe/Si heterostructure p-TFET, revealing a linear onset as well as a pronounced saturation of the drain current I_d in reverse direction, being clear indications of a sufficient high carrier concentration n at the source tunnel junction.

4.1. In forward direction, an exponential onset is observed as expected in case of a tunnel diode. In addition to the output characteristics, the output saturation of a transistor can be evaluated by means of the output conductance $g_d = \frac{\partial I_d}{\partial V_d}$ as function of the drain voltage V_d as illustrated in figure 4.2.6. In case of a MOSFET, the output conductance g_d as a further figure of merit in terms of analog circuit design degrades due to short-channel effects, thus limiting their scalability. Since the resistance of a tunnel junction can be assumed as much higher than the resistance of the channel, TFETs do not inherently suffer from short-channel effects, allowing for a low output conductance g_d as compared to MOSFETs. In case of the planar SiGe/Si heterostructure p-TFET, the resulting output conductance g_d exhibits a sharp transition to low values, i.e. for a gate voltage V_g of $-0.1\,\mathrm{V}$ which corresponds to a supply voltage V_{DD} of $0.43\,\mathrm{V}$ in case of a minimum voltage V_{off} of $0.33\,\mathrm{V}$ at an off-current I_{off} of $200\,\mathrm{pA/\mu m}$, the output conductance g_d drops in the range of $0.1\,\mu\mathrm{S/\mu m}$, once more outperforming state-of-the-art NW n- and p-TFETs with diameters down to $10\,\mathrm{nm}$ [68, 69]. Accordingly, the output conductance g_d coincides with the pronounced saturation of the drain current I_d observed in the corresponding output characteristics, suggesting the planar SiGe/Si heterostructure p-TFET as a feasible candidate for operational transconductance amplifiers realized by means of TFETs [70].

Subsequently, the intrinsic voltage gain $A_i = \frac{g_m}{g_d}$ as the most important figure of merit in terms of analog circuit design can be derived, weighting both contributions from the transconductance g_m and the output conductance g_d. The obtained values of the intrinsic voltage gain A_i as a function of the gate voltage V_g are presented in figure 4.2.7, revealing maximum values of the intrinsic voltage gain A_i above 100 and still above 10 at supply voltages V_{DD} of $0.3\,\mathrm{V}$ and $0.5\,\mathrm{V}$ respectively, enabled by a high transconductance g_m and a low output conductance g_d in parallel. Thus, the planar SiGe/Si heterostructure p-TFET

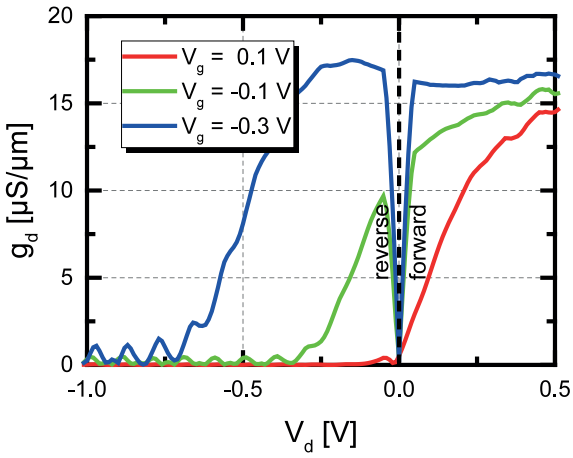


Figure 4.2.6: Output conductance g_d of the planar SiGe/Si heterostructure p-TFET as a function of the drain voltage V_d, exhibiting a sharp transition to low values, i.e. for a gate voltage V_g of $-0.1\,\mathrm{V}$ which corresponds to a supply voltage V_{DD} of $0.43\,\mathrm{V}$ in case of a minimum voltage V_{off} of $0.33\,\mathrm{V}$ at an off-current I_{off} of $200\,\mathrm{pA/\mu m}$, the output conductance g_d drops in the range of $0.1\,\mu\mathrm{S/\mu m}$.

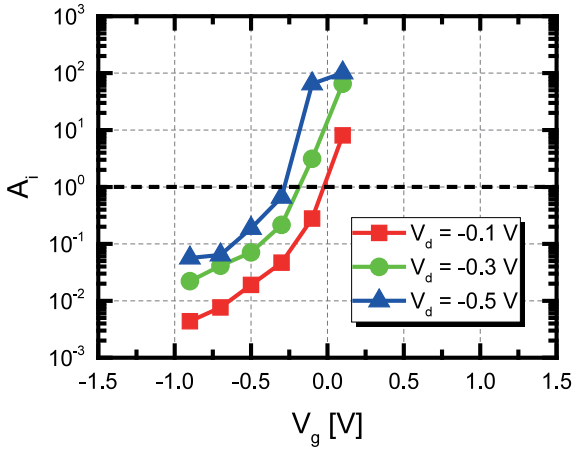


Figure 4.2.7: Intrinsic voltage gain A_i of the planar SiGe/Si heterostructure p-TFET as a function of the gate voltage V_g, revealing maximum values of the intrinsic voltage gain A_i above 100 and still above 10 at supply voltages V_{DD} of 0.3 V and 0.5 V respectively, enabled by a high transconductance g_m and a low output conductance g_d in parallel.

reveals its promising potential not only for usage in digital but also in analog and sensor applications [21, 22, 23, 24].

As already mentioned, scaling of MOSFETs requires a trade-off between an improvement of the on-current I_{on} due to a decreased resistance of the channel and a degradation of the on-current I_{on} due to short-channel effects. Thereby, the on-current I_{on} of a conventional MOSFET as well as a SCHOTTKY barrier MOSFET exhibits a pronounced dependency on its corresponding gate length L_g [44]. The on-current I_{on} of a TFET in turn does not scale with the gate length L_g due to the resistance of the tunnel junction dominating over the resistance of the channel as visible from figure 4.2.8. No pronounced dependency of the on-current I_{on} of the planar SiGe/Si heterostructure p-TFET as a function of the gate length L_g becomes obvious, thus excluding parasitic contributions from a SCHOTTKY junction at the interface between $CoSi_2$ and n^{++}-SiGe [71]. In addition, the diminished influence of the SCHOTTKY barrier implies a sufficient high carrier concentration n of the n^{++}-SiGe layer, coinciding with the sharp source doping profile obtained by ECV measurements on a Si bulk reference sample as already discussed in chapter 4.1.

Subsequently, in order to exclude parasitic contributions of a p-MOSFET due to the introduction of a counter doped pocket at the source tunnel junction and to ensure proper p-TFET operation, the device was measured in p-MOS mode by swapping source and drain but keeping the applied biases for drain voltage V_d and gate voltage V_g constant. In case of a p-MOSFET dominating charge transport, a reproduction of the transfer characteristics is expected whereas in case of p-TFET operation, switching control of the transistor is lost due to the (gated) tunnel diode biased in forward direction, enabling thermionic emission. The corresponding transfer characteristics in case of biasing in p-MOS mode are shown in figure 4.2.9, indicating a reproduction of the TFET curve only at a drain voltage V_d of

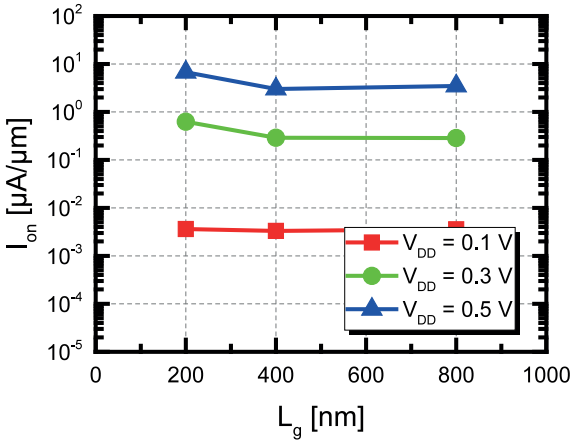


Figure 4.2.8: On-current I_{on} of the planar SiGe/Si heterostructure p-TFET as a function of the gate length L_g, revealing no pronounced dependency of the on-current I_{on} of the planar SiGe/Si heterostructure p-TFET as a function of the gate length L_g, thus excluding parasitic contributions from a SCHOTTKY junction at the interface between $CoSi_2$ and n^{++}-SiGe.

$-0.1\,\mathrm{V}$ whereas at higher absolute drain voltages $|V_d|$ the device exhibits no more switching and is always on. As a consequence, charge transport in the planar SiGe/Si heterostructure p-TFET can be sufficiently described by the characteristics of a (gated) tunnel diode and

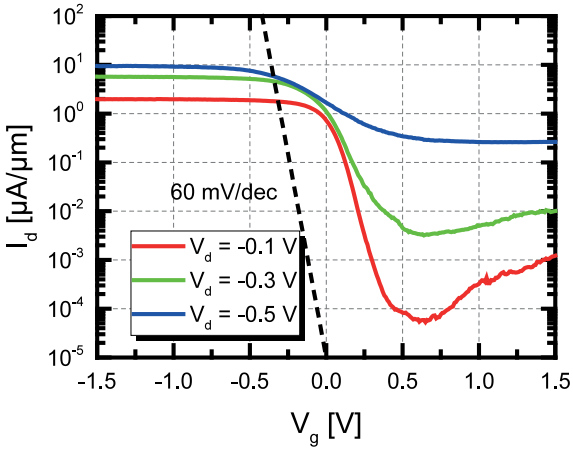


Figure 4.2.9: Measured transfer characteristics of the planar SiGe/Si heterostructure p-TFET in case of biasing in p-MOS mode, indicating a reproduction of the TFET curve only at a drain voltage V_d of $-0.1\,\mathrm{V}$ whereas at higher absolute drain voltages $|V_d|$ the device exhibits no more switching and is always on due to the (gated) tunnel diode biased in forward direction, enabling thermionic emission.

not by those of a p-MOSFET, resulting in thermionic emission dominating charge transport in case of biasing in p-MOS mode, but BTBT dominating charge transport in case of biasing in p-TFET mode as desired.

Measuring a (gated) tunnel diode in forward direction in case of biasing in p-MOS mode becomes also obvious in the corresponding output characteristics as depicted in figure 4.2.10. Contrary to the output characteristics in case of biasing in p-TFET mode, the output characteristics in case of biasing in p-MOS mode reveal an exponential onset in reverse direction without any saturation of the drain current I_d due to the loss of switching control.

In this regard, TCAD simulations allow for a qualitative reproduction of the measured transfer characteristics of the planar SiGe/Si heterostructure p-TFET in case of biasing in p-MOS mode as illustrated in figure 4.2.11. The more the absolute drain voltage $|V_\mathrm{d}|$ is increased, the less the transistor exhibits switching, coinciding with the experimental results. A comparison of the corresponding band structures at drain voltages V_d of $-0.1\,\mathrm{V}$ and $-0.5\,\mathrm{V}$ as presented in figure 4.2.12 highlights this loss of switching control for increasing absolute drain voltages $|V_\mathrm{d}|$ due to the onset of thermionic emission. At a drain voltage V_d of $-0.1\,\mathrm{V}$, the n^{++}-SiGe layer still acts as an energy barrier for holes from the intrinsic SiGe channel whereas at a drain voltage V_d of $-0.5\,\mathrm{V}$ its conduction and valence band are risen that much in energy that flat-band conditions prevail, thus enabling thermionic emission. In this regard, the applied gate voltage V_g of $0.5\,\mathrm{V}$ has only a diminished influence on the actual band alignment of the n^{++}-SiGe layer since its high carrier concentration n effectively screens the gate electric field, coinciding with the vanishing dependency of the drain current I_d on the gate voltage V_g in the corresponding transfer characteristics.

In addition, TCAD simulations allow for a separation of the different contributions from SRH generation-recombination, TAT and BTBT to the overall drain current I_d as visible

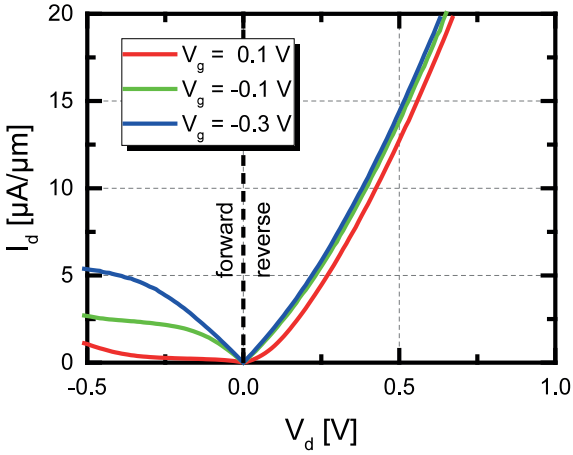


Figure 4.2.10: Measured output characteristics of the planar SiGe/Si heterostructure p-TFET in case of biasing in p-MOS mode, revealing an exponential onset in reverse direction without any saturation of the drain current I_d due to the loss of switching control.

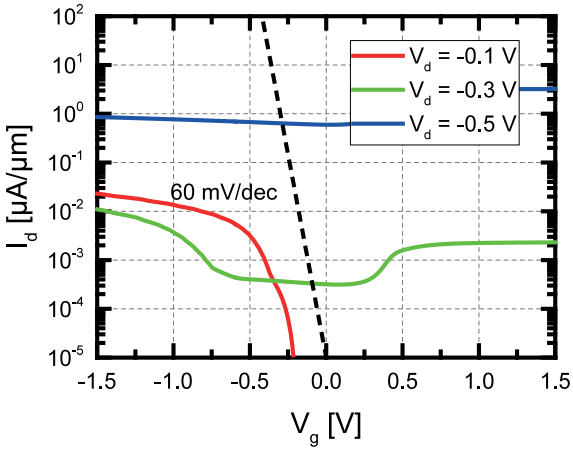


Figure 4.2.11: Simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET in case of biasing in p-MOS mode. The more the absolute drain voltage $|V_\mathrm{d}|$ is increased, the less the transistor exhibits switching due to the (gated) tunnel diode biased in forward direction, enabling thermionic emission.

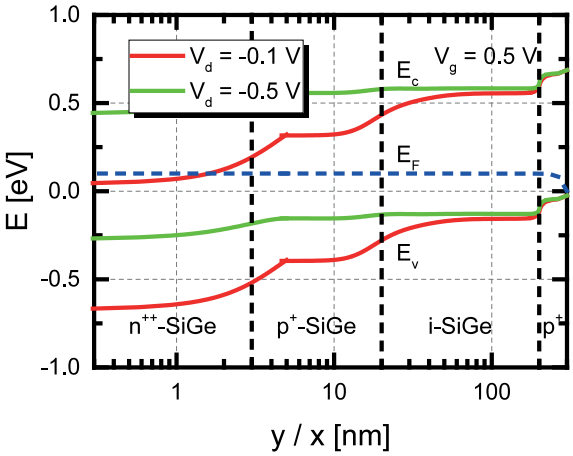


Figure 4.2.12: Simulated band structure of the planar SiGe/Si heterostructure p-TFET in case of biasing in p-MOS mode at a gate voltage V_g of 0.5 V for drain voltages V_d of −0.1 V and −0.5 V, allowing for thermionic emission in case of the latter due to prevailing flat-band conditions.

from figure 4.2.13 in case of biasing in p-TFET mode. The planar SiGe/Si heterostructure p-TFET reveals a subthreshold swing SS lower than 60 mV/dec, unmasking TAT as the contribution in charge for a degradation of the subthreshold swing SS. TAT exhibits an earlier onset as compared to BTBT, thus distorting the actual value of the onset voltage V_onset as a measure of the gate voltage V_g required in order to deplete parts of the source

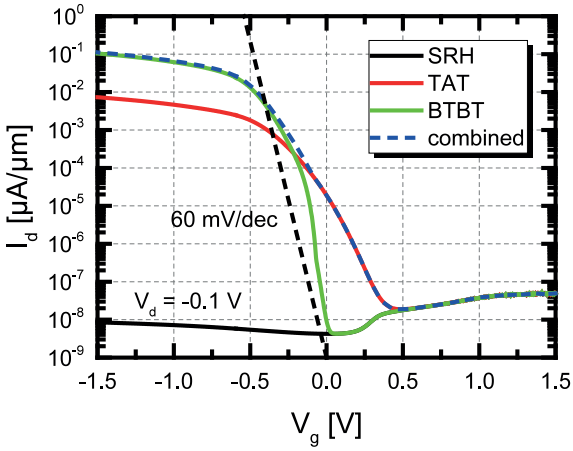


Figure 4.2.13: Simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET in case of biasing in p-TFET mode at a drain voltage V_d of $-0.1\,\mathrm{V}$, revealing a subthreshold swing SS lower than 60 mV/dec, unmasking TAT as the contribution in charge for a degradation of the subthreshold swing SS.

region directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines. Furthermore, TCAD simulations predict a negligible contribution from SRH generation to the overall drain current I_d, allowing for a low off-current I_off of the planar SiGe/Si heterostructure p-TFET and thus, coinciding with the experimental results.

Summarizing, the planar SiGe/Si heterostructure p-TFET equally benefits from both a selective and self-adjusted silicidation in order to enlarge the area for BTBT directly underneath the gate and a counter doped pocket within the SiGe layer in order to facilitate depletion in this area as a precondition for line tunneling aligned with the gate electric field lines [72]. In this regard, the introduction of a counter doped pocket at the source tunnel junction results in a sharpened doping profile and thus, enables a n^{++}-p^{+} tunnel junction as visible from the simulated doping profile shown in figure 4.2.14. The corresponding band structure at a drain voltage V_d of $-0.1\,\mathrm{V}$ and at a gate voltage V_g of $-0.5\,\mathrm{V}$ presented in figure 4.2.15 reveals a stronger band bending in direction perpendicular to the gate due to the use of a counter doped pocket and thus, a decreased tunneling length, being beneficial for BTBT. Without a counter doped pocket, band bending in direction perpendicular to the gate is less pronounced, consequently requiring higher gate voltages V_g to enable BTBT. In order to be able to evaluate the influence of the counter doped pocket on the overall device performance quantitatively, a reference sample without a counter doped pocket was processed in parallel to the ones with counter doped pocket. In addition, the temperature T during DS for 1 min in nitrogen atmosphere was varied between 400 °C and 500 °C as already indicated in chapter 4.1 in order to optimize the process flow for the planar SiGe/Si heterostructure p-TFET. The transfer characteristics and corresponding output characteristics shown in figures 4.2.16 and 4.2.17 summarize the obtained experimental results for these three different devices. The planar SiGe/Si heterostructure p-TFET drastically benefits from a counter doped pocket

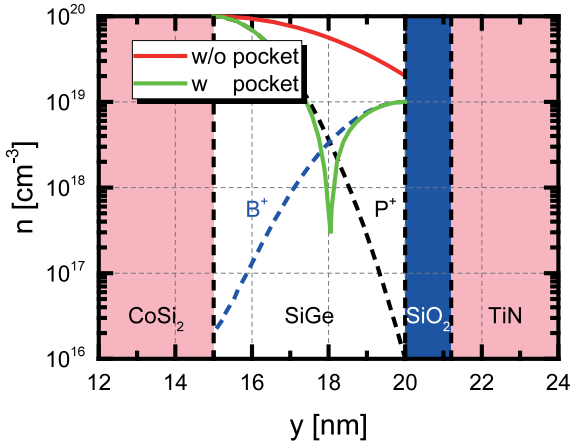


Figure 4.2.14: Simulated doping profile of the planar SiGe/Si heterostructure p-TFET. The introduction of a counter doped pocket at the source tunnel junction results in a sharpened doping profile and thus, enables a n^{++}-p^{+} tunnel junction, being much steeper as compared to the case without counter doped pocket.

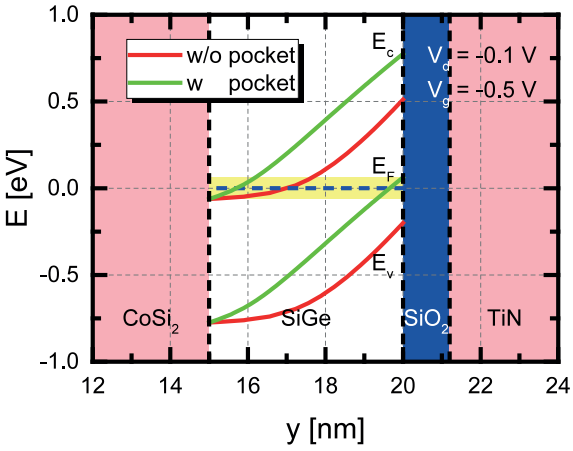


Figure 4.2.15: Simulated band structure of the planar SiGe/Si heterostructure p-TFET in direction perpendicular to the gate at a drain voltage V_d of $-0.1\,\mathrm{V}$ and at a gate voltage V_g of $-0.5\,\mathrm{V}$, revealing a stronger band bending in direction perpendicular to the gate due to the use of a counter doped pocket and thus, a decreased tunneling length, being beneficial for BTBT. Without a counter doped pocket, band bending in direction perpendicular to the gate is less pronounced, consequently requiring higher gate voltages V_g to enable BTBT.

enabling a high on-current I_on, a small subthreshold swing SS and a linear onset of the drain current I_d in parallel whereas the device without counter doped pocket suffers from a S-shaped, superlinear onset of the drain current I_d as a clear indication of a degraded source

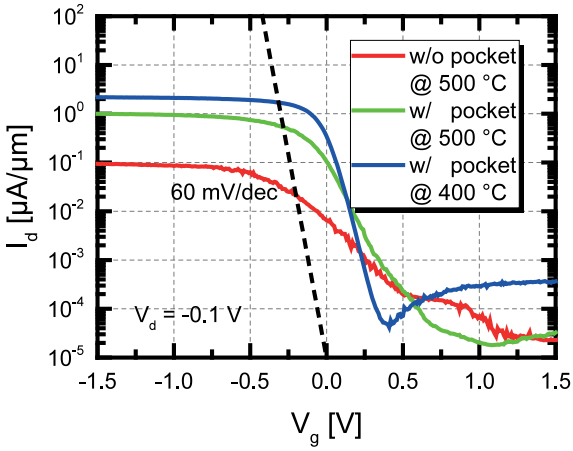


Figure 4.2.16: Measured transfer characteristics of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_d of $-0.1\,\mathrm{V}$, comparing the influence of the counter doped pocket as well as the impact of the temperature T during DS for 1 min in nitrogen atmosphere on the overall device performance. The planar SiGe/Si heterostructure p-TFET drastically benefits from a counter doped pocket enabling a high on-current I_on and a small subthreshold swing SS in parallel.

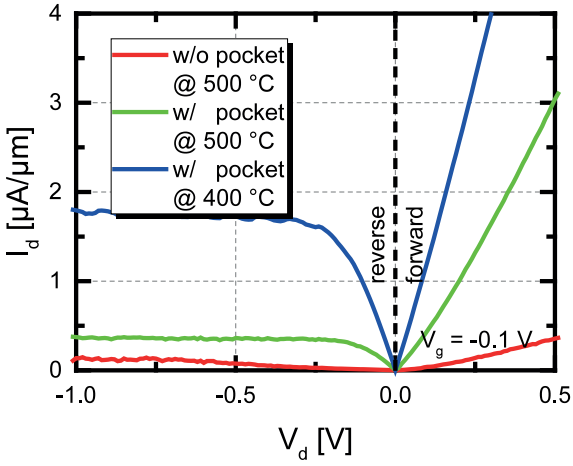


Figure 4.2.17: Measured output characteristics of the planar SiGe/Si heterostructure p-TFET at a gate voltage V_g of $-0.1\,\mathrm{V}$, comparing the influence of the counter doped pocket as well as the impact of the temperature T during DS on the overall device performance. The planar SiGe/Si heterostructure p-TFET drastically benefits from a counter doped pocket enabling a linear onset of the drain current I_d whereas the device without counter doped pocket suffers from a S-shaped, superlinear onset of the drain current I_d as a clear indication of a degraded source tunnel junction.

tunnel junction. Furthermore, a low temperature T of 400 °C during DS results in a sharper source doping profile and overall improved device performance.

The beneficial impact of both the selective and self-adjusted silicidation and the counter doped pocket at the source tunnel junction on the transfer characteristics of the planar SiGe/Si heterostructure p-TFET becomes even more obvious in TCAD simulations comparing a pure point tunneling device arising without a selective and self-adjusted silicidation with a line tunneling device either providing a counter doped pocket at the source tunnel junction or not. The corresponding carrier concentration n_s of the source was set to $1 \times 10^{20}\,\mathrm{cm}^{-3}$ with respect to the experimental reference obtained from ECV measurements as depicted in figure 4.1.5 whereas the carrier concentration n_d of the drain was assumed as $1 \times 10^{18}\,\mathrm{cm}^{-3}$. If considering a counter doped pocket, its carrier concentration n_p was set to $1 \times 10^{19}\,\mathrm{cm}^{-3}$. As further parameters for the TCAD simulations, the EOT was assumed as 1.2 nm in accordance with the EOT extracted from CV measurements on MOS capacitors as discussed in chapter 2.4.2 and the gate length L_g was set to 200 nm. Subsequently, the gate metal work function was adjusted to match the onset of the planar SiGe/Si heterostructure p-TFET with counter doped pocket at a gate voltage V_g of about 0 V, yielding a gate metal work function of 5.2 eV. TCAD simulations performed with Sentaurus Process suggest that low carrier concentration n_d of the drain of only $1 \times 10^{18}\,\mathrm{cm}^{-3}$, being beneficial for suppression of the ambipolar switching characteristics on the one hand [73], but resulting in a limitation of the drain current I_d for higher absolute gate voltages $|V_g|$ due to an increased series resistance on the other hand as visible from the measured transfer characteristics illustrated in figure 4.2.1. In this regard, a lower carrier concentration n_d of the drain despite its higher implantation dose of $2 \times 10^{14}\,\mathrm{cm}^{-2}$ as compared to the carrier concentration n_p of the counter doped pocket stemming from an implantation dose of $2 \times 10^{13}\,\mathrm{cm}^{-2}$ can be explained by the low thermal budget available in order to sustain the compressive, biaxial strain ε within the SiGe layer as already discussed in chapter 4.1, limiting solid phase epitaxial regrowth (SPER) as well as thermal activation of charge carriers. The higher implantation dose results in more pronounced damage within the SiGe layer at the drain side and thus, in a lower effective carrier concentration n_d of the drain as compared to the carrier concentration n_p of the counter doped pocket as visible from a contour plot of the simulated active carrier concentration n after implantation with Boron ions and thermal activation at a low temperature T of 500 °C for 1 min in nitrogen atmosphere presented in figure 4.2.18. In accordance with the results from TCAD process simulations, TCAD device simulations allow for a quantitative evaluation of the resulting transfer characteristics, comparing a pure point tunneling device arising without a selective and self-adjusted silicidation with a line tunneling device either providing a counter doped pocket at the source tunnel junction or not as shown in figure 4.2.19. The corresponding hole band-to-band (hBTB) generation rates at a drain voltage V_d of -0.1 V and at a gate voltage V_g of -0.5 V are depicted in figure 4.2.20, visualizing either point or line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT. On the one hand, without the concept of a selective and self-adjusted silicidation no increased area directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines can be realized, resulting in solely point tunneling, confined to a local area. On the other hand, the introduction of a counter doped pocket at the source tunnel junction enables a sharpened doping profile and thus, a reduced tunneling length, being beneficial for both the hBTB generation rate and the subthreshold swing SS. Moreover, a counter doped pocket at the source tunnel junction helps in reducing the onset voltage V_{onset} as a measure of the gate voltage V_g required in order to deplete parts of the source region directly underneath the gate as a precondition for line tunneling aligned

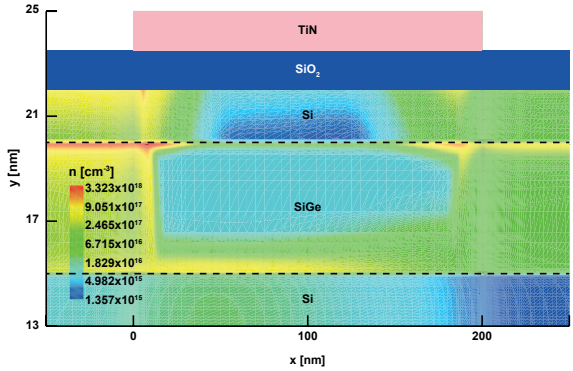


Figure 4.2.18: Contour plot of the simulated active carrier concentration n after implantation with Boron ions and thermal activation at a low temperature T of 500 °C for 1 min in nitrogen atmosphere, revealing a lower carrier concentration n_d of the drain despite its higher implantation dose of $2 \times 10^{14}\,\mathrm{cm}^{-2}$ as compared to the carrier concentration n_p of the counter doped pocket stemming from an implantation dose of $2 \times 10^{13}\,\mathrm{cm}^{-2}$.

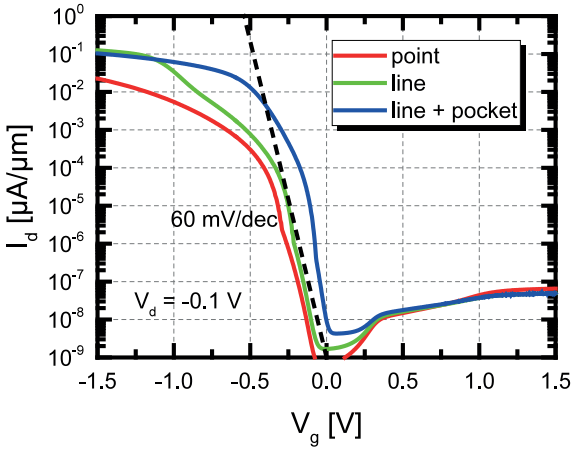


Figure 4.2.19: Simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_d of −0.1 V, revealing the beneficial impact of the selective and self-adjusted silicidation as well as the counter doped pocket in terms of on-current I_on and subthreshold swing SS.

with the gate electric field lines. In this regard, a reduction of the onset voltage V_onset can be achieved by tuning either the band gap E_g of the SiGe layer, the thickness t_ox of the gate oxide or the carrier concentration n_s of the source which has to be depleted in a region directly underneath the gate in order to allow for line tunneling aligned with the gate electric field lines as already discussed in chapter 2.3.5. In this regard, the carrier concentration n_s of the source is scaled by the carrier concentration n_p of the counter doped pocket as already

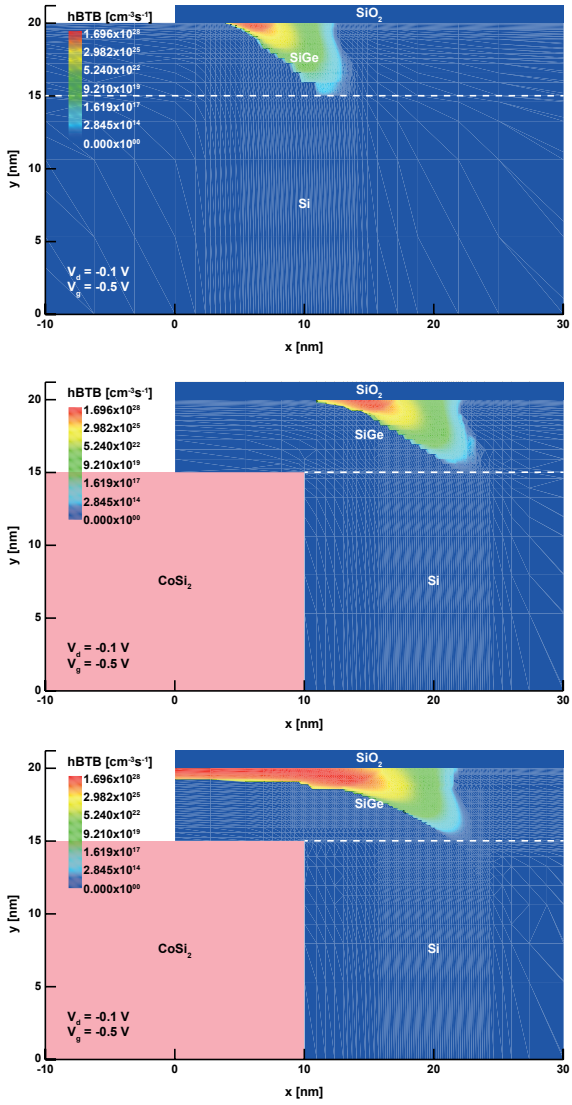


Figure 4.2.20: Contour plots of the simulated hBTB generation rates of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_d of $-0.1\,\mathrm{V}$ and at a gate voltage V_g of $-0.5\,\mathrm{V}$, comparing a pure point tunneling device with a line tunneling device either providing a counter doped pocket at the source tunnel junction or not. The line tunneling device with counter doped pocket not only exhibits the highest hBTB generation rate but also the greatest extent in a region directly underneath the gate.

suggested by the simulated doping profiles illustrated in figure 4.2.14, defining the overall steepness of the resulting doping profile at the source tunnel junction. This dependency of the onset voltage V_{onset} on the carrier concentration n_{p} of the counter doped pocket becomes even more obvious when varying the carrier concentration n_{p} of the counter doped pocket between $1 \times 10^{19}\,\mathrm{cm}^{-3}$, $2 \times 10^{19}\,\mathrm{cm}^{-3}$ and $5 \times 10^{19}\,\mathrm{cm}^{-3}$ as presented in figure 4.2.21, indicating a reduction of the onset voltage V_{onset} for increasing carrier concentrations n_{p} of the counter doped pocket. Subsequently, the impact of the thickness t_{ox} of the gate oxide on the simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET as well as on its onset voltage V_{onset} is considered by reducing the EOT from 1.2 nm to 0.8 nm in case of a further optimized process for gate stack cleaning and deposition as visible from figure 4.2.22. As predicted, a reduction of the thickness t_{ox} of the gate oxide not only results in a lowered onset voltage V_{onset}, but also enables a drastically improved subthreshold swing SS of the planar SiGe/Si heterostructure p-TFET due to improved electrostatic control, being beneficial for BTBT. The impact of the band gap E_{g} of the SiGe layer on the simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET as well as on its onset voltage V_{onset} is considered by going from compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ with an indirect band gap E_{g} of about 0.71 eV at room temperature $T = 300\,\mathrm{K}$ to compressively, biaxially strained $Si_{0.3}Ge_{0.7}$ with an indirect band gap E_{g} of about 0.63 eV at room temperature $T = 300\,\mathrm{K}$ as shown in figure 4.2.23, renouncing even higher Ge mole fractions x due to the lack of consistent BTBT parameters required in order to sufficiently treat compressively, biaxially strained SiGe as a material with direct band gap E_{g}. In this regard, enabling of a direct band gap E_{g} transition for higher Ge mole fractions x than 0.7 is expected to give a drastic boost to the generation rates G of electrons and holes according to equation

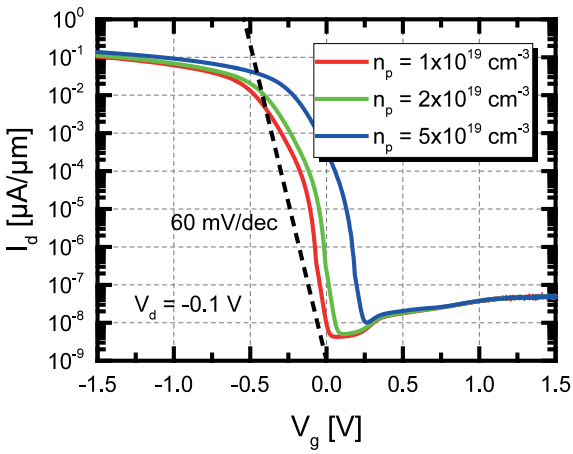


Figure 4.2.21: Simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_{d} of $-0.1\,\mathrm{V}$ when varying the carrier concentration n_{p} of the counter doped pocket, revealing a reduction of the onset voltage V_{onset} as a measure of the gate voltage V_{g} required in order to deplete parts of the source region directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines for increasing carrier concentrations n_{p} of the counter doped pocket.

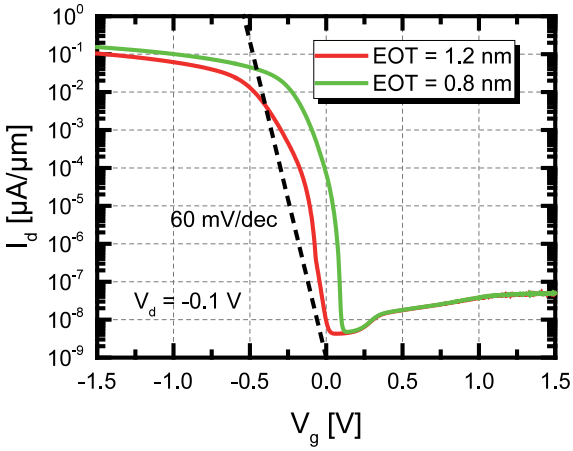


Figure 4.2.22: Simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_d of $-0.1\,\mathrm{V}$ when reducing the EOT from 1.2 nm to 0.8 nm, highlighting a drastically lowered subthreshold swing SS due to an improved electrostatic control, being beneficial for BTBT.

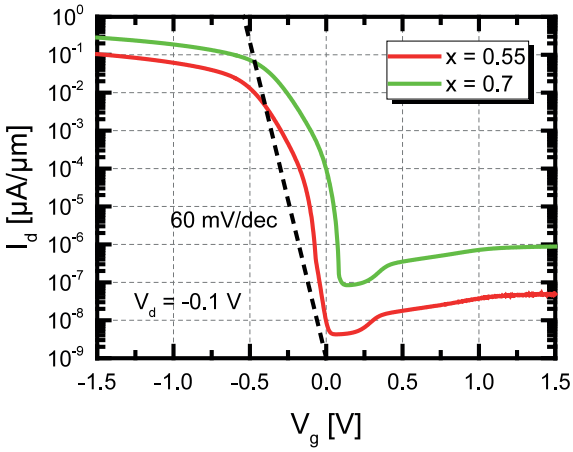


Figure 4.2.23: Simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_d of $-0.1\,\mathrm{V}$ when increasing the Ge mole fraction x from 0.55 to 0.7, enabling both an increased on-current I_on and an improved subthreshold swing SS.

(2.3.11), resulting in both an increased on-current I_on and an improved subthreshold swing SS [74]. Nevertheless, even in the case of an indirect band gap E_g transition, a reduction of the band gap E_g of the SiGe layer not only results in a lowered onset voltage V_onset, but also enables both an increased on-current I_on and an improved subthreshold swing SS of the planar SiGe/Si heterostructure p-TFET. However, this increase of the on-current I_on scales with an increase of the off-current I_off due to an increased SRH generation, resulting in an

only comparable ratio of on- to off-current $\frac{I_{on}}{I_{off}}$ with the latter to be effectively overcome by going from an indirect to a direct band gap E_g transition. In this regard, increasing the Ge mole fraction x above 0.7 in order to enable a direct band gap E_g transition requires a reduction of the thickness of the SiGe layer with respect to the critical thickness caused by the lattice mismatch between Si and Ge as already discussed in chapter 2.4.1. As a consequence, a variation of the thickness t_{SiGe} of the compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ between 3 nm, 5 nm and 7 nm is taken into account by means of TCAD simulations as visible from figure 4.2.24. Both the simulated transfer characteristics and the onset voltage V_{onset} are quite sensitive to a change of the thickness t_{SiGe} of the SiGe layer, defining the source tunnel junction. Increasing the thickness t_{SiGe} of the SiGe layer from 5 nm to 7 nm results in degraded electrostatic control due to the exponential decay of the electric field F within the SiGe layer, thus reducing the on-current I_{on} of the planar SiGe/Si heterostructure p-TFET. However, decreasing the thickness t_{SiGe} of the SiGe layer from 5 nm to 3 nm also reveals a degraded transfer characteristics due to arising quantization effects, limiting line tunneling aligned with the gate electric field lines. Thus, the initial thickness t_{SiGe} of the SiGe layer of 5 nm seems to be a reasonable trade-off between degraded electrostatic control and arising quantization effects, coinciding with simulations from [75] which take field-induced quantum confinement (FIQC) into account, claiming an optimal thickness of the counter doped pocket in the range of 3 nm to 4 nm.

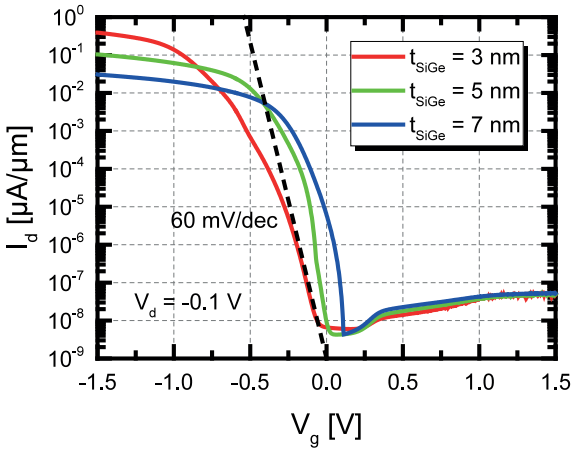


Figure 4.2.24: Simulated transfer characteristics of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_d of -0.1 V when varying the thickness t_{SiGe} of the compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ between 3 nm, 5 nm and 7 nm, revealing degraded electrostatic control due to the exponential decay of the electric field F within the SiGe layer as well as a limitation of line tunneling aligned with the gate electric field lines due to arising quantization effects.

4.2.2 Pulsed Measurements

DC characterization in combination with TCAD simulations as provided in chapter 4.2.1 allowed for a sufficient description of the switching behavior of the planar SiGe/Si heterostructure p-TFET, being dominated by the influence of the selective and self-adjusted silicidation as well as the counter doped pocket at the source tunnel junction. Contributions from a parasitic MOSFET or a parasitic SCHOTTKY barrier MOSFET, resulting in a subthreshold swing SS greater or equal than 60 mV/dec, could be excluded experimentally by measuring the transfer characteristics of the planar SiGe/Si heterostructure p-TFET in p-MOS mode on the one hand and investigating the dependency of the on-current I_{on} on the gate length L_{g} on the other hand. TCAD simulations suggested the observed degradation of the subthreshold swing SS of the planar SiGe/Si heterostructure p-TFET above 60 mV/dec stemming from TAT. Subsequently, this chapter discusses pulsed measurements as one possibility to diminish the influence of TAT and thus, allow for an improved subthreshold swing SS of the planar SiGe/Si heterostructure p-TFET. As already discussed in chapter 2.3.3, TAT relies on trapping and detrapping of thermally excited carriers. This thermal excitation occurs on a certain time scale, making TAT sensitive to a time-dependent variation of voltage pulses applied to the device.

Pulsed measurements are realized by means of a three terminal setup performed with a Tektronix AWG7122C Arbitrary Waveform Generator applying voltage pulses to the device and a Tektronix DPO70604C Digital & Mixed Signal Oscilloscope visualizing the resulting voltage pulses arising from the device as its answer to the input [76, 77]. Measurements of the transfer characteristics are performed in both p-TFET mode and p-MOS mode by pulsing the gate voltage V_{g} as a function of the time t while keeping the drain voltage V_{d} constant at -0.1 V and visualizing the corresponding source current I_{s}. The pulse length t_{pulse} for the gate pulse is kept constant at 1 ms with a repetition rate of 20 ms. The resulting time response of the planar SiGe/Si heterostructure p-TFET to the gate pulse in case of biasing in both p-TFET mode and p-MOS mode is depicted in figures 4.2.25 and 4.2.26. The source current I_{s} as a function of the time t exhibits a faster relaxation in case of biasing in p-MOS mode as compared to in case of biasing in p-TFET mode. For this particular case, the (gated) tunnel diode is biased in forward direction, resulting in charge transport enabled by thermionic emission over a potential barrier. However, in case of biasing in p-TFET mode, charge transport depends on both BTBT and TAT with the latter being a time dependent mechanism further degrading a relaxation of the source current I_{s}. Thus, analysis of the time response to the gate pulse in case of biasing in p-MOS mode allows for an evaluation of the relaxation of the source current I_{s} of the planar SiGe/Si heterostructure p-TFET caused by parasitic capacitances, yielding a value of the corresponding time constant τ in the range between 400 µs and 500 µs. As a consequence, the time response of the planar SiGe/Si heterostructure p-TFET to the gate pulse is dominated by parasitic capacitances below this time scale whereas an even longer relaxation of the source current I_{s} must result from a further time dependent process such as TAT. Subsequently, in order to quantitatively evaluate the influence of TAT, the respective source current I_{s} in case of biasing in both p-TFET mode and p-MOS mode is extracted at times t of 400 µs, 500 µs and 1 ms for different gate voltages V_{g} and is plotted in parallel with the corresponding transfer characteristics of the planar SiGe/Si heterostructure p-TFET obtained by DC characterization, allowing

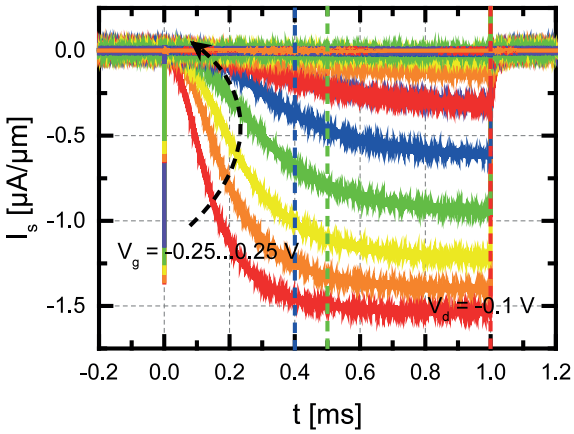


Figure 4.2.25: Measured time response of the planar SiGe/Si heterostructure p-TFET to the gate pulse at a drain voltage V_d of $-0.1\,\mathrm{V}$ in case of biasing in p-TFET mode, exhibiting a slower relaxation as compared to in case of biasing in p-MOS mode. For this particular case, charge transport depends on both BTBT and TAT with the latter being a time dependent mechanism further degrading a relaxation of the source current I_s.

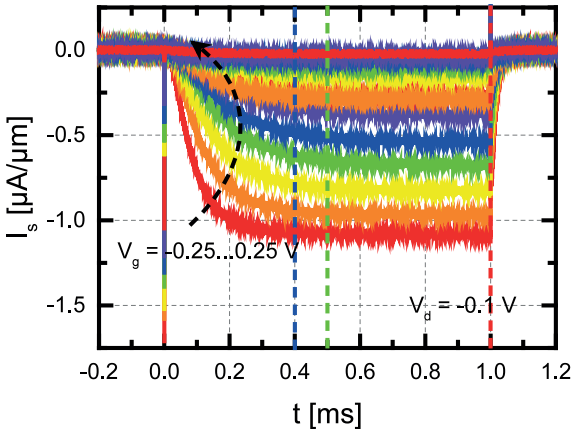


Figure 4.2.26: Measured time response of the planar SiGe/Si heterostructure p-TFET to the gate pulse at a drain voltage V_d of $-0.1\,\mathrm{V}$ in case of biasing in p-MOS mode, exhibiting a faster relaxation as compared to in case of biasing in p-TFET mode. For this particular case, the (gated) tunnel diode is biased in forward direction, resulting in charge transport enabled by thermionic emission over a potential barrier.

for a comparison between DC and pulsed measurement as illustrated in figures 4.2.27 and 4.2.28. As expected, pulsed measurements do not differ from DC measurements in case of biasing in p-MOS mode since charge transport is based on thermionic emission over a potential barrier. However, in case of biasing in p-TFET mode, pulsed measurements reveal

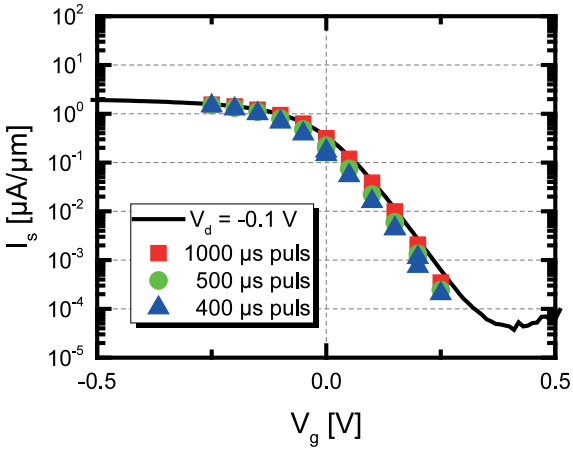


Figure 4.2.27: Transfer characteristics of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_d of $-0.1\,\mathrm{V}$ obtained by pulsed measurements in case of biasing in p-TFET mode, revealing a lowered subthreshold swing SS due to a diminished influence of TAT, scaling with the actual pulse length.

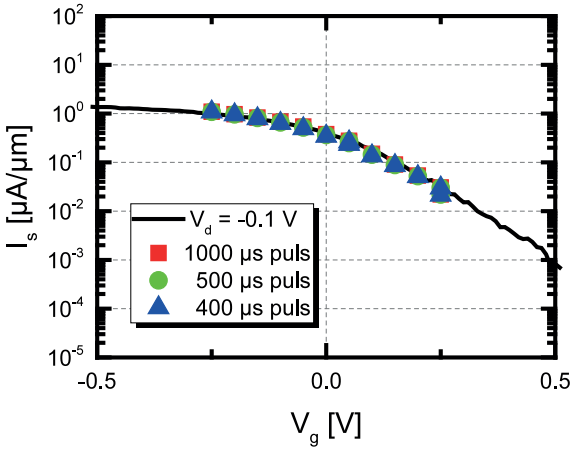


Figure 4.2.28: Transfer characteristics of the planar SiGe/Si heterostructure p-TFET at a drain voltage V_d of $-0.1\,\mathrm{V}$ obtained by pulsed measurements in case of biasing in p-MOS mode, revealing no difference as compared to DC measurements since charge transport is based on thermionic emission over a potential barrier due to the (gated) tunnel diode biased in forward direction.

a lowered subthreshold swing SS due to a diminished influence of TAT, scaling with the actual pulse length. Thus, a degradation of the transfer characteristics of the planar SiGe/Si heterostructure p-TFET due to TAT can be encountered by means of pulsed measurements, enabling a reduced activation of traps and thus, a more pronounced contribution from BTBT.

Coming along with the lowered subthreshold swing SS due to a diminished influence of TAT, a later onset of the transfer characteristics of the planar SiGe/Si heterostructure p-TFET can be observed as already discussed in chapter 2.3.3.

4.2.3 Low Temperature Analysis

In order to allow for a more detailed discussion of the physics emerging in the planar SiGe/Si heterostructure p-TFET low temperature T measurements are performed. The corresponding transfer characteristics at different temperatures T in case of biasing in p-TFET mode are presented in figure 4.2.29, highlighting the different contributions from both TAT and BTBT to the overall drain current I_d of the planar SiGe/Si heterostructure p-TFET. In this regard, the assignment of the respective gate voltage windows ΔV_g to TAT and BTBT respectively will be discussed in detail below. The transfer characteristics reveal the drain current I_d of the planar SiGe/Si heterostructure p-TFET nearly determined by solely BTBT at low temperatures T due to a freeze-out of traps, resulting in a drastically improved subthreshold swing SS far below 60 mV/dec. The corresponding dependency of the subthreshold swing SS on the temperature T is shown in figure 4.2.30, revealing a non-linear relation as predicted for a TFET with a minimum subthreshold swing SS in the BTBT regime as low as 30 mV/dec [78, 79]. However, below a temperature T of about 120 K, the subthreshold swing SS no longer improves for decreasing temperatures T due to a freeze-out of phonons occurring at one fourth of the Debye temperature $T = \frac{\Theta_\mathrm{D}}{4}$ [80, 81], thus limiting phonon-assisted BTBT as the dominant mechanism to charge transport in compressively, biaxially strained SiGe for Ge mole fractions up to $x \leq 0.7$ as already discussed in chapter 2.4.1. In addition to the subthreshold swing SS, the on-current I_on of the planar SiGe/Si heterostructure p-TFET may yield as a further figure of merit. The corresponding dependency of the on-current I_on on the temperature T is depicted in figure 4.2.31, revealing a linear decrease of the on-current I_on of the planar SiGe/Si heterostructure p-TFET for decreasing temperatures T, being contrary to the dependency on the temperature T in case of a MOSFET as visible from equation (2.2.4) in chapter 2.2.1. In order to evaluate the impact of the temperature T on both the subthreshold swing SS and the on-current I_on in more detail, a functional relation between the drain current I_d arising in the planar SiGe/Si heterostructure p-TFET and the temperature T is required. In this regard, the dependency of the drain current I_d on the gate voltage V_g in case of line tunneling aligned with the gate electric field lines was already discussed in chapter 2.3.5. Expressing this proportionality in detail yields [36]:

$$I_\mathrm{d} = WLTP\sqrt{V_\mathrm{g} - V_\mathrm{onset}}\exp\left(S\sqrt{V_\mathrm{g} - V_\mathrm{onset}}\right), \tag{4.2.1}$$

where W and L denote the gate width and gate length respectively overlapping the source. The onset voltage V_onset as a measure of the gate voltage V_g required in order to deplete parts of the source region directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines in turn can be expressed as [37, 36]:

$$V_\mathrm{onset} = V_\mathrm{fb} + \frac{E_\mathrm{g}}{e}\left(1 + 2\frac{\kappa_\mathrm{sc}}{\kappa_\mathrm{ox}}t_\mathrm{ox}\sqrt{\frac{e^2 n_\mathrm{s}}{2E_\mathrm{g}\kappa_\mathrm{sc}}}\right), \tag{4.2.2}$$

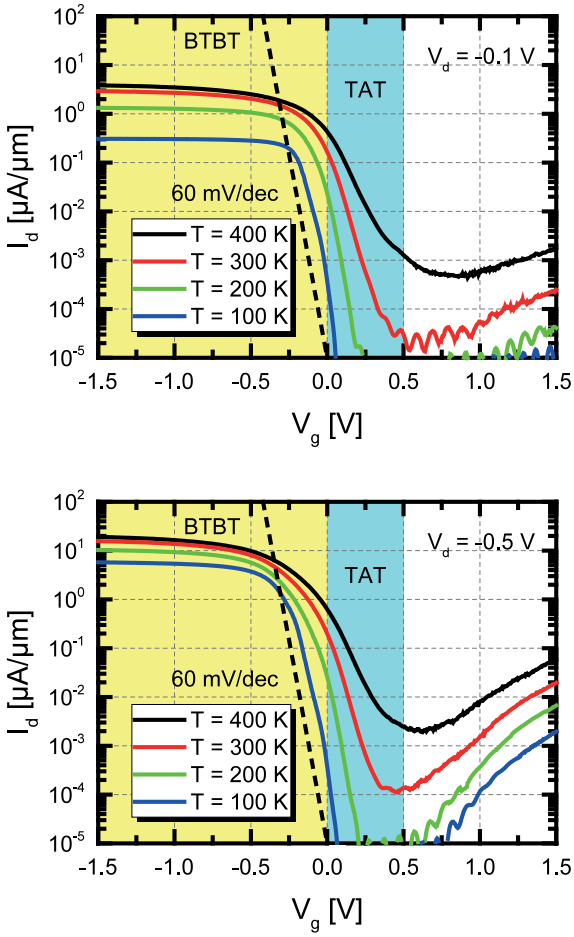


Figure 4.2.29: Measured transfer characteristics of the planar SiGe/Si heterostructure p-TFET at different temperatures T for drain voltages V_d of $-0.1\,\mathrm{V}$ and $-0.5\,\mathrm{V}$ in case of biasing in p-TFET mode, highlighting the different contributions from both TAT and BTBT to the overall drain current I_d of the planar SiGe/Si heterostructure p-TFET.

where the dielectric constant κ_sc of the semiconductor corresponds to the one of compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ in case of the planar SiGe/Si heterostructure p-TFET, suggesting a value of 14.2. Subsequently, the material dependent parameters T and S are given by [37, 36]:

$$T = \sqrt{\frac{eE_\mathrm{g}^3 n_\mathrm{s}^2}{4\kappa_\mathrm{sc}^2 \gamma}} \frac{A_\mathrm{ind}}{B_\mathrm{ind}} \exp\left(-\sqrt{\frac{2\kappa_\mathrm{sc}}{E_\mathrm{g} n_\mathrm{s}}} B_\mathrm{ind}\right) \quad \text{and} \quad S = \sqrt{\frac{2e\kappa_\mathrm{sc}}{E_\mathrm{g}^2 n_\mathrm{s} \gamma}} B_\mathrm{ind}, \tag{4.2.3}$$

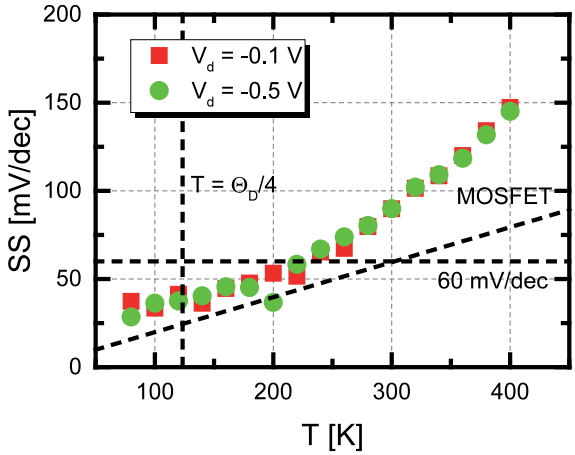


Figure 4.2.30: Subthreshold swing SS of the planar SiGe/Si heterostructure p-TFET as a function of the temperature T, revealing a non-linear relation as predicted for a TFET with a minimum subthreshold swing SS in the BTBT regime as low as 30 mV/dec. A freeze-out of phonons occurs at a temperature T of about 120 K, corresponding to one fourth of the DEBYE temperature $T = \frac{\Theta_D}{4}$ as indicated by a dotted vertical line.

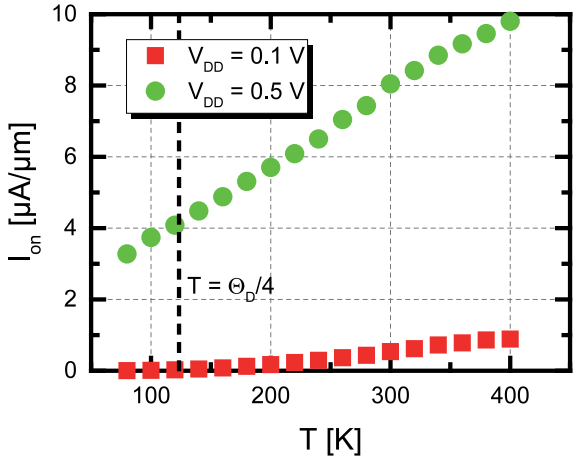


Figure 4.2.31: On-current I_{on} of the planar SiGe/Si heterostructure p-TFET as a function of the temperature T, revealing a linear decrease of the on-current I_{on} of the planar SiGe/Si heterostructure p-TFET for decreasing temperatures T, being contrary to the dependency on the temperature T in case of a MOSFET. A freeze-out of phonons occurs at a temperature T of about 120 K, corresponding to one fourth of the DEBYE temperature $T = \frac{\Theta_D}{4}$ as indicated by a dotted vertical line.

where the material dependent parameters A_{ind} and B_{ind} are defined in equation (2.3.13) in chapter 2.3.2, taking the interaction with phonons required for phonon assisted BTBT into

account. The parameter γ in turn resembles a screening length and can be described as [37, 36]:

$$\gamma = 1 + \frac{\kappa_{\mathrm{sc}}}{\kappa_{\mathrm{ox}}} t_{\mathrm{ox}} \sqrt{\frac{e^2 n_{\mathrm{s}}}{2 E_{\mathrm{g}} \kappa_{\mathrm{sc}}}}. \tag{4.2.4}$$

However, the material dependent parameter P introduced in equation (4.2.1) does not show up in the original references since the analytical model was derived for the case of line tunneling aligned with the gate electric field lines in a direct band gap E_{g} semiconductor. As a consequence, the exponent of the electric field F describing the generation rates G of electrons and holes according to equation (2.3.11) as derived by KANE's semiclassical, local model was assumed as 2. In order to account for the indirect band gap E_{g} of compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ in case of the planar SiGe/Si heterostructure p-TFET the exponent was adjusted to 2.5 as already discussed in chapter 2.3.2, yielding the additional parameter P which is given by [37]:

$$P = \left(\frac{E_{\mathrm{g}} n_{\mathrm{s}}}{2 \kappa_{\mathrm{sc}}} \right)^{1/4}. \tag{4.2.5}$$

Summarizing, equation (4.2.1) not only provides the functional relation between the drain current I_{d} and the gate voltage V_{g} in case of line tunneling aligned with the gate electric field lines, but also reveals the corresponding dependency of the drain current I_{d} on the band gap E_{g} of the semiconductor. In addition, the dependency of the band gap E_{g} of the semiconductor on the temperature T can be described by means of VARSHNI's relation as follows [82, 83]:

$$E_{\mathrm{g}}(T) = E_{\mathrm{g},0} - \frac{\alpha T^2}{T + \beta}, \tag{4.2.6}$$

with $E_{\mathrm{g},0}$ denoting the band gap at a temperature T of 0 K as well as α and β being material dependent parameters. In this regard, the band gap $E_{\mathrm{g},0}$ of compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ in case of the planar SiGe/Si heterostructure p-TFET at a temperature T of 0 K was extrapolated from its band gap $E_{\mathrm{g},300}$ at room temperature $T = 300\,\mathrm{K}$ with the latter assumed as 0.71 eV according to TCAD simulations. Subsequently, by combining equations (4.2.1) and (4.2.6), the functional relation between the drain current I_{d} arising in the planar SiGe/Si heterostructure p-TFET and the temperature T can be derived, allowing for an evaluation of the dependencies of both the subthreshold swing SS and the on-current I_{on} on the band gap E_{g}. In this regard, the dependency of the on-current I_{on} on the band gap E_{g} is given by:

$$I_{\mathrm{on}} \propto \underbrace{T}_{\propto E_{\mathrm{g}}^{-1/4} \exp(-E_{\mathrm{g}})} \underbrace{P}_{\propto E_{\mathrm{g}}^{1/4}} \underbrace{\sqrt{V_{\mathrm{g}} - V_{\mathrm{onset}}}}_{\propto E_{\mathrm{g}}^{1/4}} \exp\Big(\underbrace{S}_{\propto E_{\mathrm{g}}^{3/4}} \underbrace{\sqrt{V_{\mathrm{g}} - V_{\mathrm{onset}}}}_{\propto E_{\mathrm{g}}^{1/4}} \Big) \propto E_{\mathrm{g}}^{1/4}. \tag{4.2.7}$$

Plotting the on-current I_{on} of the planar SiGe/Si heterostructure p-TFET as a function of the fourth root of the band gap $E_{\mathrm{g}}^{1/4}$ as illustrated in figure 4.2.32 reveals a linear dependency as a clear indication of line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT. However, a slight degradation of this linear dependency can be observed which can be explained by the analytical model itself, derived for semiconductors with a direct band gap E_{g} and only adapted to an indirect band gap E_{g} by adjusting the

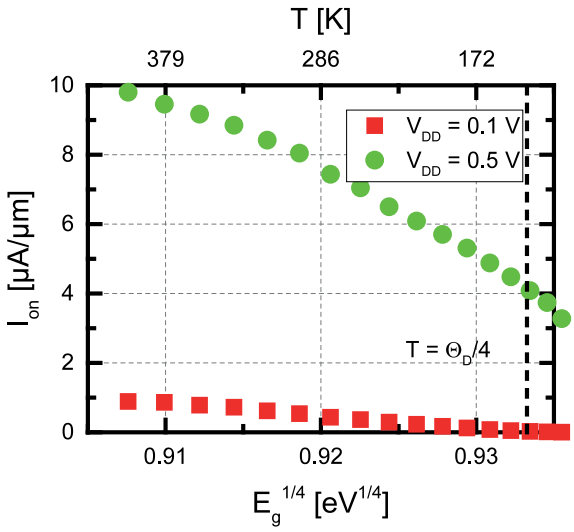


Figure 4.2.32: On-current I_{on} of the planar SiGe/Si heterostructure p-TFET as a function of the fourth root of the band gap $E_{\mathrm{g}}^{1/4}$, revealing a linear dependency as a clear indication of line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT. A freeze-out of phonons occurs at a temperature T of about 120 K, corresponding to one fourth of the Debye temperature $T = \frac{\Theta_{\mathrm{D}}}{4}$ as indicated by a dotted vertical line.

exponent of the electric field F from 2 to 2.5. Moreover, the actual value of the band gap E_{g} of compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ of 0.71 eV might be underestimated since TiN metal gates deposited by AVD are known to introduce compressive stress in Si layers [84], enabling an additional compressive strain ε in the embedded SiGe layer and thus a further decreased band gap E_{g}. Subsequently, the dependency of the subthreshold swing SS on the band gap E_{g} can be derived by means of equations (4.2.1) and (4.2.6):

$$SS = \left[\frac{\partial \log I_{\mathrm{d}}}{\partial V_{\mathrm{g}}}\right]^{-1} \propto \underbrace{\overbrace{\sqrt{V_{\mathrm{g}} - V_{\mathrm{onset}}}}^{\propto E_{\mathrm{g}}^{1/4}}}_{\propto E_{\mathrm{g}}^{3/4}} \propto E_{\mathrm{g}}^{-1/2}. \tag{4.2.8}$$

Plotting the subthreshold swing SS of the planar SiGe/Si heterostructure p-TFET as a function of the reciprocal of the second root of the band gap $E_{\mathrm{g}}^{-1/2}$ as presented in figure 4.2.33 also reveals a linear dependency as a clear indication of line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT. In contrast to the on-current I_{on}, no degradation of this linear dependency becomes obvious which can be explained by the subthreshold swing SS being the reciprocal of the first derivative of the logarithmic of the drain current $\log I_{\mathrm{d}}$ with respect to the gate voltage V_{g}, thus vanishing the contribution from the material dependent parameter P introduced by adjusting the exponent of the electric field F from 2 to 2.5. Instead, a saturation of the subthreshold

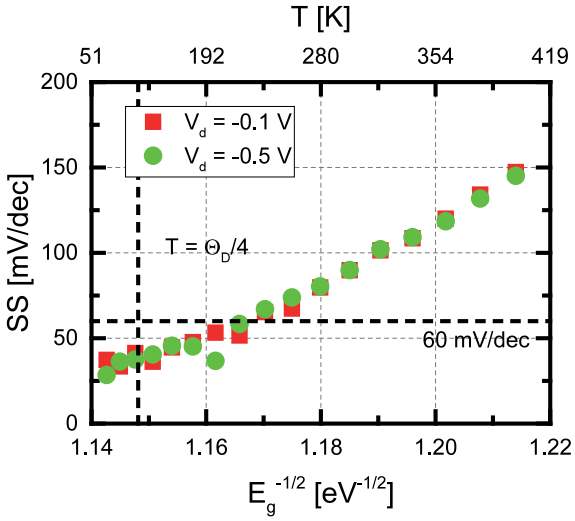


Figure 4.2.33: Subthreshold swing SS of the planar SiGe/Si heterostructure p-TFET as a function of the reciprocal of the second root of the band gap $E_g^{-1/2}$, revealing a linear dependency as a clear indication of line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT. A freeze-out of phonons occurs at a temperature T of about 120 K, corresponding to one fourth of the DEBYE temperature $T = \frac{\Theta_D}{4}$ as indicated by a dotted vertical line.

swing SS below a temperature T of 120 K becomes obvious once more due to the freeze-out of phonons occurring at one fourth of the DEBYE temperature $T = \frac{\Theta_D}{4}$ as already discussed.

In addition to the dependencies of both the subthreshold swing SS and the on-current I_{on} on the temperature T, the dependencies of the material dependent parameters A_{ind} and B_{ind} on the temperature T are worth to be investigated, allowing for an analysis of the impact of the temperature T on BTBT arising in the planar SiGe/Si heterostructure p-TFET. In this regard, transforming of equation (4.2.1) yields:

$$\ln\left(\frac{I_d}{\sqrt{V_g - V_{onset}}}\right) = \ln(WLTP) + S\sqrt{V_g - V_{onset}}. \tag{4.2.9}$$

Taking equation (4.2.3) into account, the material dependent parameter B_{ind} at a given temperature T can be obtained as the slope of a linear regression with respect to equation (4.2.9) whereas the material dependent parameter A_{ind} is proportional to its intercept. Thus, a value of the material dependent parameter B_{ind} of 10.6 MV/cm at room temperature $T = 300$ K is revealed in case of a drain voltage V_d of -0.1 V whereas a drain voltage V_d of -0.5 V suggests a value of 20.2 MV/cm at room temperature $T = 300$ K. That significant difference in the values of the material dependent parameter B_{ind} can be attributed to a missing treatment of the influence of an applied drain voltage V_d on BTBT in KANE's semiclassical, local model, allowing for BTBT currents flowing even when no drain voltage

V_d is applied since generation rates G of electrons and holes are only a function of the electric field F, but not of the drain voltage V_d as already discussed in chapter 2.3.1. As a consequence, the value of the material dependent parameter B_ind of 20.2 MV/cm at a drain voltage V_d of -0.5 V is less trusted since a higher absolute drain voltage $|V_\mathrm{d}|$ only modulates the overall channel resistance but has no beneficial impact on the actual potential barrier at the source tunnel junction, determining BTBT. Taking the value of the material dependent parameter B_ind of 10.6 MV/cm at a drain voltage V_d of -0.1 V into account, a much smaller value as compared to literature is revealed [42], suggesting values of the material dependent parameter B_ind in the range of 13.8 MV/cm to 15.9 MV/cm in case of compressively, biaxially strained $Si_{0.45}Ge_{0.55}$. In this regard, a small value of the material dependent parameter B_ind results in increased generation rates G of electrons and holes according to equation (2.3.12) and thus, enhanced BTBT. The extracted value of the material dependent parameter B_ind of 10.6 MV/cm at room temperature $T = 300$ K corresponds to a Ge mole fraction x of more than 0.7 and subsequently, to a band gap E_g of at most 0.63 eV in case of compressively, biaxially strained SiGe [42], arising from a further reduced band gap E_g as compared to solely pseudomorphic growth. Thus, the smaller value of the material dependent parameter B_ind coincides with a reduced band gap E_g due to additional compressive strain ε arising from the TiN metal gate deposited by AVD as already indicated. It is worth mentioning that a band gap E_g of 0.63 eV suggests an optimal supply voltage V_DD of the planar SiGe/Si heterostructure p-TFET of about 0.5 V according to $V_\mathrm{DD}^\mathrm{optimized} \approx \frac{E_\mathrm{g}}{1.2e}$ [85], coinciding with the results obtained by DC measurements as already discussed in chapter 4.2.1.

Subsequently, the corresponding dependency of the material dependent parameter B_ind on the band gap E_g can be evaluated by means of equation (2.3.13). Plotting the square of the third root of the material dependent parameter $B_\mathrm{ind}^{2/3}$ as a function of the band gap E_g as shown in figure 4.2.34 reveals a linear dependency with the slope of the curve being proportional to the third root of the reduced tunneling mass $m_\mathrm{r}^{1/3}$ as a clear indication of BTBT dominating charge transport in the planar SiGe/Si heterostructure p-TFET. In addition, the degradation of the linear dependency due to the freeze-out of phonons occurring at one fourth of the Debye temperature $T = \frac{\Theta_\mathrm{D}}{4}$ becomes obvious as well.

In summary, low temperature T measurements enable evaluation of BTBT and its influence on subthreshold swing SS and on-current I_on due to a freeze-out of traps. Line tunneling aligned with the gate electric field lines is revealed as the dominant contribution to BTBT in the planar SiGe/Si heterostructure p-TFET. In order to allow for further analysis of the traps and their impact on the charge transport arising in the planar SiGe/Si heterostructure p-TFET, an extraction of their activation energy E_a is required. In this regard, the dependency of the drain current I_d on the activation energy E_a is given by [27, 86, 87, 32]:

$$I_\mathrm{d} \propto \exp\left(-\frac{E_\mathrm{a}}{k_\mathrm{B}T}\right), \tag{4.2.10}$$

By means of an Arrhenius plot as depicted in figure 4.2.35 the corresponding activation energy E_a of the traps is extracted as the slope of the natural logarithm of the drain current $\ln(I_\mathrm{d})$ in the high temperature T regime according to equation (4.2.10). Below a temperature T of 240 K a freeze-out of traps occurs, coming along with the slope of the natural logarithm of the drain current $\ln(I_\mathrm{d})$ nearly vanishing, thus resulting in no further contribution of TAT

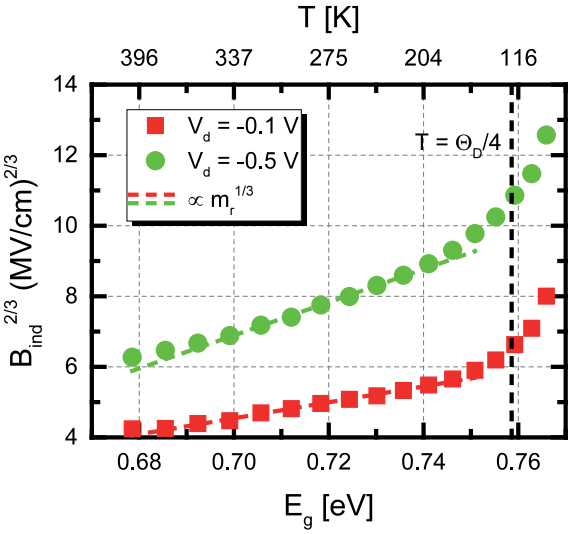


Figure 4.2.34: Third root squared of the material dependent parameter $B_{\mathrm{ind}}^{2/3}$ of the planar SiGe/Si heterostructure p-TFET as a function of the band gap E_{g}, revealing a linear dependency as a clear indication of BTBT dominating charge transport in the planar SiGe/Si heterostructure p-TFET. The slope of the curve is proportional to the third root of the reduced tunneling mass $m_{\mathrm{r}}^{1/3}$. A freeze-out of phonons occurs at a temperature T of about 120 K, corresponding to one fourth of the Debye temperature $T = \frac{\Theta_{\mathrm{D}}}{4}$ as indicated by a dotted vertical line.

to the overall drain current I_{d} of the planar SiGe/Si heterostructure p-TFET. However, a pronounced dependency of the slope of the natural logarithm of the drain current $\ln(I_{\mathrm{d}})$ on the gate voltage V_{g} becomes obvious in the high temperature T regime, enabling an extraction of the activation energy E_{a} of the traps. Plotting the resulting activation energies E_{a} as a function of the corresponding gate voltage V_{g} as illustrated in figure 4.2.36 allows for an assignment of the respective activation energies E_{a} to SRH, TAT and BTBT as already suggested when discussing the transfer characteristics of the planar SiGe/Si heterostructure p-TFET at different temperatures T. Above activation energies E_{a} of half of the band gap $\frac{E_{\mathrm{g}}}{2}$ charge transport is dominated by SRH whereas activation energies E_{a} below 0.1 eV enable BTBT [27]. As a consequence, charge transport is dominated by TAT for activation energies E_{a} in between SRH and BTBT regime. In case of biasing in p-TFET mode, a sharp transition of the activation energy E_{a} from both SRH and TAT to BTBT regime is realized independently of the applied drain voltage V_{d} within a small gate voltage window ΔV_{g} of less than 0.4 V, being much steeper as compared to state of the art Si, SiGe or Ge source n-TFETs [88], and even comparable to III-V n-TFETs with Zn diffusion, enabling both box-like, sharp doping profiles and BTBT without phonon interaction due a direct band gap E_{g} transition [89, 90]. In addition, the extracted activation energies E_{a} hardly reach the SRH regime above $\frac{E_{\mathrm{g}}}{2}$, being responsible for the low off-current I_{off} of the planar SiGe/Si heterostructure p-TFET as already suggested when discussing the simulated transfer characteristics. However, in case of biasing in p-MOS mode, that sharp transition of the

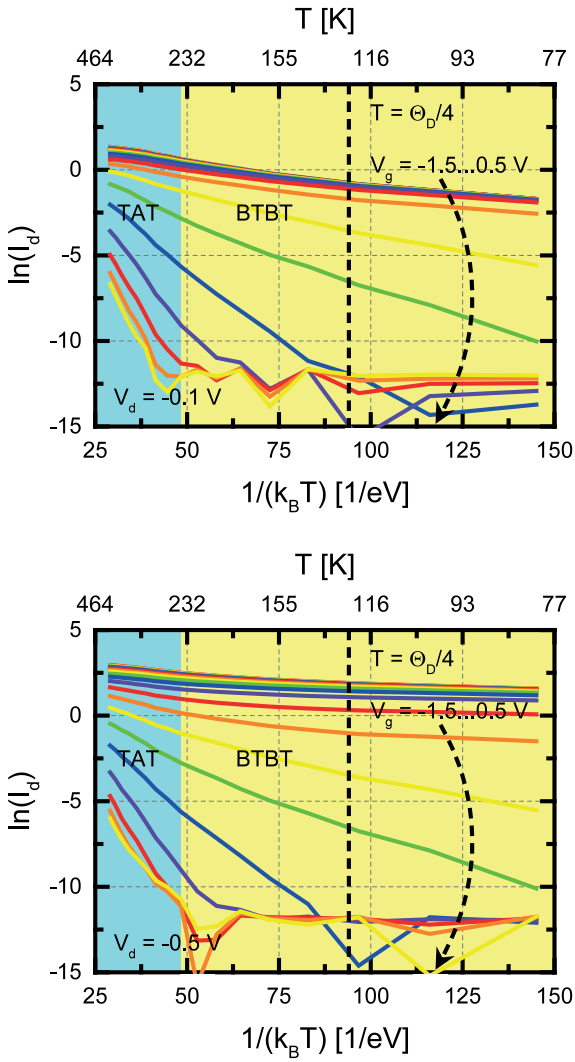


Figure 4.2.35: ARRHENIUS plot of the logarithmic of the drain current $\ln(I_\mathrm{d})$ of the planar SiGe/Si heterostructure p-TFET as a function of the reciprocal of the temperature $\frac{1}{T}$ for drain voltages V_d of $-0.1\,\mathrm{V}$ and $-0.5\,\mathrm{V}$, allowing for an extraction of the activation energy E_a of the traps as the slope of the natural logarithm of the drain current $\ln(I_\mathrm{d})$ in the high temperature T regime. A freeze-out of phonons occurs at a temperature T of about $120\,\mathrm{K}$, corresponding to one fourth of the DEBYE temperature $T = \frac{\Theta_\mathrm{D}}{4}$ as indicated by a dotted vertical line.

activation energy E_a from both SRH and TAT to BTBT regime is reproduced only at a drain voltage V_d of $-0.1\,\mathrm{V}$ whereas at a drain voltage V_d of $-0.5\,\mathrm{V}$ the dependency of the

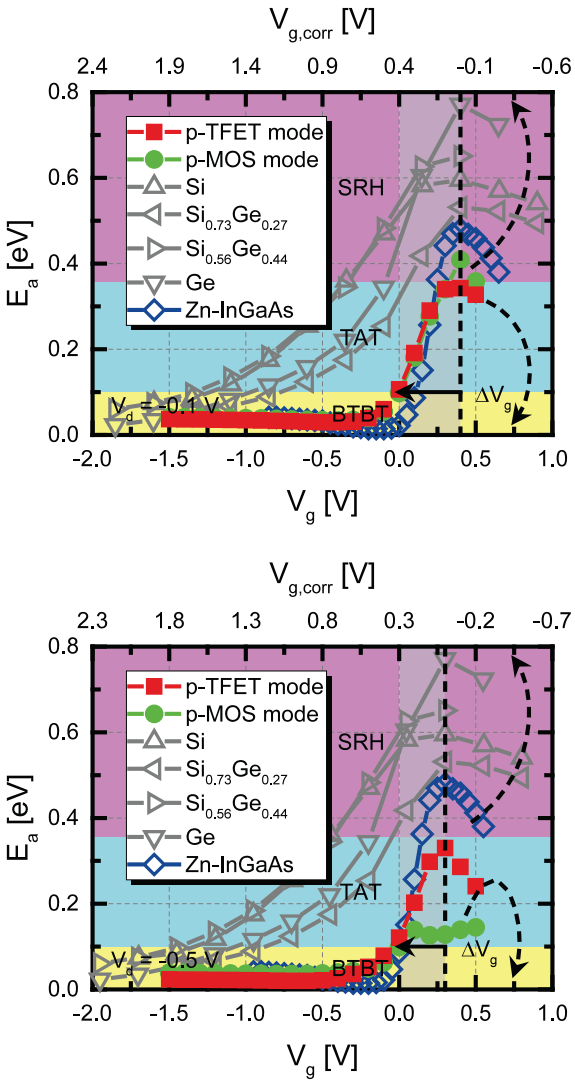


Figure 4.2.36: Activation energy E_a as a function of the gate voltage V_g for drain voltages V_d of $-0.1\,V$ and $-0.5\,V$. In case of biasing in p-TFET mode, a sharp transition of the activation energy E_a from both SRH and TAT to BTBT regime is realized independently of the applied drain voltage V_d within a small gate voltage window ΔV_g of less than $0.4\,V$. However, in case of biasing in p-MOS mode, that sharp transition of the activation energy E_a is reproduced only at a drain voltage V_d of $-0.1\,V$ whereas at a drain voltage V_d of $-0.5\,V$ the dependency of the activation energy E_a on the gate voltage V_g vanishes due to the (gated) tunnel diode biased in forward direction.

activation energy E_a on the gate voltage V_g vanishes, resulting in a nearly constant activation energy E_a at a low level of about 0.1 eV. For this particular case, the transistor is always on due to the (gated) tunnel diode biased in forward direction, enabling thermionic emission with the latter mainly driven by the drain voltage V_d, but not by the gate voltage V_g as expected in case of a (gated) tunnel diode. As a consequence, this vanishing dependency of the activation energy E_a on the gate voltage V_g in case of biasing in p-MOS mode coincides with the corresponding transfer characteristics at different temperatures T as visible from figure 4.2.37, revealing switching of the planar SiGe/Si heterostructure p-TFET only at a drain voltage V_d of -0.1 V whereas at a drain voltage V_d of -0.5 V the transistor exhibits no more switching. It is worth mentioning that this difference in the dependency of the activation energy E_a on the gate voltage V_g in case of biasing in both p-TFET mode and p-MOS mode once more highlights TFET operation of the planar SiGe/Si heterostructure p-TFET since MOSFET operation implies a reproduction of the dependency of the activation energy E_a on the gate voltage V_g when swapping source and drain but keeping the applied biases for drain voltage V_d and gate voltage V_g constant.

In summary, the planar SiGe/Si heterostructure p-TFET drastically benefits from the introduction of a selective and self-adjusted silicidation as well as a counter doped pocket at the source tunnel junction, enabling BTBT over a wide region of the gate voltage V_g with a diminished influence of SRH and TAT as derived from low temperature T measurements. In addition, this diminished influence of SRH and TAT becomes not only visible in the dependency of the activation energy E_a on the gate voltage V_g but also in the dependency of the corresponding output characteristics on the temperature T in case of biasing in p-MOS mode as presented in figure 4.2.38, being equivalent to a switching of the source tunnel junction of the planar SiGe/Si heterostructure p-TFET. A spreading of the output characteristics as a function of the temperature T is only revealed for contributions from SRH and TAT to charge transport whereas BTBT does not enable that pronounced dependency on the temperature T [42]. According to the extracted activation energies E_a as a function of the gate voltage V_g, BTBT in the planar SiGe/Si heterostructure p-TFET already sets in for gate voltages V_g below 0 V, suggesting a diminished influence of SRH and TAT not only at a high absolute gate voltage $|V_g|$ of 1.1 V but also at a low absolute gate voltage $|V_g|$ of only 0.1 V. Comparison of both output characteristics reveals a similar spreading of the drain current I_d as a function of the temperature T for both gate voltages V_g, thus confirming BTBT dominating over SRH and TAT in the planar SiGe/Si heterostructure p-TFET already at low absolute gate voltages $|V_g|$ in accordance with the extracted activation energies E_a.

4.2.4 Logic Applications

TFETs are a promising candidate for competing with MOSFETs in terms of low power electronics, but still lack in terms of logic applications. Subsequently, this chapter presents a first approach towards logic applications by means of p-logic. In contrast to CMOS-logic, p-logic only requires p-type transistors as one type of transistor. That way, a NAND gate is realized by connecting two planar SiGe/Si heterostructure p-TFETs in series and adding one pull-down resistor connected to ground serving as a voltage divider as sketched in figure 4.2.39. In this regard, a pull-down resistor is required in order to stabilize the logic signal

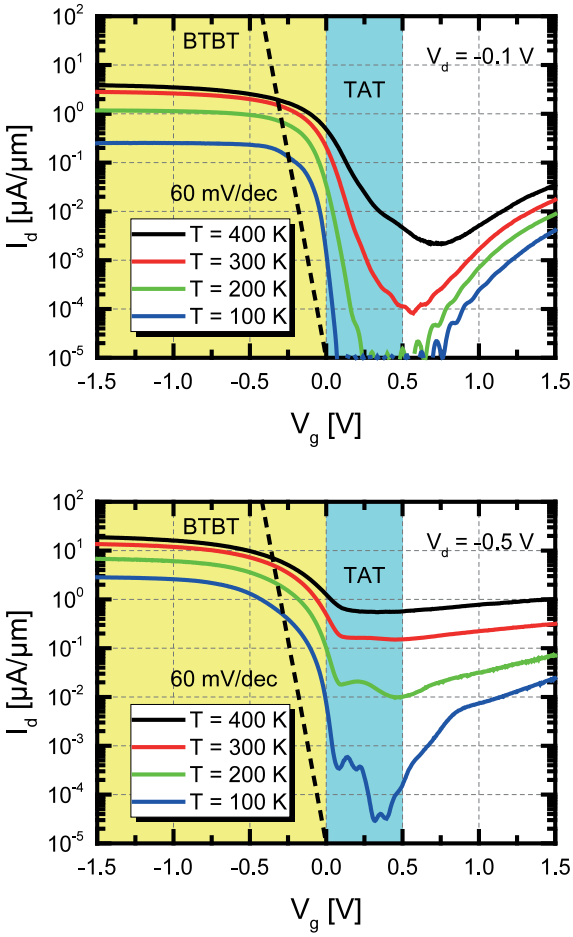


Figure 4.2.37: Measured transfer characteristics of the planar SiGe/Si heterostructure p-TFET at different temperatures T for drain voltages V_d of $-0.1\,\mathrm{V}$ and $-0.5\,\mathrm{V}$ in case of biasing in p-MOS mode, revealing switching of the planar SiGe/Si heterostructure p-TFET only at a drain voltage V_d of $-0.1\,\mathrm{V}$ whereas at a drain voltage V_d of $-0.5\,\mathrm{V}$ the transistor exhibits no more switching due to the (gated) tunnel diode biased in forward direction.

at a low logic level when no transistor is active and thus, to ensure definition of a valid logic level. In case of p-logic, this low logic level is determined by the supply voltage V_DD, thus enabling a logic 0, whereas a high logic level is defined through the ground potential, consequently realizing a logic 1 [91]. The corresponding logic table of a NAND gate is given in table 4.2.1.

Since the two planar SiGe/Si heterostructure p-TFETs and the pull-down resistor are not connected on chip-level but via coaxial cables and needles, large impedances and parasitic

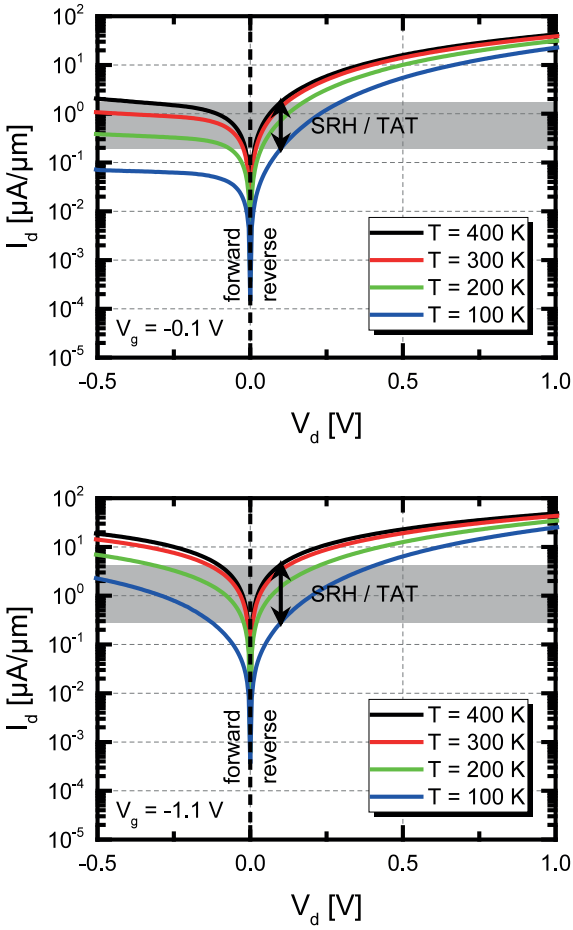


Figure 4.2.38: Measured output characteristics of the planar SiGe/Si heterostructure p-TFET at different temperatures T for gate voltages V_g of $-0.1\,V$ and $-1.1\,V$ in case of biasing in p-MOS mode, revealing a similar spreading of the drain current I_d as a function of the temperature T for both gate voltages V_g, thus confirming BTBT dominating over SRH and TAT in the planar SiGe/Si heterostructure p-TFET already at low absolute gate voltages $|V_g|$.

capacitances are to be expected, degrading the time response of the NAND gate. In this regard, maximum noise margin as a measure of the amount by which a signal exceeds the minimum threshold for proper operation is achieved by adjusting the pull-down resistor that way that switching at an input voltage V_{in} of $\frac{V_{DD}}{2}$ is enabled. The corresponding voltage transfer characteristics (VTC) with both gates swept in parallel in case of a pull-down resistor exhibiting a resistance R of $150\,k\Omega$ are shown in figure 4.2.40. For this particular case, switching of the output voltage V_{out} at an input voltage V_{in} of about $\frac{V_{DD}}{2}$ is realized, but

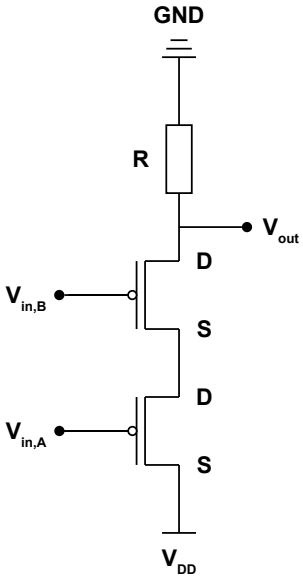


Figure 4.2.39: Schematic illustration of a NAND gate realized by p-logic.

A	B	$\overline{A \wedge B}$
0	0	1
0	1	1
1	0	1
1	1	0

Table 4.2.1: Logic table of a NAND gate with A and B denoting its inputs.

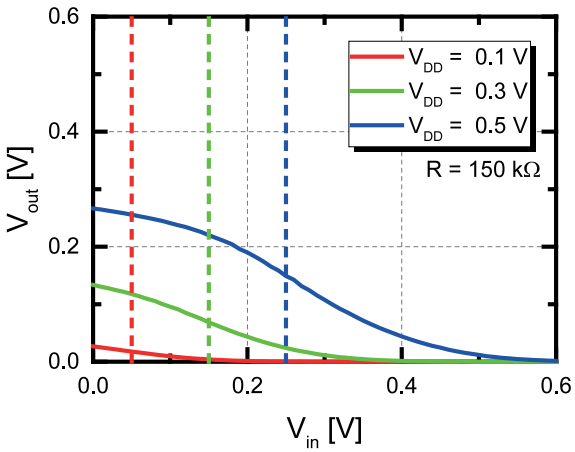


Figure 4.2.40: Measured VTC of a NAND gate with both gates swept in parallel in case of a pull-down resistor exhibiting a resistance R of 150 kΩ. For this particular case, switching of the output voltage V_{out} at an input voltage V_{in} of about $\frac{V_{\text{DD}}}{2}$ is realized, but inverting of the input voltage V_{in} is degraded due to a broad transition of the output voltage V_{out}.

inverting of the input voltage V_{in} is degraded due to a broad transition of the output voltage

V_{out}. In contrast, adjusting the pull-down resistor to a resistance R of 2 MΩ as depicted in figure 4.2.41 allows for inverting of the input voltage V_{in} to be nearly accomplished, but the transition of the output voltage V_{out} is shifted from $\frac{V_{DD}}{2}$ towards higher values, resulting in a degraded noise margin. In this regard, inverting of the input voltage V_{in} is indispensable in order to ensure definition of a valid logic level for proper NAND operation, thus yielding the resistance of the pull-down resistor to a value of 2 MΩ. The pulse length t_{pulse} of the gate pulse of one transistor is set to 2.5 ms with a repetition rate of 5 ms whereas the pulse length t_{pulse} of the gate pulse of the other transistor is set to 10 ms with a repetition rate of 20 ms. The resulting time response of the NAND gate is illustrated in figure 4.2.42, revealing p-logic operation by means of two planar SiGe/Si heterostructure p-TFETs connected in series. Even though pulse level and pulse relaxation of the output voltage V_{out} are degraded due to large impedances and parasitic capacitances within the measurement setup, the resulting time response of the NAND gate still allows for a proof of concept of logic applications down to ultra-low supply voltages V_{DD} of 0.1 V realized by means of planar SiGe/Si heterostructure p-TFETs.

4.3 Summary and Discussion

Planar SiGe/Si heterostructure p-TFETs were presented which benefit from a selective and self-adjusted silicidation in combination with a counter doped pocket at the source tunnel junction in order to enable line tunneling aligned with the gate electric field lines in an enlarged area directly underneath the gate. As a consequence, high on-currents I_{on} of 6.7 µA/µm at a supply voltage V_{DD} of 0.5 V could be achieved in parallel with an average

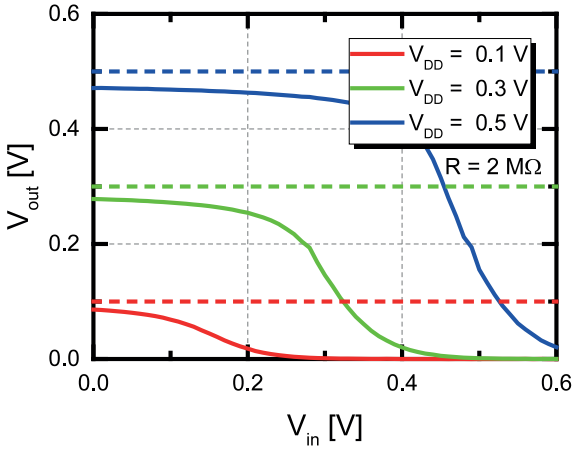


Figure 4.2.41: Measured VTC of a NAND gate with both gates swept in parallel in case of a pull-down resistor exhibiting a resistance R of 2 MΩ. For this particular case, inverting of the input voltage V_{in} is nearly accomplished, but the transition of the output voltage V_{out} is shifted from $\frac{V_{DD}}{2}$ towards higher values, resulting in a degraded noise margin.

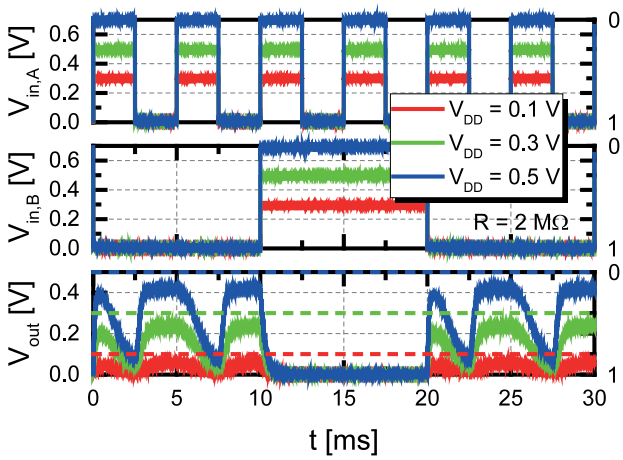


Figure 4.2.42: Measured time response of a NAND gate with both gates swept in parallel for a pull-down resistor exhibiting a resistance R of 2 MΩ, revealing p-logic operation by means of two planar SiGe/Si heterostructure p-TFETs connected in series. Only in case of both inputs providing a logic 1, a logic 0 at the output is achieved. In all other cases, a logic 1 at the output is stabilized, thus accomplishing a NAND gate.

subthreshold swing SS of about 80 mV/dec over four orders of magnitude of drain current I_d. Benchmarking the planar SiGe/Si heterostructure p-TFET with published state of the art TFETs in terms of on-current I_{on} and average subthreshold swing SS over four orders of magnitude of drain current I_d as presented in figure 4.3.1 highlights the planar SiGe/Si heterostructure p-TFET outperforming other devices due to line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT, especially at a supply voltage V_{DD} of 0.5 V as already indicated in chapter 4.2.3. TCAD simulations revealed the beneficial impact of both the selective and self-adjusted silicidation and the counter doped pocket at the source tunnel junction on the transfer characteristics of the planar SiGe/Si heterostructure p-TFET, demonstrating line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT. In this regard, both the line tunneling mechanism itself and the corresponding onset voltage V_{onset} exhibit a pronounced sensitivity on either the carrier concentration n_s of the source, the thickness t_{ox} of the gate oxide, the band gap E_g of the compressively, biaxially strained $Si_{0.45}Ge_{0.55}$ or its thickness t_{SiGe}, making a careful adjustment of these parameters indispensable when going for further optimization of the planar SiGe/Si heterostructure p-TFET. Pulsed measurements allowed for an identification of TAT being responsible for a degradation of the subthreshold swing SS. A sharp transition of the activation energy E_a from both SRH and TAT to BTBT regime within a small gate voltage window ΔV_g of less than 0.4 V was revealed by means of low temperature T measurements, faster than reported state of the art Si, SiGe or Ge TFETs, thus facilitating high on-currents I_{on} at a low supply voltage V_{DD} and a constant subthreshold swing SS in parallel. Finally, p-logic NAND operation could be demonstrated by means of two planar

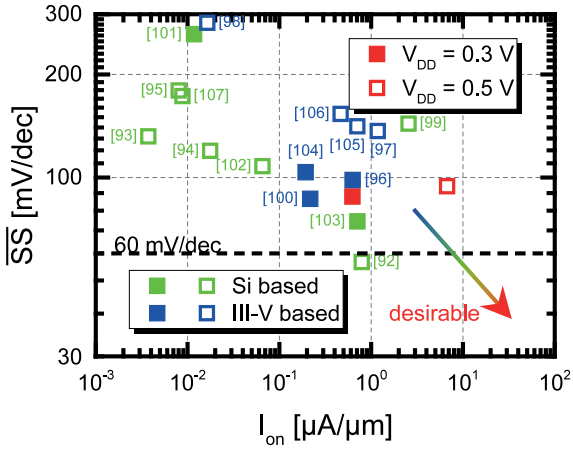


Figure 4.3.1: Benchmarking the planar SiGe/Si heterostructure p-TFET with published state of the art TFETs in terms of on-current I_{on} and average subthreshold swing SS over four orders of magnitude of drain current I_d [92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107]. In this regard, full symbols correspond to a supply voltage V_{DD} of 0.3 V, open symbols to a supply voltage V_{DD} of 0.5 V. The planar SiGe/Si heterostructure p-TFET outperforms other devices due to line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT, especially at a supply voltage V_{DD} of 0.5 V.

SiGe/Si heterostructure p-TFETs connected in series, highlighting their ability for both low power electronics and logic applications down to ultra-low supply voltages V_{DD} of 0.1 V.

5 Summary and Outlook

Within the framework of this thesis, two different proposals of a TFET device concept allowing for low power electronics have been investigated. As a first approach, a vertical SiGe/Si heterostructure n-TFET has been demonstrated which makes use of strained SiGe as a material with smaller band gap E_g at the source tunnel junction in order to increase the probability for BTBT while suppressing the ambipolar switching characteristics in parallel due to the use of Si with its higher band gap E_g as compared to SiGe at the drain tunnel junction, thus enabling a heterostructure device concept. As a second approach, a planar SiGe/Si heterostructure p-TFET was presented which not only makes use of strained SiGe as a material with smaller band gap E_g at the source tunnel junction, but also benefits from a selective and self-adjusted silicidation in combination with a counter doped pocket at the source tunnel junction in order to enable line tunneling aligned with the gate electric field lines in an enlarged area directly underneath the gate.

However, the vertical SiGe/Si heterostructure n-TFET suffered from a high subthreshold swing SS, a weak onset of the drain current I_d with a pronounced S-shape as well as no visible saturation of the drain current I_d due to a strong degradation of both tunnel junctions which may stem from poor electrostatic control caused by a defective interface between semiconductor and high-κ dielectrics as well as a pronounced surface roughness at the side walls of the fin, both favoring TAT. In addition, a pronounced ambipolar switching characteristics despite a heterostructure device concept became obvious, resulting from a much stronger contribution from TAT at the p^{++}-SiGe tunnel junction as compared to the n^{+}-Si tunnel junction, caused by the different chemical compositions of their respective interfacial oxide layers on the one hand and a much higher carrier concentration n within the SiGe layer on the other hand, scaling TAT. Thus, the vertical SiGe/Si heterostructure n-TFET may serve as a promising proof of concept for further integration of materials with small band gap E_g such as strained Ge or GeSn which allow for a direct band gap E_g transition into a three-dimensional device structure while maintaining a Si compatible technology, but needs careful optimization of its process flow in order to benefit from the versatility grading and in-situ doping enable. Besides an improved quality of the gate oxide in terms of both electrostatic control and defects favoring TAT, the problem of a pronounced surface roughness at the side walls of the fin which define the tunnel junctions of a vertical TFET has to be tackled consequently by means of wet chemical etching and/or oxidation in order to benefit from this promising TFET device concept.

The planar SiGe/Si heterostructure p-TFET in turn revealed a high on-current I_{on} of $6.7\,\mu A/\mu m$ at a supply voltage V_{DD} of $0.5\,V$ in parallel with an average subthreshold swing SS of about $80\,mV/dec$ over four orders of magnitude of drain current I_d. Benchmarking the planar SiGe/Si heterostructure p-TFET with published state of the art TFETs in terms of

on-current I_{on} and average subthreshold swing SS over four orders of magnitude of drain current I_d highlighted the planar SiGe/Si heterostructure p-TFET outperforming other devices due to line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT. Pulsed measurements allowed for an identification of TAT being responsible for a degradation of the subthreshold swing SS. A sharp transition of the activation energy E_a from both SRH and TAT to BTBT regime within a small gate voltage window ΔV_g of less than 0.4 V was revealed by means of low temperature T measurements, being much steeper as compared to state of the art Si, SiGe or Ge TFETs, thus facilitating high on-currents I_{on} at a low supply voltage V_{DD} and a constant subthreshold swing SS in parallel. Finally, p-logic NAND operation was demonstrated by means of two planar SiGe/Si heterostructure p-TFETs connected in series, highlighting their ability for both low power electronics and logic applications down to ultra-low supply voltages V_{DD} of 0.1 V.

However, in order to enable logic applications not by means of p-logic but by CMOS, both p-type and n-type configuration of the planar SiGe/Si heterostructure TFET are required on chip-level. In this regard, processing of planar SiGe/Si heterostructure n-TFETs can be realized without any need to change the process flow itself as described in chapter 4.1, just by interchanging the respective dopant types for implantation of source, counter doped pocket and drain respectively. In order to get an idea of how planar SiGe/Si heterostructure n-TFETs perform as compared to their p-type counterparts, TCAD simulations are considered once more. The simulated transfer characteristics of the planar SiGe/Si heterostructure n-TFET as depicted in figure 5.0.1 reveal a slightly higher subthreshold swing SS, but comparable on-current I_{on} with respect to the planar SiGe/Si heterostructure p-TFET. As a consequence, both the planar SiGe/Si heterostructure p- and n-TFET seem promising candidates for low power electronics. However, in terms of CMOS logic applications, TFETs exhibiting equal switching characteristics for p- and n-type configuration are indispensable,

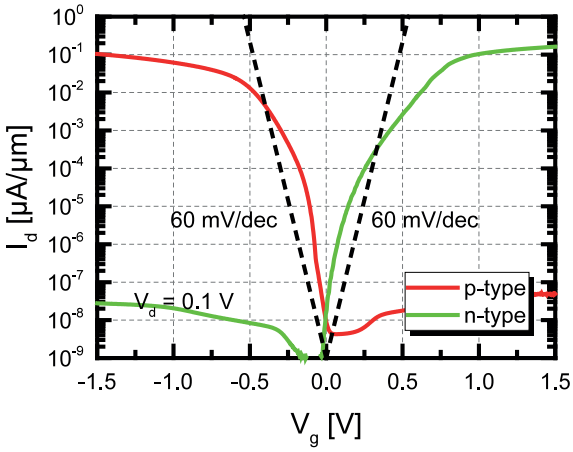


Figure 5.0.1: Simulated transfer characteristics of a planar SiGe/Si heterostructure n-TFET at a drain voltage V_d of 0.1 V, revealing a slightly higher subthreshold swing SS, but comparable on-current I_{on} with respect to the planar SiGe/Si heterostructure p-TFET.

bringing the onset voltage V_{onset} as a measure of the gate voltage V_{g} required in order to deplete parts of the source region directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines into focus of consideration. Realizing a planar SiGe/Si heterostructure n-TFET just by interchanging the respective dopant types for implantation of source, counter doped pocket and drain respectively comes along with a different onset voltage V_{onset} as compared to the planar SiGe/Si heterostructure p-TFET and thus, a threshold voltage shift ΔV_{t} in the resulting transfer characteristics which was accounted for in the TCAD simulations by adjusting the corresponding gate metal work function from 5.2 eV to 3.9 eV in case of the planar SiGe/Si heterostructure n-TFET in order to maintain switching at a gate voltage V_{g} of about 0 V. However, if an introduction of two different gate metals in order to ensure comparable switching characteristics for p- and n-type configuration should be avoided, making changes in the actual process flow inevitable, a careful adjustment of the carrier concentrations n_{s} and n_{p} of source and counter doped pocket respectively has to compensate for the different onset voltages V_{onset} of p- and n-type configuration. In addition, optimization of the carrier concentrations n_{s} and n_{p} of source and counter doped pocket respectively may account for the slightly higher subthreshold swing SS in case of the planar SiGe/Si heterostructure n-TFET, arising from the valence band ΔE_{v} offset between Si and strained SiGe as already discussed in chapter 2.4.1, favoring a p-type configuration. In this regard, the actual carrier concentrations n_{s} and n_{p} of source and counter doped pocket respectively scale with the temperature T with the latter defining diffusion and thermal activation of charge carriers. As a consequence, not only the carrier concentrations n_{s} and n_{p} of source and counter doped pocket respectively but also the extent of the counter doped pocket in a region directly underneath the gate are determined by the temperature T. However, the upper limit of the temperature T is given by the thermal budget of growth in order to sustain the compressive, biaxial strain ε within the SiGe layer as already discussed in chapter 4.1, favoring BTBT due to a further reduced band gap E_{g} as compared to relaxed SiGe. Thus, a trade-off between the actual carrier concentrations n_{s} and n_{p} of source and counter doped pocket respectively and the thermal budget of growth is required. In this regard, the limitation due to the thermal budget of growth may be tackled by in-situ doping of source and counter doped pocket, allowing for an optimized device concept which will be discussed in detail in chapter 5.1.

5.1 Design Optimizations

The planar SiGe/Si heterostructure p-TFET has been demonstrated as a promising concept for both low power electronics and logic applications down to ultra-low supply voltages V_{DD} of 0.1 V, but still lacks in terms of subthreshold swing SS below 60 mV/dec due to contributions from TAT, diminishing the influence of BTBT. Thus, a TFET device concept is required which enables a reduced defect density in order to suppress TAT on the one hand and allows for a variable adjustment of the carrier concentrations n_{s} and n_{p} of source and counter doped pocket respectively in order to realize p- and n-type configurations equally switching on the other hand. In this regard, in-situ doping during growth may enable a reduced defect density as compared to common ion implantation as already discussed in chapter 3.1 whereas selective growth enables the definition of a specific region of the TFET, i.e. the source tunnel

junction or the counter doped pocket, and thus, allows for an alignment of both regions with respect to each other. Subsequently, an optimized device concept is suggested, combining both beneficial aspects of in-situ doping and selective growth as schematically illustrated in figure 5.1.1 in case of p-type configuration, but being applicable to n-type configuration without any restrictions. This optimized, planar SiGe/Si heterostructure p-TFET is realized by growing a compressively, strained p^+-SiGe layer on top of a SOI substrate, acting as both a counter doped pocket and the drain. A thin Si cap on top of the compressively, strained p^+-SiGe layer is desirable in order to avoid the formation of a thick and defective interfacial oxide layer at the interface between SiGe and high-κ dielectrics as already discussed in chapter 3.2. The source tunnel junction is realized by selective etching of the intrinsic Si layer on the source side of the device and subsequent selective growth of n^{++}-Si into the etched gap. In this regard, the use of aqueous tetramethyl ammonium hydroxide (TMAH) allows for selective etching of Si with respect to SiGe [108]. Gate stack cleaning and deposition are performed analogously to the original, planar SiGe/Si heterostructure p-TFET as described in chapter 4.1. Thus, the resulting device is changed from a gated p-i-n structure to a gated p-n diode operated in reverse direction, enabling an inherent suppression of the ambipolar switching characteristics. However, in order to ensure a proper off-state of the suggested device, good electrostatic control is indispensable. A similar approach is sketched in [109] by means of semiclassical device simulations including quantum corrections, revealing line tunneling aligned with the gate electric field lines as well, but requiring a much more complex process flow due to an embedding of the source region into a quantum well. The combination of in-situ doping and selective growth allows for box-like, sharp doping profiles, resulting in an abrupt source tunnel junction, being beneficial for BTBT due to a decreased tunneling length. As one further advantage over the original, planar SiGe/Si heterostructure p-TFET, an alignment of source and counter doped pocket with respect to each other is no longer necessary since the counter doped pocket is stretched over the whole device, thus defining the drain contact in parallel. However, in order to exclude parasitic contributions from point tunneling in this TFET device concept and allow for solely line tunneling aligned with the gate electric field lines, source and gate have to be aligned with respect to each other, thus

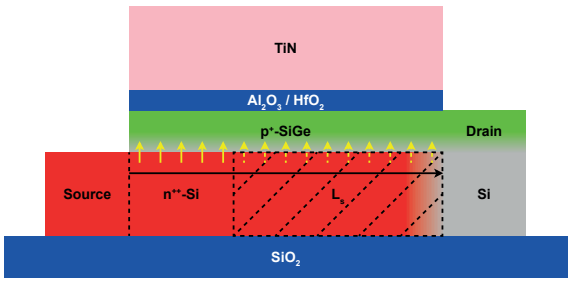


Figure 5.1.1: Schematic illustration of an optimized, planar SiGe/Si heterostructure p-TFET, enabling scaling of line tunneling aligned with the gate electric field lines in an enlarged area directly underneath the gate by varying the length L_s of the source. In order to exclude parasitic contributions from point tunneling in this TFET device concept, source and gate have to be aligned with respect to each other, thus requiring controllable etching of the intrinsic Si layer.

requiring controllable etching of the intrinsic Si layer. The resulting on-current I_{on} of the optimized, planar SiGe/Si heterostructure p-TFET can be linearly scaled by adjusting the length L_s of the source due to line tunneling aligned with the gate electric field lines being the dominant contribution to BTBT in this TFET device concept. TCAD simulations reveal this scaling of the on-current I_{on} by varying the length L_s of the source between 50 nm, 100 nm and 200 nm as visible from the resulting transfer characteristics illustrated in figure 5.1.2. The corresponding carrier concentration n_{s} of the source was set to $1 \times 10^{20}\,\mathrm{cm}^{-3}$ with respect to the experimental reference obtained from ECV measurements as discussed in chapter 4.1 whereas the carrier concentration n_{p} of the counter doped pocket was assumed as $1 \times 10^{18}\,\mathrm{cm}^{-3}$. As further parameters for the TCAD simulations, the EOT was assumed as 1.2 nm in accordance with the EOT extracted from CV measurements on MOS capacitors as discussed in chapter 2.4.2 and the gate length L_{g} was set to 200 nm. The thickness t_{SiGe} of the p^+-SiGe layer was chosen as 5 nm in order to avoid either degraded electrostatic control or arising quantization effects as indicated in chapter 4.2. Subsequently, the gate metal work function was adjusted to match the onset of the optimized, planar SiGe/Si heterostructure p-TFET at a gate voltage V_{g} of about 0 V, yielding a gate metal work function of 5.2 eV. As expected, the gated p-n diode defining the optimized, planar SiGe/Si heterostructure p-TFET enables an inherent suppression of the ambipolar switching characteristics, being indispensable in terms of CMOS applications. In addition, due to box-like, sharp doping profiles, resulting in an abrupt source tunnel junction, line tunneling aligned with the gate electric field lines is much more favorable as compared to point tunneling and thus, dominates BTBT in the optimized, planar SiGe/Si heterostructure p-TFET. The more the length L_s of the source is increased, the less parasitic contributions from point tunneling at the interface

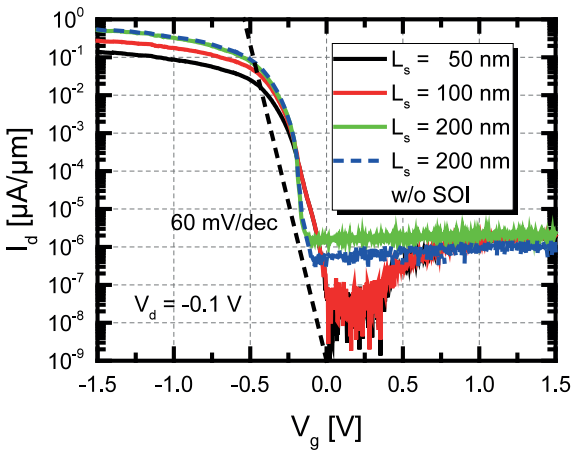


Figure 5.1.2: Simulated transfer characteristics of an optimized, planar SiGe/Si heterostructure p-TFET at a drain voltage V_{d} of -0.1 V, revealing a linear scaling of the on-current I_{on} when varying the length L_s of the source between 50 nm, 100 nm and 200 nm. Once the length L_{s} of the source equals the gate length L_{g} at a value of 200 nm, point tunneling vanishes, allowing for solely line tunneling aligned with the gate electric field lines and thus, enabling a drastically reduced subthreshold swing *SS*.

between p^+-SiGe and intrinsic Si come into play as visible from the contour plots of the simulated hBTB generation rates arising in the optimized, planar SiGe/Si heterostructure p-TFET presented in figure 5.1.3. Once the length L_s of the source equals the gate length L_g at a value of 200 nm, point tunneling vanishes, allowing for solely line tunneling aligned with the gate electric field lines. For this particular case, the subthreshold swing SS is drastically reduced with its minimum value as low as 20 mV/dec as visible from the corresponding transfer characteristics shown in figure 5.1.2. This drastically reduced subthreshold swing SS comes along with a later onset of the transfer characteristics which is related to the onset voltage V_{onset} required in order to deplete parts of the source region directly underneath the gate as a precondition for line tunneling aligned with the gate electric field lines as already discussed in chapter 2.3.5. Thus, an optimized, planar SiGe/Si heterostructure p-TFET is enabled which allows for solely line tunneling aligned with the gate electric field lines, being highly desired in terms of circuit design due to its capability of a constant subthreshold swing SS as already discussed in chapter 4.2.1. In addition, the off-current I_{off} of the optimized, planar SiGe/Si heterostructure p-TFET can be further lowered by a complete removal of the intrinsic Si layer before subsequent selective growth of n^{++}-Si source into the etched gap as also visible from the simulated transfer characteristics shown in figure 5.1.2, resulting in an overall improved ratio of on- to off-current $\frac{I_{on}}{I_{off}}$.

It is worth mentioning that by means of selective growth and in-situ doping, this TFET device concept is no longer limited to a planar, single-gate geometry and thus, allows for the introduction of a NW source and a core-shell counter doped pocket, enabling ideal electrostatic control and thus, further boosting BTBT. If applied to a heterostructure of strained Ge/GeSn, a direct band gap E_g transition is additionally enabled, combining the concept of a GAA structure with a direct band gap E_g transition and a counter doped pocket at the source tunnel junction in order to enable line tunneling aligned with the gate electric field lines in an enlarged area directly underneath the gate in one single device.

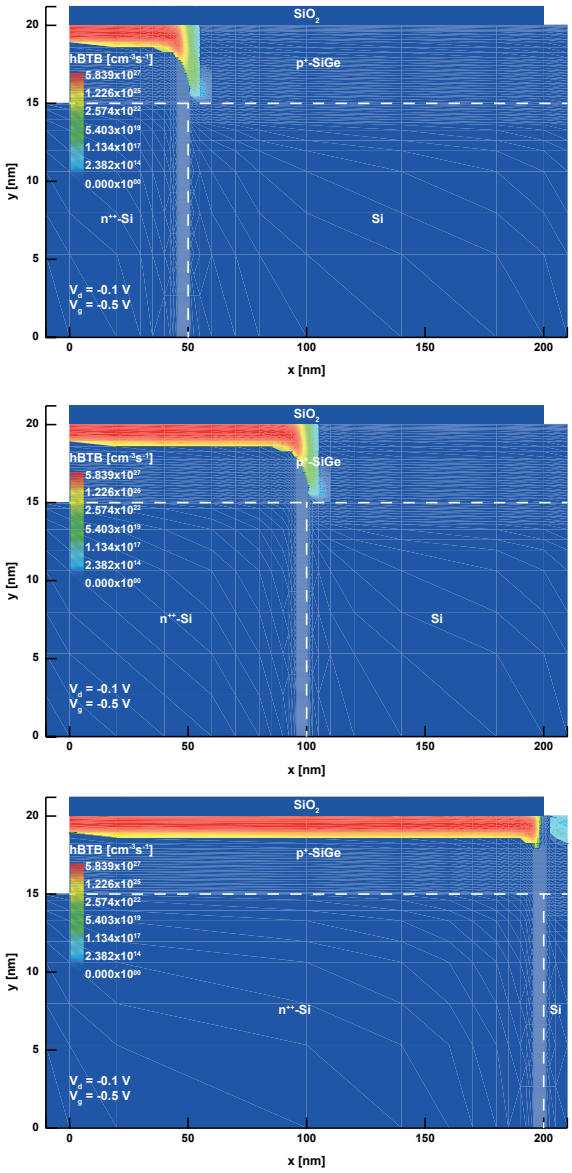


Figure 5.1.3: Contour plots of the simulated hBTB generation rates arising in the optimized, planar SiGe/Si heterostructure p-TFET when varying the length L_s of the source between 50 nm, 100 nm and 200 nm at a drain voltage V_d of -0.1 V and at a gate voltage V_g of -0.5 V, revealing reduced parasitic contributions from point tunneling at the interface between p^+-SiGe and intrinsic Si for increasing lengths L_s of the source.

Bibliography

[1] G. E. Moore. "Cramming More Components Onto Integrated Circuits". In: *Proceedings of the IEEE* 86.1 (Jan. 1998), pp. 82–85. ISSN: 0018-9219. DOI: 10.1109/JPROC.1998.658762. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=658762.

[2] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. mayz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki. "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging". In: *2007 IEEE International Electron Devices Meeting*. IEEE, 2007, pp. 247–250. ISBN: 978-1-4244-1507-6. DOI: 10.1109/IEDM.2007.4418914. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4418914.

[3] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry. "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors". In: *2012 Symposium on VLSI Technology (VLSIT)*. IEEE, June 2012, pp. 131–132. ISBN: 978-1-4673-0847-2. DOI: 10.1109/VLSIT.2012.6242496. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6242496.

[4] Intel Inc. *Intel's (INTC) CEO Brian Krzanich on Q2 2015 Results - Earnings Call Transcript*. http://seekingalpha.com/article/3329035-intels-intc-ceo-brian-krzanich-on-q2-2015-results-earnings-call-transcript?page=2. July 2015.

[5] IBM Inc. *IBM Research Alliance Produces Industry's First 7nm Node Test Chips*. http://www-03.ibm.com/press/us/en/pressrelease/47301.wss. July 2015.

[6] R. Waser. *Nanoelectronics and information technology : advanced electronic materials and novel devices*. English. Weinheim: Wiley-VCH, 2003. ISBN: 3527403639 9783527403639.

[7] J.-A. Carballo, W.-T. J. Chan, P. A. Gargini, A. B. Kahng, and S. Nath. "ITRS 2.0: Toward a re-framing of the Semiconductor Technology Roadmap". In: *2014 IEEE 32nd International Conference on Computer Design (ICCD)*. IEEE, Oct. 2014, pp. 139–146. ISBN: 978-1-4799-6492-5. DOI: 10.1109/ICCD.2014.6974673. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6974673.

[8] J. Zhang, M. De Marchi, P.-E. Gaillardon, and G. De Micheli. "A Schottky-barrier silicon FinFET with 6.0 mV/dec Subthreshold Slope over 5 decades of current". In: *2014 IEEE International Electron Devices Meeting*. IEEE, Dec. 2014, pp. 13.4.1–13.4.4. ISBN: 978-1-4799-8001-7. DOI: 10.1109/IEDM.2014.7047045. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7047045.

[9] C. Shen, J.-Q. Lin, E.-H. Toh, K.-F. Chang, P. Bai, C.-H. Heng, G. S. Samudra, and Y.-C. Yeo. "On the Performance Limit of Impact-Ionization Transistors". In: *2007 IEEE International Electron Devices Meeting*. IEEE, 2007, pp. 117–120. ISBN: 978-1-4244-1507-6. DOI: 10.1109/IEDM.2007.4418878. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4418878.

[10] L. Esaki. "New Phenomenon in Narrow Germanium p-n Junctions". In: *Physical Review* 109.2 (Jan. 1958), pp. 603–604. ISSN: 0031-899X. DOI: 10.1103/PhysRev.109.603. URL: http://link.aps.org/doi/10.1103/PhysRev.109.603.

[11] S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee. "A new three-terminal tunnel device". In: *IEEE Electron Device Letters* 8.8 (Aug. 1987), pp. 347–349. ISSN: 0741-3106. DOI: 10.1109/EDL.1987.26655. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1487205.

[12] E. Takeda, H. Matsuoka, Y. Igura, and S. Asai. "A band to band tunneling MOS device (B^2T-MOSFET) - A kind of 'Si quantum device'". In: *Technical Digest., International Electron Devices Meeting*. IEEE, 1988, pp. 402–405. DOI: 10.1109/IEDM.1988.32841. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=32841.

[13] J. Appenzeller, Y.-M. Lin, J. Knoch, Z. Chen, and P. Avouris. "Comparing Carbon Nanotube Transistors - The Ideal Choice: A Novel Tunneling Device Design". In: *IEEE Transactions on Electron Devices* 52.12 (Dec. 2005), pp. 2568–2576. ISSN: 0018-9383. DOI: 10.1109/TED.2005.859654. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1546317.

[14] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu. "Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec". In: *IEEE Electron Device Letters* 28.8 (Aug. 2007), pp. 743–745. ISSN: 0741-3106. DOI: 10.1109/LED.2007.901273. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4278352.

[15] A. M. Ionescu and H. Riel. "Tunnel field-effect transistors as energy-efficient electronic switches". In: *Nature* 479.7373 (Nov. 2011), pp. 329–337. ISSN: 0028-0836. DOI: 10.1038/nature10679. URL: http://www.nature.com/doifinder/10.1038/nature10679.

[16] Y. Yang, S. Su, P. Guo, W. Wang, X. Gong, L. Wang, K. L. Low, G. Zhang, C. Xue, B. Cheng, G. Han, and Y.-C. Yeo. "Towards direct band-to-band tunneling in P-channel tunneling field effect transistor (TFET): Technology enablement by Germanium-tin (GeSn)". In: *2012 International Electron Devices Meeting*. IEEE, Dec. 2012, pp. 16.3.1–16.3.4. ISBN: 978-1-4673-4871-3. DOI: 10.1109/IEDM.2012.6479053. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6479053.

[17] Y. Yang, G. Han, P. Guo, W. Wang, X. Gong, L. Wang, K. L. Low, and Y.-C. Yeo. "Germanium-Tin P-Channel Tunneling Field-Effect Transistor: Device Design and Technology Demonstration". In: *IEEE Transactions on Electron Devices* 60.12 (Dec. 2013), pp. 4048–4056. ISSN: 0018-9383. DOI: 10.1109/TED.2013.2287031. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6656859.

[18] S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chiussi, J. M. Hartmann, H. Sigg, J. Faist, D. Buca, and D. Grützmacher. "Lasing in direct-bandgap GeSn alloy grown on Si". In: *Nature Photonics* 9.2 (Jan. 2015), pp. 88–92. ISSN: 1749-4885. DOI: 10.1038/nphoton.2014.321. URL: http://www.nature.com/doifinder/10.1038/nphoton.2014.321.

[19] U. E. Avci, R. Rios, K. Kuhn, and I. A. Young. "Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic". In: *2011 Symposium on VLSI Technology - Digest of Technical Papers* (2011), pp. 124–125. ISSN: 0743-1562.

[20] U. E. Avci, D. H. Morris, and I. A. Young. "Tunnel Field-Effect Transistors: Prospects and Challenges". In: *IEEE Journal of the Electron Devices Society* 3.3 (May 2015), pp. 88–95. ISSN: 2168-6734. DOI: 10.1109/JEDS.2015.2390591. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7006647.

[21] B. Senale-Rodriguez, Y. Lu, P. Fay, D. Jena, A. Seabaugh, H. G. Xing, L. Barboni, and F. Silveira. "Perspectives of TFETs for low power analog ICs". In: *2012 IEEE Subthreshold Microelectronics Conference (SubVT)*. IEEE, Oct. 2012, pp. 1–3. ISBN: 978-1-4673-1587-6. DOI: 10.1109/SubVT.2012.6404307. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6404307.

[22] D. Sarkar and K. Banerjee. "Proposal for tunnel-field-effect-transistor as ultra-sensitive and label-free biosensors". In: *Applied Physics Letters* 100.14 (2012), p. 143108. ISSN: 00036951. DOI: 10.1063/1.3698093. URL: http://scitation.aip.org/content/aip/journal/apl/100/14/10.1063/1.3698093.

[23] A. R. Trivedi, S. Carlo, and S. Mukhopadhyay. "Exploring tunnel-FET for ultra low power analog applications". In: *Proceedings of the 50th Annual Design Automation Conference on - DAC '13*. New York, NY: ACM Press, 2013, p. 1. ISBN: 9781450320719. DOI: 10.1145/2463209.2488868. URL: http://dl.acm.org/citation.cfm?doid=2463209.2488868.

[24] A. R. Trivedi, M. F. Amir, and S. Mukhopadhyay. "Ultra-low power electronics with Si/Ge tunnel FET". In: *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2014*. Dresden: IEEE Conference Publications, 2014, pp. 1–6. ISBN:

9783981537024. DOI: 10.7873/DATE.2014.244. URL: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6800445.

[25] P. R. Panda, B. V. N. Silpa, A. Shrivastava, and K. Gummidipudi. *Power-efficient System Design*. Boston, MA: Springer US, 2010. ISBN: 978-1-4419-6387-1. DOI: 10.1007/978-1-4419-6388-8. URL: http://link.springer.com/10.1007/978-1-4419-6388-8.

[26] S. Datta. "Exclusion principle and the Landauer-Büttiker formalism". In: *Physical Review B* 45.3 (Jan. 1992), pp. 1347–1362. ISSN: 0163-1829. DOI: 10.1103/PhysRevB.45.1347. URL: http://link.aps.org/doi/10.1103/PhysRevB.45.1347.

[27] S. M. Sze and K. K. Ng. *Physics of Semiconductor Devices*. Hoboken, NJ: John Wiley & Sons, Inc., Oct. 2006. ISBN: 9780470068328. DOI: 10.1002/0470068329. URL: http://doi.wiley.com/10.1002/0470068329.

[28] E. O. Kane. "Theory of Tunneling". In: *Journal of Applied Physics* 32.1 (1961), p. 83. ISSN: 00218979. DOI: 10.1063/1.1735965. URL: http://scitation.aip.org/content/aip/journal/jap/32/1/10.1063/1.1735965.

[29] E. O. Kane. "Zener tunneling in semiconductors". In: *Journal of Physics and Chemistry of Solids* 12.2 (Jan. 1960), pp. 181–188. ISSN: 00223697. DOI: 10.1016/0022-3697(60)90035-4. URL: http://linkinghub.elsevier.com/retrieve/pii/0022369760900354.

[30] *Sentaurus Device User Guide*. K-2015.06. Synopsys Inc. June 2015.

[31] A. G. Chynoweth, R. A. Logan, and D. E. Thomas. "Phonon-Assisted Tunneling in Silicon and Germanium Esaki Junctions". In: *Physical Review* 125.3 (Feb. 1962), pp. 877–881. ISSN: 0031-899X. DOI: 10.1103/PhysRev.125.877. URL: http://link.aps.org/doi/10.1103/PhysRev.125.877.

[32] A. Vandooren, D. Leonelli, R. Rooyackers, A. Hikavyy, K. Devriendt, M. Demand, R. Loo, G. Groeseneken, and C. Huyghebaert. "Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs". In: *Solid-State Electronics* 83 (May 2013), pp. 50–55. ISSN: 00381101. DOI: 10.1016/j.sse.2013.01.026. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110113000397.

[33] W. Shockley and W. T. Read. "Statistics of the Recombinations of Holes and Electrons". In: *Physical Review* 87.5 (Sept. 1952), pp. 835–842. ISSN: 0031-899X. DOI: 10.1103/PhysRev.87.835. URL: http://link.aps.org/doi/10.1103/PhysRev.87.835.

[34] C.-T. Sah and W. Shockley. "Electron-Hole Recombination Statistics in Semiconductors through Flaws with Many Charge Conditions". In: *Physical Review* 109.4 (Feb. 1958), pp. 1103–1115. ISSN: 0031-899X. DOI: 10.1103/PhysRev.109.1103. URL: http://link.aps.org/doi/10.1103/PhysRev.109.1103.

[35] R. N. Hall and J. H. Racette. "Diffusion and Solubility of Copper in Extrinsic and Intrinsic Germanium, Silicon, and Gallium Arsenide". In: *Journal of Applied Physics* 35.2 (1964), p. 379. ISSN: 00218979. DOI: 10.1063/1.1713322. URL: http://scitation.aip.org/content/aip/journal/jap/35/2/10.1063/1.1713322.

[36] W. G. Vandenberghe, A. S. Verhulst, G. Groeseneken, B. Soree, and W. Magnus. "Analytical model for point and line tunneling in a tunnel field-effect transistor". In: *2008 International Conference on Simulation of Semiconductor Processes and Devices*. Vol. i. 3. IEEE, Sept. 2008, pp. 137–140. ISBN: 978-1-4244-1753-7. DOI: 10.1109/SISPAD.2008.4648256. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4648256.

[37] W. G. Vandenberghe, A. S. Verhulst, G. Groeseneken, B. Soree, and W. Magnus. "Analytical model for a tunnel field-effect transistor". In: *MELECON 2008 - The 14th IEEE Mediterranean Electrotechnical Conference*. IEEE, May 2008, pp. 923–928. ISBN: 978-1-4244-1632-5. DOI: 10.1109/MELCON.2008.4618555. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4618555.

[38] J. P. Dismukes, L. Ekstrom, and R. J. Paff. "Lattice Parameter and Density in Germanium-Silicon Alloys". In: *The Journal of Physical Chemistry* 68.10 (Oct. 1964), pp. 3021–3027. ISSN: 0022-3654. DOI: 10.1021/j100792a049. URL: http://pubs.acs.org/doi/abs/10.1021/j100792a049.

[39] R. Braunstein, A. R. Moore, and F. Herman. "Intrinsic Optical Absorption in Germanium-Silicon Alloys". In: *Physical Review* 109.3 (Feb. 1958), pp. 695–710. ISSN: 0031-899X. DOI: 10.1103/PhysRev.109.695. URL: http://link.aps.org/doi/10.1103/PhysRev.109.695.

[40] S. Sant, S. Lodha, U. Ganguly, S. Mahapatra, F. O. Heinz, L. Smith, V. Moroz, and S. Ganguly. "Band gap bowing and band offsets in relaxed and strained $Si_{1-x}Ge_x$ alloys by employing a new nonlinear interpolation scheme". In: *Journal of Applied Physics* 113.3 (2013), p. 033708. ISSN: 00218979. DOI: 10.1063/1.4775839. URL: http://scitation.aip.org/content/aip/journal/jap/113/3/10.1063/1.4775839.

[41] Y. Shiraki and N. Usami. *Silicon-germanium (SiGe) nanostructures production, properties and applications in electronics*. English. Philadelphia, PA, 2011. URL: http://www.woodheadpublishingonline.com/openurl.asp?genre=book%5C&isbn=978-1-84569-689-4.

[42] K.-H. Kao, A. S. Verhulst, R. Rooyackers, B. Douhard, J. Delmotte, H. Bender, O. Richard, W. Vandervorst, E. Simoen, A. Hikavyy, R. Loo, K. Arstila, N. Collaert, A. Thean, M. M. Heyns, and K. De Meyer. "Compressively strained SiGe band-to-band tunneling model calibration based on p-i-n diodes and prospect of strained SiGe tunneling field-effect transistors". In: *Journal of Applied Physics* 116.21 (Dec. 2014), p. 214506. ISSN: 0021-8979. DOI: 10.1063/1.4903288. URL: http://scitation.aip.org/content/aip/journal/jap/116/21/10.1063/1.4903288.

[43] M. V. Fischetti and S. E. Laux. "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys". In: *Journal of Applied Physics* 80.4 (1996), p. 2234. ISSN: 00218979. DOI: 10.1063/1.363052. URL: http://link.aip.org/link/JAPIAU/v80/i4/p2234/s1%5C&Agg=doi%20http://scitation.aip.org/content/aip/journal/jap/80/4/10.1063/1.363052.

[44] R.-H. Yan, A. Ourmazd, and K. F. Lee. "Scaling the Si MOSFET: from bulk to SOI to bulk". In: *IEEE Transactions on Electron Devices* 39.7 (July 1992), pp. 1704–1710. ISSN: 00189383. DOI: 10.1109/16.141237. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=141237.

[45] I. Kim, J. Koo, J. Lee, and H. Jeon. "A Comparison of Al_2O_3/HfO_2 and Al_2O_3/ZrO_2 Bilayers Deposited by the Atomic Layer Deposition Method for Potential Gate Dielectric Applications". In: *Japanese Journal of Applied Physics* 45.2A (Feb. 2006), pp. 919–925. ISSN: 0021-4922. DOI: 10.1143/JJAP.45.919. URL: http://stacks.iop.org/1347-4065/45/919.

[46] R. Katamreddy, R. Inman, G. Jursich, A. Soulet, and C. Takoudis. "Controlling interfacial reactions between HfO_2 and Si using ultrathin Al_2O_3 diffusion barrier layer". In: *Applied Physics Letters* 89.26 (2006), p. 262906. ISSN: 00036951. DOI: 10.1063/1.2425023. URL: http://scitation.aip.org/content/aip/journal/apl/89/26/10.1063/1.2425023.

[47] D. K. Schroder. *Semiconductor Material and Device Characterization*. Hoboken, NJ: John Wiley & Sons, Inc., Oct. 2005. ISBN: 9780471749097. DOI: 10.1002/0471749095. URL: http://doi.wiley.com/10.1002/0471749095.

[48] E. H. Nicollian and J. R. Brews. *MOS (metal oxide semiconductor) physics and technology*. English. New York, NY: Wiley, 1982. ISBN: 0471085006 9780471085003.

[49] S. Guha and V. Narayanan. "High-κ/Metal Gate Science and Technology". In: *Annual Review of Materials Research* 39.1 (Aug. 2009), pp. 181–202. ISSN: 1531-7331. DOI: 10.1146/annurev-matsci-082908-145320. URL: http://www.annualreviews.org/doi/abs/10.1146/annurev-matsci-082908-145320.

[50] S. Wirths, D. Buca, A. T. Tiedemann, P. Bernardy, B. Holländer, T. Stoica, G. Mussler, U. Breuer, and S. Mantl. "Low temperature RPCVD epitaxial growth of $Si_{1-x}Ge_x$ using Si_2H_6 and Ge_2H_6". In: *Solid-State Electronics* 83 (May 2013), pp. 2–9. ISSN: 00381101. DOI: 10.1016/j.sse.2013.01.032. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110113000452.

[51] A. Abbadie, J. M. Hartmann, C. Di Nardo, T. Billon, Y. Campidelli, and P. Besson. "An efficient wet-cleaning of SiGe virtual substrates and of thick, pure Ge layers on Si(001) after a chemical mechanical planarization step". In: *Microelectronic Engineering* 83.10 (Oct. 2006), pp. 1986–1993. ISSN: 01679317. DOI: 10.1016/j.mee.2006.02.018. URL: http://linkinghub.elsevier.com/retrieve/pii/S0167931706003145.

[52] J.-P. Colinge. "Novel gate concepts for MOS devices". In: *Proceedings of the 30th European Solid-State Circuits Conference (IEEE Cat. No.04EX850)*. IEEE, pp. 45–49. ISBN: 0-7803-8478-4. DOI: 10.1109/ESSDER.2004.1356484. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1356484.

[53] C.-W. Lee, S.-R.-N. Yun, C.-G. Yu, J.-T. Park, and J.-P. Colinge. "Device design guidelines for nano-scale MuGFETs". In: *Solid-State Electronics* 51.3 (Mar. 2007), pp. 505–510. ISSN: 00381101. DOI: 10.1016/j.sse.2006.11.013. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110106003947.

[54] M. M. Rieger and P. Vogl. "Electronic-band parameters in strained $Si_{1-x}Ge_x$ alloys on $Si_{1-y}Ge_y$ substrates". In: *Physical Review B* 48.19 (Nov. 1993), pp. 14276–14287. ISSN: 0163-1829. DOI: 10.1103/PhysRevB.48.14276. URL: http://link.aps.org/doi/10.1103/PhysRevB.48.14276.

[55] C.-H. Shih and N. D. Chien. "Sub-10-nm Tunnel Field-Effect Transistor With Graded Si/Ge Heterojunction". In: *IEEE Electron Device Letters* 32.11 (Nov. 2011), pp. 1498–1500. ISSN: 0741-3106. DOI: 10.1109/LED.2011.2164512. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6029285.

[56] C.-H. Shih and N. D. Chien. "Physical operation and device design of short-channel tunnel field-effect transistors with graded silicon-germanium heterojunctions". In: *Journal of Applied Physics* 113.13 (2013), p. 134507. ISSN: 00218979. DOI: 10.1063/1.4795777. URL: http://scitation.aip.org/content/aip/journal/jap/113/13/10.1063/1.4795777.

[57] *Model 4200-SCS Semiconductor Characterization System User's Manual*. Rev. E. Keithley Instruments Inc. May 2010.

[58] L. De Michielis, L. Lattanzio, and A. M. Ionescu. "Understanding the Superlinear Onset of Tunnel-FET Output Characteristic". In: *IEEE Electron Device Letters* 33.11 (Nov. 2012), pp. 1523–1525. ISSN: 0741-3106. DOI: 10.1109/LED.2012.2212175. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6303831.

[59] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani. "Drain-conductance optimization in nanowire TFETs by means of a physics-based analytical model". In: *Solid-State Electronics* 84 (June 2013), pp. 96–102. ISSN: 00381101. DOI: 10.1016/j.sse.2013.02.012. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110113000695.

[60] A. Abbadie, J. M. Hartmann, P. Besson, D. Rouchon, E. Martinez, P. Holliger, C. Di Nardo, Y. Campidelli, and T. Billon. "Wet cleaning and surface characterization of $Si_{1-x}Ge_x$ virtual substrates after a CMP step". In: *Applied Surface Science* 254.21 (Aug. 2008), pp. 6793–6798. ISSN: 01694332. DOI: 10.1016/j.apsusc.2008.04.107. URL: http://linkinghub.elsevier.com/retrieve/pii/S0169433208009197.

[61] J. G. Fossum and D. S. Lee. "A physical model for the dependence of carrier lifetime on doping density in nondegenerate silicon". In: *Solid-State Electronics* 25.8 (Aug. 1982), pp. 741–747. ISSN: 00381101. DOI: 10.1016/0038-1101(82)90203-9. URL: http://linkinghub.elsevier.com/retrieve/pii/0038110182902039.

[62] J. G. Fossum, R. P. Mertens, D. S. Lee, and J. F. Nijs. "Carrier recombination and lifetime in highly doped silicon". In: *Solid-State Electronics* 26.6 (June 1983), pp. 569–576. ISSN: 00381101. DOI: 10.1016/0038-1101(83)90173-9. URL: http://linkinghub.elsevier.com/retrieve/pii/0038110183901739.

[63] B. I. Boyanov, P. T. Goeller, D. E. Sayers, and R. J. Nemanich. "Film thickness effects in the Co-$Si_{1-x}Ge_x$ solid phase reaction". In: *Journal of Applied Physics* 84.8 (1998), p. 4285. ISSN: 00218979. DOI: 10.1063/1.368872. URL: http://scitation.aip.org/content/aip/journal/jap/84/8/10.1063/1.368872.

[64] W. M. Weber, L. Geelhaar, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Pamler, C. Chèze, H. Riechert, P. Lugli, and F. Kreupl. "Silicon-Nanowire Transistors with Intruded Nickel-Silicide Contacts". In: *Nano Letters* 6.12 (Dec. 2006), pp. 2660–2666. ISSN: 1530-6984. DOI: 10.1021/nl0613858. URL: http://pubs.acs.org/doi/abs/10.1021/nl0613858.

[65] L. Knoll, M. Schmidt, Q.-T. Zhao, S. Trellenkamp, A. Schäfer, K. K. Bourdelle, and S. Mantl. "Si tunneling transistors with high on-currents and slopes of 50mV/dec using segregation doped $NiSi_2$ tunnel junctions". In: *Solid-State Electronics* 84 (June 2013), pp. 211–215. ISSN: 00381101. DOI: 10.1016/j.sse.2013.02.028. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110113000890.

[66] A. Pal, A. B. Sachid, H. Gossner, and V. R. Rao. "Insights Into the Design and Optimization of Tunnel-FET Devices and Circuits". In: *IEEE Transactions on Electron Devices* 58.4 (Apr. 2011), pp. 1045–1053. ISSN: 0018-9383. DOI: 10.1109/TED.2011.2109002. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5728857.

[67] J. T. Smith, S. Das, and J. Appenzeller. "Broken-Gap Tunnel MOSFET: A Constant-Slope Sub-60-mV/decade Transistor". In: *IEEE Electron Device Letters* 32.10 (Oct. 2011), pp. 1367–1369. ISSN: 0741-3106. DOI: 10.1109/LED.2011.2162220. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5977000.

[68] C. Schulte-Braucks, S. Richter, L. Knoll, L. Selmi, Q.-T. Zhao, and S. Mantl. "Experimental demonstration of improved analog device performance of nanowire-TFETs". In: *Solid-State Electronics* 113 (Nov. 2015), pp. 179–183. ISSN: 00381101. DOI: 10.1016/j.sse.2015.05.032. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110115001641.

[69] G. V. Luong, S. Strangio, A. T. Tiedemannn, S. Lenk, S. Trellenkamp, K. K. Bourdelle, Q.-T. Zhao, and S. Mantl. "Experimental demonstration of strained Si nanowire GAA n-TFETs and inverter operation with complementary TFET logic at low supply voltages". In: *Solid-State Electronics* (Sept. 2015). ISSN: 00381101. DOI: 10.1016/j.sse.2015.08.020. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110115002488.

[70] A. Mallik and A. Chattopadhyay. "Tunnel Field-Effect Transistors for Analog/Mixed-Signal System-on-Chip Applications". In: *IEEE Transactions on Electron Devices* 59.4 (Apr. 2012), pp. 888–894. ISSN: 0018-9383. DOI: 10.1109/TED.2011.2181178. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6126073.

[71] L. Knoll, Q.-T. Zhao, R. Luptak, S. Trellenkamp, K. K. Bourdelle, and S. Mantl. "20nm Gate length Schottky MOSFETs with ultra-thin NiSi/epitaxial $NiSi_2$ source/drain". In: *Solid-State Electronics* 71 (May 2012), pp. 88–92. ISSN: 00381101. DOI: 10.1016/j.sse.2011.10.026. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110111003893.

[72] K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, W. Magnus, D. Leonelli, G. Groeseneken, and K. De Meyer. "Optimization of Gate-on-Source-Only Tunnel FETs With Counter-Doped Pockets". In: *IEEE Transactions on Electron Devices* 59.8 (Aug. 2012), pp. 2070–2077. ISSN: 0018-9383. DOI: 10.1109/TED.2012.2200489. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6226449.

[73] M. Schmidt, R. A. Minamisawa, S. Richter, A. Schäfer, D. Buca, J. M. Hartmann, Q.-T. Zhao, and S. Mantl. "Unipolar behavior of asymmetrically doped strained $Si_{0.5}Ge_{0.5}$ tunneling field-effect transistors". In: *Applied Physics Letters* 101.12 (2012), p. 123501. ISSN: 00036951. DOI: 10.1063/1.4751356. URL: http://scitation.aip.org/content/aip/journal/apl/101/12/10.1063/1.4751356.

[74] K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken, and K. De Meyer. "Direct and Indirect Band-to-Band Tunneling in Germanium-Based TFETs". In: *IEEE Transactions on Electron Devices* 59.2 (Feb. 2012), pp. 292–301. ISSN: 0018-9383. DOI: 10.1109/TED.2011.2175228. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6096396.

[75] K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, and K. De Meyer. "Counterdoped Pocket Thickness Optimization of Gate-on-Source-Only Tunnel FETs". In: *IEEE Transactions on Electron Devices* 60.1 (Jan. 2013), pp. 6–12. ISSN: 0018-9383. DOI: 10.1109/TED.2012.2227115. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6359896.

[76] *Arbitrary Waveform Generators Quick Start User Manual*. Tektronix Inc. Mar. 2012.

[77] *Digital Phosphor Oscilloscopes Quick Start User Manual*. Tektronix Inc. Dec. 2013.

[78] Y. Yoon and S. Salahuddin. "Inverse temperature dependence of subthreshold slope in graphene nanoribbon tunneling transistors". In: *Applied Physics Letters* 96.1 (2010), p. 013510. ISSN: 00036951. DOI: 10.1063/1.3280379. URL: http://scitation.aip.org/content/aip/journal/apl/96/1/10.1063/1.3280379.

[79] Y. Yoon and S. Salahuddin, eds. *Temperature-Dependent Subthreshold Characteristics in Graphene Nanoribbon Tunneling Transistors*. Vol. 55. 2. University of California, Berkeley. Portland, OR: APS March Meeting 2010, Mar. 2010.

[80] H. Ibach and H. Lüth. *Festkörperphysik : eine Einführung in die Grundlagen ; mit 16 Tabellen*. German. Berlin; Heidelberg; New York; London; Paris; Tokyo; Hong Kong; Barcelona; Budapest: Springer, 1993. ISBN: 3540521933 9783540521938.

[81] C. Kittel. *Introduction to solid state physics*. English. Hoboken, NJ: Wiley, 2013. ISBN: 9780471415268 047141526X.

[82] Y. P. Varshni. "Temperature dependence of the energy gap in semiconductors". In: *Physica* 34.1 (Jan. 1967), pp. 149–154. ISSN: 00318914. DOI: 10.1016/0031-8914(67)90062-6. URL: http://linkinghub.elsevier.com/retrieve/pii/0031891467900626.

[83] K. P. O'Donnell and X. Chen. "Temperature dependence of semiconductor band gaps". In: *Applied Physics Letters* 58.25 (1991), p. 2924. ISSN: 00036951. DOI: 10.1063/1.104723. URL: http://scitation.aip.org/content/aip/journal/apl/58/25/10.1063/1.104723.

[84] A. Nichau. "Characterization, integration and reliability of HfO_2 and $LaLuO_3$ high-κ-metal gate stacks for CMOS applications". Zsfassung in dt. und engl. Sprache; Aachen, Techn. Hochsch., Diss., 2013. PhD thesis. Aachen, 2013, XI, 179 S. : Ill., graph. Darst. URL: http://publications.rwth-aachen.de/record/229175.

[85] H. Ilatikhameneh, G. Klimeck, and R. Rahman. "Can Homojunction Tunnel FETs Scale Below 10 nm?" In: *IEEE Electron Device Letters* 37.1 (Jan. 2016), pp. 115–118. ISSN: 0741-3106. DOI: 10.1109/LED.2015.2501820. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7331599.

[86] S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta. "Temperature-Dependent *I-V* Characteristics of a Vertical $In_{0.53}Ga_{0.45}As$ Tunnel FET". In: *IEEE Electron Device Letters* 31.6 (June 2010), pp. 564–566. ISSN: 0741-3106. DOI: 10.1109/LED.2010.2045631. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5451179.

[87] P. Matheu. "Investigations of Tunneling for Field Effect Transistors". PhD thesis. Berkeley, CA, 2012. URL: http://www.eecs.berkeley.edu/~tking/theses/pmatheu.pdf.

[88] R. Rooyackers, A. Vandooren, A. S. Verhulst, A. M. Walke, E. Simoen, K. Devriendt, S. Lo-Corotondo, M. Demand, G. Bryce, R. Loo, A. Hikavyy, T. Vandeweyer, C. Huyghebaert, N. Collaert, and Aaron V. Y. Thean. "Ge-Source Vertical Tunnel FETs Using a Novel Replacement-Source Integration Scheme". In: *IEEE Transactions on Electron Devices* 61.12 (Dec. 2014), pp. 4032–4039. ISSN: 0018-9383. DOI: 10.1109/TED.2014.2365142. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6954497.

[89] A. S. Verhulst, ed. *The future of tunnel field-effect transistors*. IMEC, Leuven, Belgium. Jülich: nanoelectronic days 2015 "Green-IT", Forschungszentrum Jülich, Apr. 2015.

[90] A. S. Verhulst, ed. *Introductory material*. IMEC, Leuven, Belgium. Notre Dame, IN: Steep Transistors Workshop, University of Notre Dame, Oct. 2015.

[91] D. D. Givone. *Digital principles and design*. English. Boston; Montreal: McGraw-Hill, 2003. ISBN: 0072551321 9780072551327 0072549378 9780072549379 0072525037 9780072525038.

[92] S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu. "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}". In: *VLSI Technology, 2009 Symposium on*. June 2009, pp. 178–179.

[93] D. Leonelli, A. Vandooren, R. Rooyackers, S. De Gendt, M. M. Heyns, and G. Groeseneken. "Optimization of tunnel FETs: Impact of gate oxide thickness, implantation and annealing conditions". In: *2010 Proceedings of the European Solid State Device Research Conference*. IEEE, Sept. 2010, pp. 170–173. ISBN: 978-1-4244-6658-0. DOI: 10.1109/ESSDERC.2010.5618408. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5618408.

[94] K. E. Moselund, M. T. Bjork, H. Schmid, H. Ghoneim, S. Karg, E. Lortscher, W. Riess, and H. Riel. "Silicon Nanowire Tunnel FETs: Low-Temperature Operation and Influence of High-κ Gate Dielectric". In: *IEEE Transactions on Electron Devices* 58.9 (Sept. 2011), pp. 2911–2916. ISSN: 0018-9383. DOI: 10.1109/TED.2011.2159797. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5975213.

[95] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee. "CMOS-Compatible Vertical-Silicon-Nanowire Gate-All-Around p-Type Tunneling FETs With $\leq$ 50 mV/decade Subthreshold Swing". In: *IEEE Electron Device Letters* 32.11 (Nov. 2011), pp. 1504–1506. ISSN: 0741-3106. DOI: 10.1109/LED.2011.2165331. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6029281.

[96] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau. "Fabrication, characterization, and physics of III-V heterojunction tunneling Field Effect Transistors (H-TFET) for steep subthreshold swing". In: *2011 International Electron Devices Meeting*. IEEE, Dec. 2011, pp. 33.6.1–33.6.4. ISBN: 978-1-4577-0505-2. DOI: 10.1109/IEDM.2011.6131666. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6131666.

[97] G. Zhou, Y. Lu, R. Li, Q. Zhang, Q. Liu, T. Vasen, H. Zhu, J.-M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing. "InGaAs/InP Tunnel FETs With a Subthreshold Swing of 93 mV/dec and I_{ON}/I_{OFF} Ratio Near 10^6". In: *IEEE Electron Device Letters* 33.6 (June 2012), pp. 782–784. ISSN: 0741-3106. DOI: 10.1109/LED.2012.2189546. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6178768.

[98] D. Mohata, B. Rajamohanan, T. Mayer, M. Hudait, J. Fastenau, D. Lubyshev, A. W. K. Liu, and S. Datta. "Barrier-Engineered Arsenide-Antimonide Heterojunction Tunnel FETs With Enhanced Drive Current". In: *IEEE Electron Device Letters* 33.11 (Nov. 2012), pp. 1568–1570. ISSN: 0741-3106. DOI: 10.1109/LED.2012.2213333. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6313884.

[99] L. Knoll, Q.-T. Zhao, A. Nichau, S. Richter, G. V. Luong, S. Trellenkamp, A. Schäfer, L. Selmi, K. K. Bourdelle, and S. Mantl. "Demonstration of improved transient response of inverters with steep slope strained Si NW TFETs by reduction of TAT with pulsed *I-V* and NW scaling". In: *2013 IEEE International Electron Devices Meeting*. IEEE, Dec. 2013, pp. 4.4.1–4.4.4. ISBN: 978-1-4799-2306-9. DOI: 10.1109/IEDM.2013.6724560. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6724560.

[100] M. Noguchi, S.-H. Kim, M. Yokoyama, S.-M. Ji, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi. "High I_{on}/I_{off} and low subthreshold slope planar-type InGaAs tunnel FETs with Zn-diffused source junctions". In: *2013 IEEE International Electron Devices Meeting*. IEEE, Dec. 2013, pp. 28.1.1–28.1.4. ISBN: 978-1-4799-2306-9. DOI: 10.1109/IEDM.2013.6724707. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6724707.

[101] A. M. Walke, A. Vandooren, R. Rooyackers, D. Leonelli, A. Hikavyy, R. Loo, A. S. Verhulst, K.-H. Kao, C. Huyghebaert, G. Groeseneken, V. R. Rao, K. K. Bhuwalka, M. M. Heyns, N. Collaert, and A. V.-Y. Thean. "Fabrication and Analysis of a $Si/Si_{0.55}Ge_{0.45}$ Heterojunction Line Tunnel FET". In: *IEEE Transactions on Electron Devices* 61.3 (Mar. 2014), pp. 707–715. ISSN: 0018-9383. DOI: 10.1109/TED.2014.2299337. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6727530.

[102] M. Kim, Y. Wakabayashi, R. Nakane, M. Yokoyama, M. Takenaka, and S. Takagi. "High I_{on}/I_{off} Ge-source ultrathin body strained-SOI tunnel FETs". In: *2014 IEEE International Electron Devices Meeting*. IEEE, Dec. 2014, pp. 13.2.1–13.2.4. ISBN: 978-1-4799-8001-7. DOI: 10.1109/IEDM.2014.7047043. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7047043.

[103] Y. Morita, T. Mori, K. Fukuda, W. Mizubayashi, S. Migita, T. Matsukawa, K. Endo, S. O'uchi, Y. Liu, M. Masahara, and H. Ota. "Experimental realization of complementary p- and n- tunnel FinFETs with subthreshold slopes of less than 60 mV/decade and very low (pA/μm) off-current on a Si CMOS platform". In: *2014 IEEE International Electron Devices Meeting*. IEEE, Dec. 2014, pp. 9.7.1–9.7.4. ISBN: 978-1-4799-8001-7. DOI: 10.1109/IEDM.2014.7047020. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7047020.

[104] X. Zhao, A. Vardi, and J. A. del Alamo. "InGaAs/InAs heterojunction vertical nanowire tunnel fets fabricated by a top-down approach". In: *2014 IEEE International Electron Devices Meeting*. IEEE, Dec. 2014, pp. 25.5.1–25.5.4. ISBN: 978-1-4799-8001-7. DOI: 10.1109/IEDM.2014.7047108. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7047108.

[105] B. Rajamohanan, R. Pandey, V. Chobpattana, C. Vaz, D. Gundlach, K. P. Cheung, J. Suehle, S. Stemmer, and S. Datta. "0.5 V Supply Voltage Operation of $In_{0.65}Ga_{0.35}As/GaAs_{0.4}Sb_{0.6}$ Tunnel FET". In: *IEEE Electron Device Letters* 36.1 (Jan. 2015), pp. 20–22. ISSN: 0741-3106. DOI: 10.1109/LED.2014.2368147. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6949120.

[106] D. Cutaia, K. E. Moselund, M. Borg, H. Schmid, L. Gignac, C. M. Breslin, S. Karg, E. Uccelli, and H. Riel. "Vertical InAs-Si Gate-All-Around Tunnel FETs Integrated on Si Using Selective Epitaxy in Nanotube Templates". In: *IEEE Journal of the Electron Devices Society* 3.3 (May 2015), pp. 176–183. ISSN: 2168-6734. DOI: 10.1109/JEDS.2015.2388793. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7001544.

[107] C. Le Royer, A. Villalon, L. Hutin, S. Martinie, P. Nguyen, S. Barraud, F. Glowacki, F. Allain, N. Bernier, S. Cristoloveanu, and M. Vinet. "Fabrication and electrical characterizations of SGOI tunnel FETs with gate length down to 50nm". In: *Solid-State Electronics* (Nov. 2015). ISSN: 00381101. DOI: 10.1016/j.sse.2015.10.007. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110115002907.

[108] U. Wieser, D. Iamundo, U. Kunze, T. Hackbarth, and U. König. "Nanoscale patterning of Si/SiGe heterostructures by electron-beam lithography and selective wet-chemical etching". In: *Semiconductor Science and Technology* 15.8 (Aug. 2000), pp. 862–867. ISSN: 0268-1242. DOI: 10.1088/0268-1242/15/8/313. URL:

http://stacks.iop.org/0268-1242/15/i=8/a=313?key=crossref.256159f372f2c78290e181620ed17a10.

[109] W. Hsu, J. Mantey, L. F. Register, and S. K. Banerjee. "On the Electrostatic Control of Gate-Normal-Tunneling Field-Effect Transistors". In: *IEEE Transactions on Electron Devices* 62.7 (July 2015), pp. 2292–2299. ISSN: 0018-9383. DOI: 10.1109/TED.2015.2434615. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7118174.

List of Publications

Journal Papers

- S. Blaeser, S. Glass, C. Schulte-Braucks, K. Narimani, N. von den Driesch, S. Wirths, A. T. Tiedemann, S. Trellenkamp, D. Buca, Q.-T. Zhao, and S. Mantl. "Line Tunneling Dominating Charge Transport in SiGe/Si Heterostructure TFETs". In: *IEEE Transactions on Electron Devices* (2016). to be published

- C. Schulte-Braucks, D. Stange, N. von den Driesch, S. Blaeser, Z. Ikonic, J. M. Hartmann, S. Mantl, and D. Buca. "Negative differential resistance in direct bandgap GeSn p-i-n structures". In: *Applied Physics Letters* 107.4 (July 2015), p. 042101. ISSN: 0003-6951. DOI: 10.1063/1.4927622. URL: http://scitation.aip.org/content/aip/journal/apl/107/4/10.1063/1.4927622

- G. V. Luong, L. Knoll, S. Blaeser, M. J. Süess, H. Sigg, A. Schäfer, S. Trellenkamp, K. K. Bourdelle, D. Buca, Q.-T. Zhao, and S. Mantl. "Demonstration of higher electron mobility in Si nanowire MOSFETs by increasing the strain beyond 1.3%". In: *Solid-State Electronics* 108 (June 2015), pp. 19–23. ISSN: 00381101. DOI: 10.1016/j.sse.2014.12.015. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110114003086

- Q.-T. Zhao, S. Richter, C. Schulte-Braucks, L. Knoll, S. Blaeser, G. V. Luong, S. Trellenkamp, A. Schäfer, A. T. Tiedemann, J. M. Hartmann, K. K. Bourdelle, and S. Mantl. "Strained Si and SiGe Nanowire Tunnel FETs for Logic and Analog Applications". In: *IEEE Journal of the Electron Devices Society* 3.3 (May 2015), pp. 103–114. ISSN: 2168-6734. DOI: 10.1109/JEDS.2015.2400371. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7031858

- L. Knoll, S. Richter, A. Nichau, S. Trellenkamp, A. Schäfer, S. Wirths, S. Blaeser, D. Buca, K. K. Bourdelle, Q.-T. Zhao, and S. Mantl. "Strained silicon based complementary tunnel-FETs: Steep slope switches for energy efficient electronics". In: *Solid-State Electronics* 98 (Aug. 2014), pp. 32–37. ISSN: 00381101. DOI: 10.1016/j.sse.2014.04.006. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110114000549

- S. Richter, S. Blaeser, L. Knoll, S. Trellenkamp, A. Fox, A. Schäfer, J. M. Hartmann, Q.-T. Zhao, and S. Mantl. "Silicon–germanium nanowire tunnel-FETs with homo- and heterostructure tunnel junctions". In: *Solid-State Electronics* 98 (Aug. 2014), pp. 75–80. ISSN: 00381101. DOI: 10.1016/j.sse.2014.04.014. URL: http://linkinghub.elsevier.com/retrieve/pii/S0038110114000628

Conference Contributions

- S. Blaeser, S. Glass, C. Schulte-Braucks, K. Narimani, N. von den Driesch, S. Wirths, A. T. Tiedemann, S. Trellenkamp, D. Buca, Q.-T. Zhao, and S. Mantl. "Novel SiGe/Si line tunneling TFET with high I_{on} at low V_{DD} and constant SS". in: *2015 IEEE International Electron Devices Meeting*. IEEE, Dec. 2015, pp. 22.3.1–22.3.4. ISBN: 978-1-4673-9894-7. DOI: 10.1109/IEDM.2015.7409757. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7409757

- Q.-T. Zhao, S. Richter, L. Knoll, G. V. Luong, S. Blaeser, C. Schulte-Braucks, A. Schäfer, S. Trellenkamp, D. Buca, and S. Mantl. "(Invited) Si Nanowire Tunnel FETs for Energy Efficient Nanoelectronics". In: *ECS Transactions* 66.4 (May 2015), pp. 69–78. ISSN: 1938-6737. DOI: 10.1149/06604.0069ecst. URL: http://ecst.ecsdl.org/cgi/doi/10.1149/06604.0069ecst

- S. Mantl, L. Knoll, G. V. Luong, S. Richter, S. Blaeser, S. Wirths, C. Schulte-Braucks, S. Trellenkamp, D. Buca, and Q.-T. Zhao. "Tunneling Field Effect Transistors for Low Power Electronics". In: *NATO Advanced Research Workshop "Functional Nanomaterials and Devices for Electronics, Sensors, Energy Harvesting"*. Apr. 2015

- S. Blaeser, S. Richter, S. Wirths, S. Trellenkamp, D. Buca, Q.-T. Zhao, and S. Mantl. "Experimental demonstration of planar SiGe on Si TFETs with counter doped pocket". In: *EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon*. IEEE, Jan. 2015, pp. 297–300. ISBN: 978-1-4799-6911-1. DOI: 10.1109/ULIS.2015.7063832. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7063832

- Q.-T. Zhao, L. Knoll, S. Richter, C. Schulte-Braucks, G. V. Luong, S. Blaeser, Anna Schäfer, S. Trellenkamp, and S. Mantl. "Strained silicon nanowire tunnel FETs and NAND logic". In: *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*. IEEE, Oct. 2014, pp. 1–4. ISBN: 978-1-4799-3282-5. DOI: 10.1109/ICSICT.2014.7021495. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7021495

- Q.-T. Zhao, L. Knoll, S. Richter, M. Schmidt, S. Blaeser, G. V. Luong, S. Wirths, A. Nichau, A. Schäfer, S. Trellenkamp, J. M. Hartmann, K. K. Bourdelle, D. Buca, and S. Mantl. "Strained Si nanowire tunnel FETs and inverters". In: *2013 Third Berkeley Symposium on Energy Efficient Electronic Systems (E3S)*. IEEE, Oct. 2013, pp. 1–2. ISBN: 978-1-4799-3372-3. DOI: 10.1109/E3S.2013.6705867. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6705867

- S. Mantl, L. Knoll, S. Richter, M. Schmidt, S. Wirths, A. Nichau, A. Schäfer, S. Blaeser, S. Trellenkamp, J. M. Hartmann, K. K. Bourdelle, D. Buca, and Q.-T. Zhao. "Si based tunneling field effect transistors and inverters". In: *71st Device Research Conference*. IEEE, June 2013, pp. 193–194. ISBN: 978-1-4799-0814-1. DOI: 10.1109/DRC.2013.6633859. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6633859

- S. Wirths, S. Blaeser, A. Biswas, A. T. Tiedemann, P. Bernardy, B. Holländer, G. Mussler, U. Breuer, D. Buca, and S. Mantl. "Growth of graded doped Si/SiGe Heterostructure Tunnel FET". in: *European Material Research Society 2013, E-MRS*. May 2013

- S. Mantl, L. Knoll, M. Schmidt, S. Richter, A. Nichau, S. Trellenkamp, A. Schäfer, S. Wirths, S. Blaeser, D. Buca, and Qing-Tai Zhao. "Si based tunnel field effect transistors: Recent achievements". In: *2013 14th International Conference on Ultimate Integration on Silicon (ULIS)*. IEEE, Mar. 2013, pp. 15–20. ISBN: 978-1-4673-4802-7. DOI: 10.1109/ULIS.2013.6523480. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6523480

- S. Richter, S. Blaeser, L. Knoll, S. Trellenkamp, A. Schäfer, J. M. Hartmann, Q.-T. Zhao, and S. Mantl. "SiGe on SOI nanowire array TFETs with homo- and heterostructure tunnel junctions". In: *2013 14th International Conference on Ultimate Integration on Silicon (ULIS)*. IEEE, Mar. 2013, pp. 25–28. ISBN: 978-1-4673-4802-7. DOI: 10.1109/ULIS.2013.6523482. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6523482

Curriculum Vitae

Personal details

Name	Sebastian Blaeser
Date of birth	May 11th, 1984
Place of birth	Düsseldorf, Germany
Nationality	German

Professional experience

10/2011 - 06/2015	Forschungszentrum Jülich, Peter Grünberg Institute 9 PhD student in the group of Prof. Siegfried Mantl
02/2011 - 05/2011	RWTH Aachen University, 2nd Institute of Physics A Research assistant in the group of Prof. Gernot Güntherodt
10/2010 - 12/2010	RWTH Aachen University, 2nd Institute of Physics A Research assistant in the group of Prof. Gernot Güntherodt

Education

10/2009 - 09/2011	RWTH Aachen University Master of Science in Physics
10/2006 - 09/2009	RWTH Aachen University Bachelor of Science in Physics
10/2004 - 09/2006	RWTH Aachen University Studies of Electrical Engineering
08/1994 - 06/2003	Suitbertus Gymnasium, Düsseldorf Allgemeine Hochschulreife

Languages

German	Mother tongue
English	Fluent
French	Basic

Acknowledgments

I would like to express my gratitude to a wide range of people without whose continuous support and helpfulness this thesis would not have been realized.

At first, I thank Prof. Siegfried Mantl for giving me the opportunity to become a member of his research group and for the supervision of my Ph.D. thesis. He always encouraged me and showed up new perspectives when I got stuck. I also thank Prof. Christoph Stampfer for being the second reviewer of my thesis.

I thank my group advisor Dr. Qing-Tai Zhao for introducing me to a wide range of topics related to semiconductors as TFETs, silicides and clean room technology. I am grateful for numerous helpful discussions and support whenever needed.

I thank Dr. Stephan Wirths for spending many hours in growing the different substrates as starting point of every processed TFET and for fruitful discussions whenever we shared the office.

I thank Andreas Tiedemann, Karl-Heinz Deußen and Patric Bernardy for various ALD / AVD depositions and FGA runs. Thanks to Christian Scholtysik, Andre Dahmen and Katja Palmen for ion implantations as well as to Steffi Lenk for TEM analysis.

I thank Dr. Stefan Trellenkamp for numerous hours of e-beam writing and the staff of the HNF for their support in clean room. Thanks to Alfred Fox for introducing me to low temperature measurements.

I also thank Dr. Simon Richter, Dr. Lars Knoll, Dr. Anna Schäfer, Linjie Liu, Gia Vinh Luong, Keyvan Narimani, Nils von den Driesch, Christian Schulte-Braucks and Stefan Glass for a pleasant working time in the institute and many helpful discussions.

Last but not least, I particularly thank my parents and my fiancée Patrizia for their imperturbable support, encouragement and patience - without you, this journey would not have been possible.

Band / Volume 110
Microswimmers – From Single Particle Motion to Collective Behaviour
Lecture Notes of the DFG SPP Summer School 2015
edited by G. Gompper, C. Bechinger, S. Herminghaus, R. E. Isele-Holder, U.B. Kaupp, H. Löwen, H. Stark, R. G. Winkler (2015)
ISBN: 978-3-95806-083-8

Band / Volume 111
Long range order in 3D nanoparticle assemblies
E. Josten (2015), 238 pp
ISBN: 978-3-95806-087-6

Band / Volume 112
Silicon nanowire structures for neuronal cell interfacing
S. Pud (2015), 153 pp
ISBN: 978-3-95806-089-0

Band / Volume 113
Memristive Phenomena -
From Fundamental Physics to Neuromorphic Computing
Lecture Notes of the 47th IFF Spring School 2016
22 February – 04 March 2016, Jülich, Germany
ed. by R. Waser and M. Wuttig (2016), ca 1000 pp
ISBN: 978-3-95806-091-3

Band / Volume 114
Single-Cell Analysis of Microbial Production Strains
in Microfluidic Bioreactors
A. M. Grünberger (2015), XIX, 225 pp
ISBN: 978-3-95806-092-0

Band / Volume 115
Magnetic order and spin dynamics in the
extended kagome system $CaBaCo_2Fe_2O_7$
J. Reim (2015), viii, 144 pp
ISBN: 978-3-95806-097-5

Band / Volume 116
Structural and electronic investigations on homo- and hetero-organic layers involving CuPc on silver single crystal surfaces
K. M. Schönauer (2015), x, 148 pp
ISBN: 978-3-95806-112-5

Band / Volume 117
First-principles investigation of inelastic magnetic excitations
in nanostructures deposited on surfaces
B. J. Schweflinghaus (2016), v, 204 pp
ISBN: 978-3-95806-115-6

Band / Volume 118
Magnetic, structural, and electronic properties of $NiFe_2O_4$ ultrathin films
M. Hoppe (2016), vii, 118 pp
ISBN: 978-3-95806-122-4

Band / Volume 119
First-principle investigation of displacive response in complex solids
D. A. Klüppelberg (2016), xi, 179 pp
ISBN: 978-395806-123-1

Band / Volume 120
Beam Cooling at COSY and HESR - Theory and Simulation -
Part 1 Theory
H. Stockhorst, T. Katayama and R. Maier (2016), v, 192 pp
ISBN: 978-3-95806-127-9

Band / Volume 121
Scanning tunneling microscopy of single-molecule magnets and hybrid-molecular magnets: Two approaches to molecular spintronics
V. Heß (2016), x, 127 pp
ISBN: 978-3-95806-128-6

Band / Volume 122
Bulk and surface sensitive energy-filtered photoemission microscopy using synchrotron radiation for the study of resistive switching memories
M. C. Patt (2016), viii, 247 pp
ISBN: 978-3-95806-130-9

Band / Volume 123
Group IV Epitaxy for Advanced Nano- and Optoelectronic Applications
S. Wirths (2016), vi, 116, XXX pp
ISBN: 978-3-95806-132-3

Band / Volume 124
Strained Silicon-Germanium/Silicon Heterostructure Tunnel FETs for Low Power Applications
S. Blaeser (2016), iv, 91, xvii pp
ISBN: 978-3-95806-135-4

Schlüsseltechnologien /
Key Technologies
Band / Volume 124
ISBN 978-3-95806-135-4