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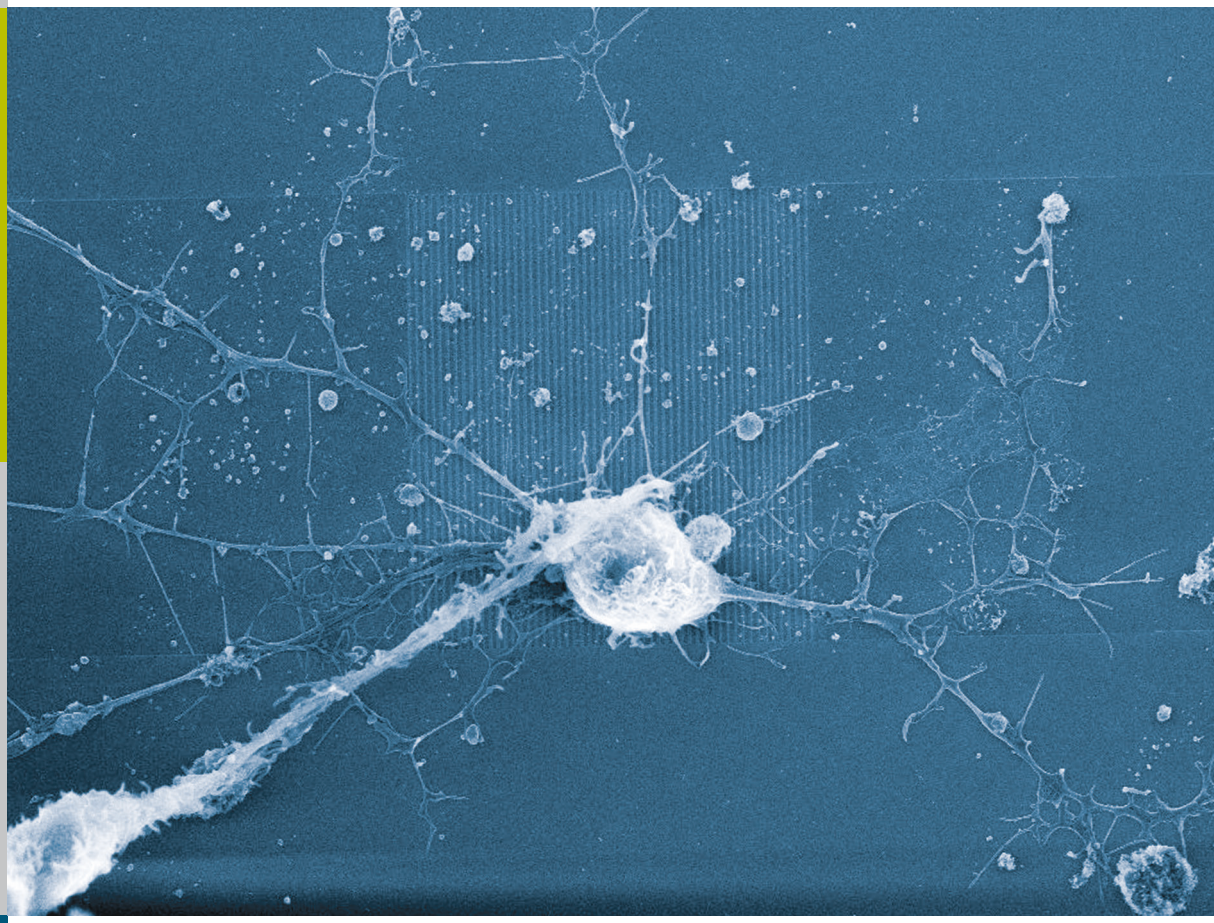

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Abstract

During last decade silicon nanowire (NW) field effect transistors (FETs) attracted considerable attention of researchers as perfect candidates for development of highly sensitive and reliable biosensors, which are compatible with cost-efficient CMOS technology. Recently the liquid-gated FETs were used to demonstrate proof of principle extracellular measurements of neuronal cells action potential, which is of great interest regarding the large variety of applications like monitoring of electrical communication within neuronal networks, transmission paths of ionic channels etc. The NWs are expected to provide an improved contact between neuronal cells and NW surface, which is of crucial importance for signal transduction from the cell to the channel of the NW. However, it is still challenging to establish robust tool for the extracellular monitoring of electrogenic cell activity. One of the important milestones of the research in this area is the signal-to-noise ratio (SNR), which determines the detection limit of such type of sensors. Therefore, current work is devoted to design, technology development and fabrication of Si NW FET structures for neuronal cell interfacing and characterizing of their transport properties and reliability utilizing technique of noise spectroscopy. During the work we study the transport properties of single Si NW FET transistors, in order to improve understanding of the factors influencing SNR of the NW biosensors. The results demonstrate modulation effect of the channel current by single trap located in the gate dielectric, which reflects extreme charge sensitivity of the NW FET devices. Arising from these investigations we developed and fabricated the Si NW FET structures based on arrays of 50 NWs connected in parallel. Fabricated liquid-gated NW FET structures are characterized in order to find optimal regimes of operation. The revealed front-back gate coupling effect was used to improve the SNR of the fabricated devices by 50%. According to our measurements, the developed Si NW FET structures meet the requirements needed for extracellular detection of the neuronal cell activity. The interface between neuronal cells and fabricated structures was studied using FIB technique. The results demonstrate that the cells contact NWs without a cleft.

Zusammenfassung

In den letzten Jahren haben Silizium-Nanodraht (NW) Feldeffekttransistoren (FETs) bei Forschern großes Interesse geweckt als perfekte Kandidaten für die Entwicklung von hochempfindlichen und robusten Biosensoren, die mit kostengünstiger CMOS-Technologie kompatibel sind. Seit kurzem werden NW-FETs mit einem Elektrolyt-gesteurten Gate verwendet, um grundsätzliche Machbarkeit extrazellulärer Messungen vom Aktionspotential der neuronalen Zellen aufzuzeigen, da diese von großem Interesse sind im Hinblick auf verschiedene Anwendungen wie die Überwachung von elektrischer Kommunikation innerhalb der neuronalen Netzwerke, Übertragungswege der Ionenkanäle usw. Silizium-Nanodrähte sollen einen verbesserten Kontakt zwischen neuronalen Zellen und NW-Oberfläche vermitteln, der für die Signalübertragung von der Zelle auf den jeweiligen Kanal der NW von herausragender Bedeutung ist. Allerdings gibt es noch einige Herausforderungen in der Etablierung eines robusten Werkzeugs zur extrazellulären Überwachung der Aktivität von elektrisch aktiven Zellen. Einer der wichtigen Meilensteine der Forschung in diesem Bereich ist das Signal-Rausch-Verhältnis (SNR), das die Empfindlichkeit von dieser Art von Sensoren bestimmt. Die vorliegende Arbeit widmet sich daher dem Design, der Entwicklung der Technologie und der Herstellung von Si NW FET-Strukturen für die extrazelluläre Ankopplung von neuronalen Zellen und der Charakterisierung ihrer Transporteigenschaften und Zuverlässigkeit unter Verwendung leistungsfähiger Methode der Rausch-Spektroskopie. Im Verlauf dieser Arbeit wurden die Transporteigenschaften von Si NW FET Transistoren untersucht, die auf einzelnen Nanodrähten basieren, um das Verständnis der Einflussfaktoren auf das SNR der NW Biosensoren zu verbessern. Die Ergebnisse zeigen insbesondere einen Modulationseffekt des Kanalstroms durch singuläre Falle im Gate-Dielektrikum, der die extreme Empfindlichkeit zu der Ladung von NW FET Bauelementen wiederspiegelt. Auf Grund von diesen Untersuchungen wurden von uns die Si NW FET-Strukturen basierend auf Anordnungen von 50 parallelgeschalteten Nanodrähten entwickelt und hergestellt. Die hergestellten NW FET-Strukturen wurden elektrisch charakterisiert, um ein optimales Betriebsregime zu finden. Die untersuchte Front-Back-Gate-Kopplungswirkung in den NW FETs wurde zur Verbesserung des Signal-Rausch Verhältnisses um 50% genutzt. Nach unseren Messungen, erfüllen die entwickelten Si NW FET-Strukturen die Anforderungen für extrazelluläre Detektion, neuronaler Zellaktivität. Die Schnittstelle zwischen neuronalen Zellen und hergestellten NW Strukturen wurde darüber hinaus mit fokussierter Ionenstrahl (FIB) untersucht. Die Ergebnisse zeigen, dass die Zellen in direkten Kontakt mit der Oberfläche der NW Strukturen treten.

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1. Introduction

The tremendous progress in physical and biological in recent years has facilitated deeper understanding of different biological objects even down to a molecular level and thus formed a strong demand on development of highly-sensitive, selective, stable and reliable biosensors[1]–[4] for real-time analysis and monitoring of biochemical reactions in vivo and in vitro. There are numerous biosensing techniques based on different physical principles such as optical, mechanical and electrical methods for monitoring state of the biosystems[5]. Among other techniques using field-effect transistors (FETs) as biosensors stand out as a promising approach due to their ability to directly translate changes of the gate surface potential into modulation of a drain current[6] and therefore the possibility of real-time monitoring of different processes resulting in surface potential changes. In response to the need for increased sensitivity and higher spatial resolution[7], [8], a new generation of nanoscale FET sensors, based on nanowires, nanotubes[2], nanoribbons[9] and graphene sheets[10] has emerged. In particular, silicon nanowire (Si NW) FETs showed themselves as promising biosensors[11]. Their CMOS-compatibility and flexibility in terms of shapes and sizes, as well as the reproducibility offered by silicon processing technology[12], [13] define the Si NW FETs as excellent candidates for such important applications as label-free detection of biological species [14]–[17] and extracellular investigation of electrogenic cell activity[18]–[20].

Investigation of neuronal cells activity is of great interest from point of view fundamental biophysics as well as for large variety such applications as monitoring of electrical communication within neuronal networks, transmission paths of ionic channels, the use of neuronal networks as biosensor to monitor pharmaceutical agents, pollutants etc. Studying the behavior of grown in vitro neuronal networks gives an overview about functioning of much more complex systems like brain and improves understanding of cell communication at a single synaptic level[21], [22]. These kinds of studies can be strongly facilitated by novel methods of effective bi-directional communication with living cells grown in vitro. Therefore, during last decades several techniques for recording cell activity were developed: glass micropipette[23] and patch clamp electrodes[24], voltage-sensitive dyes[25], microelectrode arrays (MEAs)[26], [27], FETs [28], [29]. Among these approaches MEA and FET techniques have advantages due to improved spatial resolution and direct multiplexed detection of the signal[30]. Another important feature of these approaches is realization of the non-invasive communication with cells. MEAs are considered as prototypes of

brain-machine interface[31]. Further improvement of MEA technique required not only development of stable electrode tolerant to chemical reactions on the electrodes, but also different methods of excitation and recording using FET technology. At the same time, FETs approach enables direct monitoring of the brain activity and hence, this technique for neuronal interfacing attracts most attention in the last decade. However, implementation of the FET based readout from neuronal cells is a challenging task especially if we are speaking about small cell densities on the chip or even single cells.

The state of a single cell or cell system can be monitored by either their metabolic products (in the case of the chemical synapse - neurotransmitter) or extracellular potential monitoring. Such a biochemical sensing of compounds released from the cell during action potential requires much effort on functionalization of the FET surface for selective detection of the substances produced by the cells. Instead, for investigation of the electrogenic cells activity (e.g. neuronal cells) one can utilize their specific features like generating of spontaneous or triggered action potentials and measure shifts of the cell membrane potential. The activity of a neuron leads to ionic- and displacement currents flowing through the cell membrane, resulting in an extracellular voltage drop along the cleft between the cell membrane and the gate insulator of the ion sensitive FET[32]. This voltage drop can be recorded as it modulates the drain current of a FET [33]. However, planar FET technique cannot entirely monitor the different complex processes taking place in the system FET - neuronal cell. The main reasons for this are low spatial resolution and the high cleft between silicon oxide surface and the neuronal cell, which can be up to 100 nm over the sensor surface [34]. Such a large distance makes the seal resistance of the cell over the sensor very small and leads to drastic reduction of useful signal[35]. Therefore, the signal can be also determined not by direct transfer of the membrane potential but due to fluxes of ions, which accompany repolarization of the cell and influence the surface potential of the gate dielectric. In order to get reasonable signal, there is a need to culture cells in a stable way onto the FETs and the interface between them and the gate dielectric should provide reasonable seal resistance. The cleft between neuronal cell and the sensor surface can be shrunk down to 4nm using silicon nanowires (NWs) as transducer. This was confirmed in first studies related to the topic on nanowires produced by bottom-up process [30], [36]. The bottom-up processed nanowires, usually fabricated by chemical vapor deposition, are cheap and easy to produce, but these wires have irreproducible sizes and exhibit problems with

alignment of the nanowires and contacting them. In contrast, another method of NW fabrication is the top-down approach, which is based on lithographical patterning of the Si wafer and allows fabricating highly reproducible, stable and nanowire devices using complementary metal-oxide-semiconductor (CMOS)-compatible fabrication processes.

Si NW FETs designed for monitoring neuronal cell electrogenic activity should be able to register discrete events of neuronal cell action potential by extracellular changes of the gate potential in frame of real-time recording. Therefore, measurement techniques based on averaging of the signal over time are not applicable and the signal-to-noise ratio (SNR) of the raw output from the sensor should be higher than one. Implementing such strong requirements is a rather challenging task while working with extremely small signals, such as extracellular recordings from a single cell. Thus, the important milestone of the research in the area of NW-based biosensors for monitoring living cells activity is the signal-to-noise ratio (SNR)[9], [37]. Understanding of the factors influencing the SNR in Si NW FET sensors is of crucial importance for development of reliable NW biosensors with sufficient sensitivity. The SNR of a FET sensor is determined by the transconductance, g_m, of the Si NW transistor and by the intrinsic noise of the device. Therefore, the SNR can be improved both by optimization of the fabrication technology [38], [39] and by finding the optimal transport regimes to maximize the sensitivity[40]–[42]. The Si NW transistors are fabricated using wet chemical etching to improve quality of the sidewalls of the FET devices and reduce surface noise[43].

According to the above-discussed challenges, this work is devoted to the development of Si NW structures sensitive and reliable enough for effective extracellular monitoring of the neuronal cells activity in vitro. We consider both methods of improving device sensitivity: optimizing fabrication technology and operation mode of the NW FET. As a feedback for improving device characteristics we utilize noise spectroscopy – a powerful approach for investigating device performance and structure. The structures in the presented work were designed in different geometries in order to investigate influence of the channel parameters on SNR. After the fabrication of Si NW FETs, the SNR of produced devices was enhanced by finding optimal regime of the operation. We have shown significant improvement of the SNR by utilization of the front-back-gate coupling effect. Analysis of experimentally obtained data using existing models of noise behavior has shown switching of scattering mechanism under influence of back gate biasing.

The above discussed is implemented in the objective of the presented work: fabrication of stable, reliable and sensitive Si NW FET transistors optimized for biosensor measurements of electrogenic cell activity. The objective is achieved by fulfilling following scientific tasks:

- Fabrication and design of high-quality Si NW FET structures for providing improved interface between cells and the NW surface.
- Characterization of fabricated structures using electron microscopy and electrical characterization using noise spectroscopy in order to improve understanding of the factors influencing the sensor performance.
- Investigating influence of the electrolyte gate on performance and SNR of Si NW FET devices for excluding role of the surface effects on the transport in Si NW FETs
- Identifying influence of different NW parameters, such as contact resistance, charge carrier distribution on transport properties of a NW FET by means of theoretical modelling and noise spectroscopy.
- Analysis of Si NW / neuronal cell interface using focused ion beam (FIB).
- Simulation of the fabricated devices in Sentaurus technology and computer aided design (TCAD) program for establishing directions for improving the device fabrication technology and performance.
- Investigation of the SNR of fabricated Si NW array biosensor devices by studying regimes of the operation and influence of the geometry of the NW FETs.
- Test measurements of the fabricated nanowire structures using pulse signals with characteristics similar to neuronal cell action potential.

2. Theoretical, experimental background and state of the art

2.1 Silicon nanowire based biosensors

2.1.1 Introduction

Complementary metal oxide semiconductor (CMOS) field-effect transistor (FET) technology has been extensively developed since date of its invention in 1963. Success of the CMOS technology is based on constant improving of the device characteristics, fabrication technology and cost-efficiency driven by society and market demand. The dimensions of the FETs, as elementary units of the CMOS technology, are decreasing following the Moor's law[44], [45]. When the characteristic dimensions of the MOSFET have dropped down to the size of 1 micron, further miniaturization became challenging due to appearing of the short-channel effects [46], [47]. The solution for these challenges is using novel device geometries like devices with buried oxide [48], FinFETs [49], gate-all-around FETs [50] as well as NW FETs. The NW FET is the next step for miniaturization of CMOS devices.

Convenience and availability of nowadays CMOS technology makes production of CMOS-compatible electronic devices extremely favorable from the point of view of cost efficiency, device reproducibility and reliability. Therefore the idea of using FET for sensing of the gate potential has evolved into idea of sensing surface potential in electrolyte using CMOS-compatible liquid-gated FET[51]. The device developed for this purpose is an ion-sensitive field effect transistor (ISFET) and is used to sense pH of different solutions[52], [53]

2.1.2 Ion-sensitive field effect transistors as biosensors

Since its invention ISFETs have been utilized not only as pH sensor but also in a variety of applications including biosensing [54]. The basic principle of ISFET lies in replacing of a metal gate of the MOSFET by electrolyte gate. Figure 2.1 shows schematic comparison of a MOSFET and an ISFET [53]. In the case of the ISFET the drain current of the FET is defined by a potential of the electrolyte, which is in its turn defined by the reference electrode.

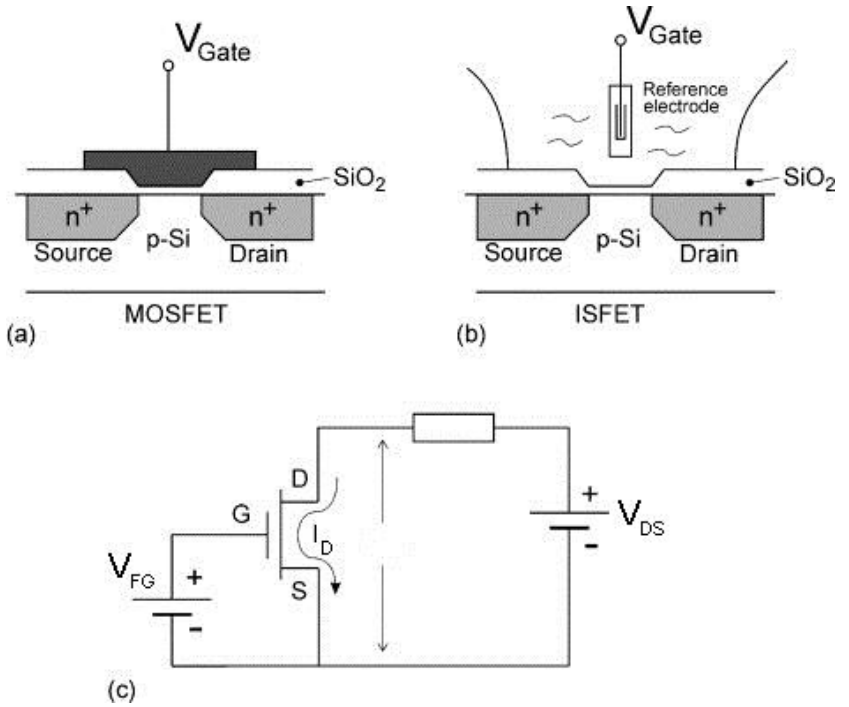

Figure 2.1 Schematic representation of (a): MOSFET, (b): ISFET and (c): electronic diagram for measurement with grounded source scheme. The figure is adapted from [53].

The drain current, I_D, in the schematic (c) of Figure 2.1 is defined in the same way for both MOSFET and ISFET in the non-saturated mode[55]:

$$I_D = C_{ox}\mu\frac{W}{L}\left[(V_{FG} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right], \tag{2.1}$$

where C_{ox} is the gate oxide capacitance per unit area, μ is the mobility of the charge carriers in the channel of the FET, W is the width of the channel, L is the length of the channel, V_{FG} is the front gate voltage, V_{DS} is the drain-source bias, V_{Th} is the threshold voltage. According to Eq. (2.1) the drain current of the FET can be changed via changing drain-source bias or the gate voltage. The gate voltage influences charge carrier distribution and concentration in the channel. If V_{FG} is higher than V_{Th}, then transistor is considered to be in an open state. At gate voltages below the threshold a diffusion current is dominating the drift component. The threshold voltage is the term, which

contains the initial surface potential (including interface potential of Si/SiO_2) needed to overcome by gate voltage to open the transistor channel. In the case of a MOSFET, V_{Th} contains difference between workfunctions of metal gate and silicon, ϕ_M and ϕ_{Si}, potential of the charges accumulated in the gate oxide, Q_{ox}, charges captured to the surface states, Q_{ss}, and charges of the space charge region, Q_{scr}, and difference between Fermi level and middle of the bandgap , $2\phi_f$ [53], [55]:

$$V_{Th} = \frac{\phi_M - \phi_{Si}}{q} + \frac{Q_{ox} + Q_{ss} + Q_{scr}}{C_{ox}} + 2\phi_f. \tag{2.2}$$

In the case of ISFET the threshold voltage also incorporates surface potential of the interface electrolyte/gate oxide and the metal workfunction is replaced by the potential of a reference electrode, E_{ref} , in the electrolyte:

$$V_{Th} = E_{ref} - \psi_0 + \chi_{sol} - \frac{\phi_{Si}}{q} + \frac{Q_{ox} + Q_{ss} + Q_{scr}}{C_{ox}} + 2\phi_f, \tag{2.3}$$

where ψ_0 is the potential generated by adsorbed ions on the surface and χ_{sol} is the surface dipole potential of a solvent. Changes of the threshold voltage leads to a shift the whole transfer curve of the transistor along the gate voltage axis. At a constant V_{FG} changing of the V_{Th} results in changes of the drain current, according to Eq. (2.1).

Surface potential of the ISFET in the electrolyte depends on quantity of adsorbed on the gate dielectric H^+ ions. Channel of an ISFET sensor is usually covered by oxides such as SiO_2, Al_2O_3 and Ta_2O_5 [52]. The surface has ion binding sites, which adsorb hydrogen ions [56].

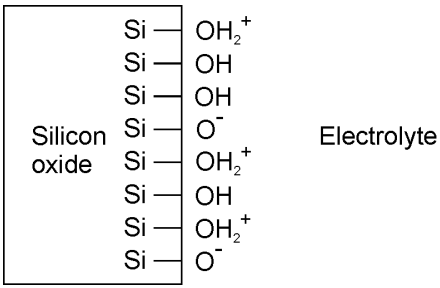

Figure 2.2 Schematic diagram of the Silicon oxide/electrolyte interface adapted from [57]

The following reactions take place at the surface of gate dielectric [58]:

$$AOH \rightleftarrows AO^- + H_s^+, \qquad AOH_2 \rightleftarrows AOH + H_s^+, \tag{2.4}$$

where A – atom of silicon (aluminum or other oxide forming element), H_S – hydrogen atoms in close vicinity to the interface. After establishing equilibrium at the interface, the reactions (2.4) run at constant reaction rate in both directions. So the equilibrium dissociation constants can be defined as:

$$K_a = \frac{[AO^-][H_s^+]}{[AOH]} \; and \; K_b = \frac{[AOH_2]}{[AOH][H_s^+]}, \tag{2.5}$$

where square brackets are used to define concentrations of ions or compounds. After reaching the equilibrium state also an equilibrium surface potential will be established. It is determined by surface concentration of the hydrogen atoms, $[H_s^+]$, which in its turn is defined by the concentration of the hydrogen ions in the bulk of the electrolyte[59]:

$$[H_s^+] = [H^+]e^{-\frac{q\psi_0}{kT}}, \tag{2.6}$$

where q – is the elementary charge, ψ_0 – is the potential of the interface dielectric/electrolyte, k – is the Boltzmann constant, T – is the temperature in Kelvin. As it can be seen from Eq. (2.6), concentration of the of the hydrogen ions on the surface is related to the bulk concentration of hydrogen ions through the surface potential. Thus, taking into account the conservation of quantity of binding sites N_S:

$$N_S = [AOH] + [AO^-] + [AOH_2^+] \tag{2.7}$$

and the charge per unit area σ_0:

$$\sigma_0 = q([AOH_2^+] - [AO^-]), \tag{2.8}$$

one can obtain a relation between interface potential and pH of the solution[51]:

$$\psi_0 = \left(2.303\frac{kT}{q}\right)\left(\frac{\beta}{\beta+1}\right)(pH_{pzc} - pH), \tag{2.9}$$

where pH_{pzc} is the pH value at which the point of zero charge is reached and β is a dimensionless sensitivity coefficient:

$$\beta = \frac{q^2 N_s \delta}{C_{eq} kT}, \tag{2.10}$$

where $\delta = 2\,(K_a K_b)^{\frac{1}{2}}$, C_{eq} is the equivalent capacitance of the interface adopted from Gouy-Chapman-Stern theory for double layer. The equation (2.9) reflects the sensitivity of the surface potential to the pH of the electrolyte solution. As we can see from Eq. (2.3) ψ_0 is included to the threshold voltage of an ISFET and therefore changes of ψ_0 lead to changes of the V_{Th}, which can be detected by shift of the ISFET transfer curves. Using Eq. (2.9) a maximum sensitivity of the surface potential to the pH can be estimated. It equals 59 mV/pH and is called a Nernstian limit [51]. This limitation has fundamental origin. Nevertheless, there are publications revealing supernernstian behavior of some surfaces and devices[60], [61]. However, such a behavior can be explained in a way, which does not violate the Nernstian rule.

Equations (2.6) and (2.9) demonstrate that concentration of adsorbed hydrogen ions on the surface of the gate dielectric is defined by the bulk concentration of ions and determines a surface potential of the gate dielectric. The theory of the pH sensitive ISFET considers only binding of the simplest ions to the surface of the transistor, because binding of other heavier ions is less probable then adsorption of H^+. At the same time, modification of the transistor surface with specific chemistry can make the adsorption ion-specific [62], [63] and thus enable detection of various species like DNA, proteins, antibodies[54], [57]. Such a modification combined with field effect sensing makes a background for fabrication of field-effect based biosensor. However, demand of modern biology and biomedicine in sensitivity and spatial resolution requires downscaling of the transducer down to submicron sizes and even to nanometer scale[8], [64]. Increasing sensitivity of the sensors is usually achieved by increasing resolution of measuring changes of the ψ_0[41], [42], [65], because sensitivity of ψ_0 to the ion concentration is limited by the nernstian rule. One of the possible ways to increase the charge sensitivity of the devices is using novel confined geometries like Si NW FETs[66].

2.1.3 Silicon nanowire FET biosensors.

Silicon nanowire FET biosensors have emerged as a next step of miniaturization of an ISFET[11], [67] due to enhanced sensitivity[68] and spatial resolution[69] provided by small size and high surface-to-volume ratio. The first nanowire structures were used for detection of ionic composition of the electrolyte [70], biomolecules[71] and biomarkers[15]. They show higher

charge sensitivity than bulk ISFETs. Figure 2.1 demonstrates a schematic representation of NW FET biosensor. The surface of the NW is often covered with (3-Aminopropyl)triethoxysilane (APTES) in order to provide protection of Si NW surface and possibility for further selective modification of the NW gate[70].

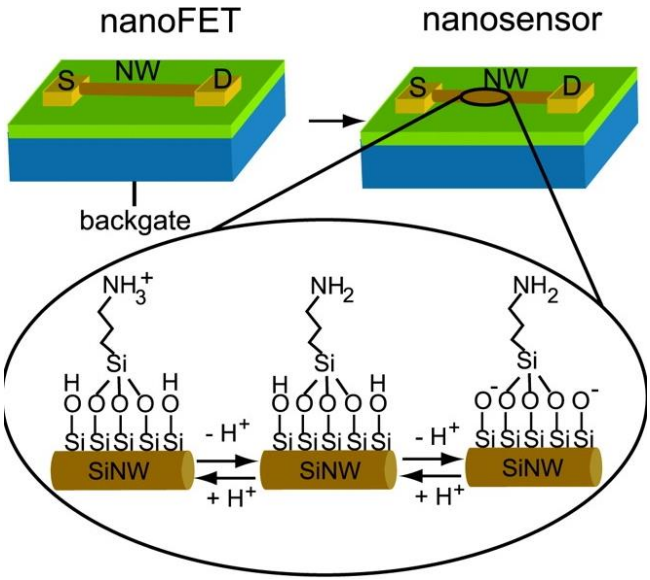

Figure 2.3 Schematic image of Si NW FET with the sketch of the NW pH sensing after silanization procedure. The figure is adapted from [70].

The first attempts of fabrication of Si NW FET biosensors have demonstrated proof of principle of biomolecule detection[72]. However, the nanowire biosensors were first fabricated using a “bottom-up” approach. In this case he Si NWs are usually fabricated by means of chemical vapor deposition or using wet chemistry and then they are contacted[73]. This approach has advantage of cost-efficiency and high crystalline quality of the produced NWs provided by self-organized silicon nanowire growth. On the other hand fabrication of bottom-up nanowires requires additional attention to be drawn to achieve uniformity of the size distribution[74] as well as steps for integration of the NWs with CMOS circuitry and assembling them in desired direction[75], [76]. Alternative way of fabrication is entirely based on the CMOS technology and is called “top-down” approach [73], when the NW structures are patterned on the silicon substrate using

lithographic procedures like e-beam lithography or deep UV lithography. This method is more expensive than the bottom-up production, but it provides highly reliable and reproducible devices, which are easy to integrate and scale down[77]. Effective detection of biomolecules has also been demonstrated using Si NW FETs produced by top-down approach[14], [78]. Moreover the power of CMOS downscaling and integration has been used for development of ultimate commercial device for full sequencing of 20-basepair DNA based on Si NW FETs[79].

In presented work we have chosen the top-down approach in order to have full control of the nanowire dimensions and achieve highly reproducible devices.

The schematic illustration of the Si NW FET fabricated using top-down approach is shown on Figure 2.4. The NW is passivated with thin oxide layer (typically from 5 to tens of nanometers) and then exposed to an electrolyte solution. Contact regions are protected from liquid using organic materials like polydimethylsiloxane (PDMS) and/or photoresists like SU8 or PI2545. In order to achieve ohmic contact between NW and metal contact pads, outer regions of the NW are heavily implanted[55].

For the electric measurements NW FETs are usually connected in the grounded source configuration as it is shown in Figure 2.4. The drain voltage, V_{DS}, as well as front-gate voltage, V_{FG}, and back-gate voltage, V_{BG}, are set against the source, which is connected to the ground. Front gate voltage is applied using Ag/AgCl reference electrode. Reference electrode can be integrated directly on the chip[80] or it can be realized in form of reference FET sensor, which serves as a reference for determining all potentials in the system [81]. The back gate voltage can be used to tune the NW's threshold voltage and the operation mode[82] as well as for increasing sensitivity of the device [40]. Electrical transport characteristics of Si NW FETs can be qualitatively described in the frame of classical model of a MOSFET[55] (see Eq. (2.1)) with small amendments. If we consider a linear mode, when the transistor is operated at a relatively small V_{DS}, the Eq. (2.1)will be simplified to:

$$I_D = C_{ox}\mu\frac{W}{L}(V_{FG} - V_{Th})V_{DS}. \tag{2.11}$$

Eq. (2.11) is similar to the basic definition of the drift current:

$$I_D = nevS = \frac{N}{WLH}e\mu E_{DS}WH = eN\mu\frac{V_{DS}}{L^2} = \frac{eN}{L}\mu\frac{V_{DS}}{L}, \tag{2.12}$$

where n – is the carrier concentration, H – is the channel height, E_{DS} – is the drift electric field, N is the quantity of charge carriers, e – is the elementary charge. Now if we compare Eq. (2.12) and (2.11) we can see that $C_{ox}W(V_{FG} - V_{Th})$ represents quantity of carriers in the channel per unit length attracted by the gate voltage, V_{DS}/L represents the electric field between source and drain electrodes.

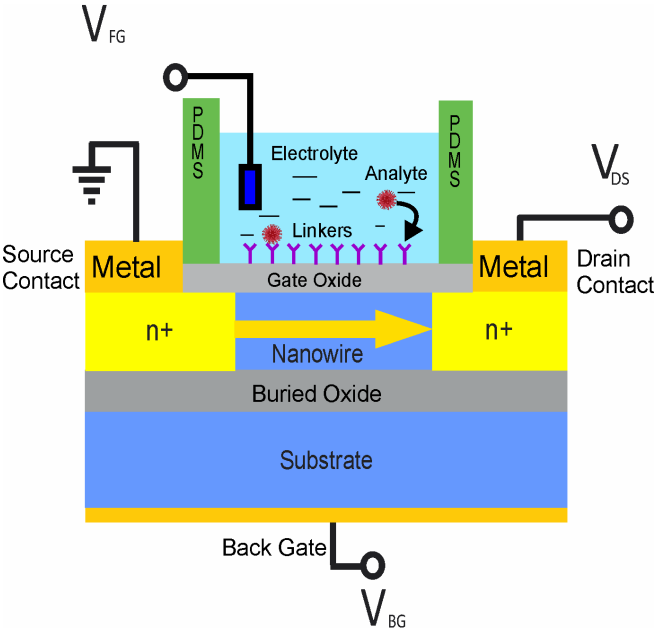

Figure 2.4 Sketch of the liquid-gated Si NW FET (the side view). The image represents Si NW with contact regions implanted with As atoms. The schema illustrates electric connection of the Si NW FET in the grounded source configuration.

Linear mode of operation can be used to characterize the device transport properties such as channel mobility and concentration of the carriers in the channel. Figure 2.5 shows typical output and transfer characteristics of Si NW array FET, measured in a configuration from Figure 2.4. The devices characterized in Figure 2.5 were fabricated in the frame of present work and represent Si NW FETs based on array of 50 NWs connected in parallel in order to improve signal-to-noise ratio and preserve nanostructured surface. Linear mode of the transistor can be observed in Figure 2.5(A) from V_{DS}=0 V, to 0.5 V for most of the front gate voltages. Transistor channel can be treated as a

resistor in the linear mode, whereas at higher drain voltages it reaches the saturated mode, when drain current is almost independent of the drain voltage due to channel pinch-off[55]. Figure 2.5(B) demonstrates transfer characteristics of the Si NW FET. The changes of gate voltage are translated into changes of drain current. The threshold voltage of this device is calculated using Eq. (2.11) and is equal 0.88 V.

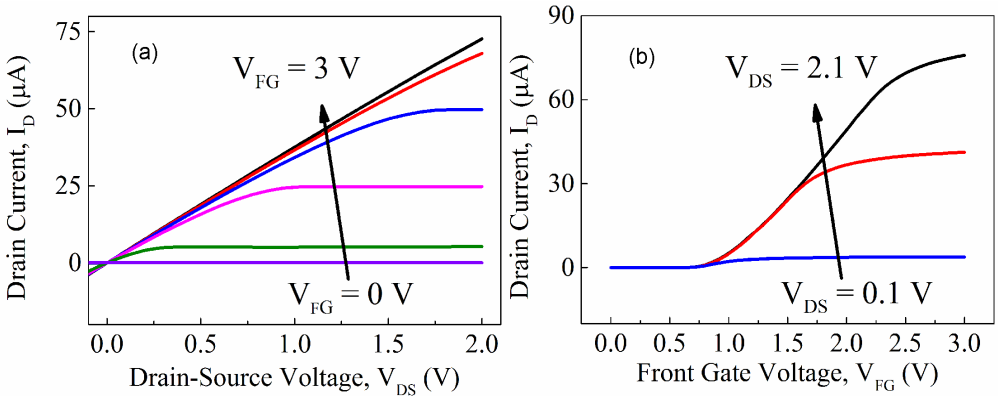

Figure 2.5 I-V characteristics of liquid-gated Si NW array FET (channel length of 6μm, width of 250 nm, device consists of 50 NWs connected in parallel) with As doped contact regions. (A): Output characteristics, (B) Transfer characteristics.

One of the main characteristics of a transistor is the transconductance, g_m, which is the measure of the gate control over the drain current.

$$g_m \equiv \frac{\partial I_D}{\partial V_{FG}}\bigg|_{V_{DS}=const} = \frac{W}{L}\mu C_{ox} V_{DS}. \qquad (2.13)$$

As we can see from Eq. (2.13) and Figure 2.5(B), the g_m is proportional to the drain voltage of the transistor. Therefore, the real sensor measurements are usually carried out in the saturation mode of the transistor at possibly higher drain biases, to get maximal level of the transconductance. However, the channel noise should be also taken into account when choosing a working point for measurements. As it has been discussed above, characterization of the transistor is usually done at low drain biases in order to simplify the data extraction and provide quasistatic conditions for carriers in the channel. For example, it is possible to estimate mobility and concentration of the carriers in the channel using Eq. (2.13) and the Eq.(2.12):

$$\mu = \frac{g_m L}{W C_{ox} V_{DS}} \tag{2.14}$$

$$n = \frac{I_D C_{ox}}{q g_m H} \tag{2.15}$$

where H – is the height of the NW channel channel. It should be noted, that this FET model does not consider carrier distribution in the channel, but it is still suitable for estimations. Role of carrier distribution in the channel is considered in [83]. The classical prediction describes macroscopic characteristics of Si NW FETs until very small sizes (down to characteristic size of 20 nm in all directions). Beyond this limit a quantum behavior of the NW structures can be observed[84]–[86] even at room temperature.

One of the potential problems for estimation of the values from Eq. (2.14) and (2.15) is evaluation of the gate capacitance per unit area, C_{ox}, which in case of complicated geometries like gate-all-around transistors and low dimensional structures deviates from the well-known plain capacitor equation. The violations of the parallel-plate capacitor model can already occur at submicron scale of the transistors. The most efficient way to consider this problem is performing an experimental measurement of the gate capacitance. The measurement of gate capacitance of germanium NW FETs has been reported in [87]. However, such an approach requires sophisticated measurement technique in order to recover capacitance values far below parasitic capacitance of the cabling. Alternative to this approach may be using coupling of back and front gate of the Si NW FET in order to evaluate the front gate capacitance[88].

As we have discussed above, selectivity of the NW FETs is achieved by chemical functionalization of the NW surface[89]. The wires are covered with a layer of molecules, which will selectively adsorb analyte molecules from the solution[90]. An examples of such specific surface chemistry are single-stranded DNA[79], antibodies[12], [14] and emerging aptamers[91]. Working principle of functionalized NW FET sensors is similar to what we have shown for the case of an ISFET and different pH of the electrolyte gate solution. Adsorption of the analyte molecule onto the linker molecule results in changes of the surface potential, which can be registered in the channel by changes of the drain current or other parameters[92]. Linker molecules are usually connected to the gate dielectric of the sensor through an intermediate layer of organic

molecules, which have on one side chemical affinity to the material of the gate (silicon oxide or other oxides, silicon) and on the other side organic or inorganic radical, which simplifies binding to the linker molecules. There are several approaches of Si NW FETs functionalization: direct functionalization of silicon surface with polymer brush of alkyl-ended molecules[93]–[97]; functionalization of the gate oxide with silane containing organic compounds[98], [99]; covering the surface of the sensor with a selective membrane, which translates selective chemical adsorption into changes of the pH at the surface of the NW[100]. In the case of chemical modification of the NW, it is important that organic molecules of the functionalization layer form a dense layer on the surface of the sensor, because uncovered places of the sensor can give false contribution to the signal due to unspecific adsorption. Besides, imperfections of the polymer brush in case of alkylation of silicon surface directly lead to the gate leakage and thus sensor failure. All of the discussed approaches of Si NW functionalization have their advantages and disadvantages, which may be favorable for different applications.

Silicon nanowire field effect transistors are promising structures for monitoring the activity of living cells, particularly electrogenic cells like neurons[101], [102] and heart cells[103]. The state of a single cell or cell system can be monitored by either their metabolic products (in the case of the chemical synapse - neurotransmitter) or extracellular potential measurements. Bio chemical sensing requires much effort on functionalization of the sensor surface for selective detection of the substances produced by the cells. For investigation of the electrogenic cells activity (e.g. neuronal cells) one can utilize their specific features like generating of spontaneous or triggered action potentials and measure shifts of the cell membrane extracellular potential. The activity of a neuron leads to ionic- and displacement currents flowing through the cell membrane, resulting in an extracellular voltage drop along the cleft between the cell membrane and the gate insulator of the ion sensitive FET that modulates its drain current[33].

The detection of electrical signal from neuronal cells has been demonstrated using traditional FET technique [28]. However, planar FET technique cannot entirely monitor the different complex processes taking place in the system FET/ neuronal cell in the transistor signal. The main reason for this is low spatial resolution. In addition, the cleft between silicon oxide passivated surface and the neuronal cell is about 40 nm [34] which is 4 times larger than Debye screening length in physiological solution (about 10 nm). Distance between cell and surface of the detection spot determines the value of so called seal resistance R_{seal} (will be discussed in more later

on), which is a measure for leakage of the useful signal to the bulk electrolyte. That's why in the case of a planar FET the signal outcome from the cell may be determined not by direct transfer of the membrane potential but by the fluxes of ions, which accompany repolarization of the cell and influence the surface potential of the gate dielectric. The cells have to be cultured in a stable way onto the FETs and the interface between them and the gate dielectric should be improved. The cleft between neuronal cell and the sensor surface can be shrunk down to 4nm using Si NW FETs. This was confirmed in first studies related to the topic [30], [36] on nanowires produced using bottom-up process. However, as it was discussed above, the bottom-up processed nanowires grown by chemical vapor deposition are cheap and easy to produce, but these wires have irreproducible sizes and may experience complications with integration. The top-down produced Si NWs for neuronal cell interfacing are still under development[101]. The main challenges are signal-to-noise ratio of Si NW FETs and stability in liquid environment during at least 10 days in vitro.

2.1.4 Signal-to-noise ratio in silicon NW FETs

Silicon NW FET based biosensors represent a big step forward in development of modern biomedicine and biology. However, there are still the challenges remaining to achieve highly sensitive, reliable and reproducible operation. The important milestone of the research in the area of FET sensors is the signal-to-noise ratio (SNR), which determines the detection limit of a sensor [9], [37], [104]. SNR is defined as a relation between useful signal and fluctuations of the device parameters. When we are registering changes of the Si NW FET current, than the registered change will contain component corresponding to the useful signal, δI_S, and as well component corresponding to the channel current fluctuations δI_{fl}:

$$\delta I = \delta I_S + \delta I_{fl}. \tag{2.16}$$

Then, by definition, the SNR will be:

$$SNR \equiv \frac{\delta I_S}{\delta I_{fl}}. \tag{2.17}$$

It is always advantageous if biosensors detect in real time discrete events, such as binding of the biological objects to the surface or action potentials of an electrogenic cell. Therefore, in a wide range of applications, Si NW FET biosensors have to provide real-time detection of the analyzed

events. In this case, averaging techniques, which usually operate with mean values and are used to suppress noise, are not applicable and the SNR of the raw output from the sensor should be higher than one. Implementing such strong requirements might be a rather challenging task because biosensors are often dealing with extremely small signals, such as monitoring tiny changes of concentration of the analyte or extracellular recordings from a single cell. Therefore, understanding the factors having an impact on the SNR is of crucial importance for developing reliable biosensors with sufficient sensitivity.

Real signals in biological environments are usually extremely small (in the range of tens of microvolts), and hence after a measurement the value of δI_S, generated by the analyte may be below the level of channel noise. Therefore instead of Eq. (2.17), where we compare the response of the NW channel current to the intrinsic noise of the device, it is more suitable to use a relation between input signal δV_{FG} and the level of equivalent input noise δV_{fl} (the effective fluctuation of gate voltage potential, which causes corresponding fluctuation of the channel current δI_{fl}). The aforementioned can be realized by multiplying the numerator and denominator of Eq. (2.17) by g_m:

$$SNR = \frac{\delta I_S}{\delta I_{fl}} = \frac{\delta I_S \, g_m}{\delta I_{fl} \, g_m} = \frac{\delta V_{FG}}{\delta V_{fl}}. \tag{2.18}$$

The biosensor signals are usually detected in the low frequency range of spectra. For example, extracellular measurements of action potentials from neuronal cells[28] require detection of signals with average duration about 3 ms, whose principle components are, on average, not faster than 10 kHz. Therefore the signal from sensor δI is often filtered to the frequency range of the input signal in order to remove unnecessary high-frequency fluctuations. In this respect it is more convenient to switch to the spectral representation of the equivalent input noise in Eq.(2.18):

$$SNR = \frac{\delta \mathrm{V_{FG}}}{\sqrt{\int_{f_1}^{f_2} S_u df}} = \delta \mathrm{V_{FG}} \frac{g_m}{\sqrt{\int_{f_1}^{f_2} S_I df}}, \tag{2.19}$$

where S_I is the drain current spectral density and S_u is the equivalent input voltage spectral density. The lower is the value of S_u , the higher is the SNR.

According to Eq. (2.19) the improvement of the SNR can be realized by finding conditions with the lowest equivalent input noise. Therefore the SNR can be improved by optimization of the fabrication technology [38], [39], to obtain low-noise devices due to high quality of the device

interfaces, and by finding the appropriate transport regimes to maximize the sensitivity. However, to date there remain important challenges in establishing the optimal transistor operation modes for biosensing. Currently, two main concepts are considered for optimization of sensitivity: using the subthreshold mode[105] or above-threshold mode[41]. In the present work we will answer these questions and demonstrate that using each of the modes is advantageous in different applications[40]. Optimization of the sensor structures using chemical wet etching during NW fabrication as well as finding of the optimal regime for low-noise of the NW operation is considered.

Described challenges of the NW biosensing require comprehensive investigation of Si NW FET transport properties as well as the factors having impact on it. Analysis of the current fluctuations in liquid-gated NW FETs combined with data of their I-V characterization derives information about noise sources in the device as well as ways to optimize performance of the sensor. Such an analysis of transport is based on noise spectroscopy, a technique for characterizing the dynamic properties of the investigated structure. In the next section we are going to discuss background of noise spectroscopy in FET devices.

2.2 Noise Spectroscopy

2.2.1 Introduction

Noise spectroscopy provides analysis of the device performance and structure by studying the fluctuation phenomena. The method itself is very convenient for the extraction of information about the origin of noise in the sample. Noise spectroscopy can be used for the analysis of the device quality, transport properties and improvement of the technology, which is one of the main directions for the development of advanced NW FETs and miniaturization of the CMOS elementary base. A lot of publications are devoted to analysis of fluctuation phenomena in Si NW FETs [41], [66], [106], [107], because the major point of the biosensor performance optimization is improving signal-to-noise ratio. Historically Si NW FET biosensors evolved from regular MOSFET structures. Most of knowledge in the sphere of noise spectroscopy for submicron MOSFET structures is eligible for NW biosensors as well. For example, it has been shown that presence of the electrolyte as a front-gate of a FET biosensor (BioFET) does not influence noise properties of the structure [41]. Therefore we are going to use experience and understanding of

noise in MOSFETs, as it was accumulated over the years of existence of the CMOS technology [108]–[110]. In this section we will consider main noise sources of Si NW transistor.

2.2.2 Spectral density

Drain current of a FET under stationary conditions contains a fluctuation component, i_n, which is changing in time:

$$I(t) = \bar{I} + i_n(t). \tag{2.20}$$

Function $i_n(t)$ is a random value and therefore a mean value of current cannot be used for analysis of the fluctuation, because $i_n(t)$ gives zero after averaging. The value of mean-square deviation (MSD) is usually used for analysis of the fluctuations:

$$< i_n^2(t) > = \lim_{T\to\infty} \frac{1}{T} \int_0^T i_n^2(t)dt. \tag{2.21}$$

This value gives an idea about the measurement precision and the level of the fluctuations in a biosensor measurement. Practically MSD is the value, which can be used in the denominator of the signal-to-noise ratio of a FET, if we take a root square of it (root mean-square deviation (RMSD)). However, the MSD value is not enough for quantitative analysis of the fluctuation processes. For these purposes a frequency representation of MSD is used – spectral density of fluctuations.

$$\int_{-\infty}^{+\infty} |x(t)|^2 \, dt = \frac{1}{2\pi} \int_{-\infty}^{+\infty} |\hat{x}(\omega)|^2 d\omega, \tag{2.22}$$

where *x(t)* – is some fluctuating value. Any physical quantity can accounted as *x(t)*, it can be current, voltage, power or even a resistance of the sample. Spectral density of *x(t)* is denoted by S_x is calculated from time trace of *x* as follows:

$$S_x(\omega) = |\hat{x}(\omega)|^2 = \left| \int_{-\infty}^{+\infty} x(t) e^{-i\omega t} dt \right|^2. \tag{2.23}$$

Spectral density is an additive value. If fluctuations of the sample current have different origin and do not correlate between each other, then the resulting spectral density will be a superposition of spectral densities of each type of noise. Spectral density of voltage fluctuations can be recalculated into spectral density of current fluctuations using Ohm's law:

$$S_I = \frac{S_V}{R^2}, \tag{2.24}$$

where R – is the differential resistance of the sample and circuitry. Eq. (2.24) is very important in measurements of noise, because it allows recalculating desired values by only one measured value: S_I in case of current amplifier and S_V in case of voltage amplifier.

As we have already discussed, sensitivity of Si NW FET biosensors is a hot topic and there is a number of publications in this direction [38], [106], [111]. However, there are still challenges of finding optimal device geometry and operation mode. In the next subsection we will consider typical sources of noise in Si NW FETs. Many of these noise sources are discussed in literature for the case of planar MOSFET and submicron MOSFET [107], [110], [112]–[115].

2.2.3 Main sources of noise in Si NW FET

One of the most important and well-known types of noise is the thermal noise or so called Johnson-Nyquist noise. Thermal noise is present in all objects, which can be characterized with some electrical resistance, which is in thermodynamic equilibrium with its environment. Depending on the schematic of the device connection (open circuit or a shortcut) the thermal noise appears as fluctuations of voltage on the ends of circuit or as fluctuations of current through the sample. Thermal noise has first been observed independently by Johnson[116] and Nyquist[117] in 1928. Using measurements of thermal noise Johnson managed to estimate Boltzmann constant with significant accuracy.

Electrons and holes in a semiconductor have thermal energy and are constantly expressing random thermal motion. The events of scattering on lattice, when carriers can either loose or gain energy due to interaction with lattice atoms, occur randomly and on average compensate each other in the state of thermodynamic equilibrium. Such random motions cause fluctuations of carrier concentration on the terminals of the sample, which result in thermal fluctuations of current or voltage in the circuit. Spectral density of thermal noise is not frequency dependent in a broad frequency range and can be calculated as follows:

$$S_v = 4kTR, \tag{2.25}$$

where k – is the Boltzmann constant, R – sample resistance, T – temperature of the sample. Resistance of the sample, as well as temperature can be precisely measured using measurement of level of the thermal noise. It should be noted, that spectral density of the current will be inverse proportional to the resistance according to Eq. (2.24).

$$S_I = \frac{4kT}{R}. \tag{2.26}$$

According to Eq. (2.25) and (2.26) we can conclude that high-ohmic samples should be measured using current amplifier, whereas measurements of noise in the low-resistance samples is more efficient with voltage amplifier.

As it has been mentioned in subsection 2.1.4, in the case of signal from a biosensor, we are mostly interested in the low-frequency range of spectra (up to 10 kHz). In this frequency region thermal noise is more often dominated by other types of noise like generation-recombination or flicker noise. However if the FET is in the subthreshold mode, which might be considered as optimal in some kinds of experiments [105], the thermal noise can be the major factor, defining voltage spectral density of the investigated sample.

Another type of frequency independent noise is the shot noise [118]. First this noise was described by Schottky in 1918 [119], when he registered this type of noise in the valve diodes. The shot noise appears in the samples, in which the charge carriers should overcome some potential barrier in order to contribute to electric current. The classical examples of such devices are a p-n junction and a Schottky barrier (contact metal-semiconductor). These fluctuations originate from the discreteness of the charge carriers in the current. Discrete charge carriers are randomly passing the potential barrier. As the result current in the sample can be written as a sum of short pulses, where each pulse represents single carrier passing a potential barrier:

$$i(t) = -q\sum_{k=1}^{K}\delta(t - t_k), \tag{2.27}$$

where q – is the elementary charge, t_k – moment of crossing a barrier by a k-th carrier, and K – number of all pulses. Spectral density of this noise is proportional to the current value:

$$S_I = |2qI|. \tag{2.28}$$

As we can see, this type of noise is "white" as the thermal noise. The situation when shot noise is observed in a MOSFET happens not quite often at room temperatures. Usually it is dominated by thermal noise as well as by other components. Shot noise may appear in a FET structure as a sign of non-ohmic contacts of the device or gate leakage current. Also FETs demonstrate shot noise in a subthreshold mode[120]. In the above threshold mode of the FET sensor, where most of the biosensing experiments take place, white noise is usually dominated by low-frequency excess noise components such as generation-recombination or flicker noise (1/f) components.

Generation-recombination (GR) noise is introduced and named after corresponding dynamic processes in a semiconductor. The main origins of this type of noise are generation and recombination of charge carriers. The GR noise can be caused by following processes in the channel of the NW FET:

- Band-to-band generation and recombination
- Exchange of the carriers with shallow levels in the bandgap
- Generation-recombination of the carriers through deep levels
- Exchange processes with traps in the gate dielectric

Characteristics of GR noise contain information about the process, which caused this noise: characteristic time, depth of the level, capture cross-section [121]. Therefore, investigation of the GR component plays an important role in localizing and charactering the defects in semiconductor structures. Spectral density of the GR noise has a lorentzian shape with time constant, which corresponds to the relaxation time of the GR process:

$$S_I(\omega) = \frac{S_I(0)}{1 + \omega^2\tau^2}, \tag{2.29}$$

where $S_I(0)$ – is the value of a plateau of the Lorentzian. $S_I(0)$ is usually related to concentration of the carriers and recombination centers, which take part in the GR process [121], [122], τ – is the time constant of a process. GR noise in MOSFETs as well as in NW FETs is investigated in a number of publications and books, because it can have different nature and contains information about intrinsic device structure [121], [123]–[125].

Another type of the low-frequency noise is the well-known flicker noise or 1/f noise. The most general definition of this type of noise introduces the flicker noise as a fluctuation of the material conductance with spectral density close to the inverse proportion to the frequency[126]:

$$S_I \sim \frac{I^{\beta}}{f^{\gamma}}, \tag{2.30}$$

where f – is the frequency, γ – index close to 1, and β – is the index close to 2. The reason for such a general definition comes from a complex nature of the flicker noise. Flicker noise exists in many different systems and its origin still causes debates in scientific society. A lot of work has been devoted to the nature of flicker noise in MOSFETs [38], [108], [125], [127], [128]. Nowadays the three main models for flicker noise in semiconductors are considered: mobility fluctuations model[129], number fluctuation model[127] and the number and correlated mobility fluctuation model[130], which includes both approaches. We will not speak here about more fundamental mechanisms of flicker noise like dielectric polarization noise [131] or quantum 1/f noise [132], because in FET structures these components are usually hidden by more powerful mechanisms like mentioned above. However, it should be noted that it is possible to register dielectric polarization noise of the gate dielectric in 0D ISFET structures [133].

One of the first explanations of the flicker noise is the mobility fluctuations model. In 1969 Hooge proposed an empirical equation for description of the 1/f noise in homogenous samples[134]:

$$\frac{S_I}{I^2} = \frac{1}{N}\frac{\alpha_H}{f}, \tag{2.31}$$

where I – is the current through the sample, N – is the quantity of charge carriers in the sample, f – frequency, α_H – empirical constant, which is nowadays named after Hooge and is usually about $2\text{x}10^{-3}$. However it has been shown later, that the value of α_H can vary[108] from 10^{-4}-10^{-6} for high-quality samples without defects to much higher than $2\text{x}10^{-3}$ for the samples with higher concentration of the defects. Hooge's model explains empirical equation (2.31) as a result of the mobility fluctuations of charge carriers. Hooge's constant is dimensionless value, which allows comparing levels of noise in different devices and materials, regardless from nature of the objects.

An alternative model is interpreting of flicker noise as a superposition of number generation-recombination processes with time constant distributed by some rule. In 1955

McWhorter[135] considered a model, which describes many traps with spatial and energy distribution inside the semiconductor contributing to overall noise by their GR processes. Further, the McWhorter model was adopted for the case of MOSFETs [108], [136], [137] including the fact that most of the exchange processes take place between charge carriers of the channel and traps in the gate dielectric. The model assumes that the traps are spatially and energetically equally distributed in the gate dielectric. The spatial and energy distribution of the traps results in distribution of the probabilities for the carriers being captured onto the traps. Overall sum of the contributions from all of the traps gives the 1/f behavior of the spectral density. The concentration of the traps defines the level of the flicker noise [138]:

$$S_{V_{FB}} = \frac{q^2 kT\lambda N_t}{WLC_{ox}^2 f}, \tag{2.32}$$

where N_t – is the concentration of the traps distributed by the energy in [cm^{-3}eV^{-1}], λ – is the inverse tunneling depth (about 0.1 nm) of the carrier into the gate dielectric:

$$\lambda = \frac{\hbar}{\sqrt{2m^*\phi_b}}, \tag{2.33}$$

where ħ – is the Planck's constant, m^* – is the effective mass of the carrier, ϕ_b – is the height of the potential barrier between semiconductor and the gate dielectric. In the case of McWhorter model the spectral density of fluctuation of the flat band voltage is equal to the equivalent input noise [114]:

$$S_{V_{FB}} \approx S_U = \frac{S_I}{g_m^2} \tag{2.34}$$

where g_m – is the transconductance of the transistor (Eq. (2.13)), S_U – is the equivalent input noise of the transistor, V_{FB}.

Both McWhorter and Hooge models are combined in the model of number and correlated mobility fluctuations (ΔN – Δμ) [130], where both fluctuations of the mobility and the quantity of channel carriers are considered. Fluctuations of the drain current can be written in a form of exact differential[114]:

$$\delta I_d = \frac{\partial I_d}{\partial V_{FB}}\Big|_{\mu=const} \delta V_{FB} + \frac{\partial I_d}{\partial \mu}\Big|_{V_{FB}=const} \delta\mu, \tag{2.35}$$

$$\delta I_d = g_m \delta V_{FB} \mp \alpha I_d \mu \delta Q_{ss}, \tag{2.36}$$

where δQ_{ss} – is the fluctuation of the surface state charges, α – is the parameter, which reflects sensitivity of the mobility to the surface state charges[139]. Eq. (2.36) contains relation between fluctuations of the flat band voltage fluctuations and current fluctuations. If we switch to the frequency representation:

$$\frac{S_I}{I^2} = \left(1 \pm \alpha\mu C_{ox} \frac{I_d}{g_m}\right)^2 \frac{g_m^2}{I^2} S_{V_{FB}}. \tag{2.37}$$

Dividing of the Eq. (2.37) by square transconductance allows switching to the value of equivalent input noise, which can be measured experimentally:

$$S_U = \left(1 \pm \alpha\mu C_{ox} \frac{I_d}{g_m}\right)^2 S_{v_{FB}}. \tag{2.38}$$

Depending on the quality of the structures and the conductance type the parameter α can be close to 0 as well as significantly large (up to 10^4 V s/C [139]). Its value determines role of the mobility fluctuations in the overall 1/f noise.

Usually under the conditions of real experiment, the flicker noise component of the spectra is measured as a function of different parameters like V_{FG}, V_{BG}, V_{DS}. Often there is a question in interpretation of the flicker noise origin, finding a proper model for its description in case of particular experiment. The information about the most appropriate description of 1/f noise may be extracted from dependence of the flicker noise on the carrier concentration in the channel, front and back gate voltages[127]. In case of the volume noise (Hooge model) equivalent input noise is changing in the proportionally to the gate voltage, whereas in the case of McWhorter model S_u is independent of the gate voltage. Applicability of the correlated model is usually verified by plotting dependence of the normalized current spectral density, $\frac{S_I}{I^2}$, as a function of $\frac{g_m^2}{I^2}$. If the dependence reflects proportionality, then according to (2.37) the model is applicable. However, with downscaling of the NW devices the flicker noise characteristics may deviate from the predicted nature due to discrete nature of the traps in the gate dielectric.

Miniaturization of the silicon devices, particularly NWs, leads to decreasing the effective gate surface area. For the case of the flicker noise generated by processes of carrier exchange with the gate dielectric, the decreasing the gate area leads to decreasing the amount of traps, which take part in the exchange processes. As it is shown in [140], miniaturization of the FET devices results in the breakdown of the 1/f dependence into superposition of lorentzian-shaped components. Further device miniaturization (down to the channel of submicron dimensions) may lead to a critical area of the gate, when only a single trap in the gate dielectric or channel influences the channel current. In such a case, we may observe switching of the current between two discrete levels, corresponding to the state with the occupied and unoccupied trap. Such type of noise is called random telegraph signal (RTS) noise, because it has two-level fluctuation of the device current (for example see Figure 2.6). Probability of the carriers being captured and released from a single trap is characterized by average capture and emission times, $<\tau_c>$ and $<\tau_e>$ (Figure 2.6). The probability of a carrier capture is $1/\tau_c$ and the probability of carrier emission is $1/\tau_e$. A behavior of the capture and emission times in the case of a single trap is generally described by Shockley-Read-Hall (SRH) dynamics[140]. In this respect capture and emission times can be represented as:

$$\tau_c = \frac{1}{\sigma n v_{th}} \; and \; \tau_e = \frac{1}{\sigma n_1 v_{th}}, \tag{2.39}$$

where σ – is the capture cross section of the trap, n – is the carrier concentration, v_{th} - is the thermal velocity of the carriers, n_1 – is the Shockley-Read-Hall factor of the trap occupancy, which equals concentration of the free carriers in the channel, when Fermi level coincides with the level of the trap. In fact the trap can be situated anywhere in the channel or in the gate dielectric. In the case of the gate dielectric the concentration of the carriers, *n,* should be considered taking into account tunneling of the carriers to the trap[141]. The tunneling drastically decreases the concentration of the carriers in close vicinity of the trap. According to (2.39) increasing of the capture time and thus decreasing of the capture probability. In addition, there are effects related to the fact that a trap may change its energy and capture cross-section after capturing a charge carrier. These effects are described in frame of the Coulomb blockade energy concept[142]–[144]. If the trap is located near the drain of the NW it may considerably modulate the channel conductivity [145].

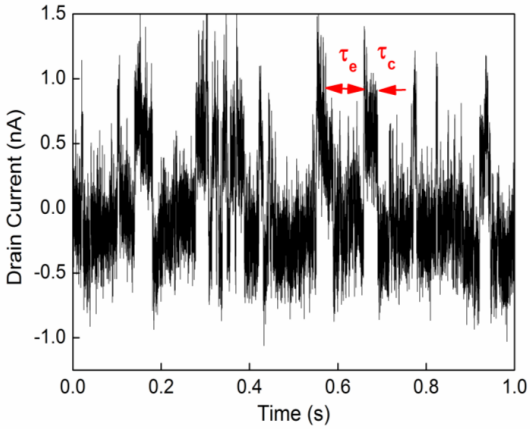

Figure 2.6 Example of a drain current time trace containing RTS fluctuations. Red arrows indicate capture and emission time of the process.

The RTS noise is generally an unwanted effect because it introduces a two- or more levels of the current, between which the drain current is randomly switching. Such a noise may hinder the useful signal in case of real-time biomolecules detection or in the case of extracellular investigation of neuronal cells. However, the useful signal can be distinguished from the RTS noise by the histogram of the time trace. RTS noise is a non-Gaussian process because of switching between two or more levels of current, but the value of current at each of the levels is distributed normally. Therefore, RTS histogram usually represents two or more Gaussian peaks corresponding to each of the current levels (see Figure 2.7). In real measurements, the useful signal is usually not a random process and thus its histogram should not have distinct separation of two Gaussian peaks like in Figure 2.7(B). Such a difference can be used as a verification procedure to distinguish if the measured signal is valid or not.

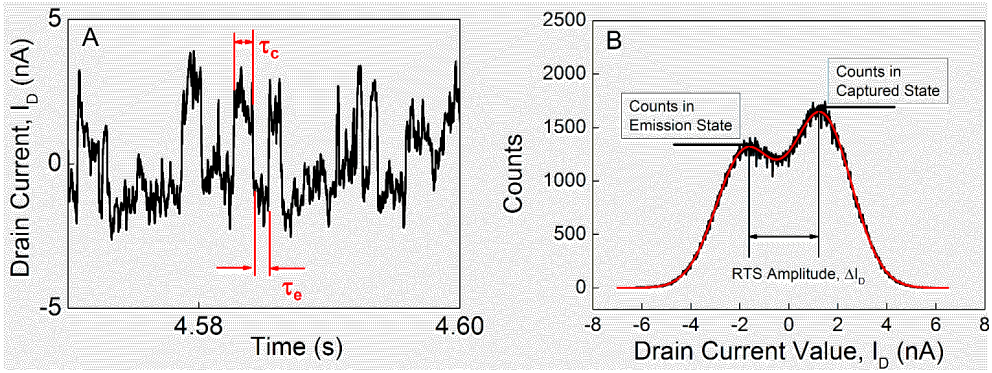

Figure 2.7 Time trace (A) of the drain current and its corresponding histogram (B) for the liquid-gated Si NW sample with length of 500 nm and the width of 100nm at V_{DS} = - 0.1 V, V_G = - 0.9V and pH of the gating solution pH = 7.5. The image is adapted from [92].

The capture time is dependent on the concentration of the carriers (Eq. (2.39)) and thus on the gate voltage. In the case of strongly confined geometries like silicon-on-insulator (SOI) based devices, Si NWs and gate-all-around FETs the dependence of the capture time on the concentration of the carriers may deviate from the SRH behavior and can be much stronger function of n than Eq. (2.39) [146], [147]. We have used the capture time as a sensitive value for detection of surface potential of liquid-gated Si NW FET. Monitoring of the τ_c instead of the drain current resulted in the increase sensitivity of Si NW FET device to the surface potential by a factor of 400% , because of a strong dependence of behavior of τ_c on carrier concentration [92].

The spectral density of the RTS noise is represented by a Lorentzian-shaped component [148]. The time constant of a process is defined by capture and emission times:

$$\tau = \frac{\tau_c \tau_e}{\tau_c + \tau_e}. \tag{2.40}$$

The the plateau of the Lorentzian is defined by the RTS amplitude and the capture and emission times:

$$S_I(0) = 4\frac{(\Delta I)^2 \tau^2}{\tau_c + \tau_e}, \tag{2.41}$$

where ΔI – is the RTS amplitude, which can be determined from Figure 2.7(B).

As it was mentioned in subsection 2.2.2, the spectral density of the signal fluctuations is an additive value, if the noise sources are not correlated between each other. Therefore an observed spectra are represented by a combination of all mentioned types of noise. In the Figure 2.8 an example of superposition of three types of noise is presented.

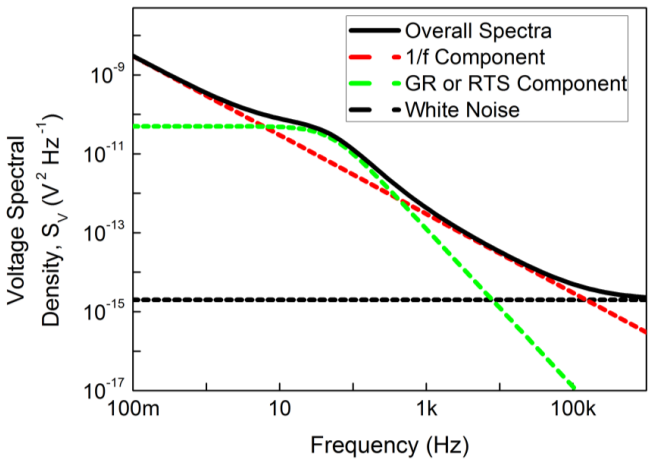

Figure 2.8 Spectral density of the drain-source voltage fluctuations (solid line) and its components (dashed lines).

Different noise mechanisms in the sample are often investigated separately. Therefore, corresponding noise spectra component should be discriminated from the overall spectra by means of fitting or by finding of the FET mode where other noise mechanisms are suppressed and the component under is most pronounced. For simplified fitting of the noise spectra, we have developed a special software, which will be described later.

The overall noise is important when the real measurements are performed, because in this case the useful signal is compared to the whole noise of the measurement system. The knowledge about the noise components and their behavior allows improving fabrication technology and finding operation modes in such a way that the overall noise of the device is reduced and signal-to-noise ratio is optimal. It should be noted that for obtaining optimized signal-to-noise ratio of the FET biosensor we should be aware of the signal level, which we are going to detect. Therefore, in the next subsection we will discuss the main principles of electrogenic cell functioning and the main properties of the cell/FET interface.

2.3 Electrogenic cells on FETs

2.3.1 Introduction

The building block of the biological systems are cells. They are diverse in their functionality and are often organized into functional modules which are repeated within the organism[149]. The most complex biological system in the organism is the nervous system and its elementary unit is the neuronal cell. A tremendous progress of the neuroscience in the last decades was achieved due to investigation of the neuronal cell activity and pathways in vivo as well as in vitro using novel ultimate methods including nanotechnology[150]. One of the most demanded methods of the neuronal cell investigation – is the extracellular monitoring of the cell activity, because it is not harmful and allows characterizing cellular system without any influence on it. Therefore, extracellular investigation of neuronal cells activity is of great interest from point of view fundamental biophysics as well as large variety of applications such as monitoring of electrical communication within neuronal networks, transmission paths of ionic channels, the use as biosensor to monitor pharmaceutical agents, pollutants, etc.

The state of a single cell or cell system can be monitored by either their metabolic products (in the case of the chemical synapse - neurotransmitter) or extracellular potential measurements. For investigation of the electrogenic cells activity (e.g. neuronal cells or muscle cells) one can utilize their specific features like generating of spontaneous or triggered action potentials and measure shifts of the cell membrane extracellular potential. The activity of a neuron leads to ionic- and displacement currents flowing through the cell membrane, resulting in an extracellular voltage drop along the cleft between the cell membrane and surface of the sensor. As we have discussed above, such a change of the surface potential can be registered using liquid-gated FET.

In this section we will concentrate on the origins of the electric activity of the electrogenic cells like neurons and cardiomyocytes and the interface between the cells and the devices for extracellular detection of action potential.

2.3.2 Neuronal cells and the action potential

The neuronal cells are basic units of the nervous system, which is divided into central nervous system (includes brain and spinal cord) and peripheral nervous system (remaining nerves). On the contrary to other organs neuronal cells are extremely diverse and only the smaller part of

those types is yet understood. However all of the neuronal cells still share the same working principle. The neurons are capable of changing their membrane potential and thus conducting an electrical signal as well as passing the signals from one neuron to another. The points where the neurons are connected between each other and can pass excitation or inhibition is called a synapse[149]. A typical neuronal cell is shown in Figure 2.9. The cell body of a neuron contains the nucleus, where all the genetically coded information is stored. Typically neuronal cells have two types of protrusions: axons and dendrites (see Figure 2.9). Axons are responsible for the transmitting the signal in the neuron. The length of an axon may vary in a large range from tenths of micrometers up to even 3 m. The width of the axons is usually much smaller than the body of a neuron and may vary in the range between 0.2 µm to 20µm. The size of the neurons in central nervous system is dependent on the animal species, but usually it is about 50 µm[149]. The typical size of the rat cortical neurons which are used in the present work is about 20 µm. Such values are used in the design considerations of the Si NW FETs. The electric signal, which is propagating along the axon is shielded from the outer environment by myelin shealth, which is interrupted regularly by nodes of Ranvier[149]. Branches of the axon of a neuron form connections to the further neuronal cells, called postsynaptic cells. The site where the neurons are connected with each other is called synapse. Axon transmits a signal to another neurons through a synapse. A neuronal cell can form synapses with up to 1000 of cells. On the opposite side of the axon usually a neuron also has protrusions, called dendrites. Together with the dendrites, the cell body can accept signals from another neurons through synapses[149]. The synapses may be excitatory and inhibitory (when a postsynaptic cell gets excited or silenced afther the signal transmission). The signal through the synapse can be transmitted to the next cell either electrically or chemically, however the signal inside the cell propagates as a wave of changing the membrane potential, known as action potential.

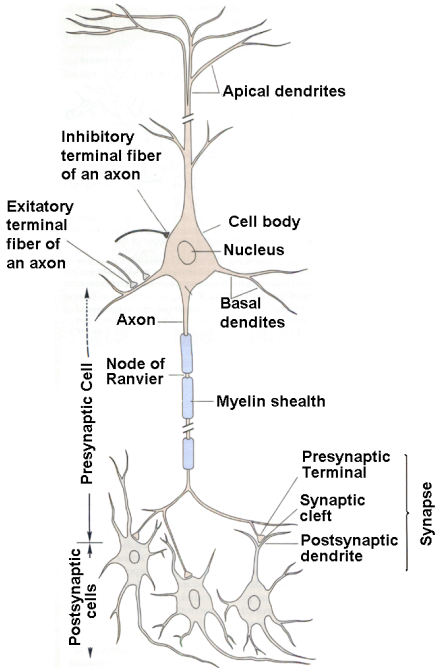

Figure 2.9 Typical neuronal cell shown with its connection to three postsynaptic cells. The schematic image adopted from [149].

The cell electricity originates from differences between concentrations of different ions inside and outside of the cell. Therefore the key role in this process is played by the cell membrane. The membranes in the cell perform a lot of different functions. Among them the plasma membrane defines the cell and separates inner part of the cell from the outer environment[151]. The cell membrane is a lipid bilayer with incorporated membrane and transmembrane proteins[152]. The special proteins called ion channels are also provide selective permeability of the membranes to the ion fluxes (see Figure 2.10).

The proteins called ion pumps promote active transport of the ions through the membrane in the direction against the electrochemical gradient. Such proteins provide difference between ion concentrations in the cell and outer environment, which results in potential difference between inner and outer side of the cell. The ion pumps work in such a way that the K^+ ions are pumped into the cell, whereas sodium and chlorine ions are pumped out of the cell. In the state of

equilibrium the cell membrane is permeable only to K^+ ions due to constantly opened resting K^+ channels Figure 2.10(a). Taking into account that as the result of ion pumps functioning, the concentration of potassium ions inside the cell is higher than outside, the flow of K^+ through the resting K^+ channel is in the direction of the cell exterior. Therefore in the equilibrium state the potential of the cell interior is negative against the environment. The resting potential of living cells varies from -100 mV to -40 mV depending on a cell type and is defined by inner and outer concentrations of ions and by permeability of the membrane. The behavior of the resting potential is described by the famous Goldman-Hodgkin-Katz equation, which is a modification of the Nernst equation for the case of multiple ions moving across the membrane with certain permeability.

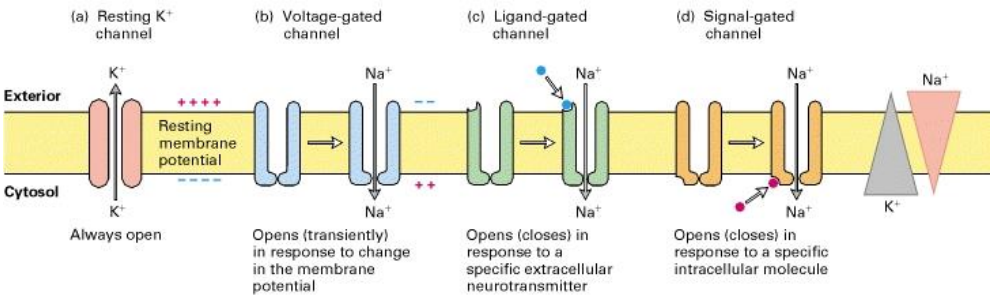

Figure 2.10 The schematic demonstration of different types of channel proteins in neuronal cell. (a) shows the resting K^+ channel, which provides the resting potential of the membrane. (b)-(d) are the channels for sodium ions, driven by voltage, neurotransmitters and different internal signal pathways of the cell. The image is adapted from [151].

The action potential is an event of cell membrane depolarization, which occurs when the cell is shifted from its equilibrium state. Such a wave of membrane depolarization can propagate along the neuronal cell. An action potential can be achieved by increasing membrane potential with outer stimulus or by chemical influence on signal and ligand gated ion channels. A depolarization of the membrane over the certain threshold causes an action potential. By reaching the threshold potential the voltage-gated Na^+ channels open and cause a fast influx of sodium ions into the cell. This effect further enhances depolarization and leads to establishing of a positive membrane potential. Then more slow voltage-gated potassium channels open and increase permeability of the membrane for the K^+ ions. The outward flux of potassium ions reduces the membrane potential and causes fast sodium ion channels to close. The potential of the membrane returns back to the

negative value. The inertia of the voltage gated potassium channels causes slight repolarization of the cell (the membrane potential drops below the equilibrium resting potential).

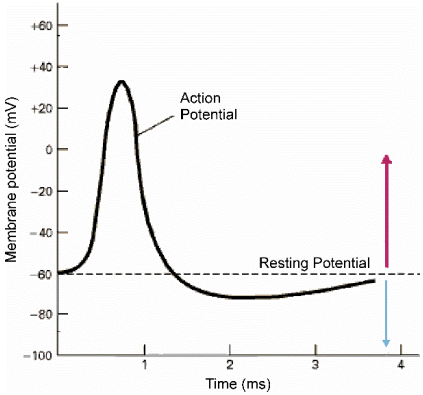

Figure 2.11 Time trace of an action potential of a neuronal cell. The figure was adapted from [151].

Action potential can be represented as an electromagnetic wave which propagates along the cell membrane and is accompanied by fluxes of different ions. It results in an extracellular voltage drop along the cleft between the cell membrane and surface of the biosensor. Such a voltage drop may be detected using Si NW FET.

2.3.3 Extracellular recording from a neuronal cell

The traditional method for electrophysiological measurements of activity of the electrogenic cells is a patch-clamp technique, which is based on the penetration of the cell membrane with a glass micropipette and direct recording of the potential difference between inner and outer part of the cell membrane[24], [153]. The patch-clamp technique is robust and reliable, however it has limitations connected with the penetration through the cell membrane. The cells don't survive the patch-clamping and therefore long-term experiments with the same cell are not possible. Another issue is the scalability of the method. Patch clamp method does not allow parallel recording from number of cells, due to art of its implementation: the micropipette is driven by an operator in semi-automated way and it is hard to put a lot of micropipettes in the field of view of the microscope.

A promising alternative to the patch clamp method is an extracellular recording of the cell activity. As it was mentioned before the propagation of the action potential along the cell membrane results in an extracellular voltage drop along the cleft between the cell membrane. This voltage drop can be registered using planar metal electrodes, so called multi-electrode arrays (MEA)[26], [27] or using an ISFET [20], [28], [32]. The advantage of extracellular measurements is that the recording is non-invasive and it may be used in parallel for the array of sensing spots. The MEA is attractive from the point of view of simplicity of fabrication technology, possibility of stimulation using the electrodes of the MEA and long-term stability in cell culture[154]. However further downscaling of the MEAs, which is important for higher spatial resolution and density of mapping, is limited by the impedance of the electrodes to the size of several microns. An alternative way of extracellular recording is using an ISFET. It has advantages of scalability, which allows using different geometries and achieving high spatial resolution.

The interface between a cell and a recording site – a microelecrode or a transistor can be represented in a form of equivalent electric circuit. The simplified sketch of such a circuit is shown in Figure 2.12.

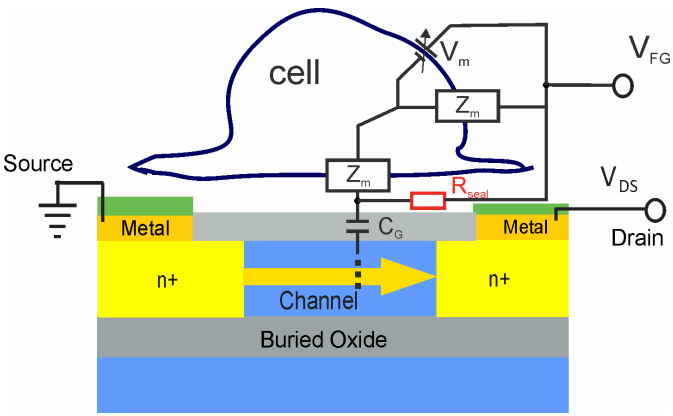

Figure 2.12 Simplified sketch of equivalent circuit of a neuronal cell on the surface of an ISFET [32], [155].

The impedance of the cell membrane, Z_m, can be treated using a Hodgkin-Huxley model [156]. The change of the membrame potential, V_m, with time will cause fluctuation of the surface potential of the ISFET in the region of cell-transistor junction, V_J [32]:

$$\frac{dV_J}{dt} = \frac{C_M}{C_M + C_G}\frac{dV_m}{dt} - \frac{1}{R_{seal}(C_M + C_G)}V_J \tag{2.42}$$

where C_M is the capacity of the cell membrane according to Hodgkin-Huxley model, C_G is the capacitance of the FET gate, R_{seal} – is the seal resistance of the cell – FET junction, which reflects quality of the coupling cell membrane and the gate oxide. If we switch to frequency representation in Eq. (2.42) by substituting V_m and V_J with the harmonic signals with amplitudes V_{m_0} and V_{J_0} we will get:

$$\left|\frac{V_{J_0}}{V_{m_0}}\right|^2 = \frac{\omega^2 C_M^2 R_{seal}^2}{\omega^2 (C_M + C_G)^2 R_{seal}^2 + 1} \tag{2.43}$$

where ω is the frequency. The action potential of neuronal cells [28] require detection of signals with average pulse duration about 3 ms. Therefore all the principal components of the useful signal are on average not faster than 10 kHz. As we can see from Eq. (2.43) at high values of the $\omega^2(C_M + C_G)^2 R_{seal}^2$ the action potential may be registered using FET almost without distortion of the pulse shape with the amplitude of $V_{m_0}\frac{C_M}{C_M + C_G}$.

The seal resistance is the main parameter, which determines quality and the amplitude of the signal at the surface of a sensor. The cleft between a cell and a sensing spot determines the R_{seal}. In reality the cells tend to float over the flat surfaces like plane silicon oxide, silicon or gold at relatively high distance from the surface (up to 100nm)[34]. Due to this reason the seal resistance significantly decreases and the relation (2.43) drops far below one. Typical amplitudes of the action potentials recorded using extracellular sensors are usually in the range of hundreds of microvolts[28]. However the seal resistance can be improved using novel nanoscaled geometries. In the case of MEA structures it has been shown that nanopillar structures may reduce the cleft between the cell and the electrode[35], [157]. In case of the FET biosensors it has been shown that the cleft between Si NW nanowires and cells is as small as 4 nm , which is almost the thickness of the adhesion promoters, which are usually applied to the surface in order to attract the cells[30], [36].

2.4 Summary

In this chapter we have used knowledge and experience from literature research to define the target directions of the presented work. As it was shown above the interface between the neuronal cell and Si NW sensor plays an important role in the efficiency of extracellular detection of the action potential. Extracellular changes of the Si NW FET surface potential in response to the electrogenic cell action potential is much lower than its original amplitude and is expected to be below 1 mV. The main spectral components of the action potential are within the range from 1 Hz to 10 kHz.

Therefore, in the present work we aim to produce silicon NW FET devices for neuronal cell interfacing which will meet the following requirements:

- Stable and reliable in terms of long-term usage in electrolyte for cell-culture experiments.
- Detection of the gate surface potential changes as small as 100 μV (filtered to the range between 1 Hz and 10 kHz) to have enough sensitivity for efficient detection of neuronal action potentials.
- Size of the gate opening in the passivation comparable with the size of the cell in order to make the surface of the NW FET accessible to the cell.

In order to fulfill the established goals we have designed Si NW transistors of different geometries and configurations. The neuronal cell/NW interface is studied in the present work using technique of focused ion beam cutting.

The fabricated NW FET structures are tested under different conditions and in different regimes of operation. We utilize the approach of the noise spectroscopy for investigation of the quality and performance of the fabricated NW structures. Though noise spectroscopy was widely used for analysis of transport properties of MOSFETs, only during last decades it was considered for investigation and improving quality of liquid-gated FET biosensors. Therefore, in the present work we study the influence of the electrolyte on the transport in Si NW FETs and confirm the applicability of developed the approaches for MOSFETs in the case of liquid-gated FETs.

In the next chapter, we will cover the methods we used for fabrication, characterization of transport in Si NW devices, estimation of the SNR in silicon NW FETs and investigation of neuronal cell / NW interface.

3. Materials and methods

3.1 Introduction

Silicon is most widely used material in modern electronics. The field of silicon-based biosensors has grown tremendously during the last decades because of exceptional variability of fabricated Si structures and cost efficiency due to their CMOS compatibility. Though silicon technology is widely used and well developed, it usually has to be adjusted for a case of each particular application. In this chapter we describe our developed protocols for Si NW array FET technology, which we used for fabrication of our NW structures. Then we describe methods used for characterization and investigation of Si NW FET transport properties, which were used for improvement of the fabrication technology and investigation of the signal-to-noise ratio behavior. At the end of the chapter the protocols of cell culture on the Si NW FET chips and preparation of the samples for focused ion beam cutting will be discussed. The figures of this chapter contain examples based on the data obtained in the experiments, which were carried out during the current work.

3.2 Silicon nanowire FETs

3.2.1 Chip layout

In the frame of current work we have developed and fabricated various Si NW FET structures. The structures have different layouts, which were developed based on analysis of experimental results and demands of the cell-culture experiments. Fabricated samples contain NWs of different geometries, which will be discussed later. There are two general types of Si NW structures, which were used for the experiments and calculations: single NW FETs and NW FETs based on the array of 50 NWs connected in parallel. Single NW FETs structures were partially obtained in frame of collaboration with Prof. Mantl group and fabricated within our group by Jing Li. The Si NW structures based on arrays of Si NWs were fabricated as a part of presented work and detailed process of their fabrication is described in the next subsection. Here the layouts and geometries of the fabricated structures are introduced.

Each of the NW array FETs contains 50 nanowires connected in parallel. The Si NW array FETs were fabricated using two types contact line doping (As or B). The fabricated FETs represent n^+-p-n^+ and p^+-p-p^+ structures. In order to study quality of the samples and find optimal sensor

geometry we have fabricated Si NW array FETs with a variety of channel dimensions. The sizes of the NWs are shown in Table 3.1. Each of the chip layouts consists of 12 or 24 NW FETs. The layout design provides 5x5 mm^2 chips with constant NW length and variable widths (blue, green and yellow in the Table 3.1) and chips with variable length and constant width (red, grey and orange in the Table 3.1). In both layouts the chips were produced on a 30x30 cm^2 pieces of silicon on insulator (SOI) wafers. Each piece contained 24 chips with different NW dimensions, as described above.

Table 3.1 The schematic map of sizes for the fabricated NW array FETs. The NWs of certain sizes belong to certain chips according to color code. The cells on the intersections of colors belong to both chips.

L(μm) / W(nm)	2	3	4	5	6	8	10	12	14	16	17	18	19	20	21	22
50																
100																
150																
200																
250																
500																

During the current work, the layout of the Si NW array FET chip has undergone several modifications based on experimental needs and an electric characterization of the fabricated chips. We show in Figure 3.1 the evolution of the chip layouts. The first and the second layouts (Figure 3.1 (a), (b)) were developed in collaboration with Jing Li. The layout 1 provides 5x5 mm^2 chips, which contain 24 NW arrays each. All of NW arrays have common source contact. The drain contacts are designed in order to have metal contacts on the outer edge of the sample. Each of the drain feedlines is designed to have equal resistance. However, while characterizing the samples fabricated using this design we encountered several disadvantages of the layout 1. Common source contact is convenient in use, but it may decrease reliability of the structures, because once the

sample gets gate-source leakage, then all of the 24 NWs get the same problem. The second issue is connected with the contact resistance. Even though the drain contacts are designed in a special way to have equal drain contact resistance, the source resistance for each of the NW FETs is different in such a configuration. Therefore, a second layout was developed as an optimized version, which avoids abovementioned issues.

The layout 2 (Figure 3.1(b)) provides 5x5 mm^2 chips as well. It has 12 NW array FETs, each with separate drain and source, which both have equal resistance. Having silicon feedlines on the chip allows avoiding potential problems with passivation of metal contacts against electrolyte solution, because all metal parts of the chip are far from the sensing area. However, the long silicon feedlines also result in increased contact resistance. The calculations of contact resistance of the NW arrays FETs give the value of 25 kOhm [40]. The channel resistance of the transistors varies from 1 MOhm to 100 kOhm in the operational range, therefore mostly the contact resistance can be neglected. Layout 2 was used for the most of the experiments presented in this work.

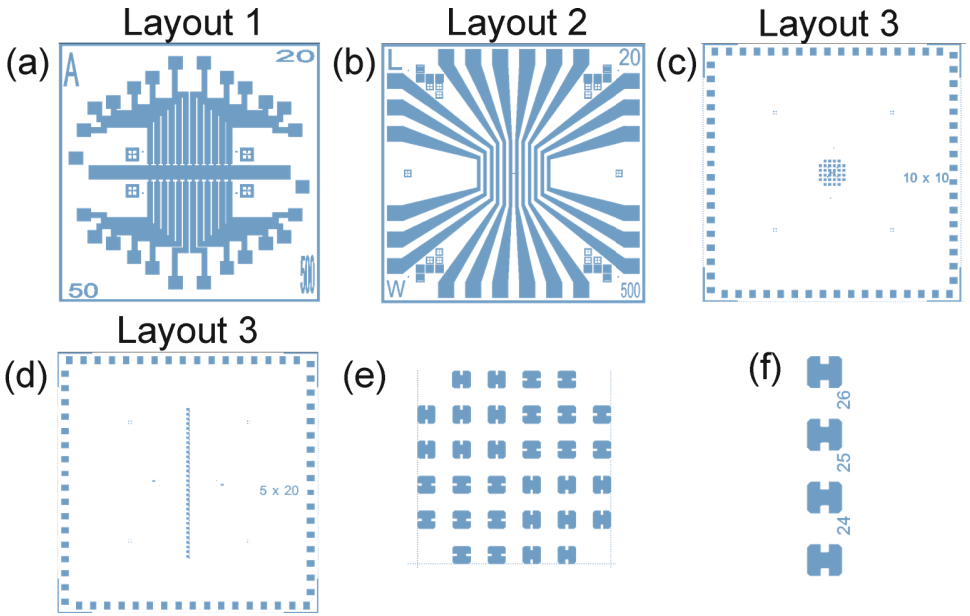

Figure 3.1 Si NW array FET chip layouts used and designed in frame of presented work. (a) - layout 1;(b) - layout 2; (c),(d) – layout 3; (e) - magnified device part of layout 3 (c);(f) magnified device part of layout 3 (d).

The third layout (Figure 3.1(c,d)) was developed in collaboration with Jan Schnitker and Regina Stockmann. It includes all the design considerations of previous layouts and takes into account specificity of cell-culture experiments. The cell measurements require more space on the chip than ISFET measurements, because using of a patch-clamp micropipette is often required. The micropipette approaches the chip surface from the top side under certain angle in order to keep possibility of observing the chip using a microscope. Therefore a chip size of 11x11 mm^2 was chosen. The layout 3 has two principal chip designs. Each of them contains 32 NW array FETs. The linear design (Figure 3.1(d), (f)) may be used with the microfluidic channel on top. The design with array of FETs ((Figure 3.1(c), (e)) represents array of 32 mapping sites for the neuronal network. The layout 3 is designed for 4-inch wafer based production. One wafer contains 16 chips with linear layout and 28 chips with array layout. Also there are 4 experimental chips foreseen on the wafer: 2 chips with NW array MOS transistors of the same dimensions as the liquid gated and 2 chips with NW array FETs and stimulation electrodes to combine stimulation and recording from neuronal cells.

In the next subsection the fabrication of Si NW array FETs will be described for the case of layout 2, however the fabrication processes for all of the described layouts will retain the same.

3.2.2 Fabrication technology

The technological process of Si NW array FET fabrication was carried out at the Helmholtz Nanoelectronic Facility (HNF) of Forschungszentrum Jülich. Si NW array FET fabrication consists of 8 technological steps. Each of the steps may have crucial impact on the quality of the final structure. Therefore all the technological procedures were done with all possible precautions. As the result we have fabricated high-quality Si NW array FETs. The characterization of the structures is discussed later.

Figure 3.2 shows the schematic representation of the workflow of Si NW array FET fabrication. We combine optical and e-beam lithography in order to reduce costs of production. The backbone of Si NW arrays and silicon feedlines are first produced by means of optical lithography and then the NW structures are produced using e-beam lithography. Now the steps of the process will be discussed in detail.

The transistors are fabricated on the basis of 200 mm <100> silicon on insulator (SOI) wafers (Figure 3.2(a)) with active layer of 75 nm silicon and buried oxide of 145 nm thickness. The supplier is SOITEC, France. Depending on the layout, which was discussed in the previous

subsection, the wafer was cut into 30x30 mm^2 pieces using a dicing saw or into two 100 mm wafers using laser.

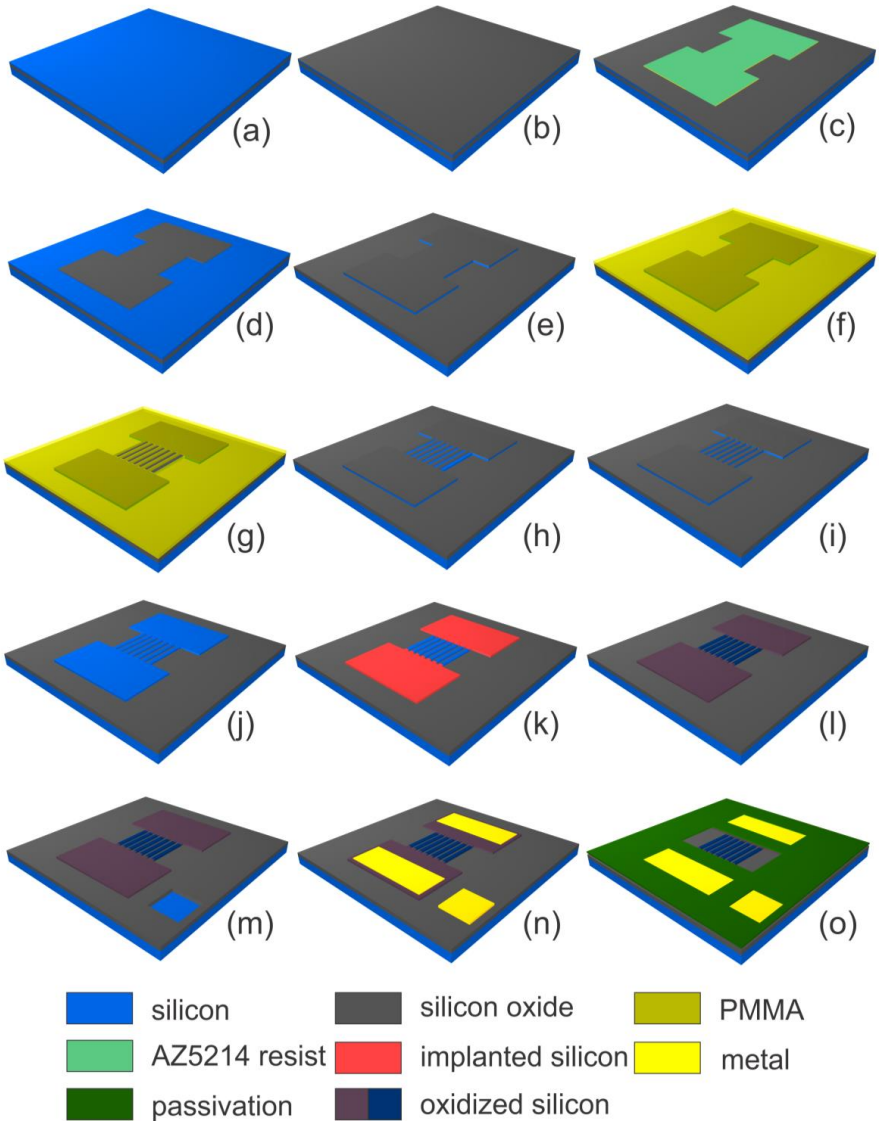

Figure 3.2 Schematic representation of the Si NW FET fabrication steps. The fabrication steps (a)-(o) are described in detail in the text.

Then the prepared pieces of SOI wafer are oxidized in order to form the etching mask for Si NWs and thin down the active layer. The samples are put in dry oxygen atmosphere at a temperature of 1000ºC for 30 min. As the result we get 37 nm of thermally grown SiO_2 and the rest of the active layer has the thickness of 50 nm (Figure 3.2(b)). The next step will be structuring of the silicon oxide mask for the formation of the silicon feedlines and the backbone of the NW structures. The first pattern contains e-beam markers, which are recognized by the e-beam writer for precise alignment.

The first step of patterning the SOI wafer is the photolithography. Here we describe the full process of sample preparation for the lithography. The sample is dehydrated at 180 ºC and then covered with hexamethyldisilazane (HMDS), an adhesion promoter. The HMDS is applied to the sample directly at the spincoater for 60 s and then spin-coated at 6000rpm in order to remove the residuals. Also HMDS may be applied from the vapor phase at temperature of 125 ºC using special HMDS deposition machine. After applying the adhesion promoter, the AZ5214 (MicroChemicals GmbH) resist is coated at 4000 rpm and then dried for 5 min at 90 ºC. The resist is then structured using photolithography ((Süss, MA-6 with 365 nm UV light-source, 7 mW/cm^2) with the exposure time of 6 s (Figure 3.2(c)). Then the samples are exposed for 45 s to the development solution AZ 326 MIF. The development process is then stopped by immersing the samples in DI water.

The second step of the SOI wafer patterning is transferring structures to the oxide mask. The oxide mask is etched (Figure 3.2(d)) using reactive ion etching (RIE) or wet chemical etching. In the case of the reactive ion etching we used the CHF_3 plasma, because it provides highly anisotropic and selective etching of silicon oxide. The etching time is machine specific and depends on power delivered by plasma to the sample surface. Usually the etch rate is controlled by a laser beam or is calibrated beforehand. In our case etching of 37 nm silicon oxide took 1 min 05 sec at the RIE. The residuals of the photoresist are removed using oxygen plasma. In the case of wet etching of the silicon oxide mask, the oxide is etched using 1% HF solution, with the etch rate of 6-7 nm/minute. Before etching of the silicon oxide the sample with patterned AZ5214 should be soft-baked for 5 min at 110 ºC in order to improve adhesion of the resist and its resistivity to HF. Then the sample is immersed into 1% HF solution for 6 min 30 sec. The HF etching is isotropic, therefore an overetch leads to reducing the width of the structures. After the etching, the resist is removed using acetone.

As the next, the active layer of silicon is etched through the oxide mask (Figure 3.2(e)) using wet chemical etching, as it will be described later for the NW processing. Then the NW structures can be fabricated using e-beam lithography.

In order to structure the silicon oxide mask and form the NW pattern, the sample is coated with e-beam resist PMMA (Figure 3.2(f)). At first, the sample is dehydrated at 180 ºC for 5 min. Then the PMMA resist (AR-P 649.04) is spin-coated onto the sample at 4000 rpm. After that PMMA is dried for 5 min at 180 ºC According to the datasheet the thickness of PMMA at this spin speed is about 150 nm. In case of our samples it was around 130 nm, which is in good agreement with the datasheet. The PMMA with such thickness has been chosen for several reasons. It is thin enough to enable relatively fast recognition of the e-beam markers and it is thin enough to hold the vertical aspect ratio of our structures (width of the thinnest NW – 50 nm, thickness of the resist is 130 nm, the aspect ratio is 2.6). Also the PMMA layer of 130 nm is enough thick to hold etching of silicon oxide mask for 1 min in RIE.

The next step is e-beam writing of the NW pattern. The developed pattern consists of two subpatterns: fine and coarse, which are written with different electron beam parameters for the reasons of cost- and time- efficiency. The example of the pattern is shown in Figure 3.3. The pattern represents inverted array of nanowires, because PMMA is positive e-beam resist. The colored parts of Figure 3.3 are written and white parts are not affected. However, in the case of such dense pattern, the NW area (white) also is partially exposed due to scattering of the electrons inside the PMMA. The effect is called proximity effect and it is reduced using proximity correction procedure. When the proximity correction is used, the e-beam writing is carried out with dose variation across the pattern, so that all parts of the pattern get equal exposure dose regardless of the proximity effect. For the fine pattern the starting dose was 200 $\mu C / cm^2$ and the beam step size was 5 nm. For the coarse pattern the dose was 210 $\mu C / cm^2$ and the beam step size was 50 nm. The distance between NWs in the array is 250 nm.

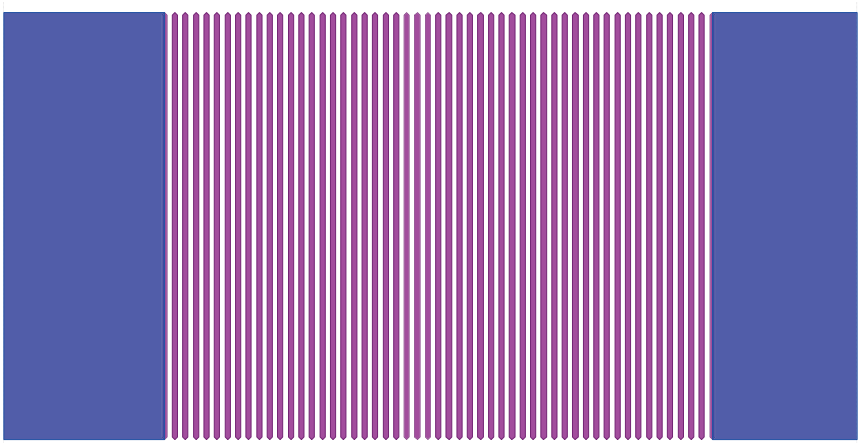

Figure 3.3 Typical NW pattern for e-beam writing (array NWs of 250 nm width and 20 μm length). The blue area represents coarse pattern and the violet area is the fine pattern.The spacing between NWs is 250 nm

After e-beam writing, the samples are put into the developing solution (AR-P 600-55) for 1 min and 10 seconds under constant stirring and then into isopropanol for 1 min as a stopping solution. As the result we get structured PMMA film on the surface of the sample (Figure 3.2(g)).

The pattern is transferred from the PMMA into the silicon oxide mask by means of RIE etching in CHF_3 plasma as described above for the first step of the silicon patterning (Figure 3.2(h)). We use tetramethylammonium (TMAH) for anisotropic wet etching of silicon[158]. It has been shown that using wet etching of silicon provides extremely high quality of device surfaces[159], which results in reduction of the device noise compared to the RIE etching of silicon[38]. TMAH etching is very selective to silicon and very anisotropic. We have etched Si in 5% TMAH water solution at a temperature of 90 ºC for 15 seconds. Under such conditions etch rate of the TMAH is 34 nm / min for <111> plane and 1.4 μm / min for <100> plane. As the result we get patterned silicon NW structures with oxide mask on top(Figure 3.2(i)). Due to strong anisotropy of etching the NWs get a trapezoidal shape, because the slow etching plane of TMAH is <111> and it is tilted from the <100> plane by 54.7º. The resulting NW array structures were characterized using scanning electron microscopy (SEM). Typical SEM images of Si NW array FETs are shown in Figure 3.4. The general view on the array of 50 NWs with width of 100 nm and

length of 20 µm is shown in Figure 3.4(a). The side view of 250 nm Si NWs allows to observe quality of the sidewalls of the NWs (Figure 3.4(b))

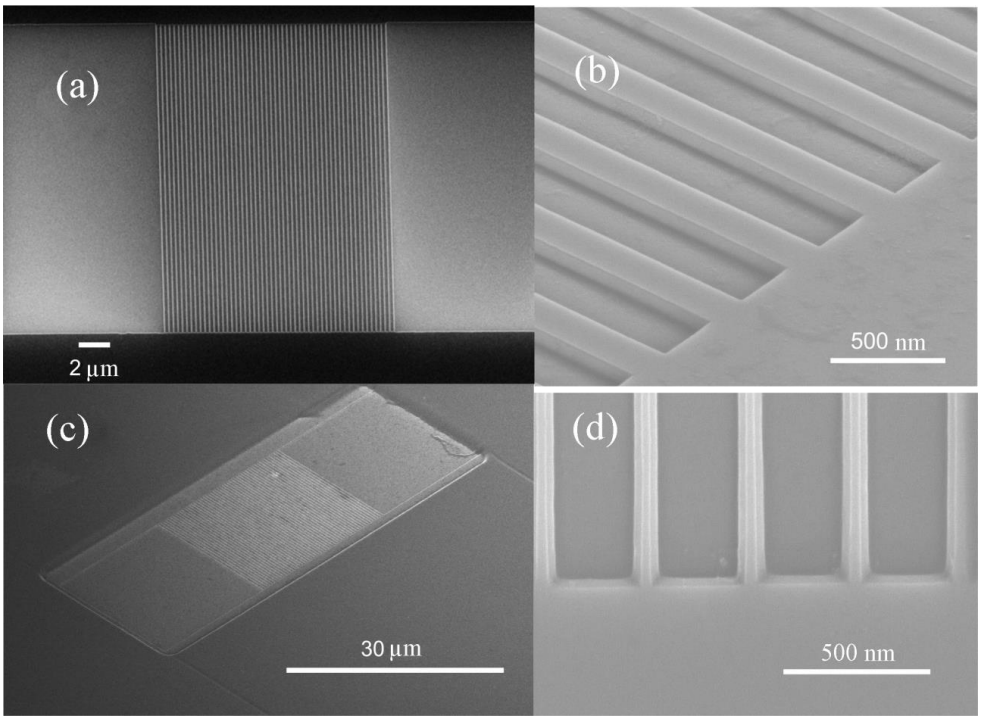

Figure 3.4 SEM images of Si NW array FET structures. (a) array of 100 nm wide and 20 µm long Si NWs; (b) side view of the contact between a silicon feedline and array of Si NWs; (c) SEM image of the NW array FET after passivation with SU-8; (d) contact between a silicon feedline and array of Si NWs (observed width is 85 nm). The <111> plane of silicon can be seen in this part of the figure;

After the pattern is transferred into silicon, the oxide mask is removed by means of wet etching of silicon oxide with 1% HF water solution for 6 min 30 seconds (Figure 3.2(j)).

Patterning of the silicon active layer is followed by the feedlines implantation with B or As atoms (Figure 3.2(k)) depending the desired type of structures: accumulation FET (p^+-p-p^+) or inversion FET (n^+-p-n^+). The NW area is protected from implantation by means of optical lithography using AZ 5214 resist (the procedure of optical lithography is described above). For the

case of B doping we use ion energy of 6 keV and the dose of 10^{15} cm^{-2} , for the case of As doping we use energy of 8 keV and the dose of $5x10^{14}$ cm^{-2}. After implantation the samples are cleaned using acetone (8-10 hours) in order for the hardened photoresist to swell and dissolve. Then the full RCA cleaning procedure is performed to remove all the organic and inorganic residuals from the surface of the NW chips. As the next, the dopants are activated using rapid thermal annealing: 5 s at 1000 ºC for boron implantation and 30 s at 950 ºC for arsenic implantation.

The next step is formation of the thermally grown silicon oxide, which will protect the NW channel from electrolyte and serve as a gate oxide (Figure 3.2(l)). The oxide is formed by dry thermal oxidation in an oxygen flow for 60 min at 820 ºC. As the result we get silicon oxide of 8 nm thickness. Such a low growth rate of 8 nm per hour is chosen in order to achieve exteme high quality of the oxide, because it plays a crucial role for device stability, reproducibility and the signal-to-noise ratio.

Designed layouts of the Si NW structures provide also a back gate contact for Si NW FETs. It is formed after growing the gate oxide. The sample is covered with the AZ5214 resist using the described procedure. The AZ resist is then patterned lithographically in order to produce openings over the places of future back gate contacts. Then the AZ resist is soft baked for 5 min at 110 ºC to improve adhesion to silicon and resistivity to etching. After that, the back gate opening is etched in the buried oxide (Figure 3.2(m)) using 10 % HF solution for 3 min (etch rate 70 nm / sec).

After formation of the back gate opening the metal contacts to the NW structures are formed. The samples are coated with AZ nlof 2020 resist: 180 ºC heating for 5 min for dehydration, 4000 rpm resist spinning, pre-bake at 110 ºC for 1 min. AZ nlof 2020 is a negative photoresist, which is specially designed for lift-off procedure. The resist is exposed with 365 nm light source for 2 s with the dose of 7 mW/cm^2 through the mask with layout for metal contacts. Then the sample is post-exposure baked for 1 min at 110 ºC, developed for 45 sec in AZ 326 MIF developer and rinsed in distilled water. After structuring the AZ nlof resist, the sample is put for 2 min in 1% HF solution to remove thermally grown gate oxide in the area of contact pad. Then 150 nm of aluminum is evaporated onto the sample. Then a lift-off procedure in acetone is performed: the sample is put into acetone for 10 hours and then cleaned using acetone, isopropanol and DI water (Figure 3.2(n)). Metal contact deposition is followed by contact annealing in the forming gas atmosphere (N_2:H_2 20:1) for 10 min at 450 ºC to form ohmic contacts between Al and Si. The metal contacts may then be adjusted for different purposes by additional lithography and lift-off steps.

For example, Ti and Au layers may be introduced on the top of aluminium layer for improving adhesion to the chip carrier or for facilitation of the wire bonding process.

Finally a passivation of the feedlines against the electrolyte solution is performed. For the case of layout 2 (Figure 3.1) the SU8-2 was used. The SU8-2 resist was spin-coated at 4000 rpm onto the samples after a dehydration step. Then the resist is soft-baked for 1 min at 65 ºC and 1 min at 95 ºC. The exposure was done with the i-line 365 nm lamp for 3s with approximate dose of 7mW/cm^2. After exposure the resist is post exposure baked for 1 min at 65 ºC and 1 min at 95 ºC and developed in mr-dev 600 for 45 seconds. Then in order to improve the resist stiffness and adhesion to the sample the whole sample was hard baked for 30 min at 180 ºC. The SU resist series have an advantage of high stability, because this resist is epoxy based. However in case of failure of lithography process or slight deviation of process parameters, the resist is almost irremovable after exposure and leaves no chance for repeating of the procedure. Therefore all of the passivation steps are first performed on the test samples, in order to establish an exact protocol for current conditions in the clean room. For the layout 3 we have chosen the PI 4525 resist, which is 100% removable with any alkaline developer until the hard bake procedure.

After all the fabrication steps the sample is cut into single chips and encapsulated for liquid measurements. The encapsulation procedure is described in the next subsection.

3.2.3 Encapsulation of the Si NW chips

Using a liquid gate for the Si NW FETs requires protection of the contact areas against electrolyte solution, because it causes gate-source or gate-drain leakage. The chips are glued into a ceramic chip carrier and then wire bonded to the contactpads of the chip carrier (Figure 3.5(a)).

The inner part of the sample is separated from the contact area with a glass ring (inner diameter of 3 mm and outer diameter 4 mm). The glass ring is glued onto the sample (Figure 3.5(b)) using polydimethylsiloxane (PDMS). The PDMS was prepared using standard protocol: mixing precursor with curing agent in relation 10:1. Then 10 mm outer ring was glued to define a boundary of a liquid bath (Figure 3.5(c)). After gluing both glass rings the sample is put into an oven for an hour at a temperature of 120 ºC to harden the PDMS. The space between glass rings is then filled with PDMS and the sample is again put into the oven for 1 hour (Figure 3.5(d)).

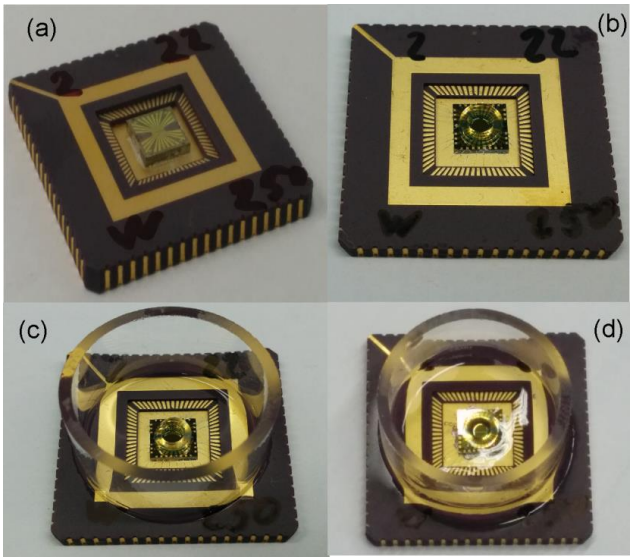

Figure 3.5 Photos of Si NW FET encapsulation process. (a) the sample in a chip carrier;(b)inner glass ring over a chip;(c) outer glass ring over a chip carrier;(d) filling of the space between glass rings using PDMS.

After encapsulation a sample is ready for liquid gated experiments. In the next subsections we will discuss the methods of Si NW FETs characterization.

3.3 Si NW FET characterization

3.3.1 I-V characterization

The quality of the samples was controlled using I-V measurements on all stages of device encapsulation. The I-V measurements of the fabricated Si NW FETs include output characteristics (dependence of the drain current, I_D, on the drain voltage, V_{DS}, at different front and back gate voltages, V_{FG} and V_{BG}) and transfer characteristics (dependence of I_D on V_{FG},V_{BG} at different V_{DS}). Typical current-voltage characteristics of Si NW array FET with NW width of 250 nm and channel length of 10 μm are shown in Figure 3.6. Transfer characteristics are used for estimation of the threshold voltage and transconductance. Channel differential resistance can be evaluated using output curves.

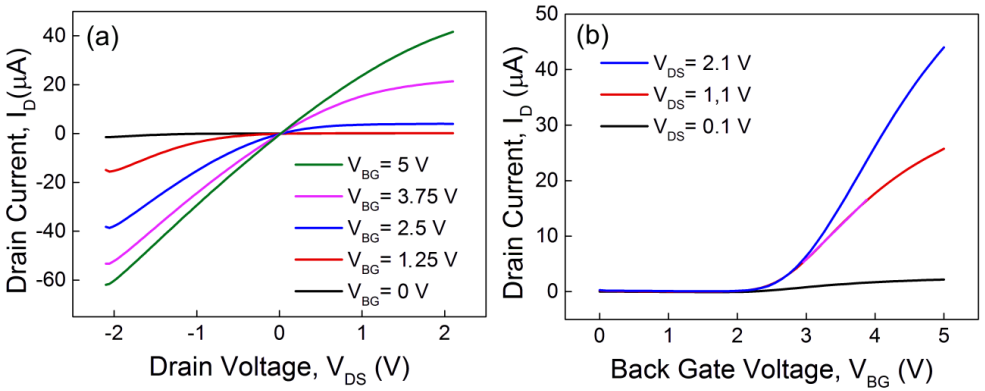

Figure 3.6 Typical output (a) and transfer (b) characteristics of Si NW array FET measured in air using back gate. The NWs width was 250 nm and the length was 10 μm, the FET consists of 50 NWs connected in parallel.

The I-V curves were measured using two Keithley source-measurement units of 2400 series and a custom software developed in-house. The sensitivity of such a setup is limited by the source-measurement units and is in the range of nanoamperes. The setup provides feature of measuring the gate leakage current during the I-V measurements. The samples with gate leakages were sorted out on the stage of encapsulation. After encapsulation of the samples and their preliminary characterization using I-V measurements, the noise spectroscopy was used in order to study transport properties and optimize performance of fabricated devices.

3.3.2 Noise spectra measurements

The main aspects of noise spectroscopy in Si NW FETs are given in Section 2.2. Here the setup for measuring noise spectra will be described. The schematic image of the noise measurement setup is shown in Figure 3.7. We do not show a part of the setup, which is responsible for applying voltage to the gate of the transistor, because its operation is similar to the block, which applies voltage to the source-drain contacts. As it is shown in Figure 3.7, the Si NW FET under study is contacted to the source and drain of the transistor and the fluctuations of the voltage on the device terminals is measured. The voltage is applied to the sample using a rechargeable battery and a variable resistor of 2500 Ohm. After the potentiometer the voltage is additionally stabilized with a large capacitor of 10 000 μF. The sample is connected in series with high precision variable resistor

R_{Load}. The value of R_{Load} can be adjusted with an accuracy of 1 Ohm. It is used for evaluation of current flowing through the sample.

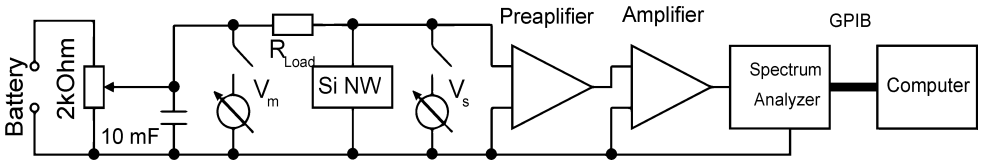

Figure 3.7 Schematic image of the noise measurement setup.

The drain current of the Si NW FET can be calculated using difference between readings of voltmeters V_m and V_s:

$$I_d = \frac{(V_m - V_s)}{R_{Load}}, \tag{3.1}$$

where V_m and V_s are readings of the voltmeters V_m and V_s from Figure 3.7. For the period of spectra acquisition the voltmeters are disconnected from the sample in order to avoid additional instrumental noise. Voltage fluctuation on the terminals of Si NW device are preamplified by our low-noise homemade amplifier (24 dB, input noise 2.2 nV^2/Hz at 100 Hz) and then amplified by Stanford low noise voltage preamplifier SR560. The amplified noise signal is then registered by HP35670 dynamic parameter analyzer and then transferred via GPIB interface to a PC.

The R_{Load} value defines the accuracy of the drain current evaluation using Eq.(3.1). The higher is the R_{Load} , the lower current can be registered. For example at R_{Load} of 100 kOhm currents of 0.1 nA can be registered. However the load resistance in parallel with the sample differential resistance together with a parasitic capacitance of the wires and amplifiers form a low pass filter, which may limit the measured signal at higher frequencies. The overall capacitance, which should be taken into account, is around C_p = 100 pF. If we assume that resistance of the sample is much higher than the load resistance, then for the case of R_{Load} =100 kOhm, the cutoff frequency will be:

$$f_{cutoff} = \frac{1}{2\pi\, R_{Load} C_p}\bigg|_{R_{Load}=100k\Omega, C_p=100pF} \approx 15915\ Hz \tag{3.2}$$

The value of 16kHz is already limiting the bandwidth, which is allowed by our spectrum analyzer and our amplifiers (0.1Hz to 100kHz). Therefore, the measured spectra are usually corrected, taking into account presence of the low pass filter.

The sample is connected in parallel to the load resistance in the AC mode (Figure 3.7) due to the shortcut through a battery and 10 mF capacitance, which has reactive resistance of 16 Ohms at 1 Hz. Therefore, the measured spectral density, $S_{V,}$ is a spectral density of connected in parallel load resistance and the sample. The equivalent resistance of the circuit is:

$$R_{eq} = \left(\frac{1}{R_{load}} + \frac{1}{R_{sample}}\right)^{-1}, \tag{3.3}$$

and Eq. (2.24) transforms into:

$$S_I = \frac{S_V}{R_{eq}^2} \tag{3.4}$$

The R_{eq} will determine also the value of the thermal noise in the circuit. The R_{Load} is selected from a tradeoff between current sensitivity and level of thermal noise and frequency cutoff. Usually the R_{load} is selected as the lowest load resistance sufficient to measure DC current with at least 10% accuracy. Such a requirement implements when the load resistance is in the range between 1/10 and 1/100 of the sample resistance.

Measured noise spectra are used to extract information about device performance and sensitivity. Careful characterization of the Si NW FET signal-to-noise ratio evaluation of the transistor equivalent input noise, which requires precise value of the device transconductance (Eq.(2.34)).

3.3.3 Transconductance measurements

The transconductance can be obtained from a transfer curve of the Si NW FET (see Eq. (2.13)). However, taking a derivative of the experimental curve decreases dramatically the accuracy, especially in the case when the density of points is relatively low. Noise measurements are time consuming and therefore usually measurements of 10-15 points per transfer curve are performed. Such amount of points is often insufficient to calculate precisely the transconductance. In order to overcome this complications we measure g_m using lock-in technique.

Figure 3.8 demonstrates a schematic for direct measuring of the NW transconductance. Stanford SR830 lock-in amplifier was used to apply AC signal to the liquid gate of Si NW FET and to detect the amplitude of the response in the channel of the NW FET.

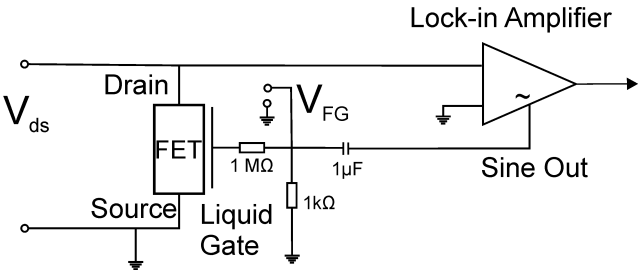

Figure 3.8 Schematic image of the lock-in technique for measuring the transconductance.

The small AC signal δV was mixed with DC component using high pass filter, which prevents DC voltage from dropping on the sine generator of the lock-in amplifier. The front-gate voltage, applied to the sample can be represented as superposition of DC component and small AC component:

$$V_{FG} = V_0 + \delta V sin(\omega_m t); \delta V \ll V_0, \tag{3.5}$$

where ω_m – is the frequency of the AC testing signal, V_0 – the DC component, which defines a transistor workpoint. δV is used in the range from 4 mV to 20 mV . Drain current is a function of the gate voltage:

$$I_D = f(V_{FG}) = f(V_0 + \delta V sin(\omega_m t)) \tag{3.6}$$

As the condition $\delta V \ll V_0$ is fulfilled, we can expand Eq. (3.6) into series:

$$I_D \approx I_D(V_0) + \frac{\partial I_D}{\partial V_{FG}} \delta V sin(\omega_m t) \tag{3.7}$$

As the result we get harmonic drain current fluctuations which can be detected using lock-in amplifier or spectrum analyzer. From the amplitude of the recorded signal we can recalculate the transconductance back, knowing the amplitude of the input signal:

$$g_m = \frac{\partial I_D}{\partial V_{FG}} \approx \frac{I_D(\omega)}{\delta V}\Big|_{\omega=\omega_m} \tag{3.8}$$

Measured value of transconductance is much more precise than calculated from transfer curve, especially in subthreshold region. In frame of current work we have compared both methods of

obtaining the transconductance as well as analyzed spectral behavior of the g_m in liquid-gated transistor.

3.3.4 Noise spectra fitting

After measuring noise spectra and transconductance, the spectra are fitted in order to extract separately different types of noise and their dependences on the measurement parameters. For this purpose we have developed custom software using C# programming language. The designed program is based on the program developed by Victor Sydoruk [160]. It includes additional features and works much faster due to implementation using .NET technology. The screenshot of the developed software is shown in Figure 3.9

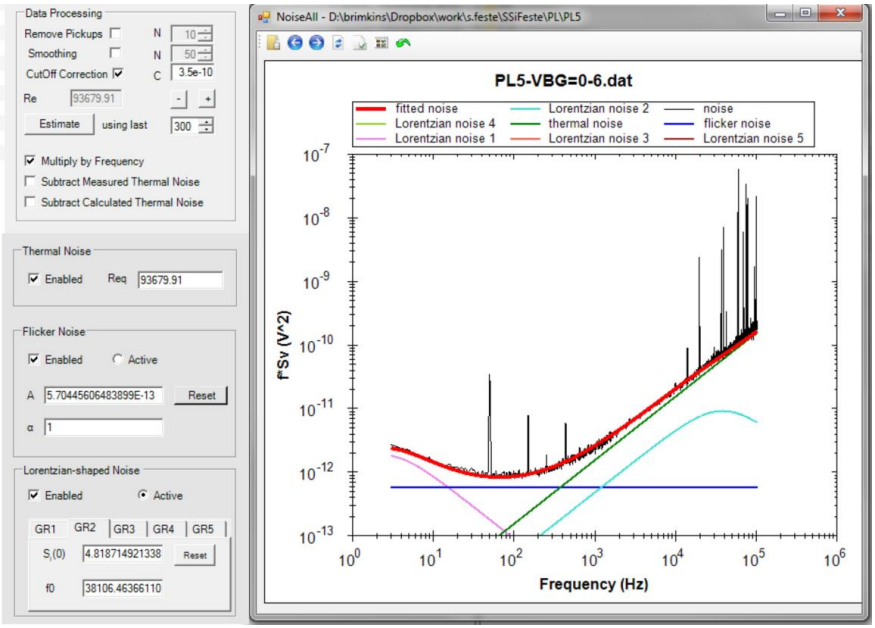

Figure 3.9 Screenshot of the developed program for fitting of the noise spectra.

The software allows fast processing of the noise spectra and includes following functions:

- Removing pick-ups from the noise spectra (unnecessary fluctuations induced by outer sources like 50 Hz and its mirrors)
- Smoothing the spectra

- R-C cutoff correction with function of automatic estimation of the scheme capacitance using least square method
- Subtraction of measured or calculated thermal noise in order to improve recognition of other types of noise
- Multiplying the spectra by frequency for improved recognition of flicker and GR noise components
- Fitting of the noise spectra (non-automatic) with superposition of flicker noise and up to 5 GR components

The developed software improves much the noise analysis process. It should be noted that the time spent for development of this software is less than the time already saved using this software for analysis of the noise spectra.

The methods described in this section allow measurements and further analysis of output and transfer characteristics of a FET, noise spectra in different operation modes, transconductance of a FET, time traces of the signal from a bio-object. The next section is devoted to the cell-culture experiments, which were performed in order to investigate interface between Si NW FET and neuronal cells.

3.4 Neuronal cells on silicon nanowires

3.4.1 Nanowire test pattern

For investigation of the interface between neuronal cells and Si NWs a special pattern was designed. A magnified part of the pattern is shown in the Figure 3.10. The pattern contains densely packed Si NW arrays and single nanowires of different dimensions (Table 3.1).

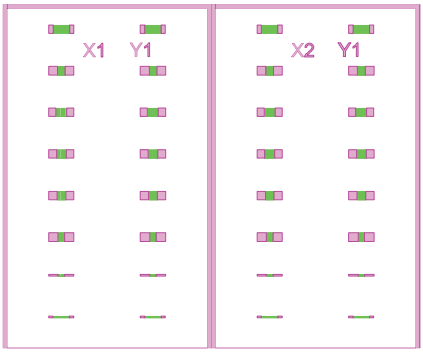

Figure 3.10 Zoomed part of the NW array pattern for investigation of Si NW/ neuronal cell interface. Pink color corresponds to the coarse pattern of e-beam writing and green color corresponds to the fine pattern.

3.4.2 Cell culture

The samples were prepared for the cell culture in several steps. First, the samples were sterilized using UV light. Then the samples were coated with 0.01 µg/ml polylysine (PLL) solution (the stock PLL solution of 10 µg/ml diluted in Grey's balanced salt solution 1:100) and kept overnight at 4 ºC. After that the samples were rinsed in DI water.

Rat cortical neurons were cultured on the samples [161] and the samples are put into the incubator with proper temperature and atmosphere. The experiments were performed on the 7th day or on the 10th day in vitro (DIV). During cell culture a half of the cell media was exchanged with fresh one every two days. Typical image of neuronal cells on Si NW structures is shown in Figure 3.11. In the field of view two neuronal cells growing directly on silicon NWs can be observed.

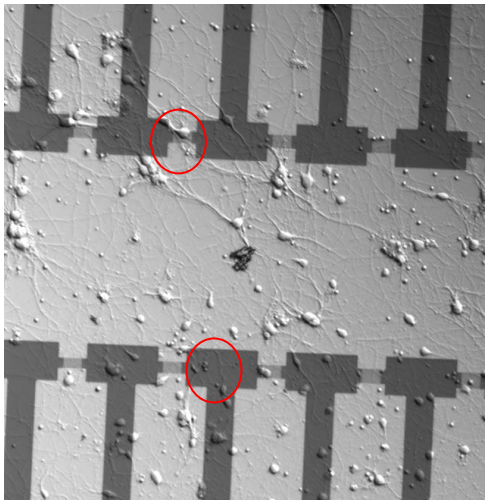

Figure 3.11 Optical image of area with neuronal cells grown on silicon NW structures after 10 DIV. Red circles show the cells directly growing on the NWs. For taking this image a differential interference contrast filter was used.

For evaluating the quality of the cell culture and selection of the cells for further investigation a live/dead staining was used.

3.4.3 Live/dead staining

The live/dead staining procedure uses special fluorescent dyes to distinguish between live and the dead cells under the fluorescent microscope. The procedure of staining is described as follows. The cell media of the cultured cells is exchanged two times with warm (37 ºC) phosphate buffer saline (PBS) and then acetomethoxy derivate of calcein (calcein AM) and ethidium homodimer-1 are added. The dyes are diluted 1/1000 by PBS. Calcein is a dye, which penetrates a cell membrane and becomes fluorescent due to interaction with intracellular ferments. It has excitation wavelength of 495 nm and its emission maximum is at 515 nm. Therefore living cells look green after using this dye. The ethidium homodimer-1 is a dye, which binds DNA, but can not penetrate a membrane of a cell. However, dead cells usually have a damaged membrane and ethidium homodimer can reach DNA inside a dead cell. The excitation wavelength is 528 nm and emission maximum is at 617 nm. The staining procedure lasts 15 min and then the staining solution is washed away with warm PBS. Then the fluorescence images are made using different light sources and filters. The dyes are toxic for the cells, therefore the experiment is done within 1 hour

after staining. Typical staining image is shown in Figure 3.12. Such images are usually combined from different channels with different optical filters(green, red, blue).

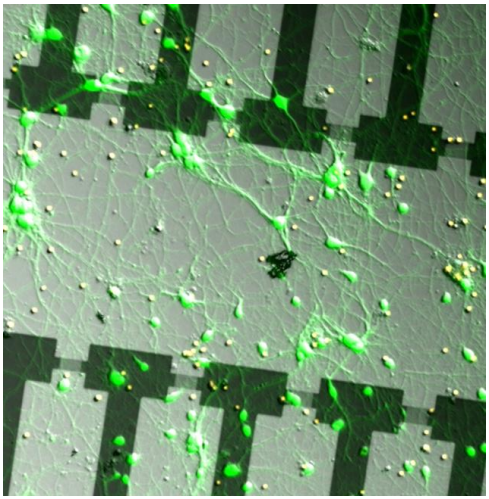

Figure 3.12 Live-dead staining of the neurons on Si NWs after 10 DIV. The figure is combined of three images: green – live cells, stained with calcein, yellow – dead cells stained with ethidium homodimer and grayscale – the differential interference contrast.

Investigation of the interface between the cells and Si NW FETs was performed using focused ion beam (FIB) and scanning electron microscopy (SEM). For the SEM imaging the cells should be fixed using a special procedure to preserve the shape of the cell.

3.4.4 Cell fixation

The protocol for cell fixation and drying was provided by Francesca Santoro. The cell fixation was performed with the neuronal cells after 10 DIV on Si NW structures. To fix the cells the cell media is exchanged with warm PBS two times. Then pure PBS is exchanged to 3.2% glutaraldehyde solution in PBS for 1 hour. After fixation the cells were washed with pure PBS again and then dehydrated by subsequent immersing into ethanol solutions (from 10 % to 100%), 10 min in each solution. After that the samples may be kept in ethanol for long time. In order to investigate the cell morphology and interface between the cells and Si NWs, the ethanol is removed using critical point drying technique [162]. Typical SEM image of the single cell on the NW structures is shown in Figure 3.13.

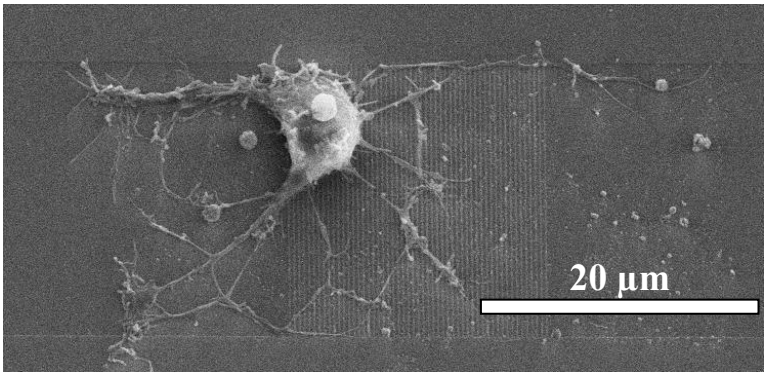

Figure 3.13 SEM image of a neuronal cell fixed on the array of silicon nanowires.

The cross-section of the neuronal cells on Si NW FETs will be discussed in detail in Results and Discussion chapter.

3.5 Summary

The materials and methods discussed in this chapter were used to conduct most of the experiments in presented work. The first single NW FETs were obtained from collaborators. These NW structures were studied from the point of view of planning and design of our Si NW array FET devices.

4. Results and discussion

4.1 Silicon nanowire FETs based on single wire

4.1.1 Introduction

In this section we demonstrate investigation of the Si NW FET properties. As it will be shown below, we reveal a strong modulation effect by a single trap situated near the NW channel in the gate dielectric. This effect reflects extremely high sensitivity of the NW transport to the changes of the electric charge on the surface of the NW. Then a sensitivity of Si NW to the changes of the surface potential will be discussed, because Si NW FET should provide sufficient voltage sensitivity in order to provide extracellular registration of the neuronal action potentials. In the next part of the subsection, the role of the electrolyte in the transport and noise characteristics is studied. As it will be shown in the overthreshold mode the liquid gated FET is similar to a MOSFET, which allows using all the noise spectroscopy experience accumulated for the CMOS technology for enhancing performance of the fabricated NW structures. In order to improve understanding of the transport properties of liquid-gated NW FETs and study the factors influencing SNR of such structures, we perform theoretical modelling of the NWs with considering different charge carrier distributions, effects of contact resistance and mobility degradation. The spectral behavior of the NW FET characteristics is studied to find the range of frequencies, where the signals are passing the FET undisturbed. And now we will start the section with estimation of charge and voltage sensistivity of single NW structures.

4.1.2 Charge and voltage sensitivity of Si NWs

Silicon nanowire structures provide high surface-to-volume ratios. Therefore the current in the Si NW FET is determined by the much lower quantity of carriers than in conventional CMOS FETs due to the small device size. It results in higher fluctuations of the conductivity and as well in higher transport modulation of the NWs. Extracellular recording from elecrogenic cells requires detection of small changes of the gate surface potential (down to 100 μV) in a frequency range between 1 Hz and 10 kHz, as we have shown in subsection 2.3.3. To be able to distinguish such a response under the level of native fluctuations of a Si NW, a comprehensive investigation of transport in Si NWs has to be performed. The analysis of the fluctuations in the Si NW FETs combined with I-V characterization contains the information about performance and transport phenomena in the device. This information is of extreme importance for device development and

further improvement of the fabrication technology. In this part of presented work we use noise spectroscopy and reveal a strong modulation of the channel conductivity under the influence of a single trap. Analysis of the 1/f component of the excess noise was used to estimate the value of the volume trap density in the thin dielectric layer for the measured samples. The investigated Si NW FETs demonstrate high quality of the device performance. The Lorentzian components of the noise spectra are registered and their behavior allows the trapping/detrapping processes on the gate dielectric traps to be characterized. The parameters of the single trap, which generates the RTS noise, in the gate dielectric layer were determined. The result of this subsection demonstrates high charge sensitivity of Si NW FETs.

The structures under investigation in this subsection are p-type NW-FETs with a cross-section of 42x42 nm^2 fabricated at Forschungszentrum Julich in group of Prof. Mantl using a top-down approach on the basis of 50 nm SOI wafer (N_A=1x10^{15} cm^{-3}, buried oxide thickness of 140 nm). An N-type polysilicon gate electrode was deposited on the 5nm thermally grown SiO_2 gate oxide layer, which covered each of the NWs. Source/drain contacts to NWs were formed by ion implantation of boron with an energy of 10 keV and a dose of 1x10^{15} cm^{-2} followed by rapid thermal annealing. Thus, the samples represent transistors with accumulation p-channel. The polysilicon covers the NW channel to form a tri-gate (Figure 4.1) in the middle part of the NW channel.

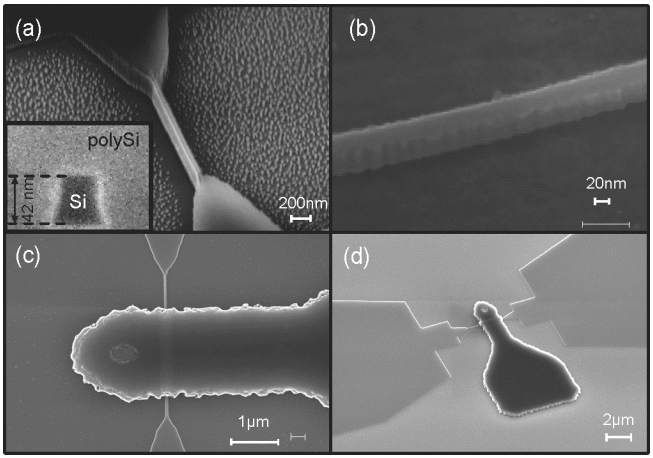

Figure 4.1 SEM images of silicon nanowire device. (a), (b) Si NW top and side view; (c), (d) SEM image of Si NWs with polysilicon gate. Inset in (a): focused ion beam cut of the wire under study.

The tri-gate configuration offers improved gate control over the channel compared to planar geometry and reflects a behavior of Si NW with liquid gate as well, because an electrolyte is surrounding the NW offering almost gate-all-around operation. The transistors are in the off-state at zero biases on the front gate and substrate, which plays the role of back gate. The current through the samples can be tuned either by front gate or by back gate voltages. We investigated noise spectra of NW-FET devices with lengths of 1.5µm and 3µm under different regimes defined by drain- source biases, V_{DS}; front-gate voltages, V_{FG}; and back-gate voltages, V_{BG}.

The output curves of the investigated samples are shown in Figure 4.2. Their behavior is characteristic for metal-oxide semiconductor devices. It should be noted, that all noise spectra were measured at low drain bias (around 100mV), which provides a linear mode of operation of the transistors in almost the entire range of gate voltages (Figure 4.2).

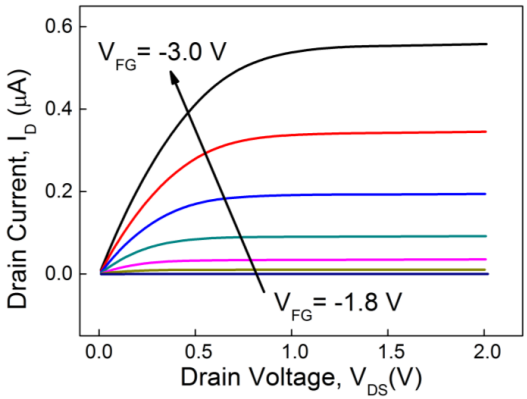

Figure 4.2 Typical output characteristics of one of the investigated NW samples. Back-gate voltage: $V_{BG} = 0$.

Transfer I-V characteristics for the 1.5µm and 3µm samples are shown in Figure 4.3(a). The curves reflect the reproducible scaling with respect to the length of the samples. Typical maximum transconductance values, $g_{m_{max}}$, for 3µm and 1.5µm samples are 1.3×10^{-7} and 2.7×10^{-7} A/V,

respectively. The threshold voltage (V_{th} ~ -1.95V) is mostly the same during all measurements. The current in the samples shows much weaker dependence on back-gate voltage (Figure 4.3(b)) compared with front-gate voltage. This is due to the fact that the buried oxide is significantly thicker than the front-gate oxide layer.

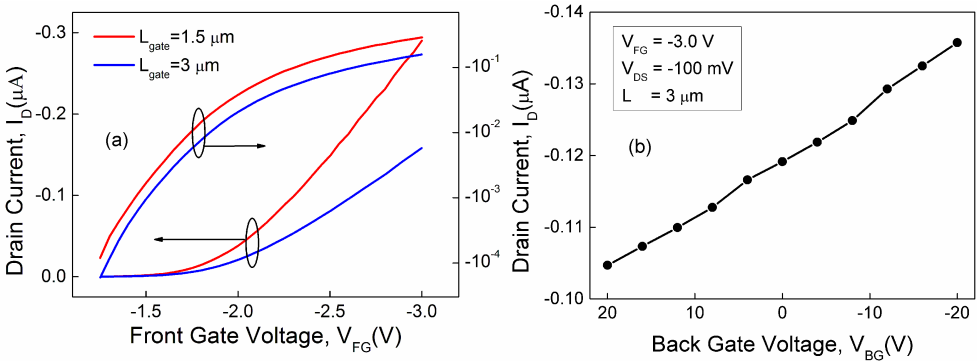

Figure 4.3 Transfer curves of the samples with different lengths (1.5 μm and 3 μm) at a drain bias of -100mV measured as a function of front gate voltage at zero back gate voltage; (b) Transfer curves of the sample of the 3μm length versus back-gate voltage at a drain bias of -100mV and front-gate voltage of -3 V.

Typical noise spectra of one of the samples measured at several front gate voltages are shown in Figure 4.4. The spectra contain two noise components: 1/f and Lorentzian shaped.

As we have discussed in the Section 2.2 the volume trap density of the gate dielectric layer can be estimated using the measurements of noise spectra and I-V characteristics. This density of traps reflects the quality of the gate dielectric and can be compared for different dielectric layers to optimize the dielectric compositions for miniaturization of the final device. During the process of device downscaling (i.e. from micron width to the submicron scale), at some size even the response of the single traps can be registered. In this case, excess noise contains not only the flicker noise component but also a number of separate Lorentzian components. At a certain level of downscaling the device size approaches a limit, at which one or several traps in the dielectric modulate the current. In this case, the signal as a function of time in the device demonstrates the RTS noise behavior. Analysis of the RTS spectra and time trace allows us to investigate the parameters of the individual traps of nanoscale devices. Individual molecules can play the role of a single trap on the surface of the device, which in this case may be used as the molecule sensor. Equivalent input

spectral density is used to calculate volume trap density. We have used the 1/f noise current spectral density (S_I) component to calculate the S_U value. Typical S_U dependence calculated for investigated samples is shown in Figure 4.4(b) for different channel length. The equivalent input power spectral density demonstrates a weak dependence on gate voltage, which indicates that the McWhorter model is applicable for estimating the volume trap density of the gate oxide.

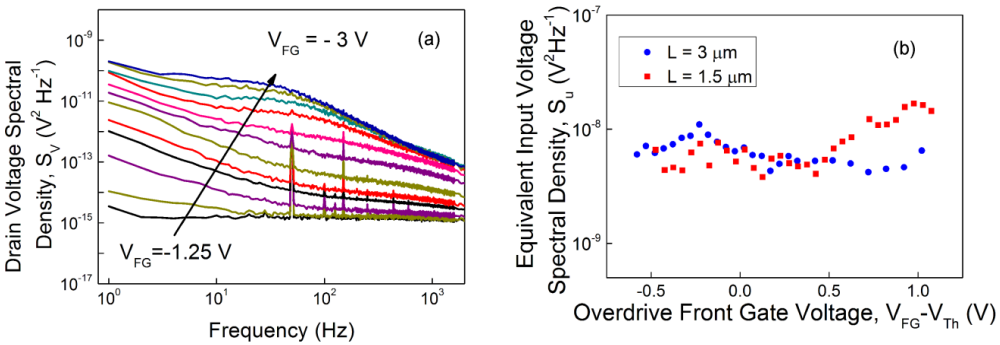

Figure 4.4 (a) Noise spectra measured for 3μm sample at different front gate voltages at a drain-source bias of 100mV; (b) Equivalent input voltage spectral as a function of overdrive gate voltage (V_{FG}–V_{Th}) at frequency of 1 Hz.

According to Eq. (2.32) and (2.34) the trap density, N_t, can be calculated as follows:

$$N_t = \frac{S_U \alpha_t C_{ox}^2 WLf}{q^2 kT} = \frac{S_I \alpha_t C_{ox}^2 WLf}{g_m^2 q^2 kT}, \tag{4.1}$$

where α_t is the inverse tunneling depth, which is defined using λ from Eq. (2.33), C_{ox} is the specific gate oxide capacitance, W is the channel width, L is the channel length, f is the frequency, q is the electron charge, k is the Boltzmann constant and T is the temperature. In our case, T is about 293K.

Using Eq. (4.1) we estimated the value of the volume trap density for all measured samples. The obtained values are within the range from $1x10^{17}$ cm^{-3} eV^{-1} to $5x10^{17}$ cm^{-3} eV^{-1}. It should be noted that these values are about one order of magnitude lower than those obtained for submicron CMOS devices [136] . By multiplying the obtained values of N_t by the oxide thickness d_{ox}, we obtain surface trap densities for our samples. They are in the range between $5x10^8$ cm^{-2} eV^{-1} and $2.5x10^9$ cm^{-2} eV^{-1} .The densities are much lower than estimated for the thin film dielectric layers of MOS transistors[163].

Investigation of the time traces of the noise signal measured using the samples under study showed that the low-frequency Lorentzian components in noise spectra is caused by a RTS noise (Figure 4.4(a)). The RTS noise is a characteristic feature of low-scale samples taking into account that 1/f noise from the point of view of the McWhorter theory or a unified model can be represented by superposition of GR processes uniformly distributed by its parameters. In the case of large-area samples, the multiple dielectric traps, equally randomly distributed by energy and depths, result in a 1/f spectrum of the excess noise. At some characteristic size (tenths of nanometers) of the transistor channel, it is quite probable that the noise of the channel can be impacted by a single trap in the gate dielectric. In this case, the RTS noise, which dominates the flicker noise may be observed. As it was discussed earlier in Section 2.2.3, the individual oxide trap is of the same nature as the traps that are responsible for 1/f noise. The spectra of both components, Lorentzian and 1/f noise, can be analyzed separately [140], [164]. The flicker noise separated into single Lorentzian noise components represents a remarkable opportunity to investigate the single trap properties and predict the properties of samples with a large number of traps in the gate dielectric. In our case, the RTS noise was registered for the samples with different lengths for a wide range of applied gate voltages.

The RTS time trace contains the capture and emission time constants of a single trap. Using these data, the capture cross-section of a trap and its position in the gate oxide layer can be calculated. Figure 4.5(a) shows the typical time trace of measured RTS noise. We used a statistical method to calculate the capture and emission time on the basis of these data[165]. If the voltage time trace contains two well-resolved levels, we can construct a histogram of voltage values (shown in Figure 4.5(b)). Histograms of RTS time traces, obtained for different front-gate and back-gate voltages, are shown in Figure 4.6. Figure 4.6 (a) and (b) contain time traces of registered RTS noise, which corresponds to GR components of Figure 4.4(a). The measurements were performed at constant V_{BG} = 0 V (Figure 4.6 (a)) and at constant V_{FG} = -3 V (Figure 4.6 (a)). Figure 4.6 (a) demonstrates that the values of capture and emission times depend on the front gate voltage. In contrast, RTS traces of Figure 4.6 (b) express negligible dependence on the back gate voltage. We can conclude that the single trap, which causes the RTS modulation of the sample conductivity, is located in the top gate dielectric, because back gate voltage has no impact on the registered RTS.

The ratio of peak heights corresponds to the relation between capture and emission times (τ_c/τ_e). The height of each peak is related to the time that the system spends in each state. The

distance between the peaks equals the RTS amplitude ΔV, which can be recalculated into the ΔI_D using equivalent resistance of the sample and load resistance (see Eq. (3.3)).

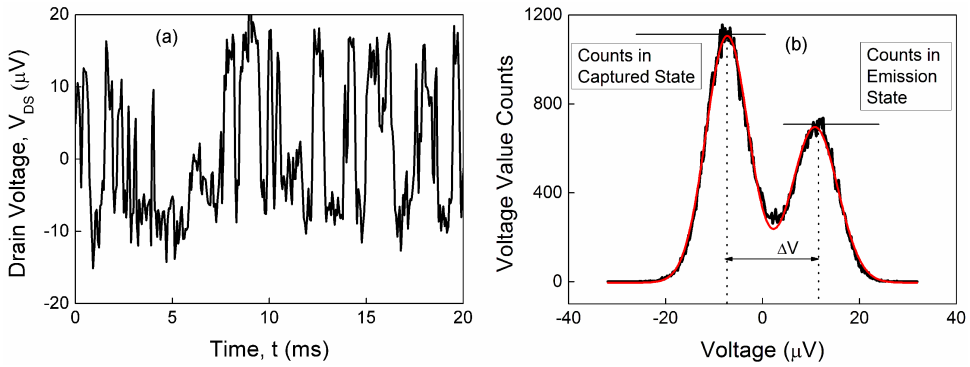

Figure 4.5 (a) Random telegraph signal noise time trace measured for 3μm sample at V_{DS} = -100 mV, V_{FG} = -3 V; (b) Histogram of the voltage values from the time trace (a).

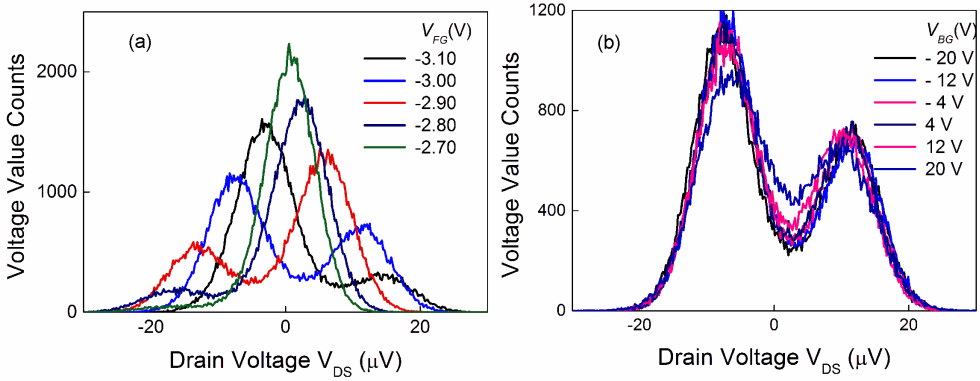

Figure 4.6 Histogram of the RTS noise time trace of the 3μm sample: (a) at V_{BG} = 0 V and at V_{FG}; (b) at V_{BG} and V_{FG} = - 3 V

The time constant τ of the Lorentzian spectra, which corresponds to the RTS noise is expressed through τ_c and τ_e as in Eq. (2.40). Using the τ_c/τ_e relation obtained from the Figure 4.5(b), Figure 4.6(a) and the value of τ obtained from the spectra (Figure 4.4(a)), the values of τ_c and τ_e can be evaluated. Figure 4.7(a) demonstrates calculated values of τ_c and τ_e plotted versus the overdrive gate voltage. Using obtained parameters of RTS noise and combining them with I-V

characterization the trap parameters such as depth, position along the channel and capture cross-section can be obtained. In order to find the position of the trap in the gate oxide we investigated the dependence of the τ_c/τ_e relation on front-gate voltage. The distance of trap from the interface between the gate oxide and silicon channel is calculated as follows[140], [141], [166]:

$$x_t = -d_{ox}\frac{kT}{q}\frac{d\left(\ln\left(\frac{\tau_c}{\tau_e}\right)\right)}{dV_{FG}}. \tag{4.2}$$

As discussed above, the relation between capture and emission times can be obtained directly from the histograms of the RTS time trace. This relation is shown in Figure 4.7(b), as a function of overdrive gate voltage. Eq.(4.2) can be used to find the trap depth, as the dependence in Figure 4.7(b) is close to linear. The d_{ox} was 5 nm for the investigated samples. The least squares fit of the data shown in Figure 4.7(b) gives the estimated trap depth x_t in the range from 1.65 nm to 1.85 nm for all measured samples.

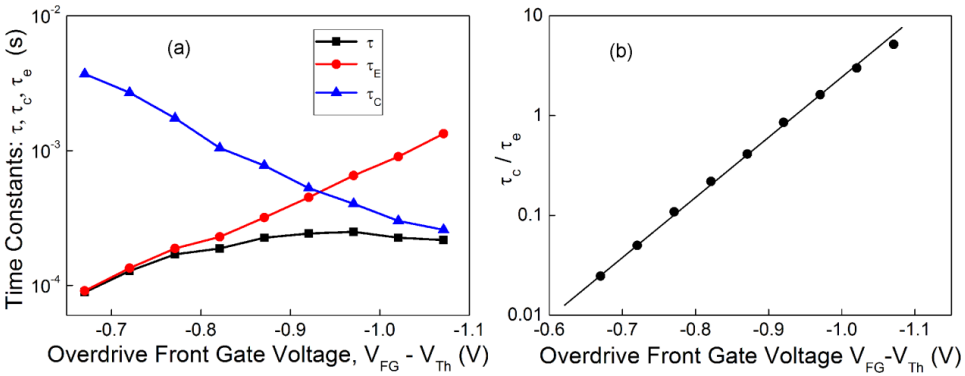

Figure 4.7 (a) Time constant τ (black line) of the Lorentzian noise component, capture time constant τ_c (blue line) and emission time constant τ_e (red line) obtained from Figure 4.6(a) and Figure 4.4(a) and plotted as a function of overdrive gate voltage. (b) Calculated ratio between capture and emission times plotted versus overdrive front-gate voltage.

The dependence of the time constants of the RTS noise on the source-drain bias contains information about the position of the active trap along the channel length. We investigated the noise of the samples in the nonlinear regime at a fixed front-gate voltage of V_{FG} = - 3.0 V and different channel biases V_{DS} = -0..-2.0 V (Figure 4.8). In addition, measurements were also made for the reverse polarity of the drain-source bias. Increasing the drain voltage V_{DS} leads to the channel

pinch-off and "scans" the channel with high-field region (Figure 4.2). With increasing bias voltage on the transistor channel, the gate dielectric potential, which forms the channel, decreases from $\Phi_s = V_{FG}$ near source to the $\Phi_s = V_{FG} - V_{DS}$ near the drain. Figure 4.8 shows that the time constant of the Lorentzian components (Figure 4.4(a)) determined by the RTS noise component decreases with increasing the drain voltage. As we have already discussed above, increasing the drain voltage decreases the Φ_s near the drain down to the value of $V_{FG} - V_{DS}$ and hence it decreases the concentration of carriers in the inversion channel near the drain electrode. These facts indicate that the Lorentzian component of the noise spectra is mainly determined by the capture time constant, τ_c (Figure 4.7(a)). Indeed, a decrease of the concentration of free carriers in the channel causes the increase of the capture probability of free carriers to the centers located in the dielectric layer and, consequently, leads to a decrease in the capture time constant from 2.5×10^{-4} to 5.0×10^{-5} s.

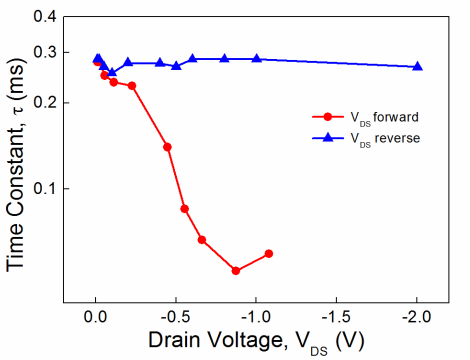

Figure 4.8 Time constant of the Lorentzian component of the noise spectra of the sample plotted versus drain voltage at $V_{FG} = -3.0$ V, $V_{BG} = 0$. Red circles correspond to the GR processes at forward polarity (source is grounded, and drain is biased) of the channel bias; blue triangles correspond to the GR-process at the reverse polarity (drain is grounded and source is biased).

In the case of a reverse bias of the Si NW transistor, we can see from Fig. 10 that the time constant does not depend on the drain voltage. This fact demonstrates that there are no changes in the concentration of free carriers near the corresponding capture center. Such behavior of the time constant is only possible if the center is located at a site where the influence of the applied drain voltage is negligibly small (where the gate dielectric potential Φ_s is constant and does not depend

on V_{DS}). Thus, we conclude that the dielectric trap, which generates the RTS noise in the investigated sample, is located in the gate dielectric layer close to the drain of the Si NW transistor.

The obtained RTS parameters allow a capture cross-section of the dielectric trap to be estimated. According to the Shockley-Reed-Hall theory, capture and emission times can be calculated using Eq. (2.39). The thermal speed of carriers is equal to:

$$v_{th} = \sqrt{\left(\frac{3kT}{m^*}\right)}, \tag{4.3}$$

where m^* – is the effective mass of the carriers. Taking into account that T = 293 K and the carriers in the FETs under study are mainly represented by holes with the effective mass equal to 0.56 of the electron mass, the thermal speed is equal to 1.55×10^5 m/s. Then the value of the capture cross-section can be estimated using Eq. (2.39). Such calculation also requires value of carrier concentration, which can be obtained from transfer curves in Figure 4.3 and Eq. (2.15). The calculated values of hole concentrations are shown in Figure 4.9(a). As we can see, the concentrations are the same for the samples with different lengths fabricated on the same wafer. This fact reflects high quality of the analyzed samples. Sublinear behavior of concentration at V_{FG} < -2.5 V appears because contact resistance and possible mobility degradation are not taken into account in this estimations. The role of contact resistance and mobility effects will be shown later in the section 4.1.4. Using Eq. (2.14) and data of Figure 4.3(a), we estimated hole mobility for NW samples to be in the range from 120 to 150 $cm^2\ V^{-1}s^{-1}$, which is in good agreement with values in literature [167].

Calculated value of capture cross-section is shown in Figure 4.9(b). It exhibits strong dependence on overdrive gate voltage. Such a behavior of capture cross-section is also testified by increasing of the emission time with overdrive gate voltage (Figure 4.7(a)). Increasing of the capture cross-section with overdrive gate and thus the carrier concentration can be explained in the frame of Coulomb blockade model [143], [168]. Indeed, increasing concentration of carriers in the vicinity of a trap leads to decreasing of the capture time and hence to higher probability of the trap to be occupied. The occupied trap is charged and it gains therefore additional energy which originates from mirror forces induced in the conducting channel as a reaction to the charged trap near the channel surface. According to this speculations a phenomenological parameter of coulomb blockade energy, which is gained by a trap after getting charged, is included into SRH theory[169]:

$$\tau_c = \tau_{c_0} e^{\frac{\Delta E}{kT}}, \tag{4.4}$$

where ΔE represents the coulomb blockade energy. The value of ΔE is defined by geometry of the samples and concentration of the carriers in the channel.

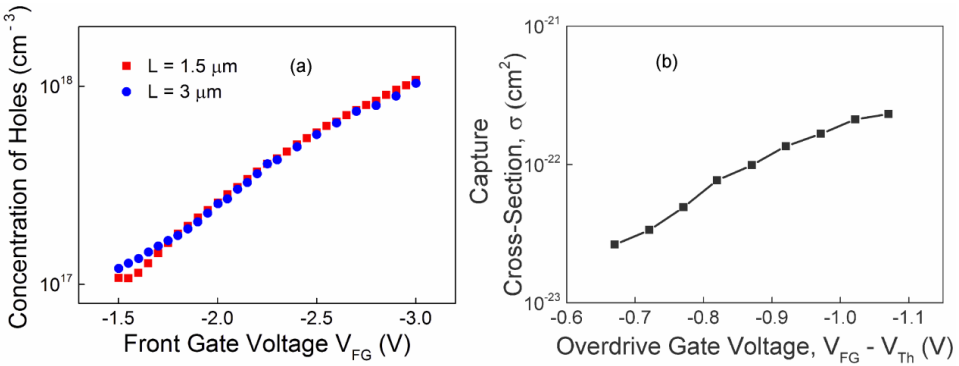

Figure 4.9 (a) – Calculated concentration of holes as a function of applied front gate voltage. (b) – Dependence of the calculated effective capture cross-section of the trap on the overdrive gate voltage.

The amplitude of RTS fluctuations is also an important value, which reflects the impact of a single surface charge on the channel conductivity[148], [170]. Dependence of the amplitude ΔI of the RTS fluctuations calculated from Figure 4.6 is shown in Figure 4.10. The amplitude is nearly constant in the observed range of front-gate voltages and equals 0.20±0.01 nA.

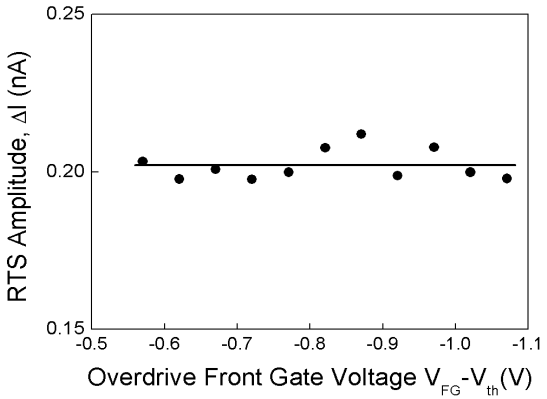

Figure 4.10 The amplitude of the RTS noise plotted versus the overdrive front-gate voltage at V_{BG} = 0, V_{DS} = -100 mV.

Capture of a free carrier on the fixed trap in the dielectric excludes it from the conductivity. The charged state of the trap results in shielding of part of the channel. At constant voltage V_{DS} applied to the channel, the exclusion of fixed charge in the regime of strong inversion leads to a decrease in the current ΔI and this decrease depends only on amount of excluded charge. Therefore, we can also conclude that the mobility remains constant in this range of gate voltages. If we assume that only one carrier is excluded from the channel during the capture and effects trap charging are negligible, then we can write:

$$\Delta I = I(N+1) - I(N) = \frac{1}{V} e\mu ES = \frac{1}{V} e\mu \frac{V_{DS}}{L} S = \frac{e\mu V_{DS}}{L^2}, \quad (4.5)$$

where N is the quantity of carriers, L – is the the channel length, S – is the area of the channel cross-section, V – is the volume of the device, which equals LS, μ – is the mobility of the holes. Using Eq. (4.5) the mobility of holes for the sample can be estimated, because we have the value of ΔI. However, the value calculated using such a method will exceed 1000 cm^2/ (V s), which makes no sense for the hole mobility in silicon devices. Thus, we can conclude that capture of the free carrier on the traps causes a modulating effect on current in the NW channel and capture of one hole considerably modulates current in the channel. If the trap has captured a hole, then more than one hole is excluded from the transport in the transistor channel due to field effect of the trap. This fact demonstrates high charge sensitivity of Si NW transistors and possibility of single molecule detection using the modulation effect of the channel conductivity in Si NW FET.

Let us now estimate voltage sensitivity of such a transistor considering only flicker noise and thermal noise components. The interesting frequency range for registering signals from electrogenic cells is between 1 Hz and 10 kHz. Using the data of Figure 4.4(b) we can assume that S_u of the flicker noise at 1 Hz is a weak function of the gate voltage and is about 10^{-8} V^2/Hz. From Figure 4.3(a) we know that maximum transconductance in the linear mode is $g_{m_{max}} = 2.7 \times 10^{-7} A/V$. Then using Eq. (2.34) we can estimate level of S_I for the flicker noise at 1 Hz. It equals 7.3x10^{-22} A^2/Hz. The thermal noise of defined by the equivalent resistance of the sample and load resistance, which was equal 100kOhms in this experiment. According to Figure 4.3(a) resistance of the samples was 300kOhms and higher. Therefore for our calculations we will take R_{eq} of 90 kOhm. Then using Eq. (2.26) the thermal noise level is estimated to be 1.8x10^{-25} A^2/Hz. Having

all the calculated values, the level of the device sensitivity can be estimated using Eq. (2.19). As a value, which defines the device voltage sensitivity, we suggest the limit voltage, δV_{limit}, which can be detected with SNR of 1:

$$\delta V_{limit} = \frac{\sqrt{\int_{1\,Hz}^{10\,kHz}(S_{I_{flicker}} + S_{I_{thermal}})df}}{g_m}, \tag{4.6}$$

For defined here parameters δV_{limit} equals 250 μV, which is already close to the range of interest for the electrogenic cell measurements. However such an estimation is not precise and the value of δV_{limit} is underestimated, because the GR components are not taken into account (Figure 4.4). Besides that, the length of the sensors for the neuronal cells should be at least 10 μm in order to fit cell dimensions. Therefore voltage sensitivity of a NW sensor should be at least 10 times higher than for the case of a single NW FET.

To sum up, we have investigated the Transport properties of p-type silicon nanowires FETs (with a cross-section of ≈ 42x42nm2 fabricated at Forschungszentrum Jülich) utilizing noise spectroscopy. Studied devices exhibit stable scalable characteristics. The values of volume trap density obtained from the level of equivalent input voltage noise. The devices with different channel lengths have almost the same equivalent input voltage spectral density indicating that the influence of contact effects on the performance of the investigated devices can be neglected. Analysis of the registered RTS noise component reveals that a single trap is located near one of the ohmic contacts in the gate dielectric. Estimated parameters of the trap and its behavior demonstrate that even a single carrier process in the gate of the NW transistor considerably modulates current in the channel. The devices have shown high charge sensitivity and good voltage sensitivity, which is though not enough for extracellular monitoring of electrogenic cell activity. The results are promising for advanced control of the channel transport in NW FETs, including the possibility of single molecule detection with increased sensitivity using the modulation effect of the channel conductivity in Si NW FET.

4.1.3 Influence of the liquid gate electrolyte on Si NW transport properties

In this subsection the influence of the electrolyte on transport properties of the Si NW FET biosensor is considered. NWs of different lengths were used to investigate the effect of the electrolyte on channel conductivity. Noise spectroscopy was employed to characterize the

performance of the Si NW FET biosensors operated via back gate with the electrolyte solution on top and without it. The influence of the electrolyte on transport was studied by changes of the device transport and noise characteristics. The results show that the electrolyte solution not only influences the threshold voltage of the transistor, but also affects the charge state of the surface traps.

Transport and noise properties were measured and analyzed in Si NW FETs produced by Jing Li in the group of Svetlana Vitusevich. The nanowires were of 500nm width and a variety of lengths from 2 to 16μm (Figure 4.11). The nanowires were produced on the basis of silicon-on-insulator (SOI) wafers using nanoimprint technology with subsequent wet chemical etching of the NW structures. The contact feedlines of the NWs were As doped and represented the n^+-p-n^+ type of FET with an inversion channel. The layout of chips with NWs was as in Figure 3.1. The NW sensors were protected from the electrolyte by a thin thermally grown SiO_2 passivation layer (10nm thickness). The measurements were performed with the phosphate-buffered saline (PBS) electrolyte on top of the passivation layer of the NW FET structure and without electrolyte (in air) at different back-gate voltages, V_{BG}. The back-gate voltage, V_{BG}, was applied to the substrate of the silicon-on-insulator (SOI) wafer. The schematic of the experiment was as it is shown in Figure 2.4. The V_{DS} was set to 100 mV in order to maintain a linear regime of operation of the NW transistor. In this regime, the differential resistance of the sample equals the normal value of resistance, which makes it much simpler to evaluate the normalized current noise spectral density, S_I / I^2, using the measured drain voltage noise spectral density. It should be noted that the noise spectra and the I-V curves were measured in a constant DC mode. The drain voltage, V_{DS}, and back-gate voltage, V_G, were applied using a battery loaded with the sample and a load resistance (Figure 3.7).

The transfer characteristics of the Si NW transistors were measured in DC mode in air and in electrolyte (Figure 4.12). These I-V curves were measured using noise measurement setup. The drain current, I_d, controlled by the back-gate voltage is higher in air than in the electrolyte in the overthreshold mode, at $V_G > V_{Th}$ (Figure 4.12 (a)). In electrolyte current is higher than in air in subthreshold mode: $V_G < V_{Th}$ (Figure 4.12 (b)). It should be noted that each point of the transfer characteristics was measured at a stabilized drain current. There is a certain time, which is needed for current to get stable. After the back-gate voltage was applied, the drain current increases with time until it reaches a certain saturation value. The time between applying the gate voltage and saturation of the drain current was around 20 min in the case of air and around one minute in the

case of electrolyte. The leakage current through the back-gate electrode was negligibly small (below 0.1nA).

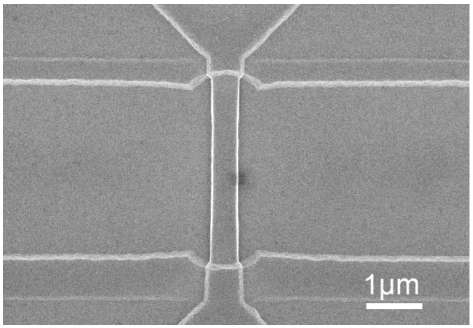

Figure 4.11 – SEM image of a 500 nm wide and 5 µm long silicon nanowire. The SU8 passivation layer, which covers silicon feedlines can be observed.

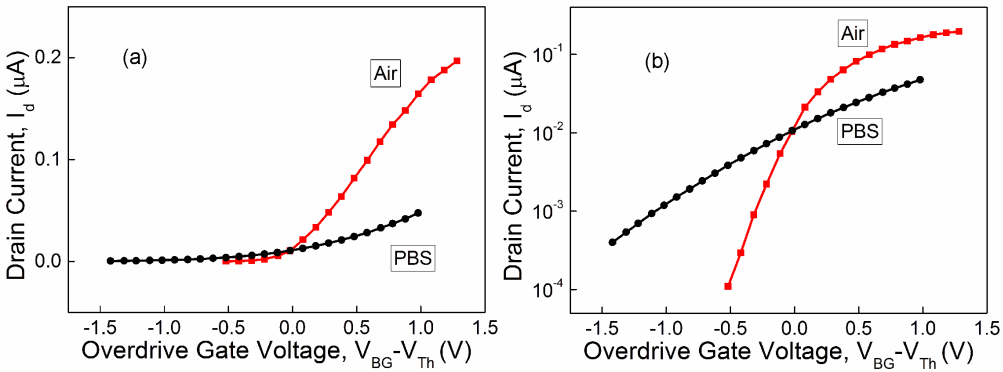

Figure 4.12 Transfer curves of the 8µm Si NW FET measured in air (red curves) and in PBS (black curves) plotted versus overdrive back gate voltage in linear (a) and logarithmic scale (b).

We suggest that such an effect is related to charging of the traps located in the top dielectric layer via back-gate electrode[171]. The time constant of such a process is as large as 20 min because the traps are charged with extremely small currents through the back-gate dielectric. The decrease of the charging time in the electrolyte can be explained by the charge screening effect.

The charges accumulated in the top passivation dielectric are immediately screened by the ions of the electrolyte solution. Therefore the channel conductivity becomes stable after setting gate voltage much faster at the presence of electrolyte than in air. However the influence of the back gate on the channel is reduced by screening effect of the electrolyte. The slope of the transfer curve is higher in air than in the PBS solution (Figure 4.12(a)). Such a difference can also be explained by charging the top dielectric layer through the back gate and the screening effect in the electrolyte. In the subthreshold region (Figure 4.12(b)), we can observe that the subthreshold current in the electrolyte is higher than in air. As mentioned above, all measurements were performed at low drain voltages (100mV). In such a regime, the subthreshold current is not related to transport through surface states, but is mainly defined by diffusion [110]. The increase of the subthreshold current in PBS solution can again be explained by screening of the potential of the top dielectric layer by ions in the electrolyte. In the subthreshold mode, negative overdrive gate voltages are applied to the sample, and screening of the negative overdrive potentials by ions in the electrolyte means shifting the surface potential to zero, which, in turn, leads to an increasing drain current. The curves measured in air and in PBS solution coincide in the vicinity of the zero overdrive gate, which implies that the screening does not occur at this point and that the zero overdrive gate voltage is close to the flat-band point. Therefore we can conclude that introducing PBS on top of the NW affects transport in the transistor through screening of the surface potential of the top dielectric layer[37].

Behavior similar to that described above is also registered in the samples with different channel lengths. The drain current with the same value of the overdrive gate voltage, $V_G–V_{Th}$, is plotted versus the channel length of the device in Figure 4.13. The drain current is well scaled with the length of the sample (Figure 4.13(a) in air and Figure 4.13(b)). Contact resistance can be estimated from the dependence of the drain current on length by linear approximation (Figure 4.13(a) in air). The value obtained is in the range between 8 and 12 kOhm for different measured chips, which is much lower than the device channel resistance, even when it is opened. Only Si NWs with shorter channels (4 and 6 μm) are affected by the contact resistance (Figure 4.13(a) in air). In the case of the PBS solution on the surface of the Si NW biosensor, the subthreshold current is higher than in air and vice versa – the overthreshold current in PBS is lower than in air. Subthreshold current in PBS (Figure 4.13(a)) is no longer scaled with length. This may be because the current in the subthreshold region is dominated by the diffusion component and strongly

affected by the traps in the gate dielectric. Presence of electrolyte screens the effect of top-gate traps, which may lead to non-monotonic current behavior.

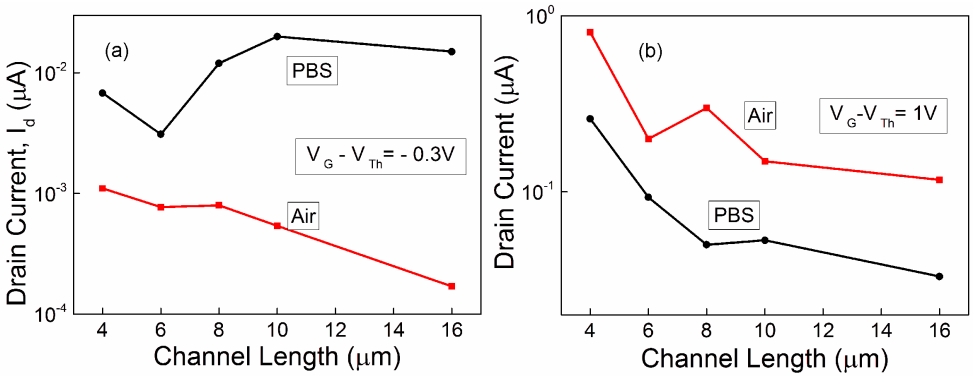

Figure 4.13 Drain current of Si NW FETs measured in air (red curves) and in PBS (black curves) as a function of channel length at V_{DS}=100 mV in subthreshold mode (a) and overthreshold mode (b).

The influence of PBS on transport in Si NW FET was also investigated by noise measurements. Figure 4.14 shows the normalized current noise spectral density, S_I / I^2, at subthreshold and overthreshold voltages measured in air and PBS. In the subthreshold region, normalized current spectral density in the device decreased when PBS was introduced onto the sample. This decrease can be partially explained (according to Eq.(2.31)) by increasing the subthreshold current by a factor of 3 in PBS (Figure 4.12(b) at an overdrive gate of -0.2V). However from Figure 4.14(a) we can see that the value of normalized current spectral density is more than one order of magnitude lower in PBS compared to that as in air. This is possible only if the exchange between the Si NW channel and the traps in the gate dielectric is affected. Thus, this decreasing noise can be explained by the changing of the surface charge state in the sample top dielectric due to PBS electrolyte adsorption and the screening effect as well as only a partial contribution of the increased subthreshold current.

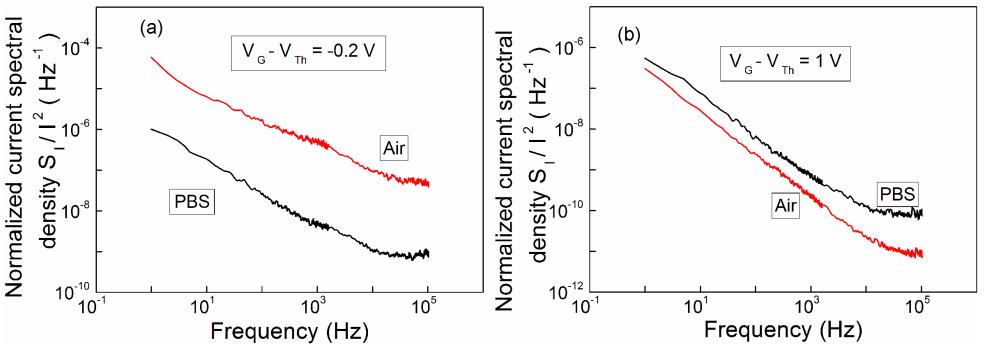

Figure 4.14 Normalized current noise spectral density, S_I/I^2, in sub-threshold (a) and overthreshold (b) mode measured in air (red curves) and PBS (black curves).

In the region above the threshold, submerging the sample in PBS results in a small increase in the amplitude of fluctuations in the sample. The influence of the electrolyte solution on the transport in Si NW FET in overthreshold can be studied using Figure 4.14 and Eq. (2.31). The normalized current spectral density is inverse proportional to quantity of carriers for all of the flicker noise models. Therefore if we multiply Eq. (2.31) by drain current, we get a value independent of the carrier concentration, taking into account the Eq. (2.12) for drift current:

$$\frac{S_I}{I_D} = \frac{\alpha_H}{N f} I_D = \frac{\alpha_H}{f} \frac{e\mu V_{DS}}{L^2} \tag{4.7}$$

According to Eq. (4.7), the value of S_I / I_D conserves if product of $\alpha_H \mu$ remains constant. The drain current in overthreshold mode is mainly determined by drift component. Therefore the data of Figure 4.14(b) can be plotted in a form of S_I / I_D. As we can see the spectra measured in the air and PBS solution coincide in Figure 4.15. Thus according to Eq. (4.7) we can conclude that presence of the electrolyte only causes decreasing of the coupling between back and front gate oxides, which results in reducing the back gate control over the drain current. However, the scattering mechanisms in the NW FET remain unaffected.

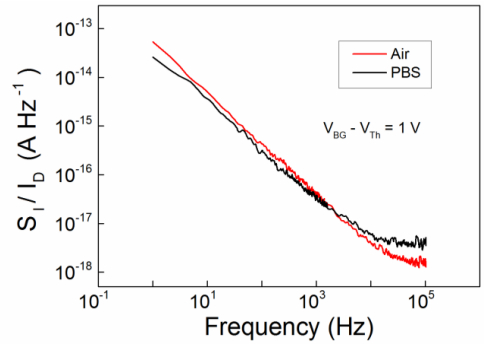

Figure 4.15 Drain current spectral density divided by the drain current in overthreshold mode in air (red curve) and in PBS (black curve)

To conclude, the impact of the electrolyte on the transport properties of Si NW FETs operated via back gate was studied utilizing I-V measurenents and noise spectroscopy. The results were obtained in DC mode under quasistatic conditions. It was shown that the submerging of the nanowire samples in PBS affects the back gate control over the NW channel by screening the charges, which accumulate in the top dielectric layer due to coupling between back and front gate. The investigated nanowire structures show good reproducibility of characteristics and scaling of parameters in most of the experiments. The estimated value of contact resistance is in the range of 10kOhms, which is much lower than channel resistance. The noise measurements show that the electrolyte influences transport properties in the Si NW channel not only by screening surface potential, but it may also change the charge state of the traps in the top dielectric layer. Particularly it is observed in subthreshold mode. As a result of such influence, the value of the excess noise is much lower in PBS than in air in the subthreshold region. In the case of overthreshold mode it is shown that immersing the sample into PBS only reduces the impact of surface traps by screening them, however the fluctuation mechanisms in the conducting channel remain unaffected.

In the next subsection we will discuss behavior of liquid-gate Si NW FET and consider role of charge carrier distribution, contact resistance and mobility degradation in the macroparameters of Si NW FET.

4.1.4 Role of the NW parameters in the NW FET device characteristics

As it we discussed above, the signal-to-noise ratio of the Si NW FET is one of the major parameters determining performance of a nanosensor. According to Eq. (2.19) the SNR is defined by transconductance of the transistor as well as by level of intrinsic fluctuations in the transistor. The noise level of a FET depends on the g_m in the case of McWhorter and correlated model (Eq. (2.36)). However, high contact resistance and degradation of the carrier mobility may suppress the transconductance without reducing device noise. Therefore understanding the main transport properties is of crucial importance for optimizing Si NW biosensors. This subsection is devoted to theoretical analysis of the transport properties of liquid-gated Si NW FETs and fitting of the obtained results to the experimental data. The impact of such microparameters as mobility, carrier concentration as well as contact resistance is considered. In the present work, we show the importance of considering the size quantization effect in the inversion layer.

The distribution of the charge carriers as well as mobility determine the static and dynamic behavior of the transistor. Indeed, the distribution in the NW FETs channel may differ from its classical counterpart due to quantum confinement in the space charge region of the channel cross-section. This may lead to overestimation of different kinds of FET parameters during fitting. Quantization may result in the shifting the maximum of the electron density from the front gate interface. It is equivalent to increasing the effective tunneling distance to the traps in the gate dielectric. The impact of the size quantization of charge carrier distribution on the transport properties was not reported for liquid-gated NW FETs.

Transfer curves were measured for Si NW FETs fabricated by Jing Li in group of Svetlana Vitusevich. The nanowires were of 200nm length and 100 nm width (Figure 4.16). The NWs were produced using e-beam lithography on the substrates described in subsection 3.2.2. The layout of chips with NWs was similar to Layout 1 in Figure 3.1, but it had shorter silicon feedlines, which provided lower contact resistance for the samples.

The statistical and dynamical behavior of the drain current is defined by the distribution of the concentration of the mobile charge carrier over the conducting channel. We consider the case of an inversion n-channel liquid-gated FET. In a most general case the concentration is a function of the surface potential and a coordinate.

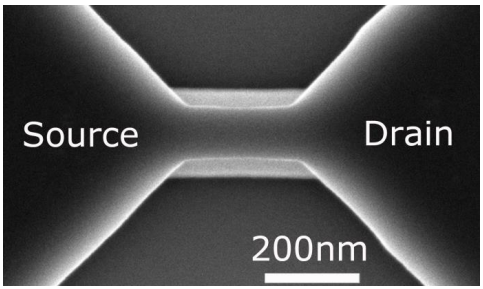

Figure 4.16 SEM image of a Si NW FET device. The scale bar is 200 nm[83].

The connection between surface potential and a gate voltage can be estimated by considering the potentials of the electrolyte double layer, ϕ_{dl}, front gate oxide, ϕ_{fox}, back gate oxide, ϕ_{box}, surface potential, ϕ_s, depletion layer, ϕ_d, and bulk silicon substrate, ϕ_{Si}

$$V_{FG} = E_{ref} + \phi_{dl} + \phi_s + \phi_{fox} + \phi_{box} + \phi_d + \phi_{Si}. \tag{4.8}$$

Schematic image of the potential distribution in liquid-gated Si NW FET is shown in Figure 4.17. Taking into account Eq. (2.3) and the unified charge control model we can extract the value of surface potential[55], [107], [128], [172]–[175]:

$$\phi_s = \varphi_T \ln\left(\frac{\eta C_{ox}\varphi_T N_A}{qtn_i^2}\right) + \varphi_T \ln\left\{\ln\left[1 + \frac{1}{2}exp\left(\frac{V_g - V_{th}}{\eta\varphi_T}\right)\right]\right\}. \tag{4.9}$$

Here $\varphi_T = kT/q$ is the thermal voltage; $\varphi_F = 2\varphi_T \ln(N_A/n_i)$ is the Fermi potential; N_A is the doping acceptor concentration in both the Si substrate and Si-NW; n_i is the intrinsic carrier concentration in bulk silicon; $\eta = 1 + (C_d + C_{it})/C_{ox}$ is the factor of the transistor non-ideality, C_d – is the capacitance of the depletion layer, C_{it} is the capacitance of the interface traps.

Let us now consider charge carrier distribution in the NW channel. The classical distribution is obtained from solving a one-dimensional poisson equation in the space charge region of Si NW[55]:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_0\varepsilon_{Si}} = \frac{q(N_A^- - N_D^+ + p - n)}{\varepsilon_0\varepsilon_{Si}} \tag{4.10}$$

where p is the hole concentration and N_D^+ is the initial donor concentration. Solving the Eq. (4.10) with the boundary conditions: $x \to \infty \Rightarrow \phi \to 0$, $x \to 0 \Rightarrow \phi \to \phi_s$, gives the equation for potential of the space charge region:

$$\phi(x) = \left\{\phi_s + \frac{qn_0}{\varepsilon_0 \varepsilon_{Si}}\left[1 - exp\left(-\frac{x}{l_s}\right)\right]\right\} exp\left(-\frac{x}{l_s}\right) \tag{4.11}$$

where l_s is defined by the Debye length for holes, L_D, and equilibrium carrier concentrations n_0 and p_0:

$$l_s = \frac{L_D}{1 + n_0/p_0}; L_D = \sqrt{\frac{\varepsilon_0 \varepsilon_{Si} \varphi_T}{q p_0}} \tag{4.12}$$

Resulting concentration of the carriers near the interface between silicon and silicon oxide can be calculated using following equation[55]:

$$n(x) = n_0 exp\left[\frac{\phi(x)}{\varphi_T}\right] \tag{4.13}$$

If we substitute $\phi(x)$ in Eq. (4.13) with Eq. (4.11) and (4.9), then we can calculate values of the carrier concentration for real Si NW dimensions.

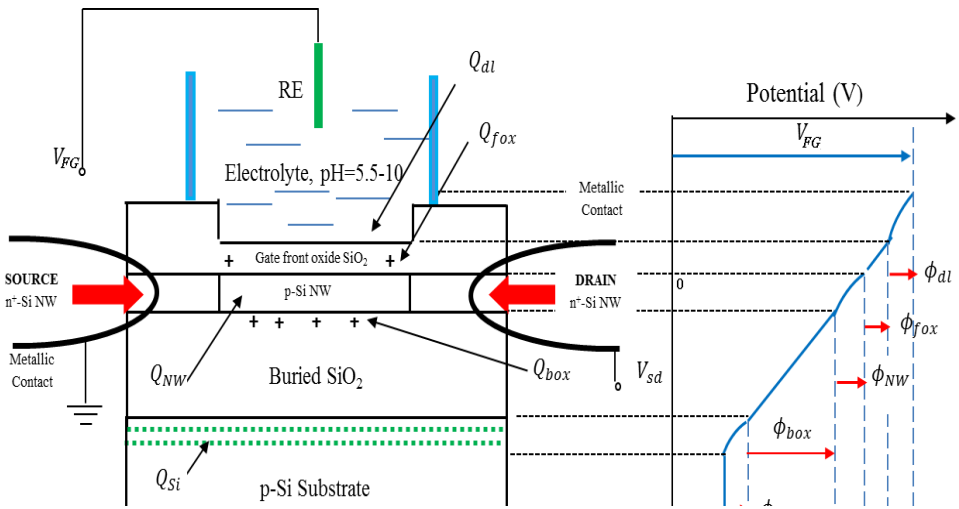

Figure 4.17 Schematic of a potential profile in a liquid-gated FET sensor. The layered structure consists of: electrolyte, front gate oxide, Si NW, BOX and substrate. RE is the reference

electrode, V_{FG} is the gate voltage applied, Q_{dl}, Q_{fox}, Q_{box}, Q_{NW}, Q_{Si} are the charges of the electrolyte double layer, front gate oxide, BOX, NW and Si substrate, respectively[83].

Figure 4.18(a) demonstrates concentration of electrons in the Si NW channel as a function of a coordinate *x* (see Figure 4.17) at different front gate voltages. For numerical computation, we use the following values, which correspond to the sample geometry and the parameters of the materials for the investigated structure: $\varphi_T = 0.026$ eV, $N_A = 10^{15}$ cm^{-3}, $t = 50$ nm, $W = 100$ nm, $L = 200$ nm, $d_{fox} = 9$ nm, $d_{box} = 500$ nm, $\varepsilon_{Si} = 11.6$, $\varepsilon_{ox} = 3.9$, $\varepsilon_w \approx 80$, $\varepsilon_r \approx 78$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/m, $m^* = 0.26m_0$, $T = 297$ ℃, m_0=9.11×10^{-31} kg.

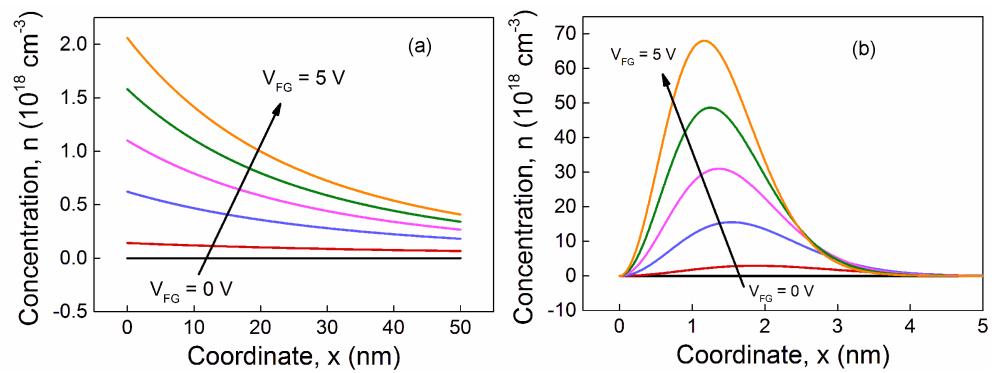

Figure 4.18 Calculated charge carrier distributions in Si NW channel: (a) using classical approach; (b) using quantum-mechanical approach.

Now let us consider peculiarities of carrier distribution in the case of the quantum approach. In this case the interface between front gate oxide and silicon is treated as a triangular potential well with infinitely high walls. The front gate voltage defines the angle of the triangle. The quantum-mechanical (QM) distribution of mobile carriers within the inversion layer in the NW FET can then be obtained by self-consistently solving Schrödinger's and Poisson's equations[176], [177]. The solution is expressed in a form of airy functions (Ai), which are a typical solution of a Schrödinger equation for a triangular potential well:

$$n(x, V_g) = n_s \times |C_i|^2 \times \left| Ai\left[\left(x - \frac{E_i}{q\mathcal{E}}\right)\left(\frac{2m^* q\mathcal{E}}{\hbar^2}\right)^{\frac{1}{3}}\right]\right|^2, x \geq 0, \qquad (4.14)$$

where n_s is the surface concentration, defined as[83]:

$$n_s = \frac{\eta C_{ox} \varphi_T}{q} \ln\left[1 + \frac{1}{2} exp\left(\frac{V_{FG} - V_{th}}{\eta \varphi_T}\right)\right] \tag{4.15}$$

and $|C_i|^2$ is the normalization factor:

$$|C_i|^2 = \frac{1}{\int_0^\infty \left[Ai\left\{\left(x - \frac{E_i}{q\mathcal{E}}\right)\left(\frac{2m^* q\mathcal{E}}{\hbar^2}\right)^{\frac{1}{3}}\right\}\right]^2 dx} \tag{4.16}$$

and

$$E_i = -\frac{(q\hbar\mathcal{E})^{\frac{3}{2}}}{(2m^*)^{\frac{1}{3}}} \times s_i, \tag{4.17}$$

where m^* is the effective electron mass, $\mathcal{E}$ is the electric field generated by the front gate voltage in the NW channel, E_i is the quantized energy levels of the electrons in a triangular potential well,[178] s_i is the i-th solution of equation: $Ai(s) = 0$. The surface electric fields are typically $\propto (10^4 \div 10^5)$, the energy levels $E_i \approx (0.03 \div 0.06)$ eV and the typical value of s_i for silicon FETs is 2.338 [177].

Using Eq. (4.14) – (4.17) and the parameters of the investigated liquid-gated Si NW FET we computed the dependence of the charge carrier concentration on the coordinate *x* in the channel for the case of quantum-mechanical approach (Figure 4.18(b)).

The concentration of the charge carriers in the quantum-mechanical (QM) approach differs considerably from the classical case (Figure 4.18). The curves in the QM case have well-pronounced peaks near the interface and the maximum values of the concentration are much higher than for the classical case. At high V_{FG} voltages the QM distribution demonstrates values close to the degeneration of silicon. Such behavior is caused by the energy quantization of the electrons in the triangular potential well near the front gate oxide / NW interface. The increase of the gate voltage results in an increase in the maximal concentration and also in a shift of the maximum towards the Si/SiO_2 interface. The majority of the electrons is located near the front gate oxide and occupy the region at a depth of 1-2 nm. More than 90% of the channel thickness does not contribute

to the dynamical processes. It should be noted that influence of the back gate oxide is not taken into account in this calculation due to high complexity of the system.

After considering classical and QM representation of the concentration profiles in Si NW it is possible to compute transfer curves and fit them to the experimentally measured dependences. The drain current of a FET consists of drift and diffusion components. Each of them is responsible for certain region of a transfer curve. The diffusion component mainly determines the sub-threshold mode and the drift component is dominant in the over-threshold region. Let us assume, that *y* axis points along the NW channel from source to drain. Then the channel current can be evaluated using the following equation[55]:

$$I_D = en\mu\frac{dV_{DS}}{dy}\,S + kT\mu\frac{dn}{dy}S = e\mu S\left(n\frac{dV_{DS}}{dy} + \varphi_T\frac{dn}{dy}\right). \tag{4.18}$$

The gradient of the concentration is responsible for diffusion current and gradient of the drain voltage is responsible for drift of charge carriers. The field caused by the applied gate voltage in the inversion layer of liquid-gated FETs changes the transport behavior of the charge carriers and results in more frequent scattering events than in the absence of the gate voltage. The mobility of charge carriers, μ, degrades due to increasing probability of scattering processes[179]–[181]. The mobility dependence on the transversal electric field (x direction) was taken into account using linear approximation:[182]

$$\mu = \mu_0 - \theta(V_G + V_{th}), \tag{4.19}$$

where μ_0 is the low-field magnitude of the mobility, θ is the coefficient taken as 28 $cm^2 / (V^2\,s)$ for the room temperature [182], [183].

The measurements were performed at low drain biases in linear mode of operation. Therefore the effect of the electron velocity saturation on the drain current was neglected during the calculation.

The influence of the front gate oxide interface on the FET sub-threshold current can be taken into account by introducing the capacity of the interface traps into the quality factor η:[55]

$$\eta = 1 + \frac{C_d + C_{D_{it}}}{C_{ox}}, \tag{4.20}$$

where $C_{D_{it}} = qD_{it}$ is the capacity determined by the interface states and D_{it} is the density of the interface traps.

In order to fit the over-threshold region of the measured I-V curve we take into account the effect of series resistance. In the case of non-ideal FET a part of the drain voltage drops on the series resistance. It results in the lower effective drain bias applied to the channel. Such a consideration together with the mobility degradation explains a sub-linear behavior of the transfer curves in a strong inversion regime (at overdrive voltages above 1V). The real values of the current can be extracted using the following equation:

$$I_{ds}(R_{ch} + R_c) = V_{ds}, \tag{4.21}$$

where R_{ch} and R_c are the channel and contact resistances, respectively. Based on our measurements of NW FETs with different lengths, we estimated the value for the series resistance to be 3500 Ohm. Also for a further calculation the following can be assumed, taking the linear regime of operation:

$$\frac{dV_{DS}}{dy} = \frac{V_{DS}}{L}. \tag{4.22}$$

Finally, the drift component of the drain current using Eq. (4.18) can be described by the following equation:

$$I_{drift}(y) = \frac{eWV_{ds}}{L}[(\mu_0 - \theta(V_G + V_{th})]\int_0^t n(x, V_{FG})dx, \tag{4.23}$$

where $n(x, V_g)$ is determined by Eq. (4.13) or (4.14) depending on approach for calculation the carrier concentration. The diffusion component is defined as follows:

$$I_{diff} = \frac{kTW\mu}{L}\left\{\int_0^t n(x, V_{FG})dx - \int_0^t n(x, V_{FG} - V_{DS})dx\right\}. \tag{4.24}$$

Figure 4.19 shows the measured transfer characteristic, $I_D(V_{FG})$, of investigated Si NW FET with a channel length of 200 nm and 100 nm width as well as the calculated transfer characteristics.

The calculations were performed using Eq.(4.23) and (4.24) with taking into account Eq. (4.19) – (4.21) for both the classical and quantum-mechanical approaches using corresponding $n(x, V_g)$ functions.

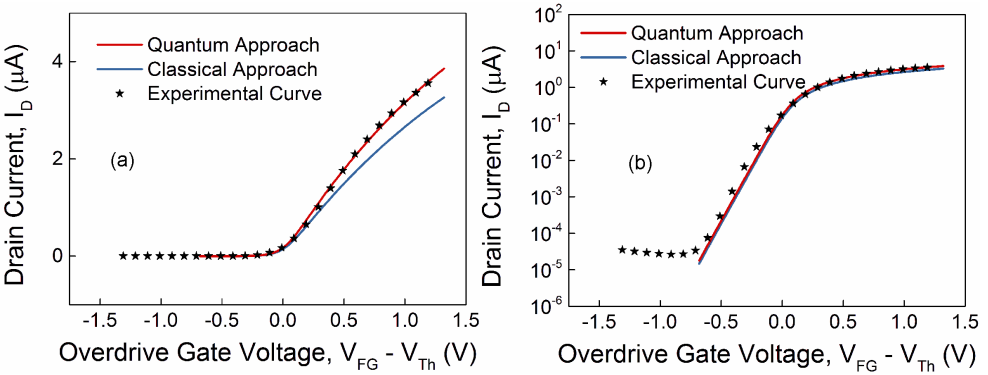

Figure 4.19 Comparison of measured (stars) and calculated (lines) transfer curves of Si NW FET: (a) – linear scale, (b) – logarithmic scale. The data calculated using classical and quantum approaches is shown as blue and red curves respectively.

The shapes of measured and calculated I-V characteristics are in good agreement. Figure 4.19 shows the curve calculated using the QM approach and fitted to the experimental data and the curve, corresponding to the classical approach, plotted with the same parameters as for the QM one. The value of low field electron mobility, μ_0, extracted from a fitting is 250 $cm^2\ V^{-1}\ s^{-1}$. It should be noted, that fitting of the transfer curve obtained using classical approach to the experimental values would give μ_0=300 $cm^2\ V^{-1}\ s^{-1}$. The overthreshold region of the transfer curve (Figure 4.19(a)) exhibits sublinear behavior at overdrive gates higher than 1 V. Such a behavior is caused both by degradation of the mobility and effects of contact resistance, which is reflected in Eq. (4.19) and Eq. (4.21), respectively. The subthreshold region of the transfer curves can be better observed in logarithmic scale (Figure 4.19(b)). Shapes of both QM and classically obtained curves are in good agreement with experimental results. The value of D_{it}, which provided such a subthreshold slope, was estimated to be 4×10^{12} $cm^{-2}\ eV^{-1}$.

It should be emphasized, that estimated value of mobility for the case the classical distribution of mobile carriers was higher than in the case of quantum-mechanical one, due to

difference in overall quantity of carriers in the inversion layer. This result stresses the importance of considering type of charge carrier distribution in the NW channel of the FETs. Findings of this subsection demonstrate importance of taking into account effects of contact resistance, mobility degradation and interface traps when considering transport and signal-to-noise ratio in Si NW FET structures. In the next subsection we will touch the topic of correct evaluation of equivalent input noise for precise calculation of SNR from the noise spectra.

4.1.5 Spectra of transconductance of Si NW FET.

Sensitivity of Si NW FETs is determined by the SNR value. As we have discussed in subsection 2.1.4, the SNR depends on the intrinsic noise of the device and its transconductance (Eq. (2.19)). Therefore, accurate estimation of the Si NW sensitivity requires precise determination of the device transconductance and the noise spectra is of crucial importance for careful device characterization. Accurate measurement techniques for the noise spectra and transconductance are discussed in subsections 3.3.2 and 3.3.3. However, the lock-in approach for measurements of g_m provides the value of transconductance only at a single selected frequency. In order to establish precise and reproducible technique for measuring sensitivity of the Si NW FET, we address in this subsection a precise measurement of the sample transconductance and its spectral behavior using advanced broadband method.

The investigated samples were Si NW FETs with 500 nm width and different length ranging from 2 μm to 22 μm. The NW FETs were fabricated by Jing Li. The layout of the structures was similar to Layout 2 in Figure 3.1. The NW contacts were doped with As atoms, therefore the samples represented n^+-p-n^+ structures. The results in this subsection are presented for Si NW FET of 8 μm length.

In Eq. (2.19) we assume that the transconductance of a Si NW FET is a frequency independent value. We are going to verify this assumption and compare measured transconductance with calculated one. Instead of using lock-in technique for scanning the transconductance within chosen frequency range we used advanced method for parallel acquisition of the whole transconductance spectra at once. For this purpose we applied stimuli in a form of white noise to the NW FET liquid gate and registered its response using spectrum analyzer. Figure 4.20 contains the schematic representation of the circuit for implementation of the proposed approach. The broadband stimuli signal is mixed with DC component of V_{FG} using capacitive coupling (See Figure 4.20). We connected a 100 kOhm resistor to the input of the homemade

amplifier, described in subsection 3.3.2. Therefore the resulting circuit can be used as the broadband AC source.

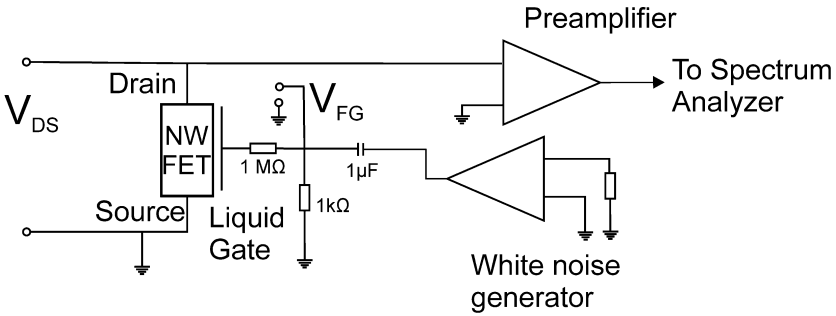

Figure 4.20 Schematic image of the circuit for measuring spectra of the FET transconductance.

According to Eq. (2.25), the fluctuations of voltage on the terminals of the resistor are proportional to its resistance and are frequency independent. Therefore a resistor connected to the input of an amplifier becomes a white noise generator. The signal from our homemade white noise generator was 200 times amplified by Stanford SR560 amplifier and applied to the liquid gate of the transistor. Figure 4.21(a) demonstrates the spectral density of the applied white noise stimuli (blue curve). It is almost flat with slight increase at low frequency range due to noise of the amplifiers and slight decrease at high frequency due to RC-cutoff by the parasitic capacitance of the amplifier. The intrinsic noise of the NW FET (black curve on Figure 4.21(a)) is much lower than applied signal and is represented mostly by flicker and thermal noise components. The induced noise is drawn in red in Figure 4.21(a). It is at least one order of magnitude higher than the intrinsic Si NW level starting throughout the whole frequency range. At approximately 10 kHz the induced noise starts increasing, which means that there is direct transfer of the applied signal through the parasitic capacitive coupling between liquid gate and the NW contacts. To verify this assumption we performed measurements of transconductance at different gate voltages (Figure 4.21(b))

The transconductance spectra can be evaluated using the value of applied noise, intrinsic noise and the induced noise (Figure 4.21(a)). According to Eq. (3.8) the transconductance is equal to the AC current induced at a certain frequency and divided by the amplitude of stimuli. If a

spectral density of the signal is known, then its value at certain frequency can be expressed as follows:

$$I_D(\omega_m) = \sqrt{S_I(\omega)|_{\omega=\omega_m}}. \tag{4.25}$$

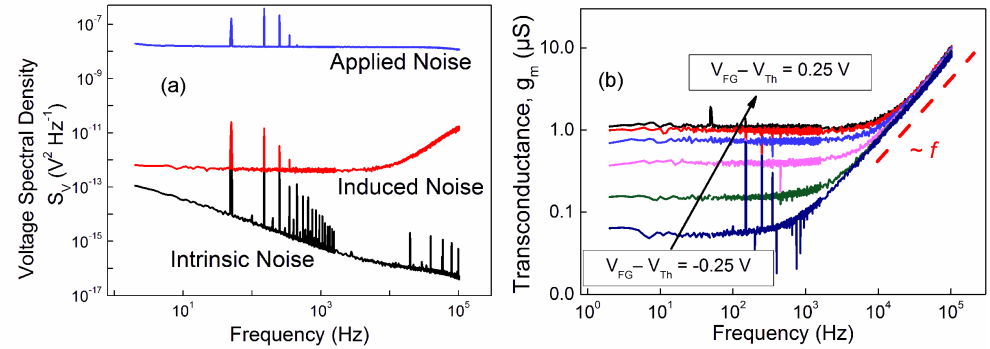

Figure 4.21 (a) Voltage spectral density of the applied white noise(blue curve), intrinsic noise of the NW FET (black curve) and induced noise in the channel of the transistor (red curve); (b) Spectra of the Si NW FET transconductance plotted at different overdrive voltages with a step of 80 mV.

Similarly, the stimuli level at certain frequency can be expressed as:

$$\delta V(\omega_m) = \sqrt{S_V(\omega)|_{\omega=\omega_m}}. \tag{4.26}$$

Therefore according to Eq. (3.8) we can define:

$$g_m^2 = \frac{S_{I_{induced}} - S_{I_{intrinsic}}}{S_{V_{applied}}}. \tag{4.27}$$

Figure 4.21(b) demonstrates calculated spectra of g_m at different overdrive gate voltages. The spectra are flat in the low-frequency region, as it is expected for a MOSFET structure [184]. However, at higher frequency range (from 10 kHz/ 100 kHz depending on the gate voltage) the estimated value of transconductance increases almost proportionally to the frequency. It should be noted that all the transconductance curves tend to converge into the one curve at a higher frequency range. Such a behavior can be explained by a capacitive coupling between the liquid gate and the

drain of the NW FET. Let us assume, that there is a parasitic capacitance, C_p, between the reference electrode and the drain contact. If we apply a weak AC component to the reference electrode (Eq. (3.5)) and take into account the effect of the parasitic capacitance, the Eq. (3.7) will modify into:

$$I_D \approx I_D(V_0) + \frac{\partial I_D}{\partial V_{FG}} \delta V sin(\omega_m t) + \omega_m C_p \delta V sin(\omega_m t). \quad (4.28)$$

If we switch to the frequency representation the AC parts of Eq. (4.28), we will get:

$$S_{I_{induced}} = (g_m^2 + \omega_m^2 C_p^2) \delta V \delta(\omega - \omega_m). \quad (4.29)$$

Eq.(4.29) describes the behavior of a FET in response of stimuli applied at a certain frequency ω_m as in the case of lock-in amplifier. If a broadband signal, as if white noise is applied, then Eq.(4.29) can be rewritten as follows:

$$S_{I_{induced}} = (g_m^2 + \omega^2 C_p^2) S_{V_{applied}} + S_{I_{intrinsic}}. \quad (4.30)$$

Let us call the value, which is plotted in Figure 4.21(b) the effective transconductance, $g_{m_{eff}}$:

$$g_{m_{eff}} = \sqrt{g_m^2 + \omega^2 C_p^2} = \frac{S_{I_{induced}} - S_{I_{intrinsic}}}{S_{V_{applied}}}. \quad (4.31)$$

In order to extract real NW FET transconductance and value of parasitic capacitance we fit the measured $g_{m_{eff}}$ using Eq. (4.31). The result of such a fitting is shown in Figure 4.22 for the case of the subthreshold region of the transfer curve. The estimated value of the parasitic capacitance is 11±1 pF, the estimated g_m value equals 50±3 nS and corresponds to the value of the low-frequency plateau. According to Figure 4.21(b) we can conclude that estimated value of C_p can be used for all measurement conditions and is defined by device geometry. Useful signal is transferred into the drain current by two independent mechanisms. Field effect dominates at lower frequencies and capacitive effect dominates at higher frequencies. It should be noted that in the frequency range from 1Hz to 10kHz, which is most interesting for biosensor experiments, transfer of the signal through a transistor is higher than parasitic capacitive effects. Therefore the effective transconductance measured at frequencies not higher than 1 kHz is equal to real transconductance of the NW FET. This statement can be verified by comparison of measured g_m with calculated one.

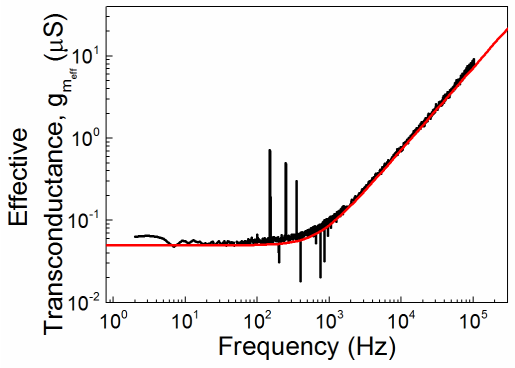

Figure 4.22 Spectra of effective transconductance (black curve) at V_{FG}–V_{Th}=-0.25 V and fitted using Eq. (4.31) (red curve).

Figure 4.23(a) demonstrates the transfer curve of the investigated Si NW FET. Transconductance of the NW FET was measured in each point of the curve. Comparison between measured and calculated values of transconductance is shown in Figure 4.23(b). Both dependences are in good agreement. The results show that lock-in method of measuring transconductance is consistent at frequencies below 1000 Hz for the case of bioFETs.

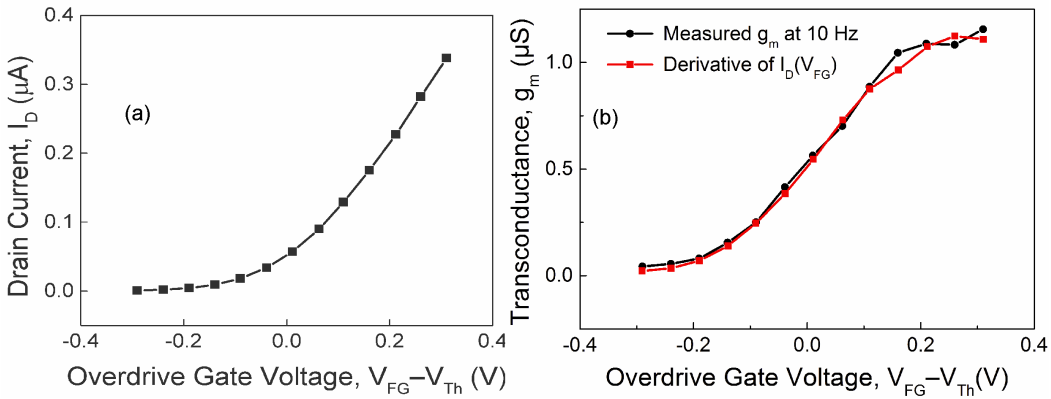

Figure 4.23 (a) Transfer curve of a Si NW FET with 500 nm width and 8 μm length. (b) Comparison of measured and calculated values of the transconductance.

4.1.6 Summary

In this section we have studied transport properties of single Si NW FETs using I-V characterization and noise spectroscopy. The investigated NW FETs demonstrate extreme charge

sensitivity, however estimated voltage sensitivity of single NW FETs not enough sufficient for extracellular recordings of neuronal cells. Therefore in the next section another device configuration based on arrays of Si NWs connected in parallel will be considered.

By studying DC and noise characteristics of a back-gated Si NW FET with and without PBS solution on top, the influence of the electrolyte gate on transport in Si NW FETs has been investigated. A front-back gate coupling through charging of the interfacial traps has been revealed. We demonstrate that the electrolyte solution impacts the transport in Si NW by screening the slow interfacial traps and thus reducing their effect on the DC current of the transistor. This screening also results in changes of NW AC behavior in subthreshold mode of the transistor. In the overthreshold mode electrolyte impacts only quantity of carriers taking part in transport through the NW.

Role of different NW parameters in transport properties of a Si NW FET was studied by calculation of the transfer curves taking into account charge carrier distribution, contact resistance and high-field mobility degradation. The results stress importance of consideration the quantum representation of charge carrier distribution for accurate characterization of device parameters.

In addition, it was shown that Si NWs in overthreshold mode transmit signals without any distortion in the frequency range between 1 Hz and 10 kHz. Above 10 kHz, the capacitive coupling between gate and source should be taken into account if the transconductance of the NW FET is below 1μS.

In the next section we will discuss design of silicon NW FETs based on array of a number of Si NWs connecter in parallel. We will call this devices Si NW array FETs. In order to obtain sufficient sensitivity for reliable extracellular recordings from neuronal cells we will consider investigation and simulation of the electric transport in fabricated Si NW array FETs for different regimes of operation. The interface between designed NW FETs and neuronal cells will be investigated using FIB.

4.2 Si NW array FET structures for neuronal cell interfacing

4.2.1 Design considerations for Si NW array FET

As we have shown in section 4.1.2, silicon NW FET structures based on single wires exhibit extremely high charge sensitivity down to elementary charges. However, we have shown that

sensitivity of single wires to the changes of the surface potential is not sufficient for reliable extracellular monitoring of electrogenic cells activity. The increasing Si NW voltage sensitivity can be achieved by increasing the device transconductance and reducing its noise.

Transconductance of a Si NW can be improved by increasing gate capacitance, mobility of charge carriers, decreasing channel length and increasing channel width (Eq. (2.13)). Increasing the mobility is rather challenging task, because it can be gained only by improving fabrication technology and cannot exceed the mobility of charge carriers in a bulk material. Therefore, increasing mobility is not considered as a main direction for increasing device sensitivity. However, to gain maximum performance of our structures we use TMAH etching for patterning NW structures. It results in improved quality of device surfaces and thus decreased level of noise and increased mobility[38]. Another way of increasing the transconductance is decreasing of the channel length, because g_m is inverse proportional to L. This approach is efficient, but its usage for extracellular detection of neuronal signal is limited because of the size of the cell. Typically, the cells have size from 10 µm to 20 µm and making the sensor much smaller than a cell may result in deterioration of the coupling between cell and NW. Besides, decreasing the channel length decreases the volume of the device and thus increases the flicker noise component (Eq. (2.32)). Due to this reason in the present work we do not downscale the transistors below 2 µm and typically consider longer samples for investigation of transport. Increasing of the gate capacitance can be performed by decreasing the gate oxide thickness or taking the oxide with higher dielectric permittivity than silicon oxide. However, decreasing of the silicon oxide thickness below 8 nm may result in lower stability of the oxide, because it also serves as a passivation of Si NW against electrolyte solution. Exchanging of silicon oxide with more permissive dielectric leads to higher amount of interface traps due to lattice mismatch between silicon and oxides of other elements. One of the favorable solutions in such a case is using combined stack of gate dielectrics, starting from this SiO_2 layer followed by high-k material deposited using atomic layer deposition (ALD). Another favorable method of improving SNR according to Eq. (2.13) is increasing width of the structure. In such a case the transconductance of the NW is increased as well as volume of the device, which leads to decreasing the flicker noise (Eq. (2.32)).

The characteristics of the NW FETs with desired parameters were simulated using Sentaurus TCAD software to predict the sensor behavior and improve the understanding of influence of the NW parameters on the transport properties. As it will be shown below the

simulations predicted strong front-back gate coupling effect, which was used for improving sensitivity of the fabricated Si NW array FETs.

In the present work we fabricated and designed Si NW FETs based on arrays of silicon NWs connected in parallel. It is equal to increasing width of the NW structures with preserving features of the nanostructured surface, which is favorable for improved coupling between electrogenic cells and the sensors. Connecting NWs in parallel forms a nanostructured grating, which preserves increased control of the gate over the channel conductivity, but at the same time increases effective width of the device. The structures are fabricated in Layouts 2 and 3 of Figure 3.1. The Layout 2 contains arrays of 50 NWs in each FET. In Layout 3 number of NWs is adjusted in each chip in order to get overall effective width of 10 μm. The NW FETs were designed and fabricated using developed technology, which is described in 3.2.2.

In order to improve understanding of Si NW FET operation and find a way for improving SNR of the designed array structures the next subsection (4.2.2) we will discuss simulation of Si NW FET in a technology computer aided design (TCAD) software taking into account both front and back gates of the NW FET.

4.2.2 Simulation of front-back gate coupling in Si NWs

In subsection 4.1.4 we have addressed modelling of liquid-gated Si NW behavior and investigated impact of different NW parameters on the device performance. We used only analytical solutions without numerical simulations. Using this approach influence of charge carrier distribution, contact resistance and high-field mobility degradation on transport properties of Si NW FET were studied. However the effect of the front-back gate coupling was not implemented due to high complexity of the model with two gates. It should be noted that the distance between front and back gate in our structures is 50 nm and therefore front-back gate coupling may play a considerable role in transport characteristics of Si NW FET. Therefore in order to study the front-back gate coupling effect carefully, we have implemented a model of our n^+-p-n^+ NW FET transistor in the Sentaurus TCAD software and simulated its behavior at different front and back gate voltages.

The model FET structure was 60 μm long. The gate length was 20 μm, the length of metal contacts was 10 μm each. Spacing between gate and metal contact was 10 μm. Thickness of the buried oxide layer was 150 nm, thickness of the front gate oxide was 9 nm. The silicon layer was

of 50 nm thickness. The contact regions of NW were simulated as implanted with Arsenic atoms to a concentration of $5x10^{19}$ cm^{-3} with a Gaussian distribution of the dopants after annealing. The active silicon layer was simulated as doped with Boron atoms to concentration of 10^{15} cm^{-3} with a uniform distribution. Front gate was realized as highly doped polysilicon layer. The back gate voltage was directly applied to the BOX without applying voltage to the substrate. After defining a model for simulations, a meshing procedure in Sentaurus Mesh software was performed. Then the device parameters transport properties were simulated in Sentaurus Device tool.

Simulated transfer curves are shown in Figure 4.24(a). The drain voltage was chosen as 50 mV. The back gate voltage varied from 0 V to 17 V. As we can see, applying back gate voltage affects threshold voltage and shifts the transfer curves towards lower front gate voltages. At lower back gate voltages (V_{BG}<12.5 V) transfer curves have linear region (V_{FG}-V_{Th}~0.3V) and sublinear region (V_{FG}-V_{Th}~0.5V÷1V), which is caused by contact resistance and mobility degradation. At higher backgate voltages (V_{BG}>12.5 V) two linear modes with two different slopes are observed before the sublinear mode is reached. Such an effect may be caused by formation of the second channel near the back gate oxide. The observation of the second linear region is also confirmed by transconductance of the NW FET, obtained as a derivative of the transfer curves (Figure 4.24(b)). Indeed for the case of higher V_{BG} a plateau corresponding to the second linear region is clearly resolved on the transconductance curves. Such a behavior was also observed for ultrathin SOI MOSFETS with standard and ultathin-BOX layer[185]. It should be noted, that maximum value of transconductance increases with increasing the back gate voltage.

In order to investigate the phenomenon of increasing the transconductance due to front-back gate coupling, we perform a virtual experiment using a constant channel resistance mode. In this approach, V_{FG} and V_{BG} are changed in such a way that drain current remains constant. Under such conditions, the charge carriers redistribute from the top surface to the bulk of the nanowire, while maintaining the current through the sample constant. Changes of the device transconductance in such a mode indicates changing of the effective mobility according to Eq. (2.13). The method can be used for estimation of gate capacitance of ultra-small NW devices [88]. Figure 4.25 shows simulated charge carrier distributions at constant current through the channel (0.5 μA/μm) and different front and back gate voltages, which correspond most particular cases: high positive front gate voltage and low back gate voltage (V_{FG} = 1.96 V and V_{BG} = 0 V), both positive front and back

gate voltages (V_{FG} = 0.7 V and V_{BG} = 12.5 V) and strong positive back gate voltage in combination with negative front gate voltage.

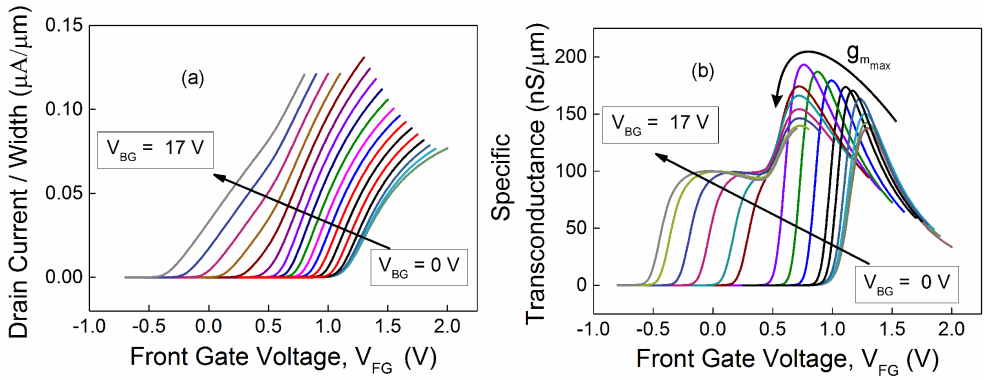

Figure 4.24 (a) Transfer curves of the n^+-p-n^+ Si NW FET simulated for different back gate voltages (V_{BG}=0 V to V_{BG}=17 V with a step of 1 V) at a drain bias of 50 mV. The ordinate is the specific drain current per μm of device width. (b) Specific transconductance derived from Figure 4.24 (a) plotted at different back-gate voltages. The straight arrow indicates changing of the V_{BG} parameter. The curved arrow indicates shift of the maximum of the transconductance.

Applying a potential, attractive for the charge carriers, to the back gate, results in a redistribution of the channel into the bulk of the NW FET. By further increasing the back gate voltage, a second channel starts forming near the back gate (Figure 4.25 (b)). And finally, after applying a repelling potential to the front gate and high positive potential to the back gate there remains only one channel near the buried oxide (Figure 4.25 (b)). Such carrier distribution causes the transfer curves with two linear modes (Figure 4.24). Each of the linear regions of the transfer curve corresponds to one of the two conducting channels (near front and back gate). The linear regions have different slopes due to different level of the front gate control over each of them. Redistribution of the charge carriers into bulk of the NW FET is also confirmed by simulated concentration profiles along the *x* axes of Figure 4.25. Figure 4.26 demonstrates charge carrier distributions of Si NW FET as a function of the coordinate *x* (Figure 4.25) in the mode of constant resistance for different V_{FG} and V_{BG} values.

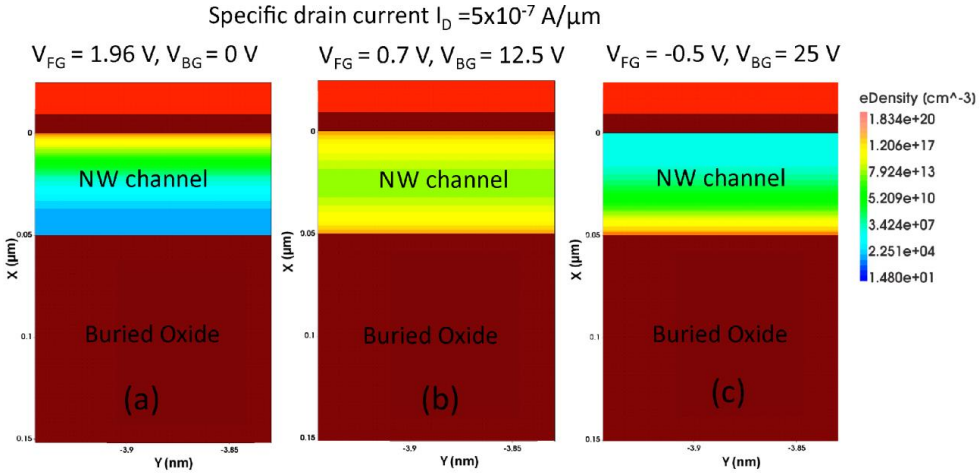

Figure 4.25 Simulated charge carrier distribution in the constant channel resistance mode. All the color maps are evaluated for the specific drain current of 0.5 µA/µm. The distributions were calculated at (a): V_{FG} = 1.96 V and V_{BG} = 0 V, (b): V_{FG} = 0.7 V and V_{BG} = 12.5 V, (c): V_{FG} = -0.5 V and V_{BG} = 25 V. The main changes of the concentration occur along the *x* axis.

As we can see from Figure 4.26, the case of Figure 4.25(b) corresponds to the situation, when charge carrier concentrations in both channels near front and back gate are equal. Increasing of the back gate voltage when the channel near the front gate is present leads to increasing of the carrier concentration in the channel (Figure 4.26). However, the current remains constant according to the experimental condition. Besides, according to Figure 4.24 (b) the transconductance of the NW FET also increases with increasing back gate voltage. Such an effect can be explained (Eq. (2.13)) only if front gate capacitance is increased due to front-back gate coupling effect. On the other hand, Figure 4.26 (b) demonstrates decreasing the overall concentration with formation of a pronounced channel near the back gate interface. At the same time we observe decreasing of the transconductance (Figure 4.24 (b)) while maintaining the drain current constant due to the conditions of constant channel resistance mode. This corresponds to decreasing of the capacitive coupling between front gate and the channel, because the channel is mostly located at the bottom interface.

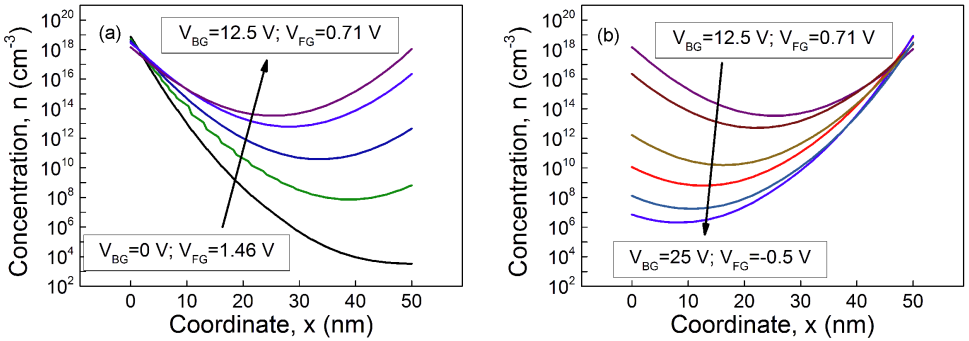

Figure 4.26 Concentration profiles in the regime of constant channel resistance simulated for different pairs of front and back gate voltages. The arrows indicate changes of V_{BG} and V_{FG}. The specific drain current maintained constant at a value of 0.05 μA/μm. (a) demonstrates concentration profiles at increasing the back gate voltage and decreasing front gate voltage, which corresponds to transition from Figure 4.25(a) to Figure 4.25(b)(V_{BG} changed from 0 V to 12.5 V and V_{FG} changed from 1.46 V to 0.71 V). (b) demonstrates concentration profiles at further increasing the back gate voltage and further decreasing the front gate voltage, which corresponds to transition from Figure 4.25(b) to Figure 4.25(b) (V_{BG} changed from 12.5 V to 25 V and V_{FG} changed from 0.71 V to -0.5 V).

The revealed effect of front-back gate coupling demonstrates that not only front gate controls the conducting channel of the NW. For optimizing the fabricated device performance the back gate impact on the conducting channel should be considered as well. Finding optimal values of V_{FG} and V_{BG} may result in better performance than traditional considering only a front gate for adjusting the device work point, because applying back gate voltage restructures the channel to the bulk regions of the NW, where scattering is lower.

To conclude, we have considered in this subsection a formation of the conducting channel of Si NW FET under influence of both front and back gates using Sentaurus simulation software. A front-back gate coupling effect has been revealed and its positive impact on transconductance was explained using constant channel resistance mode simulation. In the next subsection we will investigate experimentally an effect of liquid-back gate coupling on sensitivity of Si NW array FET and its possible application for improving device sensitivity. Sensitivity of Si NW array FET in different modes of operation will be also considered.

4.2.3 Enhancing sensitivity of Si NW FET by liquid-back gate coupling

The main goal of the presented work is fabrication of Si NW FET structures, which are stable, reliable and enough sensitive for continuous monitoring of electrogenic cell activity in vitro. In this subsection we use the Si NW array structures designed during this work and employ noise spectroscopy and transconductance measurements to establish the optimal regimes of operation for our fabricated silicon nanowire field-effect transistors (Si NW FETs) sensors. A strong coupling between the liquid gate and back gate, which was predicted in previous subsection, is revealed experimentally and used for optimization of signal-to-noise ratio in sub-threshold as well as above-threshold regimes. Increasing the sensitivity of Si NW FET sensors above the detection limit was proven by direct experimental measurements based on artificial neuronal signal.

The structures studied were Si NW FETs (Figure 4.27) designed, fabricated and encapsulated as it is described in section 3.2. The layout of structures corresponds to Layout 2 from Figure 3.1. Different FETs with Si NWs of different channel sizes were investigated. The length of the samples varied from 2 μm to 22 μm to extract information about contact resistance. The widths of each single nanowire in an array varied between different devices from 100 to 500 nm. It should be noted that the results presented hereinafter are obtained for the Si NW array FET of 50 nanowires of 250 nm width and 16μm channel length. However, the effects revealed here were similar across all of the samples measured. The noise spectra and transconductance were acquired as discussed in Section 3.3. The structures investigated in this subsection have B-doped contacts and thus represent p^+-p-p^+ accumulation FET. We assume that findings of previous subsection should be also applicable to accumulation FETs, because of the similar working principle.

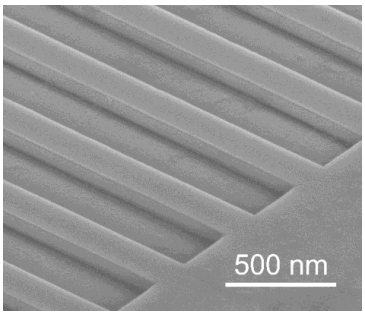

Figure 4.27 Scanning electron microscopy (SEM) image of one of the Si NW FET used during described in this subsection experiments[40].

Transfer curves of the investigated Si NW array FETs are shown in Figure 4.28(a). The characteristics show consistent scaling with the length of NW. Later on this feature will be used for extraction of contact resistance of the fabricated Si NWs. The transconductance of the 2µm sample is shown in Figure 4.28(b). It is significantly higher than for the case of single wire FET.

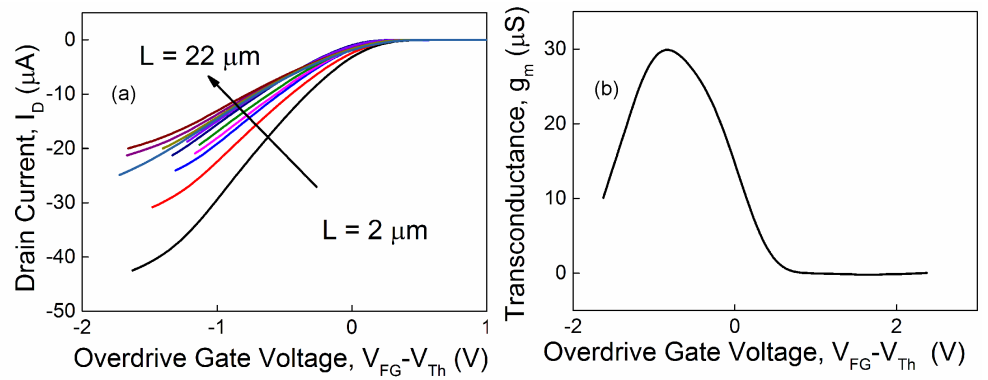

Figure 4.28 (a) Transfer curves of Si NW array FETs of different channel length (from 2 µm to 22µm) measured at V_{DS} = - 2.0 V. (b) Transconductance of 2 µm Si NW array FET.

Figure 4.29(a) illustrates the typical transfer curves measured at different V_{BG}. Application of the back gate potential shifts the threshold voltage of the Si NW FET. Such a behaviour is caused by the front-back gate coupling effect, which was predicted in previous subsection. The effect also was shown for metal gated FET structures[124], [164], [186]. However, the observed effect has not yet been reported for liquid gated Si NW FETs. In this subsection we study the influence of the back gate potential on the threshold voltage and main NW FET sensor properties such as transconductance and SNR.

As it was discussed above, the transconductance value of Si NW FETs determines how effectively the gate controls the drain current. Figure 4.29(a) demonstrates, that g_m, of a Si NW FET is dependent not only on front gate, but also on the back gate voltage. Therefore, the back gate voltage can tune the Si NW FET operation mode in terms of sensitivity. A summary of the transconductance mapping for different front and back gate voltages is shown in Figure 4.29(a) as contour plot. The transconductance exhibits a pronounced peak (Figure 4.29(b)) at certain combination of front and back gate voltage: V_{FG}≈0 V and V_{BG}≈-10 V. It should be emphasised that

increasing the back gate potential improves the maximum transconductance value of the Si NW FET and this data corresponds to findings of the previous subsection. The increase in g_m can be explained by the shift of the conducting channel from the surface to the bulk volume of the channel. As we have discussed in subsection 4.2.2, the front-back gate coupling it leads to increasing the effective front gate capacitance and the effective channel mobility due to lower scattering in the bulk NW region.

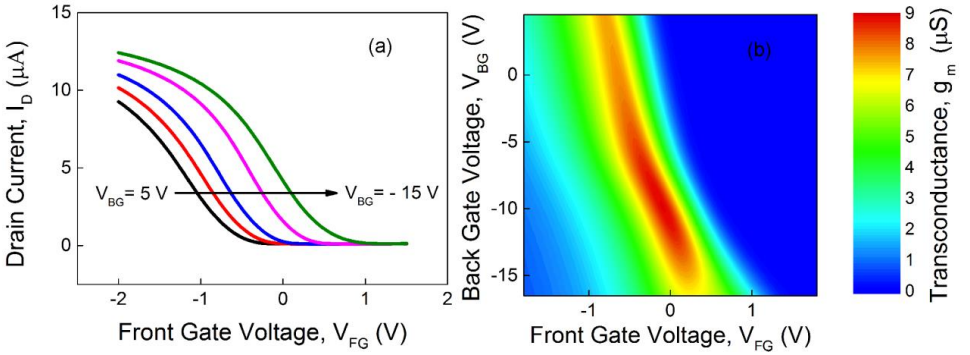

Figure 4.29 (a) Transfer curves of Si NW array FETs (250 nm width of each NW in array and 16μm channel length), V_{DS}= 1 V and V_{BG}, which varied from 5V to -15V with a step of 5V. The direction of V_{BG} changes is shown with and arrow in the figure. (b) Transconductance of the Si NW array FET measured at V_{DS} = 1 V and plotted as a colour map versus V_{BG} and V_{FG}. Red corresponds to the maximum transconductance, blue – to the minimum.

It should be noted, that the back gate voltage is applied to the whole structure, including contact regions, as can be seen in Figure 2.4. Therefore, modulation of the transconductance by changes in the back gate voltage might be caused by changes of the contact resistance. Such a possibility was not considered in the previous subsection, therefore we are going to verify this hypothesis experimentally here.

In order to exclude any contact effects, we measured transfer curves for the samples with different channel length. The V_{DS} was kept small 100 mV to ensure a linear regime of operation. At small drain biases (less than the overdrive gate voltage, V_{FG}-V_{Th}) the channel of the Si NW FET sensor can be treated as a resistor with a resistance proportional to the channel length. Resistance of the channel measured at the same values of the overdrive gate voltage in the linear region is linear function of the length[187]

$$R_{ch} = R_c + \frac{\rho}{S}L, \tag{4.32}$$

where R_{ch} is the total resistance of the Si NW channel, R_c is the overall contact resistance of both source and drain regions, ρ is the specific channel resistivity. If we perform linear fitting of the dependence of channel resistance on length, the contact resistance can be extracted as the intercept of the fitted curve with the ordinate axis. The channel resistance measured as a function of length at V_{DS} = 0.1 V and V_{FG}-V_{BG} = 0.5 V is shown in Figure 4.30(a) for different back gate voltages. Applying a negative (opening) back gate voltage decreases the channel resistance. The contact resistance, extracted using minimum least square fit interpolation is shown in Figure 4.30(b). It grows when the V_{BG} changes from 5 V to -15 V. Taking into account that the contact resistance is connected in series with the channel resistance, increasing the contact resistance can lead only to degradation of the sample transconductacne. However, according to Figure 4.29(b) the transconductance increases with higher magnitude back-gate voltage. This fact reflects that increasing the transconductance is not caused by a contribution of contact regions to the transport in the Si NW array FET.

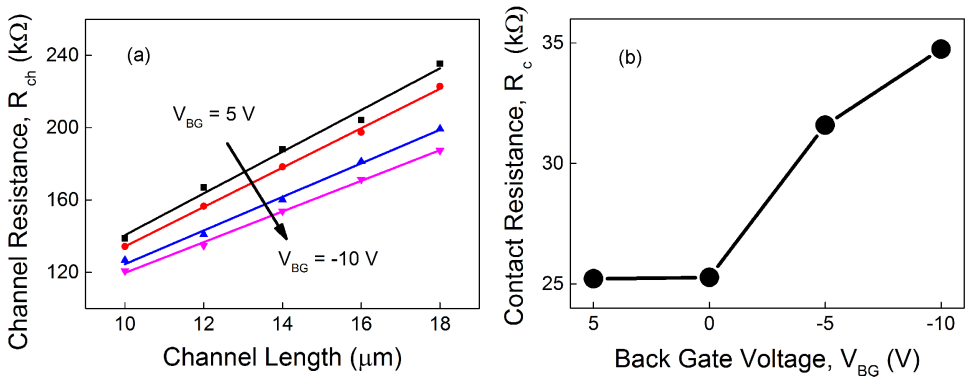

Figure 4.30 (a) Channel resistance of the Si NW array FET with channel width of 250 nm as a function of channel length at different back gate voltages. The straight lines correspond to the linear least square fit of the R_{ch} (L_{ch}) dependence. (b) Contact resistance of the Si NW array FETs plotted as a function of back gate voltage. The points are connected with lines as a guide to the eye

As we have discussed above, SNR of Si NW FET is defined not only by transconductance, but also by level of intrinsic noise of the device. According to Eq. (2.19) the lower value of S_u

leads to higher SNR. The SNR can be improved by finding the operation modes with the lowest equivalent input noise. For this purpose we will first consider a method of constant channel resistance, as in previous subsection. Noise spectroscopy of a FET in the constant resistance regime is used for finding the optimized conducting channel position[188] . As it was mentioned before in this approach, V_{FG} and V_{BG} are changed in such a way that drain current remains constant. The V_{DS} is kept at a constant small value to provide the linear regime of operation. As we have shown before under such conditions, the charge carriers redistribute from the top surface to the bulk of the nanowire. In the regime of constant resistance for the case of accumulation FET, applying a positive front-gate voltage and a negative back-gate voltage moves the conducting channel from the front gate oxide to the BOX, while maintaining the drain current constant.

For analysis of the SNR behaviour in the regime of constant resistance, we have measured transconductance and noise of the Si NW array FET at the channel resistance of 330 kOhm, which corresponds to the maximum of g_m at zero back-gate voltage. I_D was 0.3 µA during the whole measurement. Noise measurement output of these experiments are presented in Figure 4.31. Overall noise of the device decreases with increasing the back gate voltage, however in some parts of Figure 4.31 a non-monotonic behavior of spectra is observed.

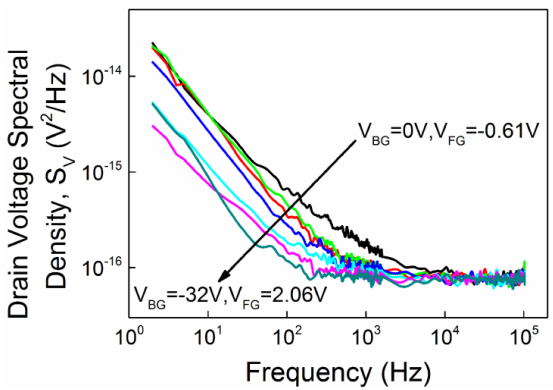

Figure 4.31 Drain voltage noise spectral density, S_V, of the array of 50 Si NWs with 250 nm width and 16 µm length, measured in the regime of constant channel resistance of 330 kOhm. Drain bias was 0.1V, front and back gate voltages were swept in such a way that the current through the sample remained constant at 0.3 µA.

As one can see from Figure 4.32(a), the transconductance demonstrates non-monotonic behaviour as we apply negative potential to the back gate (which attracts holes to the bottom

interface of the NWs) and positive potential to the front gate (which repels holes from the top surface of the NWs). Maximum of the transconductance is observed at V_{BG}= - 7 V, which is in good agreement with data of the Figure 4.29 (b). Further decrease of the transconductance with increasing back gate voltage is explained by shifting of the conducting channel from the top of the dielectric layer to the bulk of the Si NW array FET. Such a behavior corresponds to predictions of the previous subsection. The channel voltage spectral density (Figure 4.31) was measured in each point of this measurement and then recalculated to S_I using Eq. (3.4). The flicker (1/f) noise component, which causes the main fluctuations of the channel current at low frequencies (1-1000Hz) is extracted from the spectra using fitting as described in 3.3.4. It is shown together with the transconductance in Figure 4.32(a). The current spectral density of flicker noise follows the behaviour of the transconductance in the narrow region of back gate voltages (from 0 to -10 V). Taking into account that current was the same for the all measured points, we can conclude that the top dielectric layer is responsible for fluctuations generated in the channel of the nanowire for the case of low back gate biases. [130], [189]

The equivalent input spectral density value, S_u, calculated for the flicker noise component at 1Hz is shown in Figure 4.32(b). A slight decrease of the S_u value at more negative back gate potentials is observed. This fact demonstrates the high quality of the buried oxide layer[190], because moving the channel from top to the bottom interface of the NW reduces S_u. The decrease in S_u also results in the increase of the SNR (Equation (6)), which is favorable for the sensor performance. In the region of back gates between -10 V and -20 V the dependence of S_u on back gate voltage becomes flat and the value of S_u is lower than in the case of an unbiased back gate. Therefore, we consider this range of back gate voltages as optimal, because the equivalent input noise is lower than in the case of zero back gate potential and scattering of the S_u value for the V_{BG} between -10 and -20 V is lower than for higher back gate voltages (Figure 4.32(b)).

The optimal range of back gate voltages provides improved sensor characteristics. However, value of the S_u does not entirely reflect correct SNR value, because it is taken at a frequency of 1 Hz. Therefore to find the optimal regime of operation for the Si NW FET array, we performed a calculation of signal-to-noise ratio at different drain, front-gate and back gate voltages. The frequency range between 1Hz and 10 kHz was chosen for evaluation of the SNR to fit most bio-applications. Within this range, both excess noise and thermal noise should be considered in

order to estimate the SNR accurately. Therefore, for calculation of the SNR we use the full spectra of S_u and perform numeric integration according to Eq. (2.19) to get the contribution of all types of noise in the frequency range of interest. The δV_{FG} in Eq. (2.19) is taken as 1V. For the experiment we have chosen parameter ranges (V_{DS}, V_{FG}, V_{BG}) that cover entire scope of transport regimes.

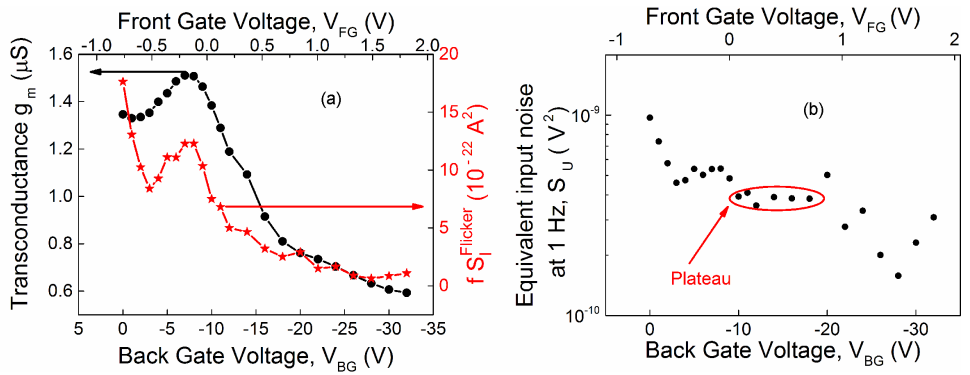

Figure 4.32 (a) Transconductance (black circles), and amplitude of flicker noise at 1 Hz (red stars), of the Si NW array FET measured in the regime of constant channel resistance. The dependencies are functions of both front (top axis) and back (bottom axis) gate voltages. The data points are connected with lines for better visual perception. (b) Equivalent input voltage spectral density calculated for the flicker noise component at 1Hz and plotted as a function of back gate and front gate voltage[40].

The front gate voltage was swept in the full range from the subthreshold to the overthreshold region; the main characteristic workpoints were defined as the combination of two drain and two back gate voltages. The two drain bias values were taken as 0.1 V and 1.0 V, which represent linear and saturation modes, respectively. For the back gate voltage, the following two values are used: 0 V, representing the normal case with an unbiased substrate and -10 V, which was chosen as an optimal value, using data from Figure 4.32(b). The transconductance of the Si NW array FET, measured using a lock-in technique at a frequency of 834 Hz, is shown in Figure 4.33(a) as a function of overdrive front gate voltage for the main cases described above: V_{DS} = 0.1 V, V_{BG} = 0 V; V_{DS} = 0.1 V, V_{BG} = - 10 V; V_{DS} = 1.0 V, V_{BG} = 0 V and V_{DS} = 1.0 V, V_{BG} = - 10 V. The normalized SNR calculated for the measured transconductance values is shown in Figure 4.33(b).

At low drain biases (Figure 4.33(b)), the SNR follows behavior of g_m (Figure 4.33(a)). Such a behavior of the SNR is related to the main contribution of the thermal noise component within the chosen frequency range (see Figure 4.34). Therefore applying a back gate voltage has no strong impact on g_m at low drain bias, but it decreases overall channel resistance (Figure 4.30(a)) and hence decreases the overall thermal noise. This results in slight increase of the SNR (Figure 4.33(b)) at the point of maximum of transconductance.

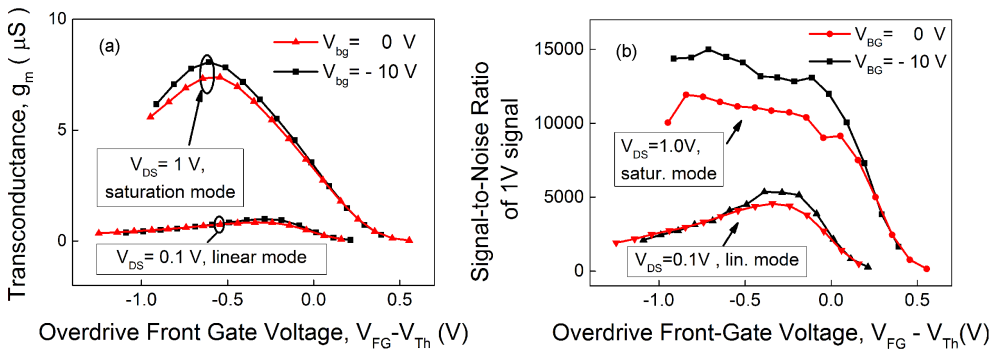

Figure 4.33 (a) Transconductance of the Si NW array FET; (b) SNR plotted as a function of overdrive front gate voltage at two drain biases (0.1 V and 1.0 V) and different back gate voltages (0V - red curves and –10 V - black curves);

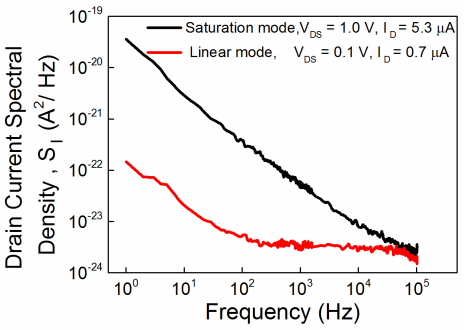

Figure 4.34 Comparison of the current noise spectral density for the cases of linear (V_{DS}=0.1V, red curve) and saturation (V_{DS}=1.0V, black curve) modes at an overdrive gate voltage (V_{FG} - V_{Th}) of -0.7 V.

At the relatively high drain voltage of 1V, there is no pronounced maximum on the SNR dependence on front gate potential in contrast to the linear region (V_{DS}=0.1V). It reflects the major contribution of the flicker and generation-recombination noise components (Figure 4.34), which change proportionally to the g_m. Therefore S_u demonstrates weak dependence on the front gate voltages in the saturation mode (V_{DS} = 1 V). It should be emphasized, that the normalized SNR at 1V drain voltage (Figure 4.33(b)) is much higher than one at 0.1V. At low drain voltage, the drain current and the transconductance of the sample are proportional to the drain-source voltage. In the saturation mode, the drain voltage has almost no effect on drain current and thus the value of the flicker noise. However, the transconductance value remains proportional to the drain voltage in the saturation mode. Therefore, the SNR value is increased at high drain voltages compared to the linear mode.

As follows from the data in Figure 4.33(b), applying the back gate voltage of -10V improves SNR of the transistor up to 1.5 times when operating in saturation mode. At the same time, the transconductance value increases by approximately 1.1 times at the maximum point. It demonstrates that applying the back gate voltage reduces the intrinsic noise of the device. It should be emphasized that the back gate voltage has a positive impact on SNR for both subthreshold and overthreshold modes (Figure 4.33(b)). This fact was not previously reported in literature.

Positive effect of the back gate voltage on sensitivity can be explained by analyzing the NW FET noise behavior. In Figure 4.35 we plot S_u of 1/f noise at 1Hz for the case of saturation mode (V_{DS}=1V) and different back gate voltages (0V and -10V).

The S_u demonstrates weak dependence on V_{FG} at V_{BG}=0 on the contrary to the case of V_{BG}= -10V, when S_u changes proportionally to the gate voltage. As we have discussed in 2.2.3, the S_u independence of gate voltage is the sign for number fluctuation noise model[108], [127], whereas proportionality to the gate voltage reflects mobility fluctuations noise model[108], [127]. Therefore, we can conclude that applying back gate potential switches the dominant mechanism of carrier scattering in the sample from surface to volume nature. The noise suppression caused by applying high back gate voltages originates from the change in the fluctuation mechanisms and this effect dominates over the decrease of the transconductance (Figure 4.32). These data represent background for increased sensitivity of silicon nanowire FETs under biased back gate conditions.

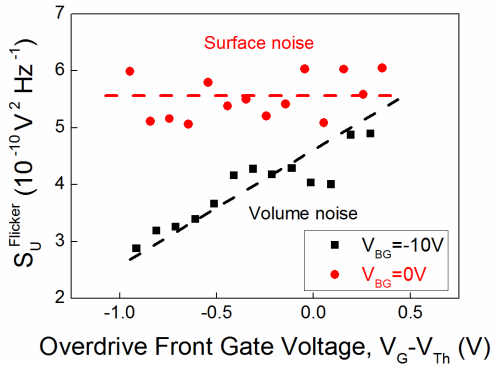

Figure 4.35 – Equivalent input noise for 1/f component extracted from measured spectra and plotted versus overdrive front gate voltage at V_{DS} = 1.0 V and different V_{BG} : red circles – V_{BG} = 0V, black squares – V_{BG} = -10V. The red dashed line reflects S_U behavior for the case of number fluctuations model of 1/f noise. Black dashed line reflects proportionality to front gate voltage – typical for mobility fluctuation model [40].

Now, having the optimized conditions obtained from the results shown in Figure 4.33(b) we approve them in the experimental measurements of the pulse signals with parameters similar to the extracellular recording of action potentials from a neuronal cell (pulse width of 3 ms). The signals were generated using specially designed for this purpose low-noise pulse generator. The layout of the generator circuit is shown in Figure 4.36(a). A function generator regulates duration and periodicity of the pulses from the circuit. In the upper position the relay Figure 4.36(a), a battery charges a 100 nF capacitor through a 100 kOhm resistor. In the lower position of the relay in Figure 4.36(a) the capacitor discharges to the ground through the 100kOhm resistor in parallel to the load resistor. An example of a pulse signal from described generator is shown in Figure 4.36(b).

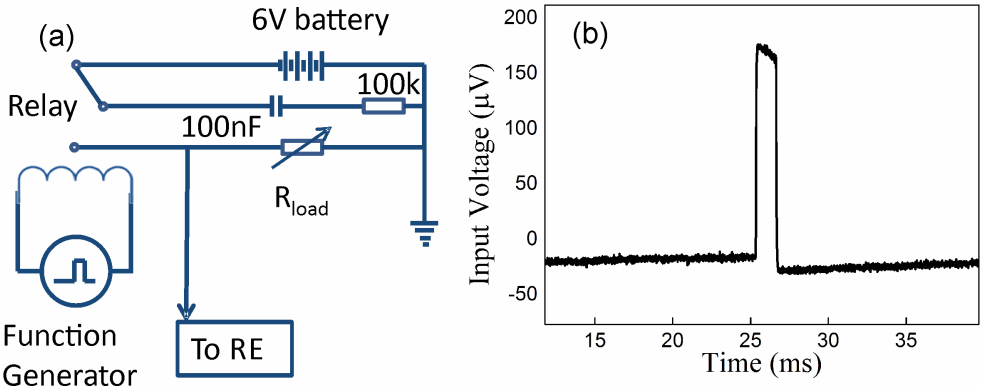

Figure 4.36 (a) Circuit for generating low-noise pulses similar to the extracellular signal from a neuronal cell. (b) Example of a pulse generated by the circuit from (a). RE is the acronym for the reference electrode

We applied the pulses generated by the circuit from Figure 4.36 (a) to the reference electrode and adjusted the amplitude of the pulses to obtain a sensor response with SNR about 1. The transistor working point was set according to the considerations of Figure 4.33(b) : V_{DS} was set to 2.0V (saturation mode) and V_{FG} was adjusted to the value of -1.3V to get the maximum g_m, V_{BG} was set to 0. Figure 4.37(a) shows the test signal and response of the sensor. Then we reduced the test signal amplitude by a factor of approximately 1.5, according to the conditions discussed previously. The signal was barely recognizable, because of the noise level of the NW FET. Then, using the chosen basing on previous experiments back gate voltage of -10V and a V_{FG} adjusted to yield the maximum transconductance, we distinguished signal despite its reduced amplitude. Figure 4.37(b)shows that the signal, which is 1.5 times lower than the initial pulse is resolved with even better SNR than in Figure 4.37(a). Hence, using of the back gate electrode allows improvement of the sensitivity to signals that are below the noise limit of the sample when no back gate voltage is applied.

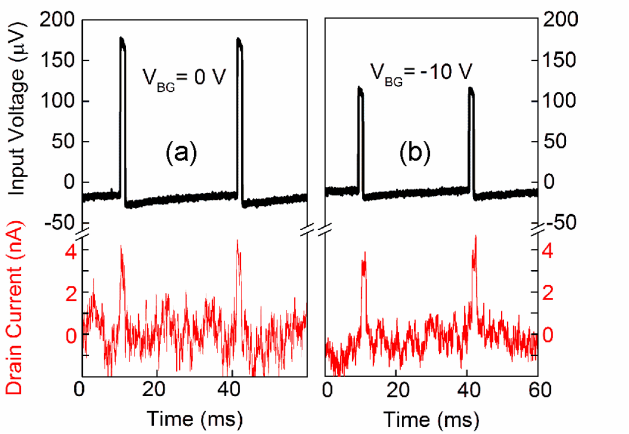

Figure 4.37 Signal recovery below the device noise level, utilising front-back gate coupling. (a) Test signal (black line) applied to the reference electrode and the response of the sensor (red line) at V_{DS} = 2.0V, V_{FG} = - 1.3V, V_{BG}= 0 V. (b) Signal is still resolved at V_{DS} = 2.0V, V_{FG} = - 0.3V, V_{BG} = - 10V, with the test signal decreased by a factor of 1.5 compared to (a). Both graphs (a) and (b) contain the signals, which were filtered to the range from 1Hz to 10 kHz[40].

In conclusion, high-quality silicon nanowire array FET biosensors with different channel dimensions were fabricated and studied. The sensitivity of the devices has been measured and proven to be sufficient enough for extracellular monitoring of the electrogenic cell activity. An effect of coupling between the liquid gate and the substrate (back gate) has been predicted in simulation and then revealed experimentally. It is shown that reassembling of the channel carriers due to front-back gate coupling effect changes the dominant scattering mechanism in the FET. The effect is used for tuning of the fabricated NW FET sensitivity. The SNR provided by the fabricated biosensor structure was improved by 50 %. The developed approach is used to recover signal below the initial detection limit. The findings of this subsection also inspire novel ways for improving sensitivity of the biosensors by designing devices with controlled channel position. The results reflect applicability of the designed and fabricated NW array FET structures for cell-based in vitro experiments. In the next subsection we will discuss behavior of neuronal cells in presence of Si NW structures and methods for guiding cells to desired spot on the chip. On the basis of the selected NW structure designs we have fabricated a test pattern for investigation of the interface between Si NWs and Si NW arrays and neuronal cells.

4.2.4 PLL patterning on Si NW FET structures

In previous chapters we have discussed the main requirements for a FET sensor to provide extracellular detection of an electrogenic cell activity. Then we designed and fabricated the Si NW FET structures according to our measurements and predictions. However, one of the major points of using Si NW FET structures is establishing improved contact between neuronal cells and surface of the FET sensor. Therefore this subsection and next ones are devoted to investigation of the interface between Si NWs and neuronal cells using FIB technique. Here we will consider guiding neuronal cells to Si NW structures.

For investigation of the interface between Si NW FET and neuronal cells we cultured rat cortical neurons, taken from a rat embryos, over Si NW test pattern, which contained the NWs of different lengths and width. The cells were prepared by Dr. Francesca Santoro. The pattern is discussed in detail in the section 3.4.1. Figure 4.38 demonstrates typical picture of the neuronal cells over the Si NW arrays after 7 days in vitro. The whole sample was covered with PLL before the cell culture. The procedure is discussed in 3.4.2. As we can see, the cells are distributed randomly over the sample and they cover the NW regions only occasionally. Therefore we can conclude, that the NW structures are fully biocompatible, but the cells have no particular preferences for seeding over the NW structures than anywhere else. Such a situation is not favorable from the point of view of finding proper samples for investigation the interface between NWs and neuronal sells. Therefore we have patterned the PLL on the surface of test NW samples using PMMA and e-beam writing.

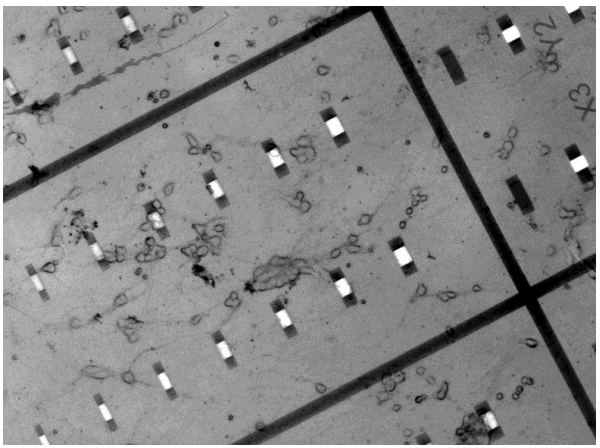

Figure 4.38 Optical image of the neuronal cells cultured over the test pattern with silicon nanowires. The image is taken using differential interference contrast filter.

The samples were fabricated as it is discussed in 3.2.2. Before the step of PLL coating, the samples were covered with layer of PMMA 649.04 (200K): heating for 5 min to 180 ºC for dehydration, spin-coating the PMMA resist for 30s at 4000 rpm on and further drying of the resist by heating to 180 ºC for 5 min. The openings for PLL were written using e-beam lithography with the dose of 250 $\mu C/cm^2$, 50 nm beam step size and 100 nA current. Then the samples were submerged into development solution AR-P 600-55 for 1 min and in isopropanol for 1 min as a development stopper. After described procedures the test samples were fabricated: silicon NW chips covered with PMMA with rectangular openings over the NW structures. In order to verify quality of PLL patterning we have coated the samples with fluorescein isothiocyanate labeled PLL (FITC-PLL), which was diluted in the same way as PLL in 3.4.2. The sample was kept after coating in the 4 ºC fridge overnight. In order to remove PLL coating everywhere except the NW regions we performed a lift-off procedure and removed PMMA and unnecessary FITC-PLL by immersing the sample for 1 min in acetone and then again for 1 min in fresh acetone for cleaning. As next a fluorescent images were taken using UV light. The grayscale image, which shows the successful PLL patterning is shown in Figure 4.39. The bright areas exhibit fluorescence and therefore correspond to the places covered with FITC-PLL.

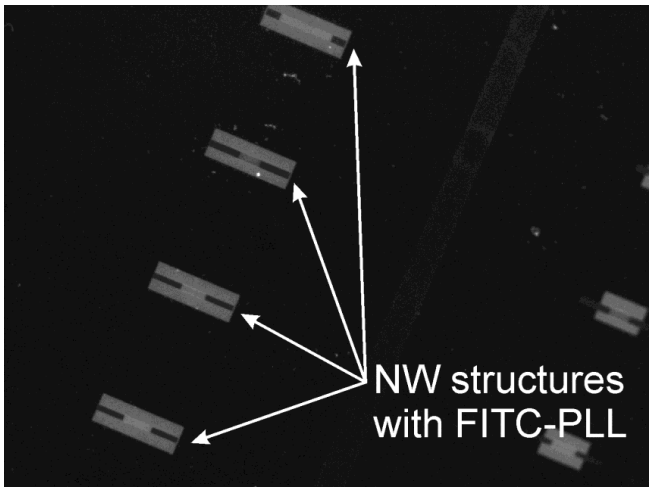

Figure 4.39 Fluorescence image of the FITC-PLL patterned on Si NW FET structures. Bright areas indicate presence of PLL on the surface.

After successful patterning of the PLL, the neuronal cells were cultured on the samples and placed into the incubator. The cell media was half-exchanged each 2 days and after 7 days in vitro, the samples were checked using live/dead staining. The optical image of combined fluorescent channels for live neurons, dead neurons and DIC channel is shown in Figure 4.40.

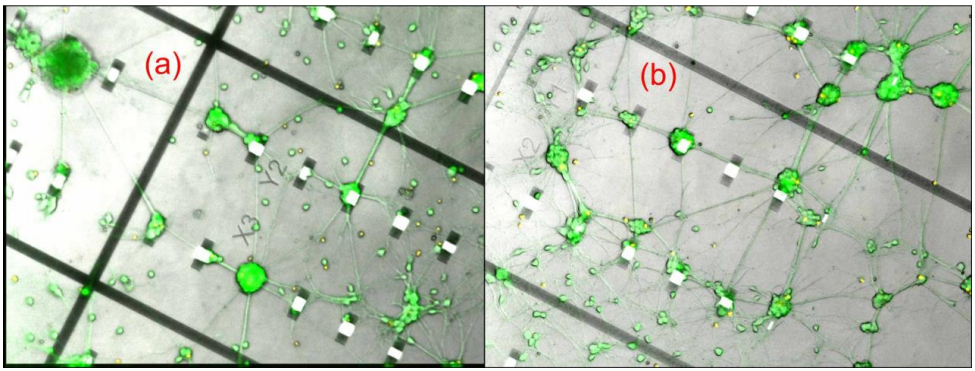

Figure 4.40 Images of live/dead staining of neuronal cells cultured on Si NW array structures. The pictures are combination of images from red and green fluorescent channels and a differential interference contrast (DIC) filter image.

As it can be seen from Figure 4.40, after the procedure of PLL patterning neuronal cells tend to agglomerate on the NW structures and mostly avoid free space. Multiple cells are gathered over the NW structures. This result reflects positive effect of PLL patterning on cell guidance. Neuronal cells can be attracted to the spots with nanowires and even form networks.

In this subsection we have shown successful PLL patterning on Si NW test pattern, which resulted in efficient cell-guidance. The results reflect possibility of designing neuronal networks directly on functional NW FET chips and extracellular investigation of the whole networks. In the next subsection we investigate interface between single neuronal cells and NW structures using FIB.

4.2.5 Investigation of Si NWs / neuronal cell interface using FIB

As we have shown above in subsection 2.3.3 the cleft between neuronal cell and sensor surface determines quality of the electric signal transmission from a cell to the transducer. A Si

NW FETs were chosen for extracellular electric signal detection as a transducer with a reduced cleft between cell and the sensor surface. The assumption was made based on literature data of measuring the cleft between neuronal cells and bottom-up processed silicon nanowires[30], [36]. Here we use critical point drying technique and FIB to investigate interface between neuronal cells and Si NW array FETs, fabricated using top-down approach.

In the previous subsection we have shown that after PLL patterning and guiding neurons the probability of finding a single neuron on one of the Si NW FET structures is much higher than in the case of uniform PLL coating. Therefore for FIB experiments we used the samples with PLL patterning. After 7 DIV the cells were fixed as discussed in subsection 3.4.4 and dried using critical point drying. Then the samples were coated with 1 nm platinum to improve SEM imaging, because cell membranes are non-conductive. Typical SEM images on the neuronal cells fixed on Si NW structures are shown in Figure 4.41. In Figure 4.41(a) two neuronal cells cover entirely single Si NW, and thus it is hard to recognize NW under the cells. In Figure 4.41(b) the cell is located in the middle of the NW structure and the axon and dendrites cover the entire NW structure.

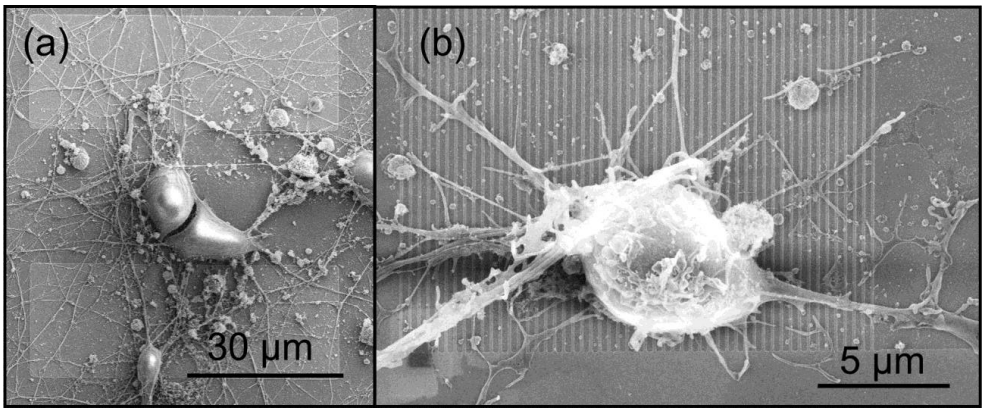

Figure 4.41 SEM images of neuronal cells on Si NW structures: (a) on single Si NW and (b) on Si NW array.

Then FIB cuts of the cells on the NW structures from Figure 4.41 were performed. Figure 4.42 (a) demonstrates general view of the cell on single NW cut in the middle of the soma. The arrow indicates Si NW, which hits the cell near its border. The magnified part, which contains NW is shown in Figure 4.42 (b).

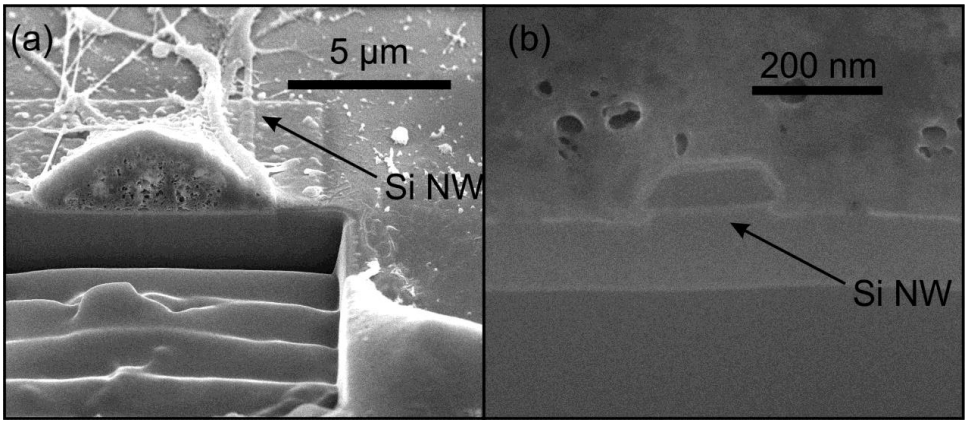

Figure 4.42 FIB cut of a neuronal cell fixed on single Si NW. (a) general view on the cross-section. The NW is indicated with an arrow. (b) The close view of a 200 nm wide Si NW engulfed by a cell.

The single NW cross-section can be observed in Figure 4.42 (b). It has a trapezoidal shape because of wet chemical etching procedure during fabrication. Silicon oxide can be clearly distinguished from silicon and material of a fixed cell body. Figure 4.42 (b) shows that the cell has engulfed the NW, which means extremely low cleft between cell membrane and surface of the NW.

For the case of Si NW arrays (Figure 4.41(b)) the FIB cut is shown in Figure 4.43. The general view Figure 4.43(a) demonstrates that the cell contacts the NWs in the middle as well as in near the border. The cells form cavities between cell membrane and surface of the NW sensor. However, if we have a closer look on Figure 4.43(b), we can see that the cavities usually have closed volume, which should prevent a leakage of the useful signal. In the middle of the cell, the membrane is firmly attached to the surface of the NWs. Figure 4.43(b) demonstrates an array of 100 nm wide Si NWs. The front gate oxide is clearly resolved in the figure. The measured value of the gate oxide thickness was 7.5 nm which reflects good agreement between the ellipsometric measurements during fabrication process with the actual value measured with FIB on the finalized Si NWs.

In order to check if the observed cavities have leakage to the electrolyte solution we performed a FIB cut of the cell both along and across the NW The cross sections are shown in Figure 4.44. The longitudinal cross-section of a cell on Si NW array structures is shown in Figure

4.44 (a), (b). The partial detaching of the cell from NW is followed by a region with tight contact between NW and the cell. The cut along the NW structures shows that the cavities of the fixed cell, which might look as a detachment from the NW, behave in the same way as on the transversal FIB cut and are fully closed from the outer environment. Figure 4.44 (c),(d) shows additional transversal cut and Figure 4.44 (d) demonstrates example of the section of a closed cavity of the cell on 250 nm wide NWs. Closed cavities are not contributing to the leakage of the signal, because of high seal resistance provided by the membrane, which is attached to the NW surface. It should be noted, that Figure 4.43 and Figure 4.44 demonstrate, that length of the NW structures up to 10 μm is sufficient to gather the signal from the entire cell. Even if the cell is slightly larger than the NWs the signal still can be transmitted to the channel in the NW though the parts of the cell attached to the NWs.

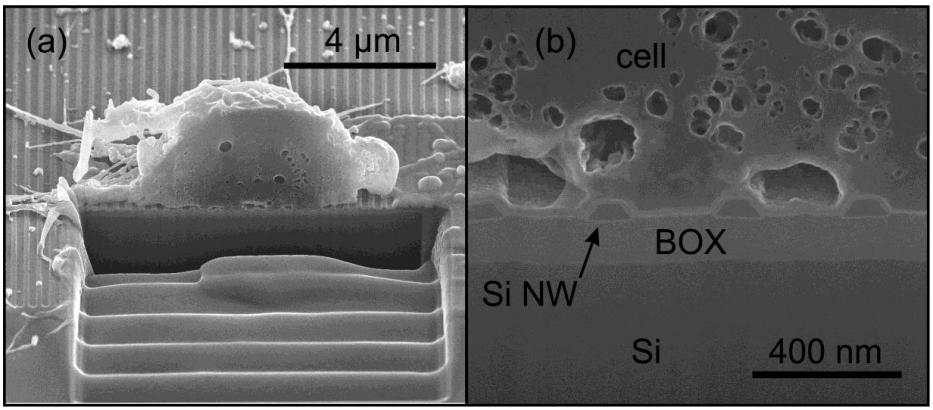

Figure 4.43 FIB cut of a neuronal cell on Si NW array. (a) general view on the cross-section. (b) Close view of a neuronal cell over 100 nm wide NWs. The cell, silicon substrate and BOX shown on the figure with corresponding titles; the arrow indicates one of Si NWs.

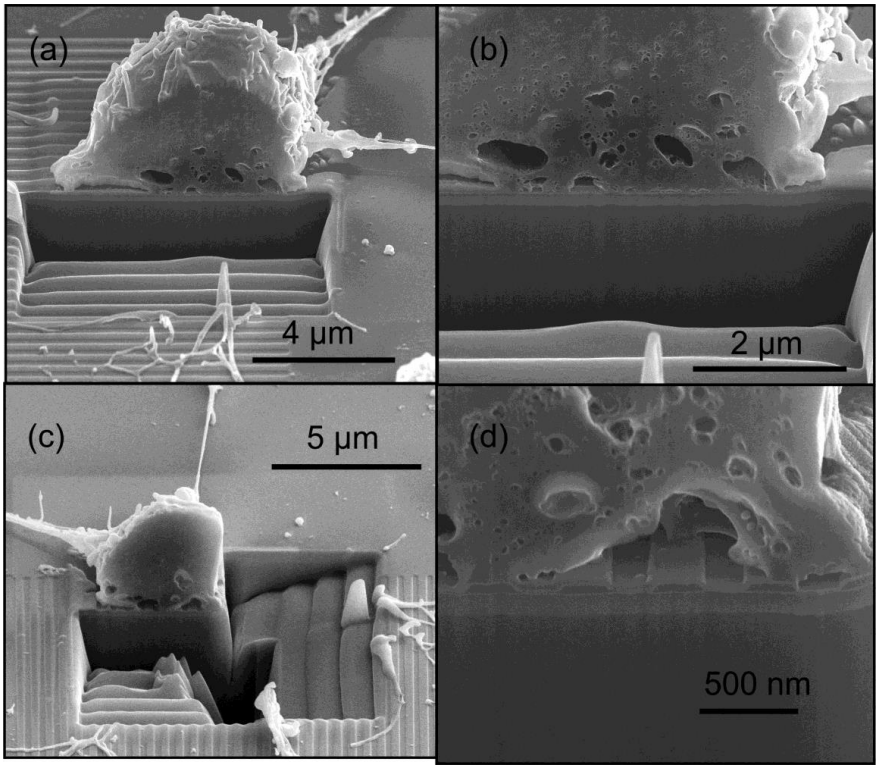

Figure 4.44 Transversal and longitudinal FIB cut of a neuronal cell on Si NW array. (a) general view on the cross-section long the wires. (b) Close view of a longitudinal cross-section. (c) general view of a cell after two FIB cuts.(d) close view on the transversal FIB cut of a neuronal cell on the Si NW array.

In conclusion, we have shown a high quality of the interface between neuronal cells and NW structures of different geometry using critical point drying technique and FIB sectioning. The fabricated structures are fully biocompatible and the neuronal cells were successfully guided to the NW structures using the PLL pattern. The results of this and previous subsection indicate applicability of the fabricated structures for extracellular monitoring of the neuronal cell activity

5. Conclusions and outlook

This thesis is devoted to design, technology development and fabrication of Si NW FET structures for neuronal cell interfacing and characterization of their transport properties and reliability utilizing technique of noise spectroscopy. The transport properties were first studied in FET transistors based on single Si NWs. The results of the investigations were used for the development and fabrication of Si NW array FET structures represented by 50 NWs connected in parallel and optimized for extracellular recording from neuronal cells. The interface between neuronal cells and fabricated structures was studied using FIB technique. Fabricated structures were characterized electrically in order to find optimal regimes of liquid-gated FET operation with maximum sensitivity.

The transport properties single Si NWs were studied using I-V measurements and noise spectroscopy to understand the main factors influencing sensitivity of Si NW FET. Results of transport investigation in short-channel Si NW MOSFETs revealed a modulation of the NW conducting channel by a single trap. Analysis of noise spectra and time traces of the device fluctuations allowed us to evaluate parameters of the single trap influencing transport in the NW. Observed strong modulation of a channel conductivity by a single trap in the gate dielectric reflects extreme charge sensitivity of Si NW FET structures, which makes possible detection of local concentrations of biomolecules down to single molecule level. However, sensitivity of the single wire FETs to changes of surface potential was found to be insufficient for extracellular monitoring of electrogenic cell activity. Based on literature research the value of 100 μV (filtered to the frequency range between 1 Hz and 10 kHz) was chosen as a target sensitivity for Si NW FET structure in order to establish a robust platform for monitoring cell activity. To meet such a requirement, the role of different NW parameters including the influence of the measurement environment on transport properties of Si NW FET structures was investigated. Influence of the electrolyte gate was studied by immersing a back gated Si NW FET into PBS solution. The effect of screening the charges of surface traps by electrolyte gate was revealed. It was shown that the electrolyte gate has no significant impact on the noise of the device at the gate voltages above the threshold voltage. In the subthreshold mode applying of the electrolyte to the NW surface results in one order of magnitude noise supression. The impact of contact resistance and high field mobility degradation was shown by comparison of the theoretical studies of the NW FET to experimentally

measured transfer curves. The results of theoretical modelling of the NW FET structures pointed out the importance of considering quantum charge carrier distribution when analyzing transport properties of NW structures. In order to study quality of the signal transduction through a Si NW FET we have studied spectral behavior of the device transconductance using developed technique of white noise stimulation. Analysis of the transconductance spectra reveal that the signal can be transmitted into the NW channel not only due to field effect of the transistor, but also due to capacitive coupling between liquid gate and drain of the NW FET. It was shown that in overthreshold mode of operation the signal is transmitted undistorted in the range between 1 Hz and 10 kHz. This reflects applicability of Si NW FETs for extracellular communication with neuronal cells.

The considerations based on investigation of single Si NW FETs transport properties were used to design and fabricate high quality Si NW array FET structures, each consisting of 50 NWs connected in parallel. In order to optimize SNR of fabricated Si NW array FETs and get maximum sensitivity we have studied behavior of the device transconductance and intrinsic noise in different regimes of NW FET operation. Transport characteristics of the developed and fabricated NW structures were simulated using Sentaurus TCAD software, taking into account influence of the back gate voltage on transport in Si NW FET. Analysis of the simulated transfer curves of Si NW FET revealed a coupling effect between front and back gate, which results in a strong impact of back gate voltage on threshold voltage and transconductance of the NW FET. The positive effect of the front-back gate coupling on transconductance was demonstrated and studied using simulation of the Si NW in constant channel resistance mode. The distribution of the charge carriers in the channel of a NW FET was simulated at different front and back gate voltages, which were chosen in a way that the drain current maintained constant. The analysis of the calculated data revealed restructuring of the conducting channel from top NW interface to the bulk part of the NW under influence of the back gate. These results reflect importance of considering back-gate electrode for finding optimal operation regimes of the NW FET biosensor. The predictions based on the simulations were then proven by real experimental measurements with the fabricated Si NW array FETs. The measurements of transconductance and noise in different operation regimes testify predicted positive effect of the back-gate voltage on SNR of the Si NW array FET. The sensitivity of the NW structures was tested using pulse signals with parameters similar to the shape of the extracellular changes of the surface potential caused by a neuronal cell action potential. The results of the sensitivity tests demonstrate that our developed and fabricated Si NW FETs can detect

signals below the value of 100 μV, which was determined as target sensitivity for establishing a robust tool for extracellular monitoring of the electrogenic cell activity. Then the quality of an interface between neuronal cells and fabricated Si NW structures was confirmed using FIB. The PLL patterning was used to guide neuronal cells to the NW structures. Analysis of the FIB cuts has shown that interface between the cells and Si NW array structures has almost no cleft. Engulfment of single wires was demonstrated. Therefore the fabricated Si NW FETs are proven to be applicable for extracellular monitoring of the signals from the electrogenic cells in vitro.

The outlook of the future work includes several directions. The first is conduction of the extracellular monitoring of neuronal cell and HL-1 cell activity using developed Si NW array FET structures. We are going to estimate the seal resistance of the cell / NW interface applying the approach from [191] but using instead of the impedance spectroscopy our developed method of transconductance spectroscopy. The method is based on applying a small AC signal to the front gate electrode and comparing the response of the NW FET with and without cells on top of the NW FET. The next direction is investigation of transport phenomena in Si NW FETs in order to utilize the full potential of the interesting effects observed during this work. The plans include extended experimental and theoretical studies of the front-back gate coupling effect for understanding of transport peculiarities related to this effect and developing optimal geometries for its utilization. Also investigation of the conduction channel modulation effect caused by a single trap in the gate dielectric, which was observed during this work, is in focus of our studies for developing novel sensing approaches based on the single trap phenomena.

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Personal publications list

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2. J. Li, ***S. Pud***, M. Petrychuk, A. Offenhäusser and S. Vitusevich. Sensitivity Enhancement of Si Nanowire Field Effect Transistor Biosensors Using Single Trap Phenomena // **Nano Lett.**,Vol.14, Issue 6, 3504-3509 (**2014**), DOI: 10.1021/nl5010724
3. ***S. Pud***, F. Gasparyan, M. Petrychuk, J. Li, A. Offenhäusser and S. A. Vitusevich. Single trap dynamics in electrolyte-gated Si-nanowire field effect transistors // **J. Appl. Phys.**, Vol. 115, 233705 (**2014**) DOI: 10.1063/1.4883757
4. J. Li, ***S. Pud***, D. Mayer, S. Vitusevich. Advanced fabrication of Si nanowire FET structures by means of a parallel approach // **Nanotechnology**, Vol.25, Issue 27, 275302 (**2014**) DOI: 10.1088/0957-4484/25/27/275302
5. ***S. Pud***, A. Kisner, M. Heggen, D. Belaineh, R. Temirov, U. Simon, A. Offenhäusser, Y. Mourzina, S. Vitusevich. Features of Transport in Ultrathin Gold Nanowire Structures // **Small**, Vol. 9, Issue 6, 846-852 (**2013**) DOI: 10.1002/smll.201202197
6. ***S. Pud***, J. Li, M. Petrychuk, S. Feste, S. Vitusevich, B. Danilchenko, A. Offenhäusser, and S. Mantl. Modulation phenomena in Si nanowire field-effect transistors characterized using noise spectroscopy and gamma radiation technique // **J. Appl. Phys.** 113, 124503 (**2013**), DOI: 10.1063/1.4795603
7. J. Li, S. A. Vitusevich, M. V. Petrychuk, ***S. Pud***, A. Offenhäusser and B. A. Danilchenko. Advanced performance and scalability of Si nanowire field-effect transistors analyzed using noise spectroscopy and gamma radiation techniques // **J. Appl. Phys.** 114, 203704 (**2013**) DOI: 10.1063/1.4833567
8. ***S. Pud***, V.Kovalenko, M.Petrychuk. Enhancement of the magnetoresistive effect in nanocomposites based on manganite $La_{0.67}Sr_{0.33}MnO_3$ and magnetite Fe_3O_4 // **Technical Physics**, Vol. 55, Issue. 4, 521-525 (**2010**). DOI 10.1134/S1063784210040158

Conference publications

1. ***S.Pud***, A.Acevedo, V.Sibiliev, M.Petrychuk, A.Offenhäusser, S.Vitusevich. Noise and transport characteristics of silicon nanowire field effect transistors with liquid gate//**13th International Young Scientists Conference on Applied Physics** pp.94-95, June 12-15, Kyiv **2013**, Ukraine

2. ***S. Pud***, J. Li, V.Sibiliev, M. Petrychuk, A. Acevedo, A. Offenhausser, S. Vitusevich. Noise and transport characteristics of silicon nanowire field effect transistors with liquid gate// **22nd International Conference on Noise and Fluctuations**, 24-28 June, Montpellier, France (**2013**), DOI:10.1109/ICNF.2013.6578984

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